

## HIGH POWER SP4T SWITCH GaAs MMIC

### ■ GENERAL DESCRIPTION

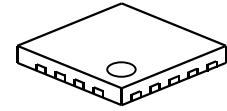
The NJG1809ME7 is a high power SP4T switch MMIC suitable for LTE-U / LAA, WLAN, and LTE applications.

This switch features very low insertion loss and high isolation up to 6GHz and excellent linearity performance with 1.8V control voltage. This switch achieves high speed switching time for WLAN application.

Integrated ESD protection device on each port achieves excellent ESD robustness. No DC Blocking capacitors are required for all RF ports unless DC is biased externally.

The small and thin EQFN18-E7 package is adopted.

### ■ PACKAGE OUTLINE



NJG1809ME7

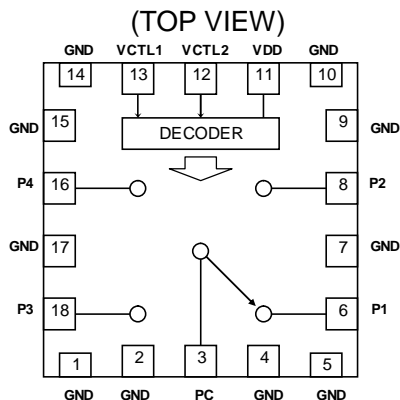
### ■ APPLICATIONS

LTE-U / LAA, WLAN (802.11a/b/g/n/ac), LTE multi-mode applications  
General purpose switching applications

### ■ FEATURES

- Low voltage logic control 1.35 to 5.0V
- Low insertion loss 0.40dB typ. @f=2.7GHz, 3.5GHz, P<sub>IN</sub>=+27dBm  
0.50dB typ. @f=5.85GHz, P<sub>IN</sub>=+27dBm
- High isolation 27dB typ. @f=2.7GHz, P<sub>IN</sub>=+27dBm  
25dB typ. @f=3.5GHz, P<sub>IN</sub>=+27dBm  
30dB typ. @f= 5.85GHz, P<sub>IN</sub>=+27dBm  
+32dBm min.
- P<sub>-0.1dB</sub> 250ns typ.
- High speed switching time 250ns typ.
- Small and thin package EQFN18-E7 (2.0x2.0x0.397mm typ.)
- RoHS compliant and Halogen Free, MSL1

### ■ PIN CONFIGURATION



#### Pin connection

- |        |           |
|--------|-----------|
| 1. GND | 10. GND   |
| 2. GND | 11. VDD   |
| 3. PC  | 12. VCTL2 |
| 4. GND | 13. VCTL1 |
| 5. GND | 14. GND   |
| 6. P1  | 15. GND   |
| 7. GND | 16. P4    |
| 8. P2  | 17. GND   |
| 9. GND | 18. P3    |

Exposed PAD: GND

### ■ TRUTH TABLE

“H”=V<sub>CTL(H)</sub>, “L”=V<sub>CTL(L)</sub>

VCTL1	VCTL2	Path
L	L	PC-P1
H	L	PC-P2
L	H	PC-P3
H	H	PC-P4

NOTE: Please note that any information on this datasheet will be subject to change.

## ■ ABSOLUTE MAXIMUM RATINGS

( $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ )

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	$P_{IN}$	$V_{DD}=2.75\text{V}$ , $V_{CTL}=0/1.8\text{V}$	+33	dBm
Supply Voltage	$V_{DD}$	VDD terminal	5.0	V
Control Voltage	$V_{CTL}$	VCTL1, VCTL2 terminal	5.0	V
Power Dissipation	$P_D$	Four-layer FR4 PCB with through-hole (101.5x114.5mm), $T_j=150^{\circ}\text{C}$	1400	mW
Operating Temp.	$T_{opr}$		-40 to +105	$^{\circ}\text{C}$
Storage Temp.	$T_{stg}$		-55 to +150	$^{\circ}\text{C}$

## ■ ELECTRICAL CHARACTERISTICS 1 (DC)

(General conditions:  $T_a=+25^{\circ}\text{C}$ ,  $V_{DD}=2.75\text{V}$ ,  $V_{CTL(H)}=1.8\text{V}$ ,  $V_{CTL(L)}=0\text{V}$ , with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{DD}$	VDD Terminal	2.5	2.75	5.0	V
Operating Current	$I_{DD}$	No RF input	-	350	700	$\mu\text{A}$
Control Voltage (LOW)	$V_{CTL(L)}$	VCTL1, VCTL2 Terminal	0	-	0.45	V
Control Voltage (HIGH)	$V_{CTL(H)}$	VCTL1, VCTL2 Terminal	1.35	1.8	5.0	V
Control Current	$I_{CTL}$	$V_{CTL(H)}=1.8\text{V}$	-	4	10	$\mu\text{A}$

## ■ ELECTRICAL CHARACTERISTICS 2 (RF)

(General conditions:  $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ ,  $V_{DD}=2.75\text{V}$ ,  $V_{CTL(H)}=1.8\text{V}$ ,  $V_{CTL(L)}=0\text{V}$ , with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Insertion Loss 1	LOSS1	$f=0.7\text{GHz}$ , $P_{IN}=+27\text{dBm}$	-	0.35	0.55	dB	
Insertion Loss 2	LOSS2	$f=2.0\text{GHz}$ , $P_{IN}=+27\text{dBm}$	-	0.40	0.60	dB	
Insertion Loss 3	LOSS3	$f=2.7\text{GHz}$ , $P_{IN}=+27\text{dBm}$	-	0.40	0.60	dB	
Insertion Loss 4	LOSS4	$f=3.5\text{GHz}$ , $P_{IN}=+27\text{dBm}$	-	0.40	0.60	dB	
Insertion Loss 5	LOSS5	$f=5.85\text{GHz}$ , $P_{IN}=+27\text{dBm}$	-	0.50	0.75	dB	
Isolation 1	ISL1	$f=0.7\text{GHz}$ , $P_{IN}=+27\text{dBm}$	32	36	-	dB	
Isolation 2	ISL2	$f=2.0\text{GHz}$ , $P_{IN}=+27\text{dBm}$	25	28	-	dB	
Isolation 3	ISL3	$f=2.7\text{GHz}$ , $P_{IN}=+27\text{dBm}$	24	27	-	dB	
Isolation 4	ISL4	$f=3.5\text{GHz}$ , $P_{IN}=+27\text{dBm}$	22	25	-	dB	
Isolation 5	ISL5	$f=5.85\text{GHz}$ , $P_{IN}=+27\text{dBm}$	PC-Pn <sup>*1</sup>	26	30	-	dB
			Pm-Pn <sup>*2</sup>	20	23	-	
Input Power at 0.1 dB Compression Point	P <sub>-0.1dB</sub>	$f=5.85\text{GHz}$	+32	-	-	dBm	
2nd Harmonics 1	2fo(1)	$f=5.18\text{GHz}$ , $5.85\text{GHz}$ , $P_{IN}=+27\text{dBm}$	-	-	-70	dBc	
2nd Harmonics 2	2fo(2)	$f=2.69\text{GHz}$ , $P_{IN}=0\text{dBm}$	-	-	-95	dBc	
3rd Harmonics 1	3fo(1)	$f=5.18\text{GHz}$ , $5.85\text{GHz}$ , $P_{IN}=+27\text{dBm}$	-	-	-70	dBc	
3rd Harmonics 2	3fo(2)	$f=1.732\text{GHz}$ , $1.91\text{GHz}$ , $P_{IN}=0\text{dBm}$	-	-	-95	dBc	
4th Harmonics	4fo	$f=5.18\text{GHz}$ , $5.85\text{GHz}$ , $P_{IN}=+27\text{dBm}$	-	-	-70	dBc	
Input 2 <sup>nd</sup> order intercept point	IIP2	$f=2.48+2.69\text{GHz}$ , $f_{\text{meas}}=5.17\text{GHz}$ , $P_{IN}=+10\text{dBm}$ each	+100	-	-	dBm	
Input 3 <sup>rd</sup> order intercept point	IIP3	$f=1.71+2.40\text{GHz}$ , $f_{\text{meas}}=5.82\text{GHz}$ , $P_{IN}=+10\text{dBm}$ each	+60	-	-	dBm	
VSWR1	VSWR1	On-state ports, $f=2.7\text{GHz}$	-	1.2	1.5	-	
VSWR2	VSWR2	On-state ports, $f=5.85\text{GHz}$	-	1.3	1.6	-	
Switching time	T <sub>SW</sub>	50% V <sub>CTL</sub> to 10/90% RF	-	250	400	ns	

\*1: Pn=P1, P2, P3, P4

\*2: Pm=P1, P2, P3, P4. Pn=P1, P2, P3, P4. m≠n

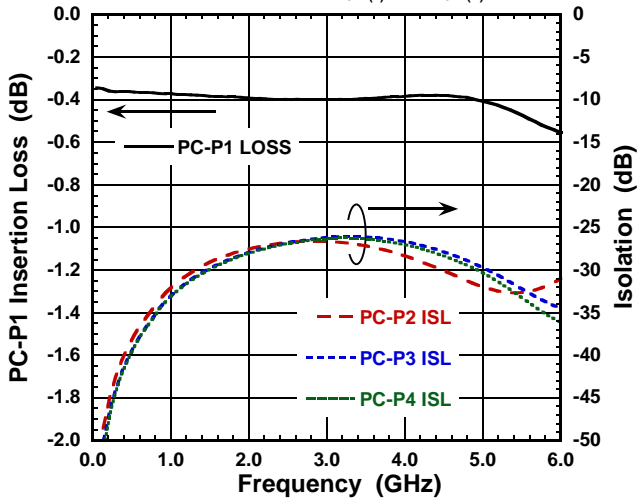
## ■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
2	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
3	PC	Common RF terminal. No DC blocking capacitor is required for this port unless DC is biased externally.
4	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
5	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
6	P1	RF terminal. No DC blocking capacitor is required for this port unless DC is biased externally.
7	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
8	P2	RF terminal. No DC blocking capacitor is required for this port unless DC is biased externally.
9	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
10	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
11	VDD	Positive voltage supply terminal. The positive voltage (+2.5 to +5V) has to be supplied. Please connect a bypass capacitor with ground plane for excellent RF performance.
12	VCTL2	Control signal input terminal. This terminal is set to High-Level (+1.35 to +5.0V) or Low-Level (0 to +0.45V).
13	VCTL1	Control signal input terminal. This terminal is set to High-Level (+1.35 to +5.0V) or Low-Level (0 to +0.45V).
14	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
15	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
16	P4	RF terminal. No DC blocking capacitor is required for this port unless DC is biased externally.
17	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
18	P3	RF terminal. No DC blocking capacitor is required for this port unless DC is biased externally.
Exposed Pad	GND	Ground pad of IC bottom side. Please connect this pad with ground plane as close as possible for excellent RF performance.

■ ELECTRICAL CHARACTERISTICS (With application circuit, loss of external circuit are excluded.)

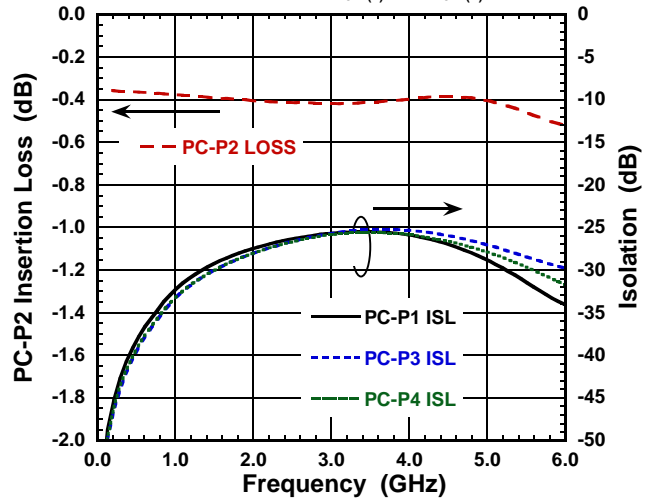
### LOSS, ISL vs Frequency

(PC-P1 ON,  $V_{DD}=2.75V$ ,  $V_{CTL(L)}=0V$ ,  $V_{CTL(H)}=1.8V$ )



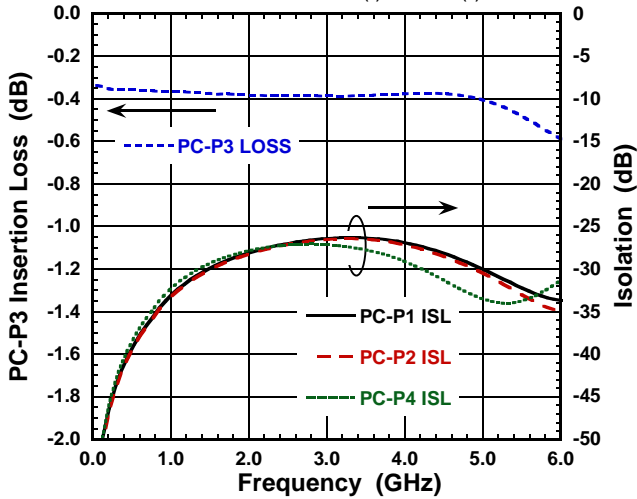
### LOSS, ISL vs Frequency

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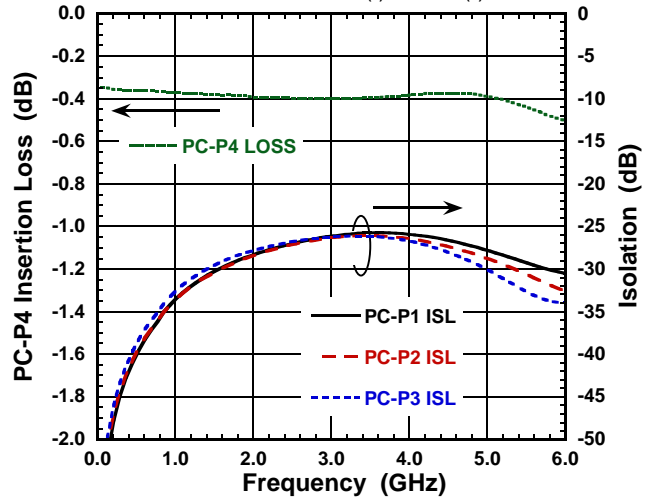
### LOSS, ISL vs Frequency

(PC-P3 ON,  $V_{DD}=2.75V$ ,  $V_{CTL(L)}=0V$ ,  $V_{CTL(H)}=1.8V$ )



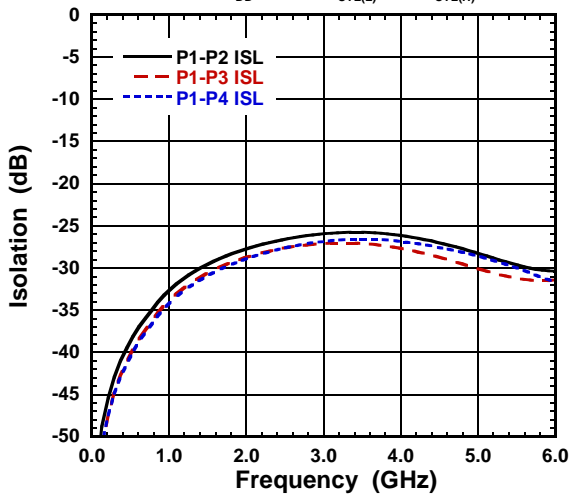
### LOSS, ISL vs Frequency

(PC-P4 ON,  $V_{DD}=2.75V$ ,  $V_{CTL(L)}=0V$ ,  $V_{CTL(H)}=1.8V$ )



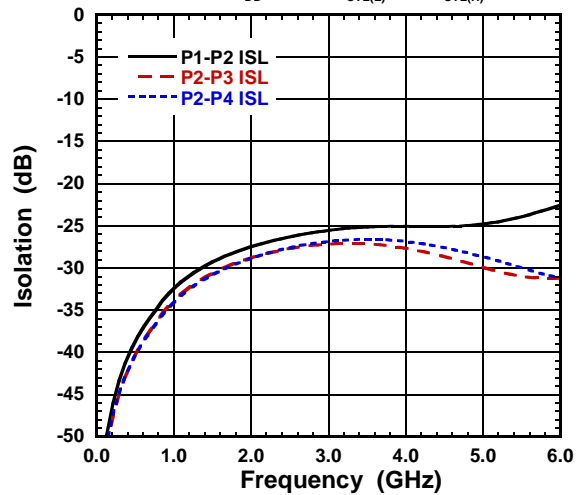
### ISL vs Frequency

(PC-P1 ON,  $V_{DD}=2.75V$ ,  $V_{CTL(L)}=0V$ ,  $V_{CTL(H)}=1.8V$ )



### ISL vs Frequency

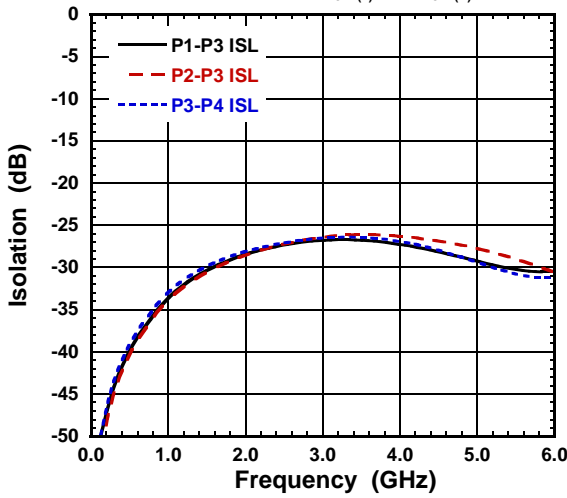
(PC-P2 ON,  $V_{DD}=2.75V$ ,  $V_{CTL(L)}=0V$ ,  $V_{CTL(H)}=1.8V$ )



## ■ ELECTRICAL CHARACTERISTICS (With application circuit, loss of external circuit are excluded.)

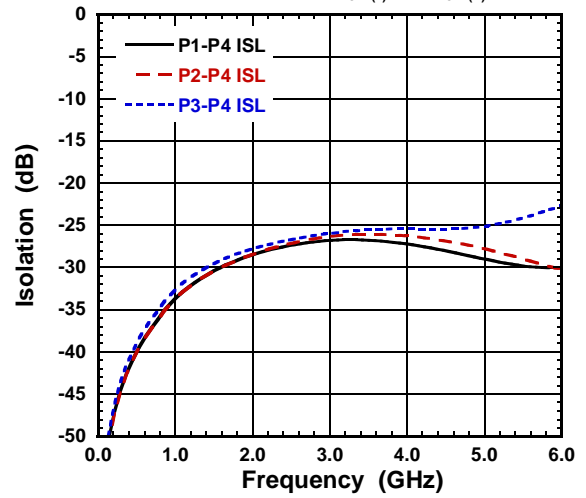
### ISL vs Frequency

(PC-P3 ON,  $V_{DD}=2.75V$ ,  $V_{CTL(L)}=0V$ ,  $V_{CTL(H)}=1.8V$ )



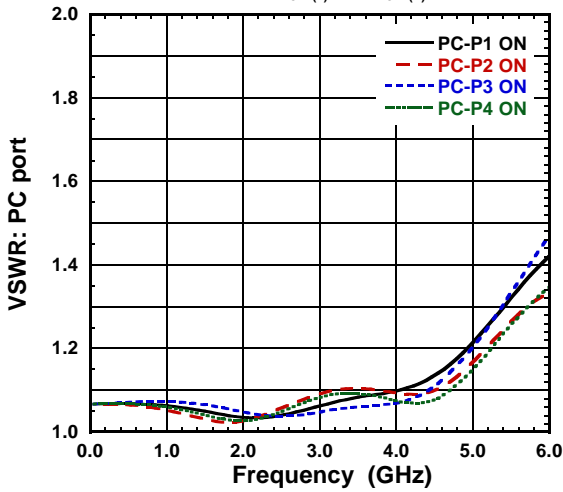
### ISL vs Frequency

(PC-P4 ON,  $V_{DD}=2.75V$ ,  $V_{CTL(L)}=0V$ ,  $V_{CTL(H)}=1.8V$ )



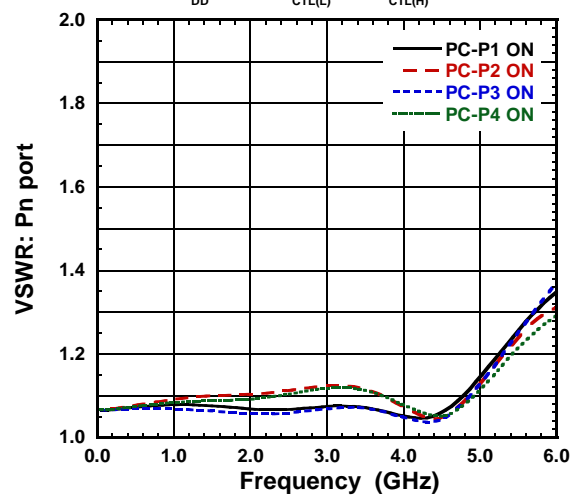
### VSWR vs Frequency

( $V_{DD}=2.75V$ ,  $V_{CTL(L)}=0V$ ,  $V_{CTL(H)}=1.8V$ )



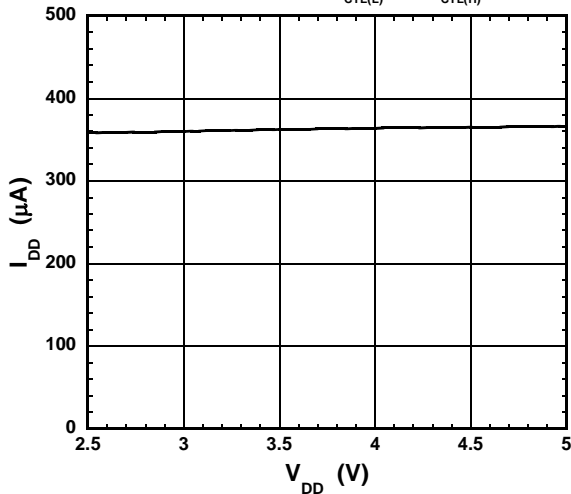
### VSWR vs Frequency

( $V_{DD}=2.75V$ ,  $V_{CTL(L)}=0V$ ,  $V_{CTL(H)}=1.8V$ )



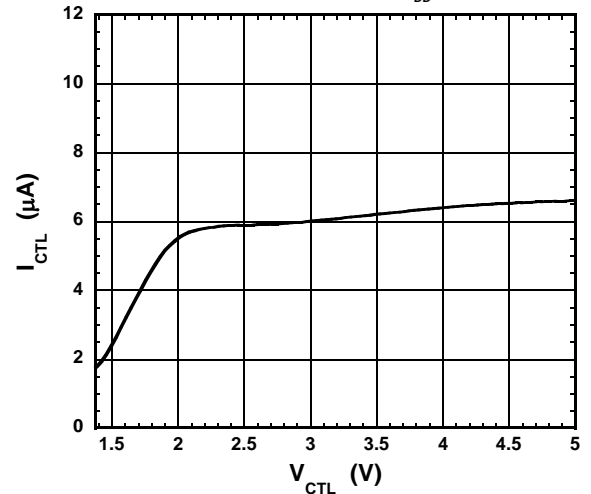
### $I_{DD}$ vs $V_{DD}$

(No RF input, PC-P1 ON,  $V_{CTL(L)}=0V$ ,  $V_{CTL(H)}=1.8V$ )



### $I_{CTL}$ vs $V_{CTL}$

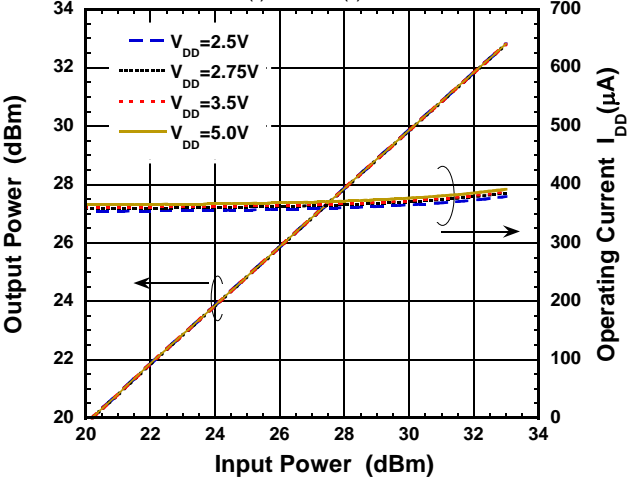
(No RF input, PC-P1 ON,  $V_{DD}=2.75V$ )



**ELECTRICAL CHARACTERISTICS** (With application circuit, loss of external circuit are excluded.)

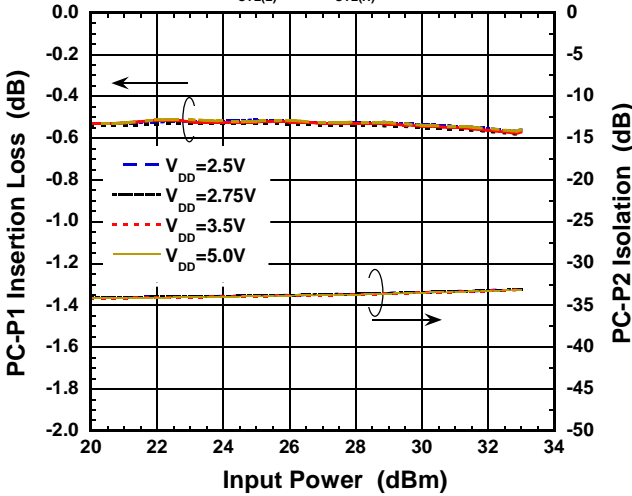
**Output Power,  $I_{DD}$  vs Input Power**

(PC-P1 ON,  $V_{CTL(L)}=0V$ ,  $V_{CTL(H)}=1.8V$ ,  $f=5.85GHz$ )



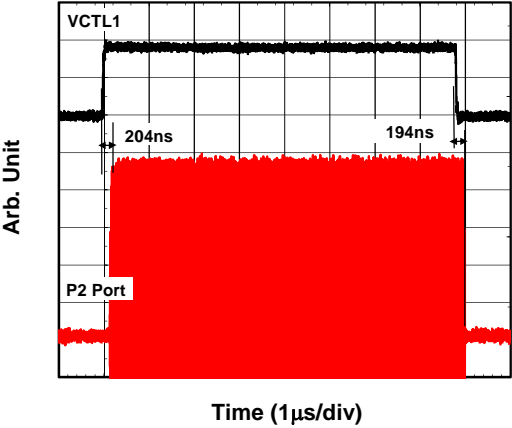
**Loss, ISL vs Input Power**

(PC-P1 ON,  $V_{CTL(L)}=0V$ ,  $V_{CTL(H)}=1.8V$ ,  $f=5.85GHz$ )



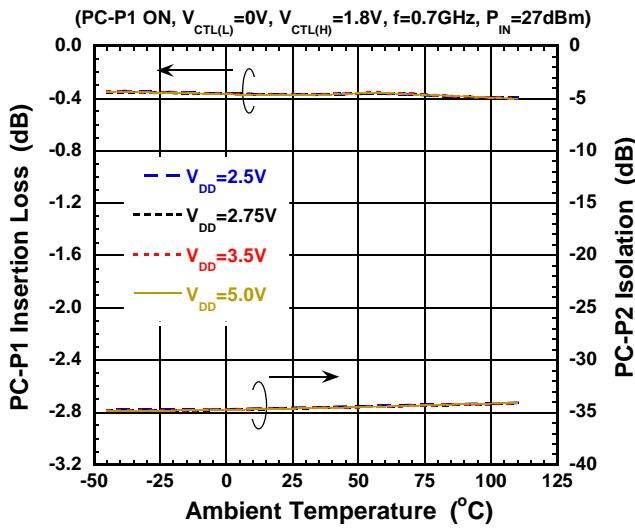
**Switching Time**

(PC-P1/P2 path,  $V_{DD}=2.75V$ ,  $V_{CTL(L)}=0V$ ,  $V_{CTL(H)}=1.8V$ )

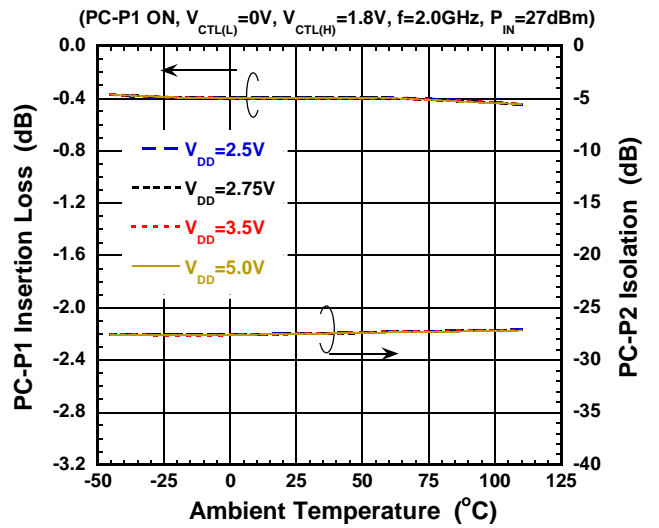


## ■ ELECTRICAL CHARACTERISTICS (With application circuit, loss of external circuit are excluded.)

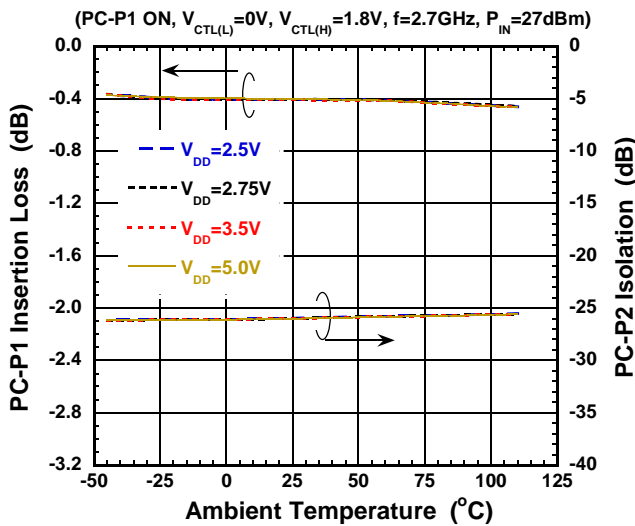
### Loss, ISL vs Temperature



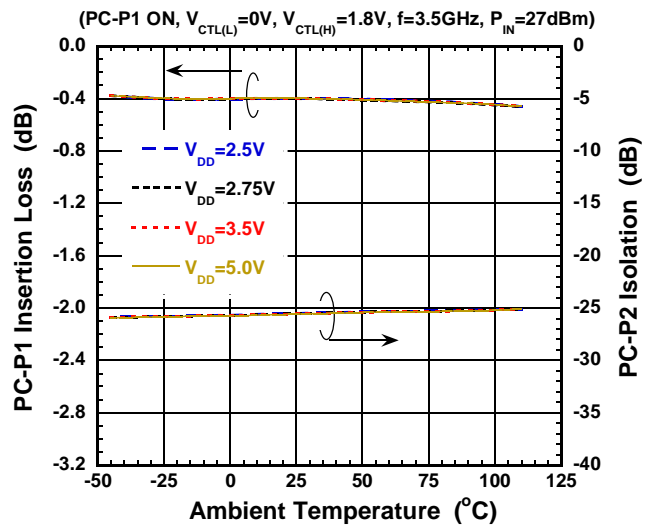
### Loss, ISL vs Temperature



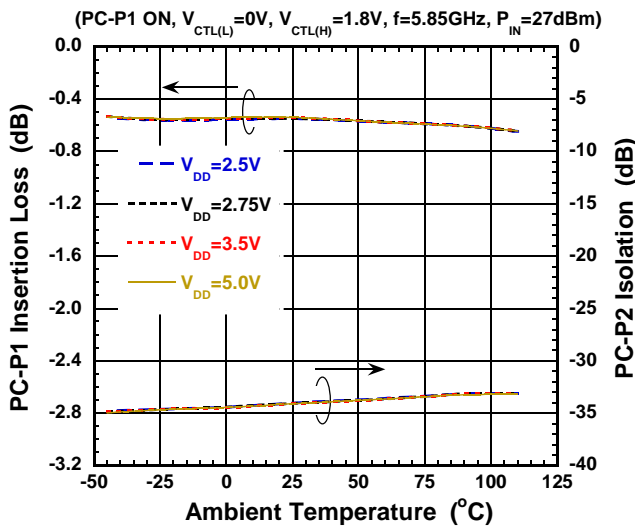
### Loss, ISL vs Temperature



### Loss, ISL vs Temperature



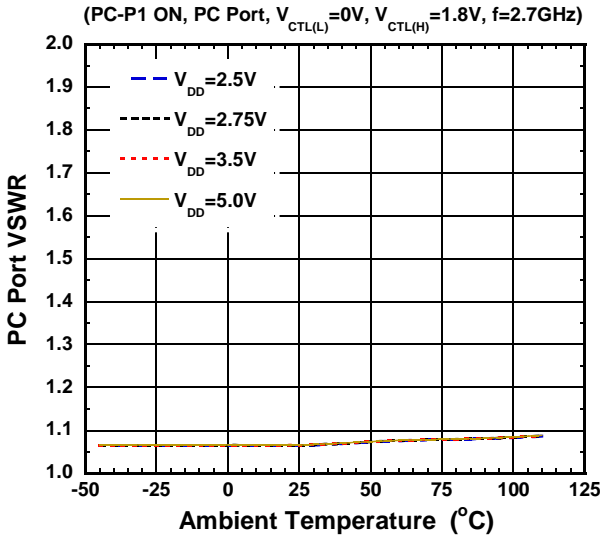
### Loss, ISL vs Temperature



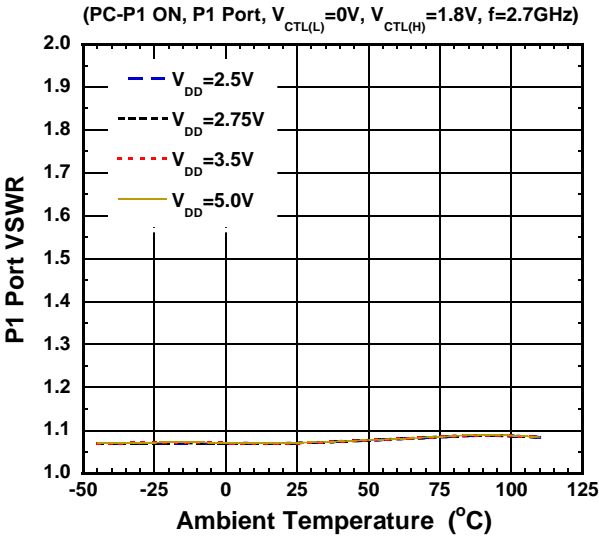


■ ELECTRICAL CHARACTERISTICS (With application circuit, loss of external circuit are excluded.)

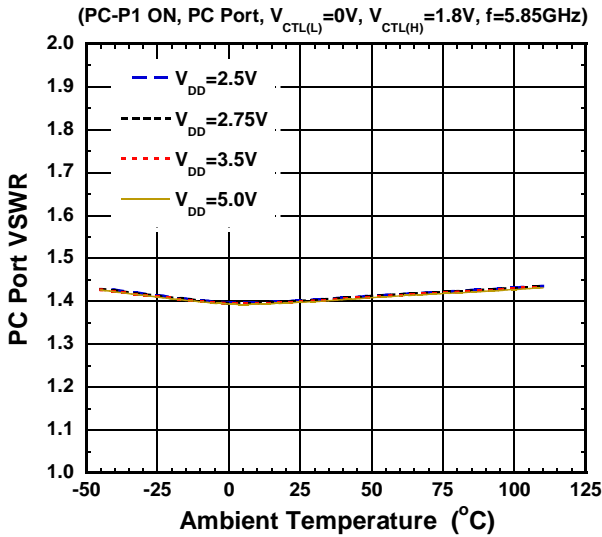
**VSWR vs Temperature**



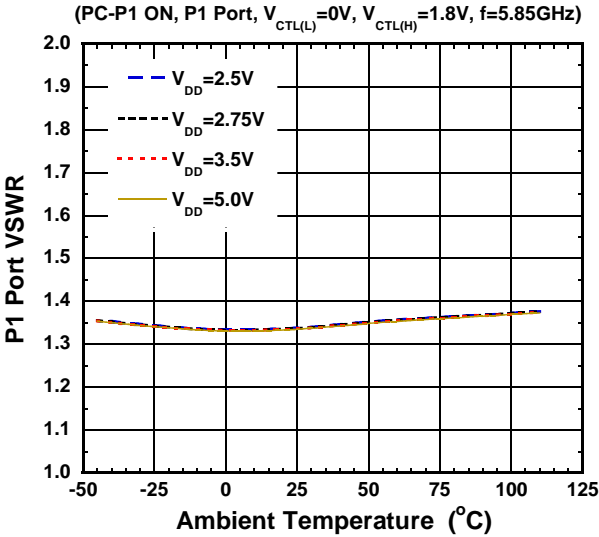
**VSWR vs Temperature**



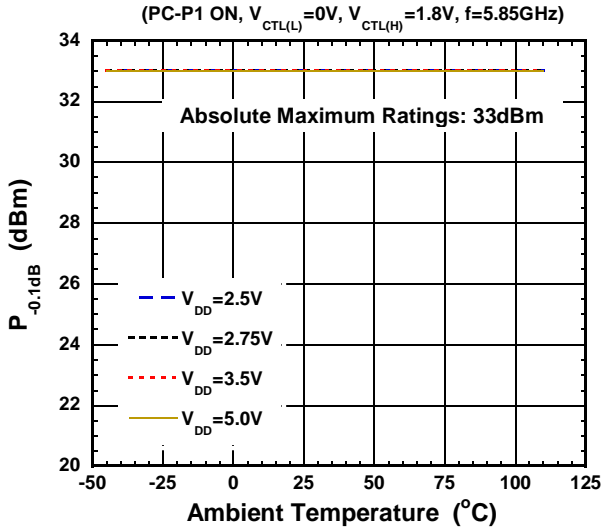
**VSWR vs Temperature**



**VSWR vs Temperature**

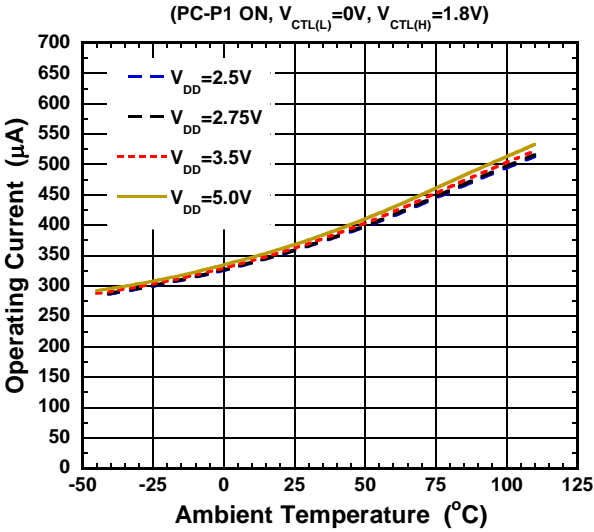


**$P_{-0.1dB}$  vs Temperature**

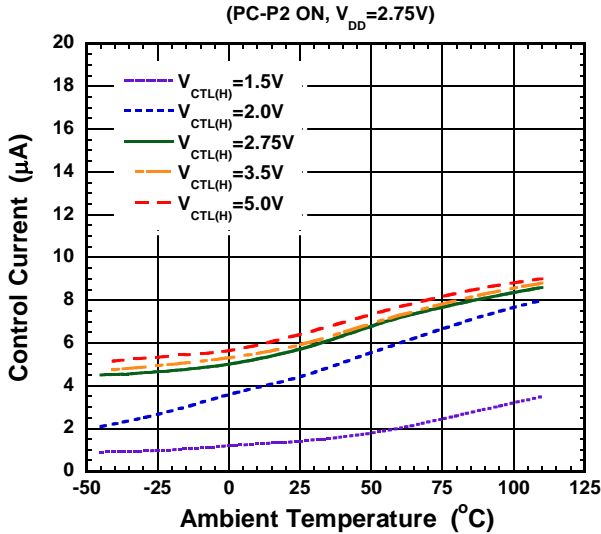


■ ELECTRICAL CHARACTERISTICS (With application circuit, loss of external circuit are excluded.)

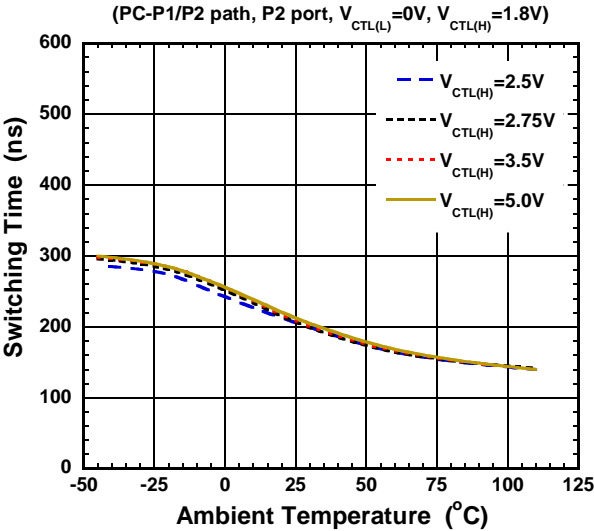
**Operating Current vs Temperature**



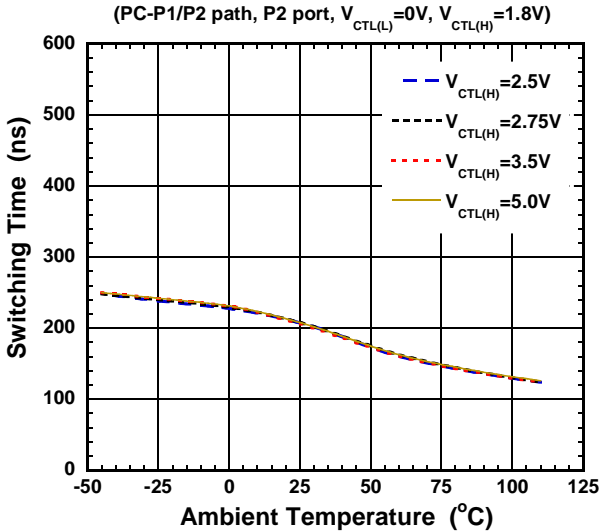
**Control Current vs Temperature**



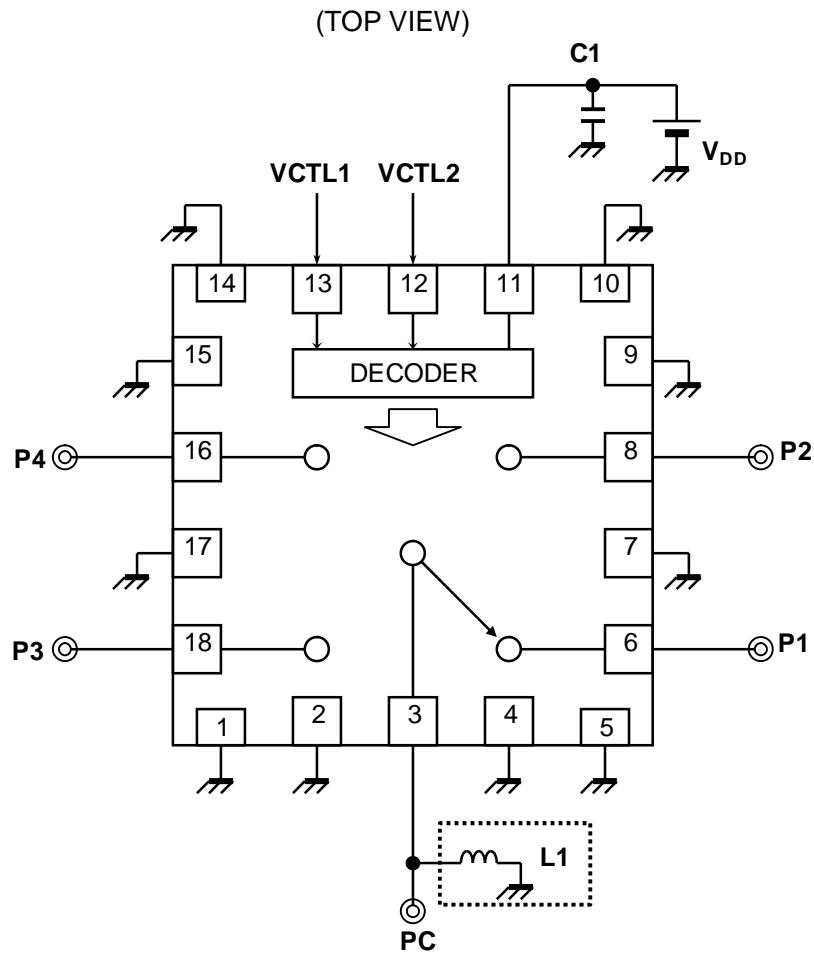
**Switching Time(rise) vs Temperature**



**Switching Time(fall) vs Temperature**



## APPLICATION CIRCUIT



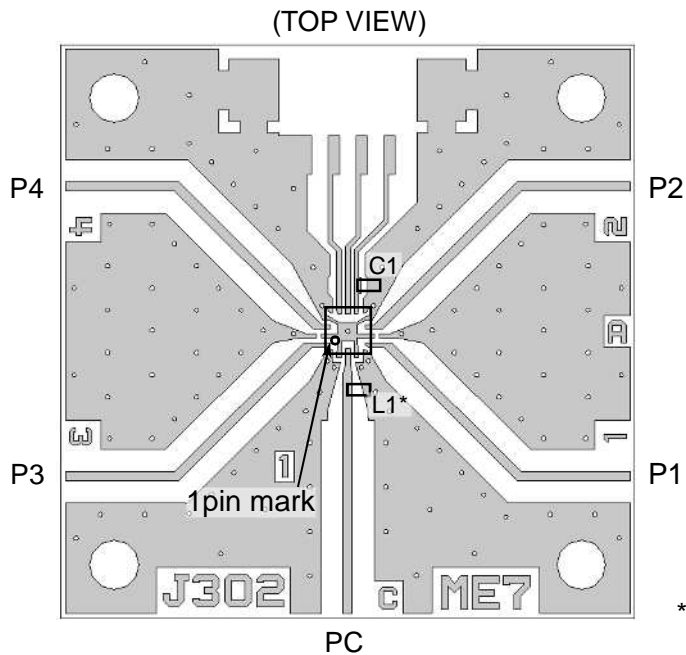
Note:

- [1] No DC blocking capacitors are required on all RF ports, unless DC is biased externally.
- [2] The inductor L1 is optional in order to achieve enhancing ESD protection level. L1 is also recommended in order to keep the DC bias level of each RF port at ground level tightly.

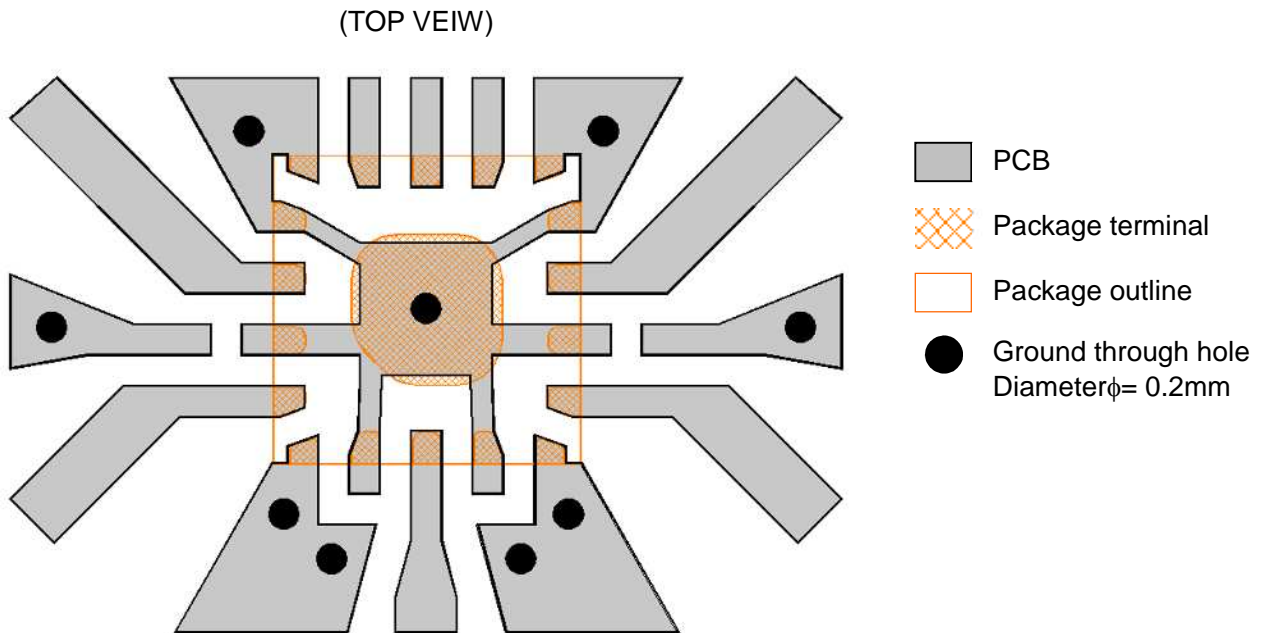
### PARTS LIST

No.	Parameters	Note
C1	1000pF	MURATA (GRM15)
L1	68nH	TAIYO-YUDEN (HK1005)

## PCB LAYOUT



## <PCB LAYOUT GUIDELINE>



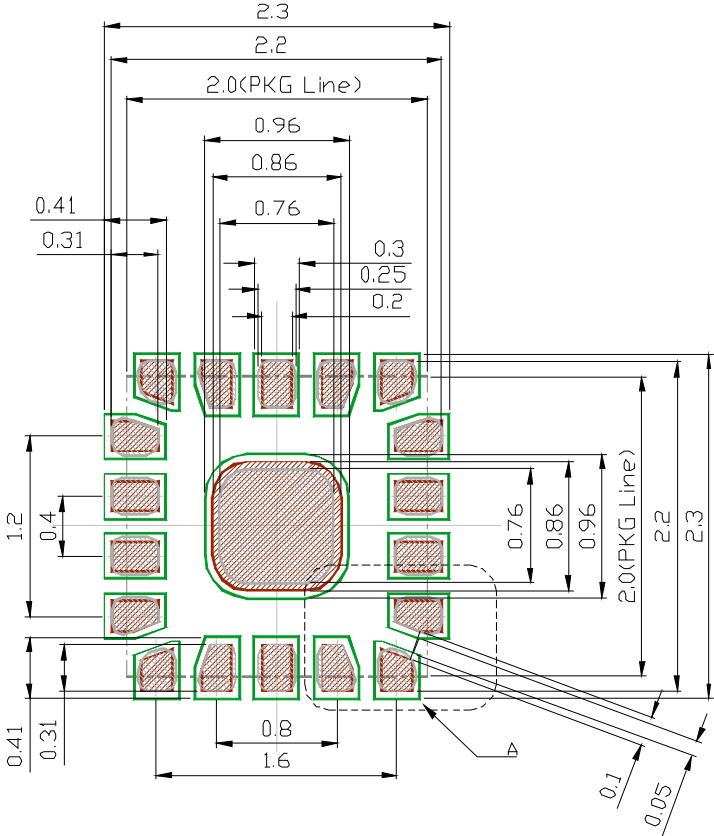
## PRECAUTIONS

- [1] No DC block capacitors are required for RF ports unless DC is biased externally. When other device biased at certain voltage is connected to the NJG1809ME7, a DC block capacitor is required between the device and this switch IC. This is because the each RF port of this switch is biased at ground level.
- [2] For avoiding the degradation of RF performance, the bypass capacitor (C1) should be placed as close as possible to VDD terminal.
- [3] For good RF performance, all GND terminals are must be connected to PCB ground plane of substrate, and through holes for GND should be placed near the IC.
- [4] Please connect Exposed PAD to PCB ground plane of substrate, and through holes for ground should be placed under the IC.

■ RECOMMENDED FOOTPRINT PATTERN (EQFN18-E7 PACKAGE REFERENCE)

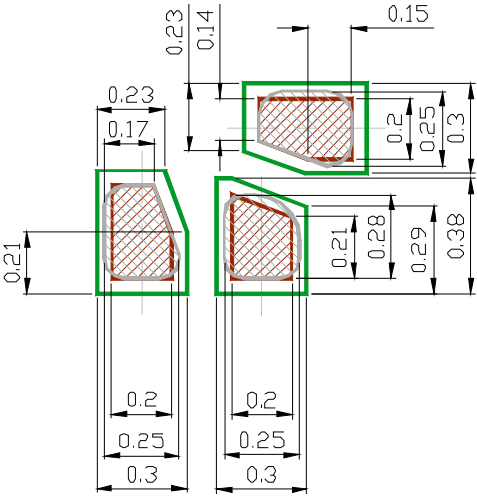
- : Land
- : Mask (Open area) \*Metal mask thickness: 100μm
- : Resist (Open area)

PKG: 2.0x2.0mm<sup>2</sup>  
Pin pitch: 0.4mm



Unit: mm

Detail A





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