GD65232, GD75232
MULTIPLE RS-232 DRIVERS AND RECEIVERS

- **Single Chip With Easy Interface Between UART and Serial-Port Connector of IBM™ PC/AT and Compatibles**
- **Meet or Exceed the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Designed to Support Data Rates up to 120 kbit/s**
- **Pinout Compatible With SN75C185 and SN75185**

**GD65232, GD75232 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)**

```
        ┌───∪───┐
 V_DD  │1     20│ V_CC
 RA1   │2     19│ RY1
 RA2   │3     18│ RY2
 RA3   │4     17│ RY3
 DY1   │5     16│ DA1
 DY2   │6     15│ DA2
 RA4   │7     14│ RY4
 DY3   │8     13│ DA3
 RA5   │9     12│ RY5
 V_SS  │10    11│ GND
        └───────┘
```
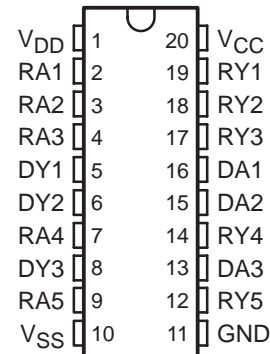
description/ordering information

The GD65232 and GD75232 combine three drivers and five receivers from the Texas Instruments trade-standard SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The pinout matches the flow-through design of the SN75C185 to decrease the part count, reduce the board space required, and allow easy interconnection of the UART and serial-port connector of an IBM™ PC/AT and compatibles. The bipolar circuits and processing of the GD65232 and GD75232 provide a rugged, low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C185.

The GD65232 and GD75232 comply with the requirements of the TIA/EIA-232-F and ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and a peripheral at signaling rates up to 20 kbit/s. The switching speeds of these devices are fast enough to support rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be expected unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates up to 120 kbit/s, use of TIA/EIA-423-B (ITU V.10) and TIA/EIA-422-B (ITU V.11) standards is recommended.

ORDERING INFORMATION

T$_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP (N)	Tube of 20	GD65232N	GD65232N
	SOIC (DW)	Tube of 25	GD65232DW	GD65232
		Reel of 2000	GD65232DWR	
	SSOP (DB)	Reel of 2000	GD65232DBR	GD65232
	TSSOP (PW)	Tube of 70	GD65232PW	GD65232
		Reel of 2000	GD65232PWR	
0°C to 70°C	PDIP (N)	Tube of 20	GD75232N	GD75232N
	SOIC (DW)	Tube of 25	GD75232DW	GD75232
		Reel of 2000	GD75232DWR	
	SSOP (DB)	Reel of 2000	GD75232DBR	GD75232
	TSSOP (PW)	Tube of 70	GD75232PW	GD75232
		Reel of 2000	GD75232PWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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logic diagram (positive logic)

RA1	2	▷	19	RY1
RA2	3	▷	18	RY2
RA3	4	▷	17	RY3
DY1	5	◁	16	DA1
DY2	6	◁	15	DA2
RA4	7	▷	14	RY4
DY3	8	◁	13	DA3
RA5	9	▷	12	RY5

schematic (each driver)

To Other Drivers

V_{DD}

11.6 kΩ

9.4 kΩ

Input DAx

75.8 Ω

4.2 kΩ

320 Ω

Output DYx

GND

To Other Drivers

10.4 kΩ

3.3 kΩ   68.5 Ω

V_{SS}

To Other Drivers
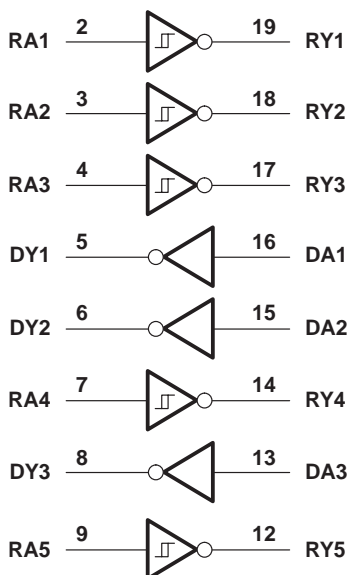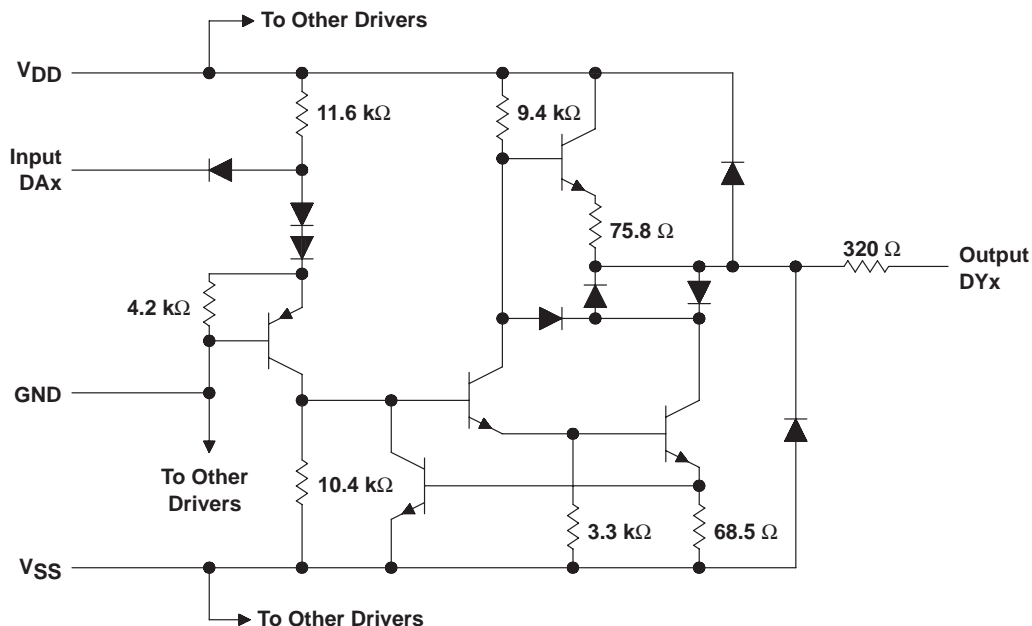
Resistor values shown are nominal.

schematic (each receiver)

To Other Receivers

V_{CC}

9 kΩ 5 kΩ 1.66 kΩ

Output
RYx

2 kΩ

Input
RAx   3.8 kΩ

10 kΩ

GND

To Other Receivers
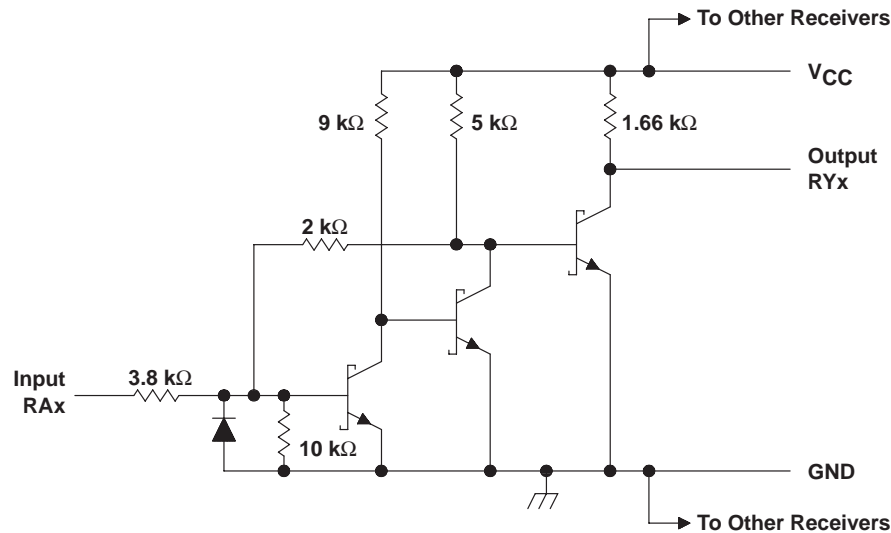
Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): V_{CC} . . . . 10 V
V_{DD} . . . . 15 V
V_{SS} . . . . −15 V
Input voltage range, V_I: Driver . . . . −15 V to 7 V
Receiver . . . . −30 V to 30 V
Driver output voltage range, V_O . . . . −15 V to 15 V
Receiver low-level output current, I_{OL} . . . . 20 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DB package . . . . 70°C/W
DW package . . . . 58°C/W
N package . . . . 69°C/W
PW package . . . . 83°C/W
Operating virtual junction temperature, T_J . . . . 150°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to the network ground terminal.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable
ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage (see Note 4)			7.5	9	15	V
V_{SS}	Supply voltage (see Note 4)			−7.5	−9	−15	V
V_{CC}	Supply voltage (see Note 4)			4.5	5	5.5	V
V_{IH}	High-level input voltage (driver only)			1.9			V
V_{IL}	Low-level input voltage (driver only)					0.8	V
I_{OH}	High-level output current	Driver				−6	mA
		Receiver				−0.5	
I_{OL}	Low-level output current	Driver				6	mA
		Receiver				16	
T_A	Operating free-air temperature	GD65232		−40		85	°C
		GD75232		0		70	

NOTE 4:   When powering up the GD65232 and GD75232, the following sequence should be used:
     1. V_{SS}
     2. V_{DD}
     3. V_{CC}
     4. I/Os
Applying V_{CC} before V_{DD} may allow large currents to flow, causing damage to the device. When powering down the GD65232 and GD75232, the reverse sequence should be used.

supply currents over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{DD}	Supply current from V_{DD}	All inputs at 1.9 V, No load	V_{DD} = 9 V,	V_{SS} = −9 V		15	mA
			V_{DD} = 12 V,	V_{SS} = −12 V		19	
			V_{DD} = 15 V,	V_{SS} = −15 V		25	
		All inputs at 0.8 V, No load	V_{DD} = 9 V,	V_{SS} = −9 V		4.5	
			V_{DD} = 12 V,	V_{SS} = −12 V		5.5	
			V_{DD} = 15 V,	V_{SS} = −15 V		9	
I_{SS}	Supply current from V_{SS}	All inputs at 1.9 V, No load	V_{DD} = 9 V,	V_{SS} = −9 V		−15	mA
			V_{DD} = 12 V,	V_{SS} = −12 V		−19	
			V_{DD} = 15 V,	V_{SS} = −15 V		−25	
		All inputs at 0.8 V, No load	V_{DD} = 9 V,	V_{SS} = −9 V		−3.2	
			V_{DD} = 12 V,	V_{SS} = −12 V		−3.2	
			V_{DD} = 15 V,	V_{SS} = −15 V		−3.2	
I_{CC}	Supply current from V_{CC}	All inputs at 5 V, No load, V_{CC} = 5 V	GD65232			38	mA
			GD75232			30	

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DRIVER SECTION

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 9 V, V_{SS} = –9 V, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	R_L = 3 kΩ,	See Figure 1	6	7.5		V
V_{OL}	Low-level output voltage (see Note 5)	V_{IH} = 1.9 V,	R_L = 3 kΩ,	See Figure 1		–7.5	–6	V
I_{IH}	High-level input current	V_I = 5 V,	See Figure 2				10	µA
I_{IL}	Low-level input current	V_I = 0,	See Figure 2				–1.6	mA
$I_{OS(H)}$	High-level short-circuit output current (see Note 6)	V_{IL} = 0.8 V,	V_O = 0,	See Figure 1	–4.5	–12	–19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current	V_{IH} = 2 V,	V_O = 0,	See Figure 1	4.5	12	19.5	mA
r_o	Output resistance (see Note 7)	$V_{CC} = V_{DD} = V_{SS}$ = 0,	V_O = –2 V to 2 V		300			Ω

NOTES: 5. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (e.g., if –10 V is maximum, the typical value is a more negative voltage).
6. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
7. Test conditions are those specified by TIA/EIA-232-F and as listed above.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF,	See Figure 3		315	500	ns
t_{PHL}	Propagation delay time, high- to low-level output	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF,	See Figure 3		75	175	ns
t_{TLH}	Transition time, low- to high-level output	R_L = 3 kΩ to 7 kΩ	C_L = 15 pF,	See Figure 3		60	100	ns
			C_L = 2500 pF,	See Figure 3 and Note 8		1.7	2.5	µs
t_{THL}	Transition time, high- to low-level output	R_L = 3 kΩ to 7 kΩ	C_L = 15 pF,	See Figure 3		40	75	ns
			C_L = 2500 pF,	See Figure 3 and Note 8		1.5	2.5	µs

NOTE 8: Measured between ±3-V and ±3-V points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$T_A = 25°C$,	See Figure 5		1.75	1.9	2.3	V
		$T_A = 0°C$ to $70°C$,	See Figure 5		1.55		2.3	
V_{IT-}	Negative-going input threshold voltage				0.75	0.97	1.25	V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)				0.5			V
V_{OH}	High-level output voltage	$I_{OH} = -0.5$ mA	$V_{IH} = 0.75$ V		2.6	4	5	V
			Inputs open		2.6			
V_{OL}	Low-level output voltage	$I_{OL} = 10$ mA,	$V_I = 3$ V			0.2	0.45	V
I_{IH}	High-level input current	$V_I = 25$ V,	See Figure 5	GD65232	3.6		11	mA
				GD75232	3.6		8.3	
		$V_I = 3$ V,	See Figure 5		0.43			
I_{IL}	Low-level input current	$V_I = -25$ V,	See Figure 5	GD65232	−3.6		−11	mA
				GD75232	−3.6		−8.3	
		$V_I = -3$ V,	See Figure 5		−0.43			
I_{OS}	Short-circuit output current	See Figure 4				−3.4	−12	mA

† All typical values are at $T_A = 25°C$, $V_{CC} = 5$ V, $V_{DD} = 9$ V, and $V_{SS} = -9$ V.

switching characteristics, $V_{CC} = 5$ V, $V_{DD} = 12$ V, $V_{SS} = -12$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output					107	250	ns
t_{PHL}	Propagation delay time, high- to low-level output	$C_L = 50$ pF,	$R_L = 5$ kΩ,	See Figure 6		42	150	ns
t_{TLH}	Transition time, low- to high-level output					175	350	ns
t_{THL}	Transition time, high- to low-level output					16	60	ns
t_{PLH}	Propagation delay time, low- to high-level output					100	160	ns
t_{PHL}	Propagation delay time, high- to low-level output	$C_L = 15$ pF,	$R_L = 1.5$ kΩ,	See Figure 6		60	100	ns
t_{TLH}	Transition time, low- to high-level output					90	175	ns
t_{THL}	Transition time, high- to low-level output					15	50	ns

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PARAMETER MEASUREMENT INFORMATION

$I_{OS(L)}$

V_{DD} or GND

$-I_{OS(H)}$

V_{SS} or GND

V_{DD}

V_{CC}

V_I

V_O

V_{SS}

$R_L = 3\ k\Omega$
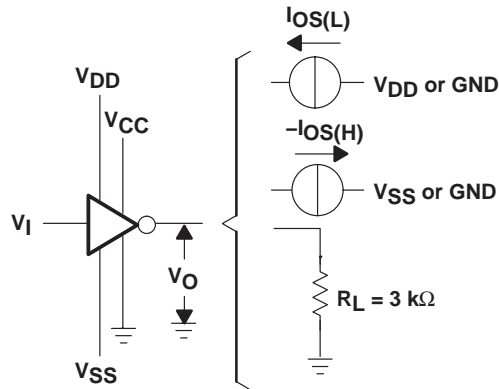
Figure 1. Driver Test Circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, and $I_{OS(L)}$

V_{DD}

V_{CC}

I_{IH}

V_I

$-I_{IL}$

V_I

V_{SS}
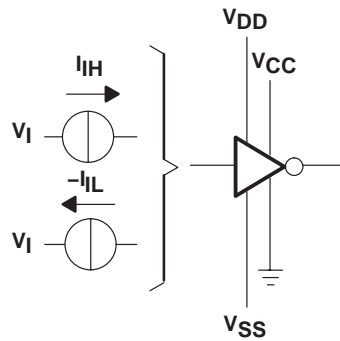
Figure 2. Driver Test Circuit for I_{IH} and I_{IL}

Input

V_{DD}

V_{CC}

Pulse Generator

See Note A

R_L

C_L

(see Note B)

V_{SS}

TEST CIRCUIT

Input

3 V

1.5 V

1.5 V

0 V

t_{PHL}

t_{PLH}

V_{OH}

90%

50%

50%

90%

Output

10%

10%

V_{OL}

t_{THL}

t_{TLH}
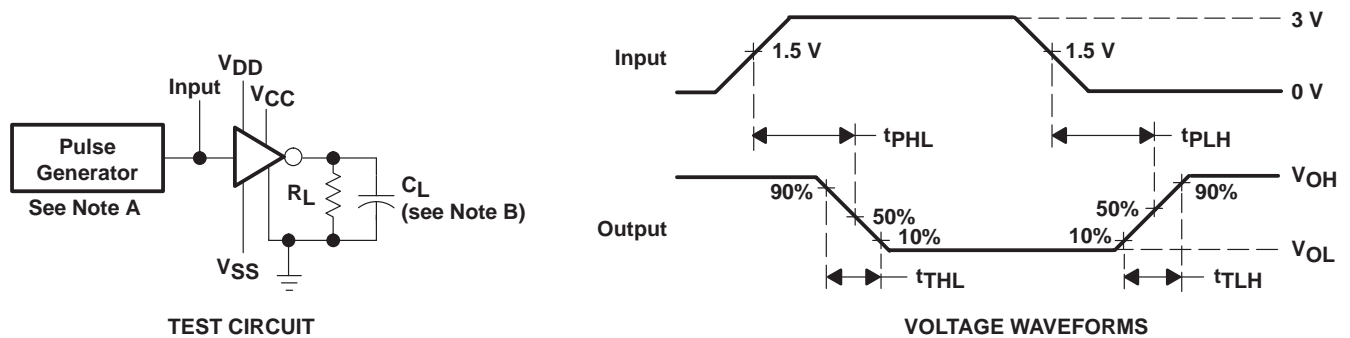
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_W = 25\ \mu s$, PRR = 20 kHz, $Z_O = 50\ \Omega$, $t_r = t_f < 50$ ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

TEXAS INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION
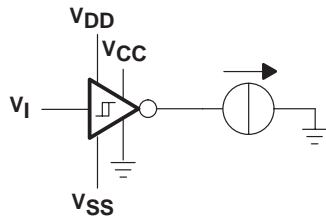
Figure 4. Receiver Test Circuit for I_{OS}
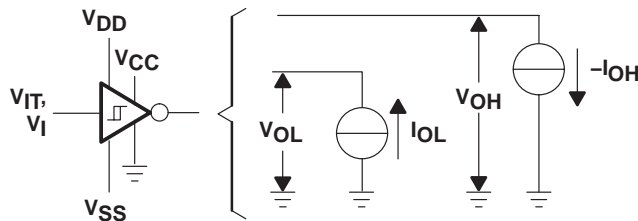
Figure 5. Receiver Test Circuit for V_{IT}, V_{OH}, and V_{OL}

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, t_r = t_f < 50 ns.
B. C_L includes probe and jig capacitance.

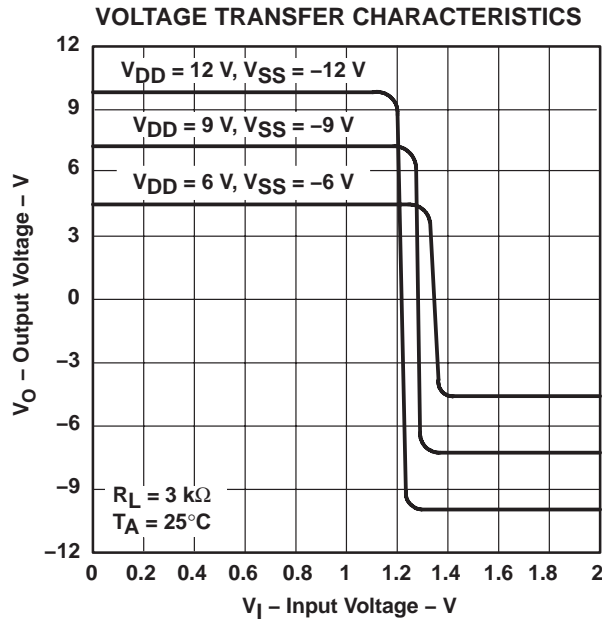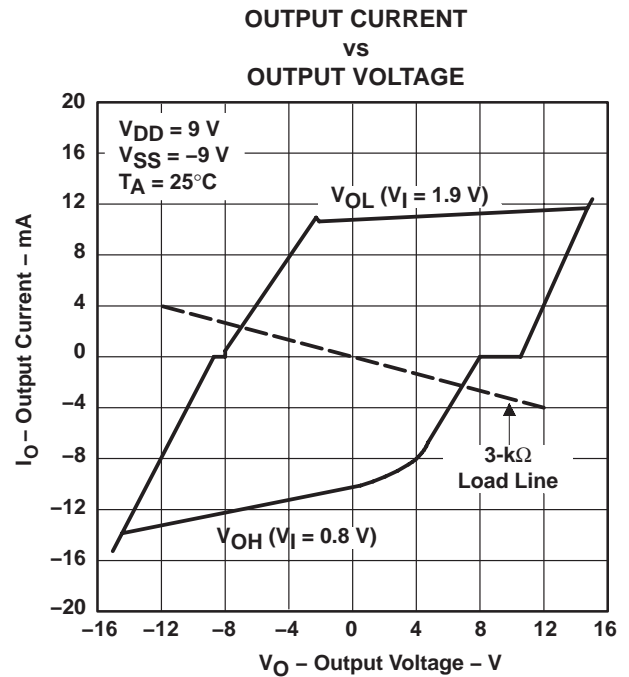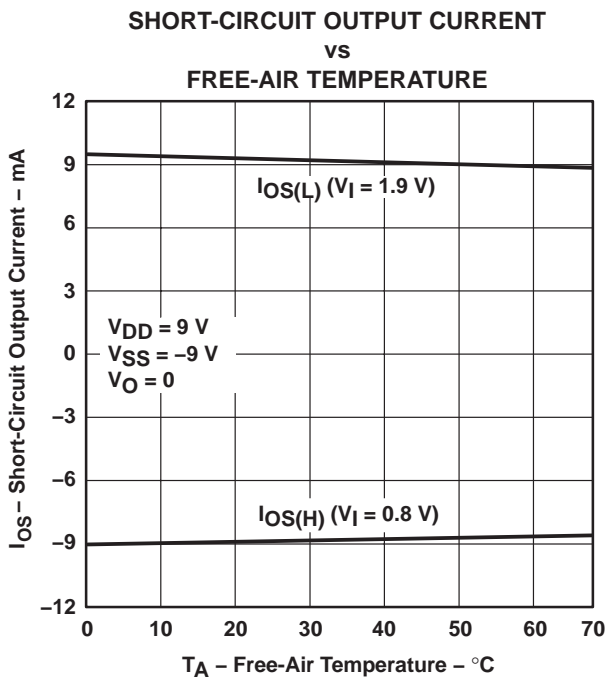**Figure 6. Receiver Propagation and Transition Times**

TYPICAL CHARACTERISTICS

DRIVER SECTION
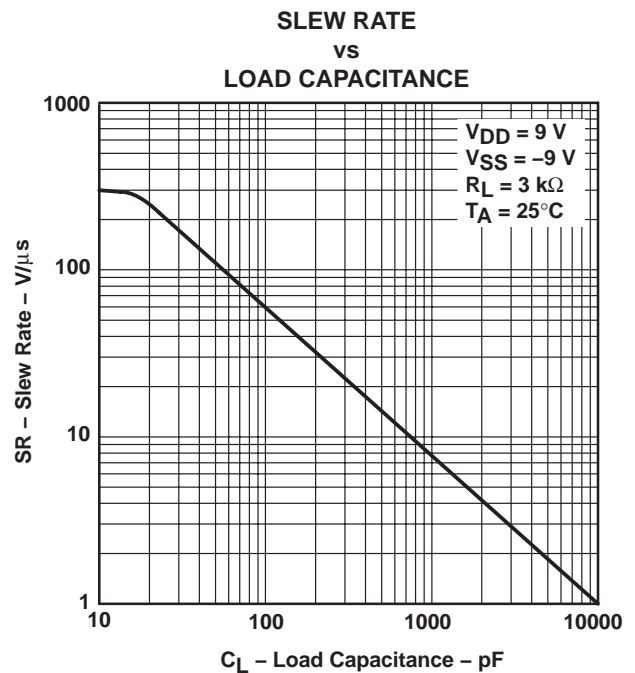
VOLTAGE TRANSFER CHARACTERISTICS

Figure 7

**OUTPUT CURRENT
vs
OUTPUT VOLTAGE**

Figure 8

**SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE**

Figure 9

**SLEW RATE
vs
LOAD CAPACITANCE**

Figure 10

TYPICAL CHARACTERISTICS

INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 11

INPUT THRESHOLD VOLTAGE
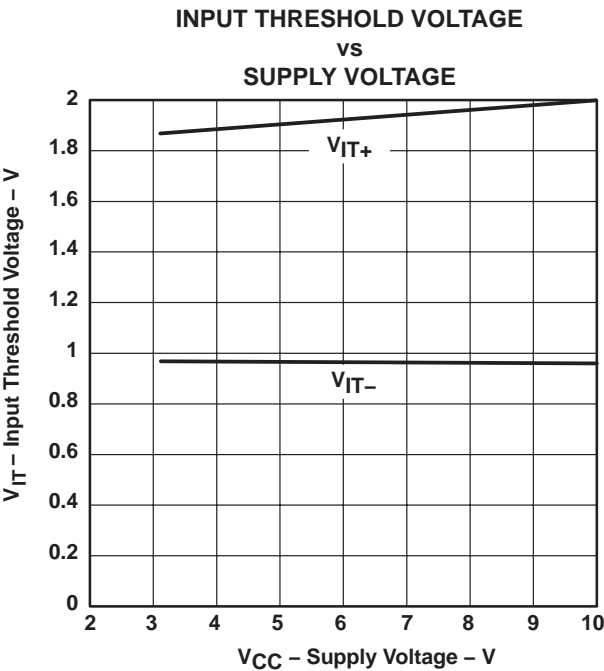**vs**
SUPPLY VOLTAGE

Figure 12

NOISE REJECTION
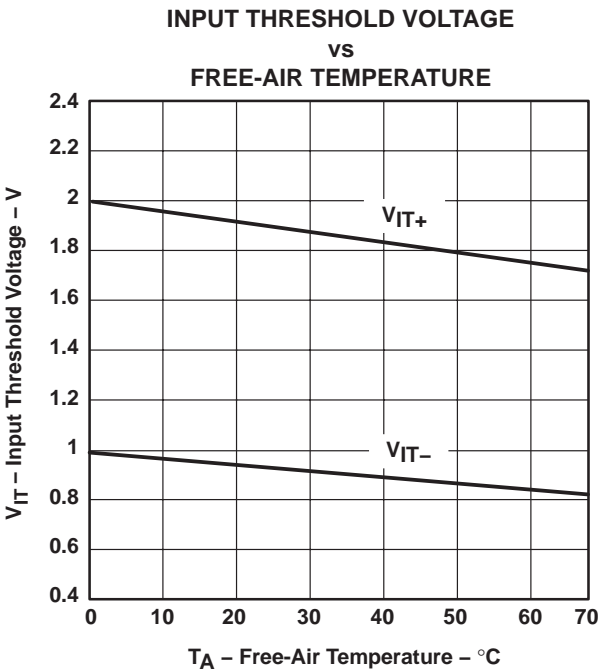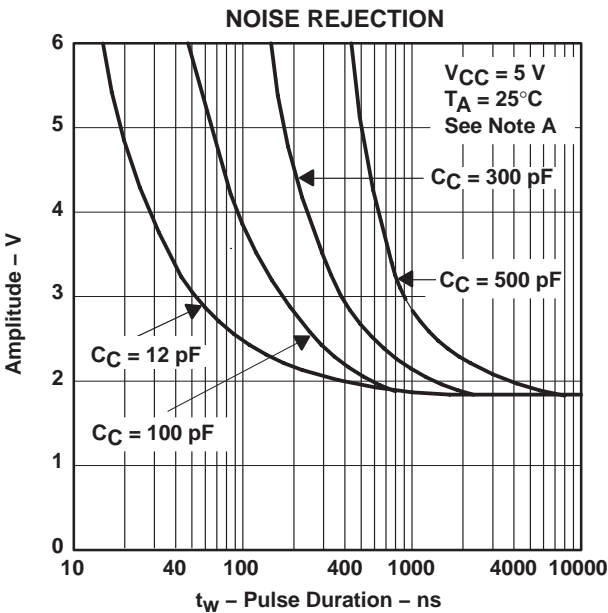
NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, does not cause a change of the output level.
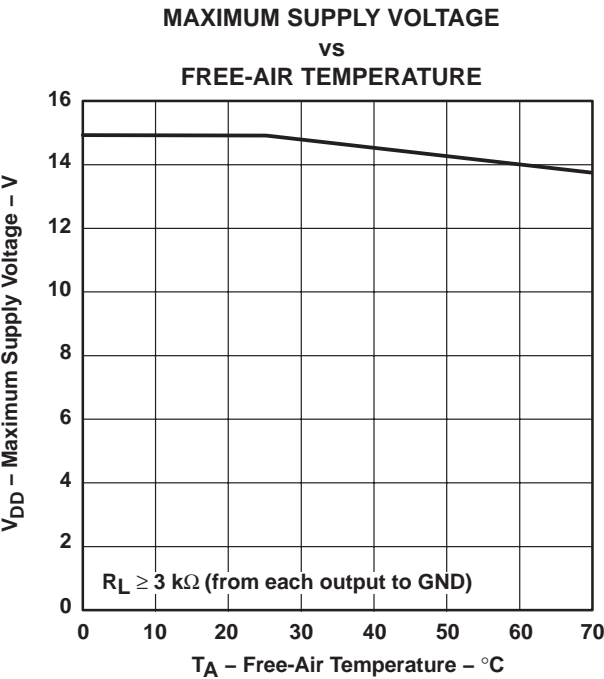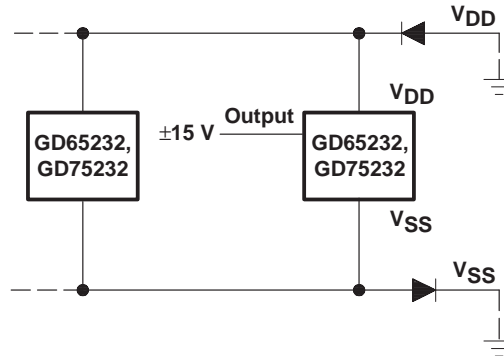
Figure 13

MAXIMUM SUPPLY VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 14

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} leads protect the GD65232 and GD75232 in the fault condition in which the device outputs are shorted to ±15 V and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).

Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F

Figure 16. Typical Connection

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
GD65232DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GD65232	Samples
GD65232DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GD65232	Samples
GD65232PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GD65232	Samples
GD75232DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	Samples
GD75232DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	Samples
GD75232DWE4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	Samples
GD75232DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	Samples
GD75232DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	Samples
GD75232N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	GD75232N	Samples
GD75232PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	Samples
GD75232PWE4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	Samples
GD75232PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	SN	Level-1-260C-UNLIM	0 to 70	GD75232	Samples
GD75232PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
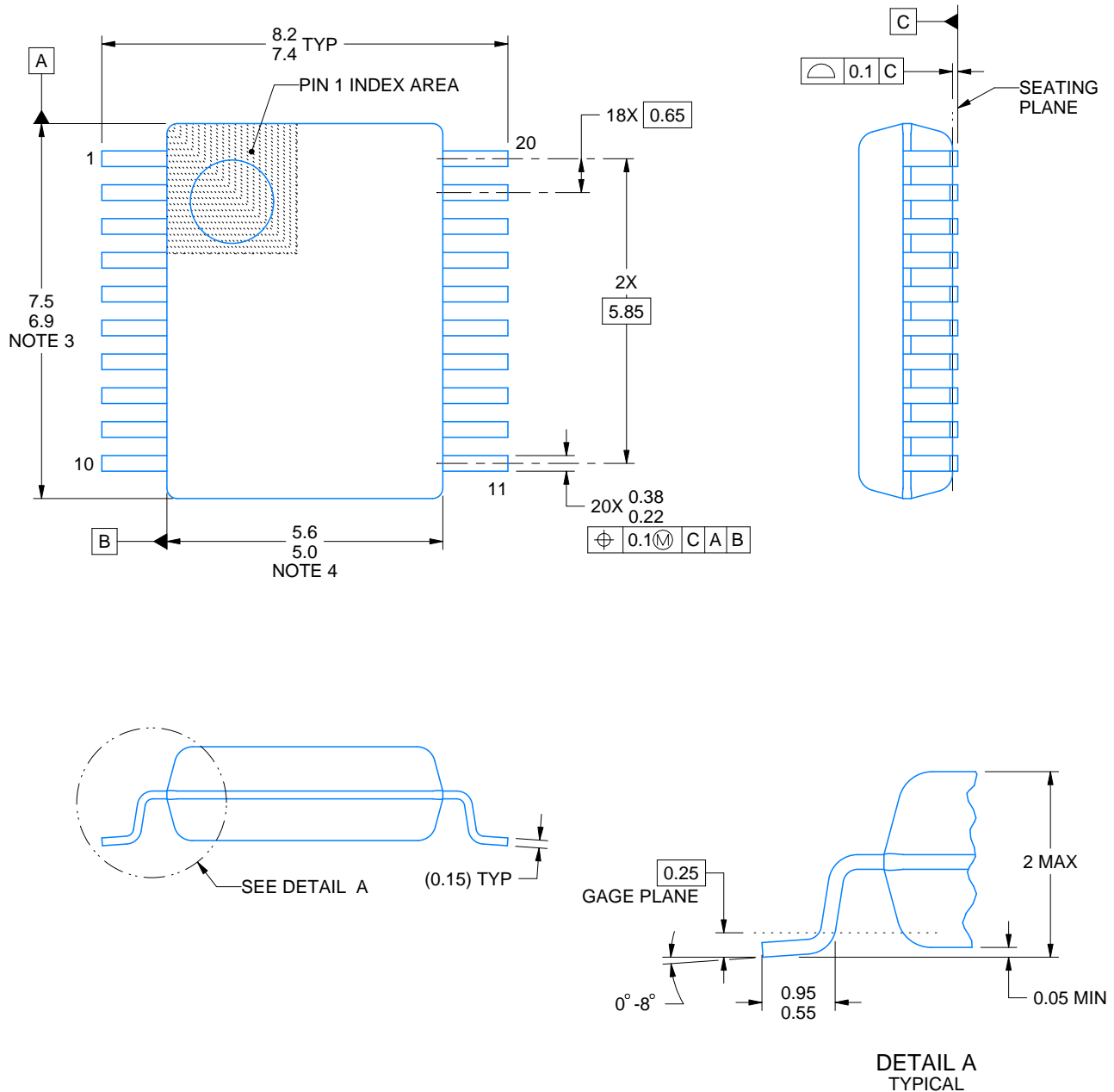

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
GD65232DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
GD65232PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
GD75232DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
GD75232DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
GD75232PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
GD75232PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
GD75232PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
GD65232DWR	SOIC	DW	20	2000	367.0	367.0	45.0
GD65232PWR	TSSOP	PW	20	2000	853.0	449.0	35.0
GD75232DBR	SSOP	DB	20	2000	853.0	449.0	35.0
GD75232DWR	SOIC	DW	20	2000	367.0	367.0	45.0
GD75232PWR	TSSOP	PW	20	2000	853.0	449.0	35.0
GD75232PWR	TSSOP	PW	20	2000	364.0	364.0	27.0
GD75232PWRG4	TSSOP	PW	20	2000	853.0	449.0	35.0

8.2 / 7.4 TYP

A

PIN 1 INDEX AREA

1

20

18X 0.65

7.5 / 6.9 NOTE 3

2X 5.85

10

11

20X 0.38 / 0.22

⊕ 0.1 Ⓜ C A B

B

5.6 / 5.0 NOTE 4

C

⌓ 0.1 C

SEATING PLANE

SEE DETAIL A

(0.15) TYP

GAGE PLANE

0.25

0°-8°

0.95 / 0.55

2 MAX

0.05 MIN

DETAIL A
TYPICAL

4214851/B   08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

20X (1.85)

1

20X (0.45)

18X (0.65)

SYMM

(R0.05) TYP

20

SYMM

10

11

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214851/B   08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (1.85)

SYMM

(R0.05) TYP

1

20

20X (0.45)

18X (0.65)

SYMM

10

11

(7)
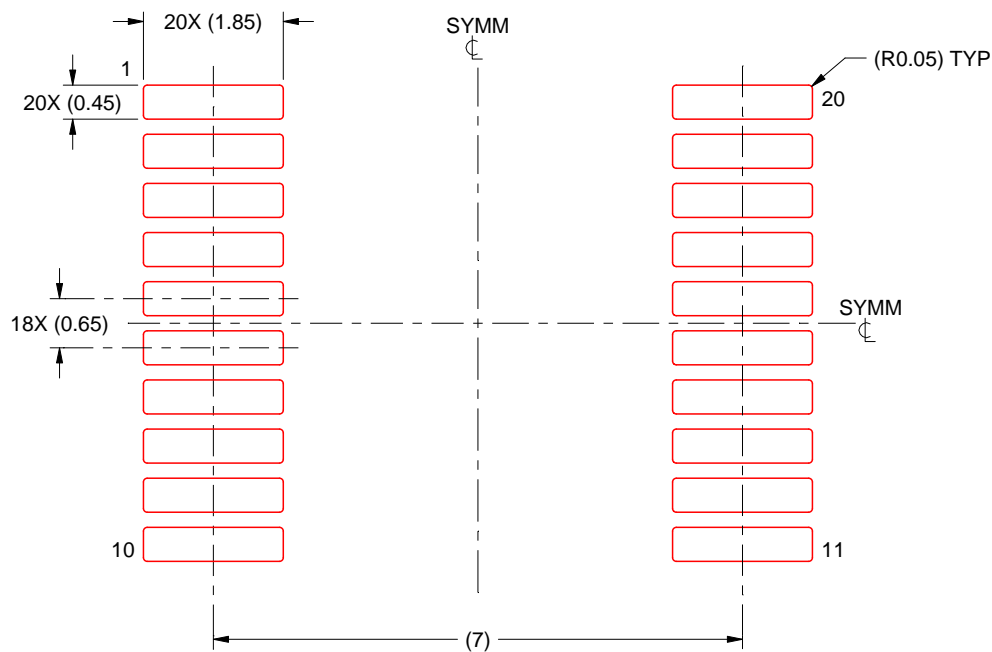
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B   08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ | 0,10 Ⓜ

20   11

Ⓓ 4,50
    4,30   6,60
            6,20

1   10

6,60
6,40

Ⓒ

0,15 NOM

Gage Plane

0,25

0°−8°

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

◁ | 0,10

4040064−5/G 02/11
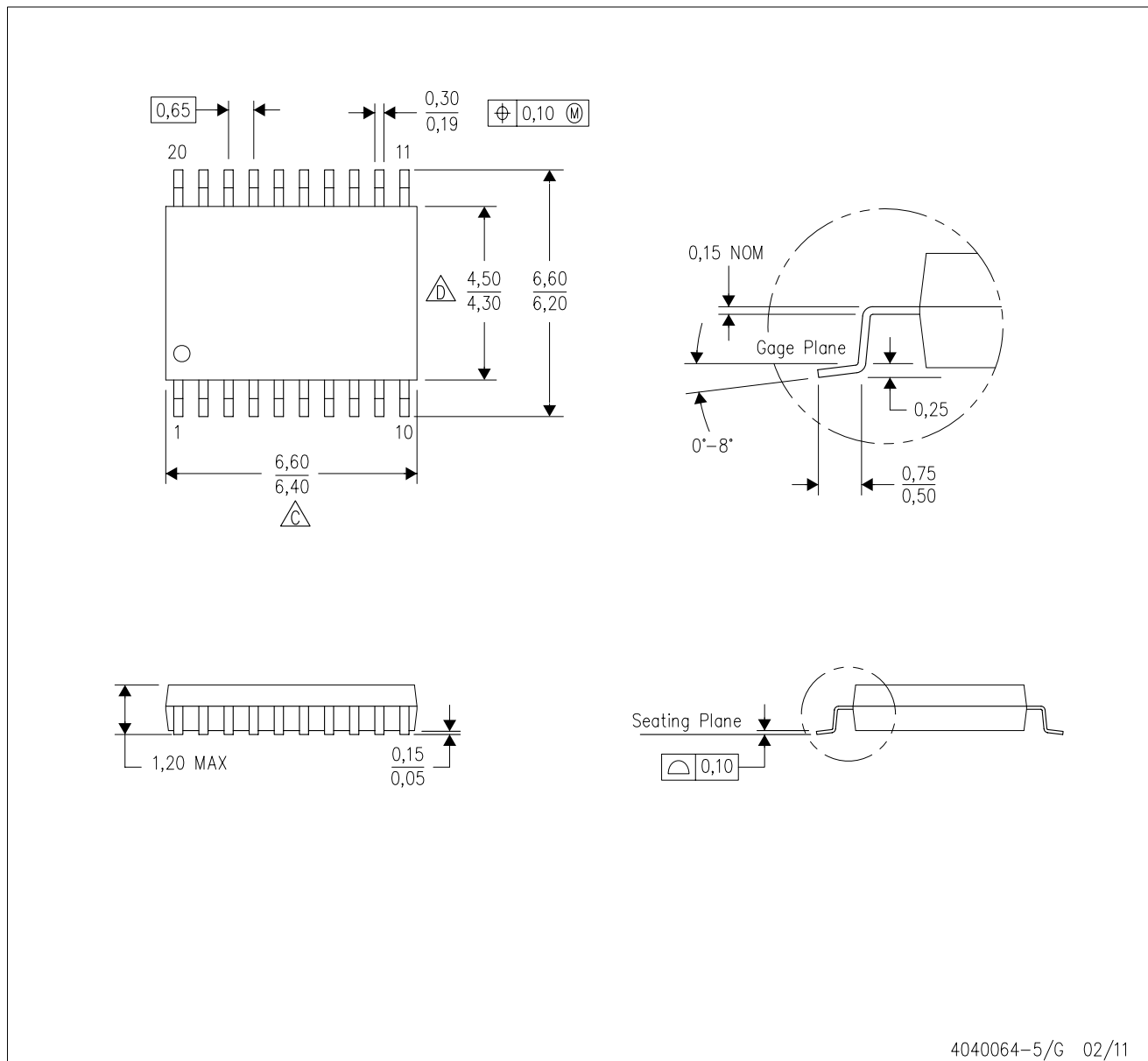
NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         Ⓒ   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
         Ⓓ   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

TEXAS INSTRUMENTS
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PW (R-PDSO-G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

1,55

5,6

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

Pad Geometry

0,07
All Around

4211284-5/G   08/15

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC-7351 is recommended for alternate design.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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N (R−PDIP−T**)

PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN
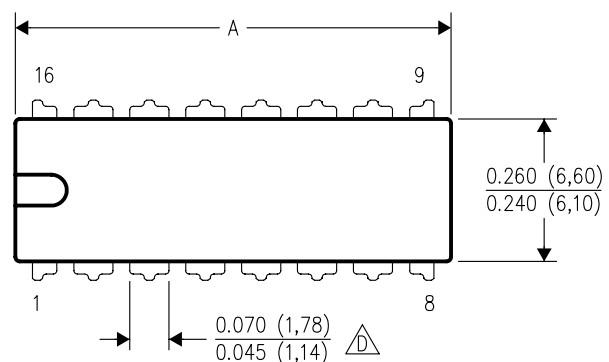
	PINS **	14	16	18	20
DIM					
A MAX		0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN		0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION /C\		AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14) /D\

0.045 (1,14)
0.030 (0,76) /D\

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option /D\
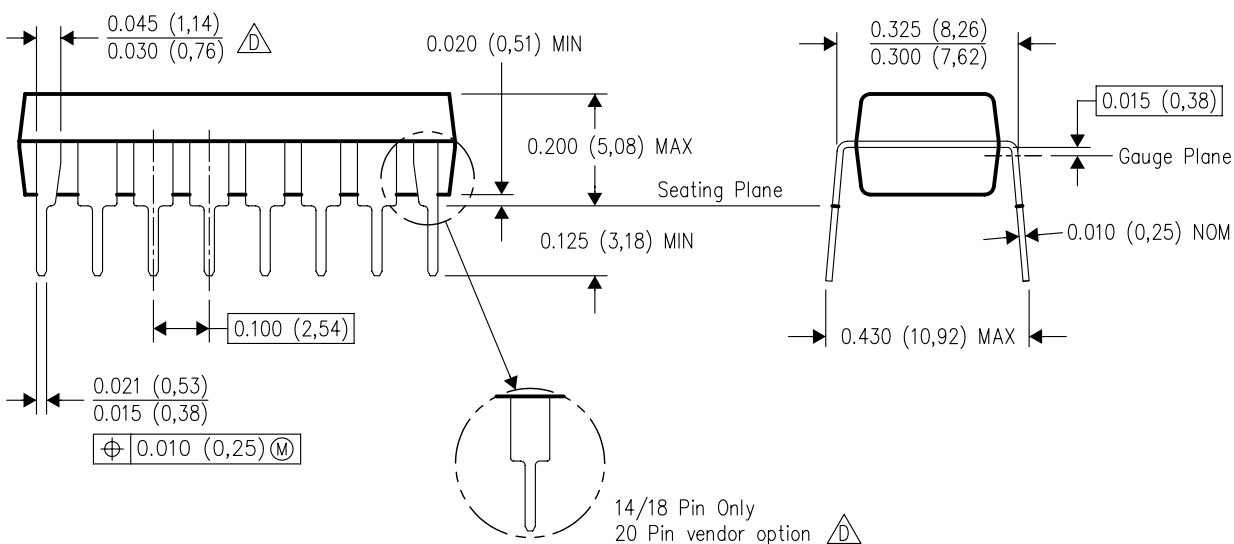
4040049/E   12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
      /C\ Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
      /D\ The 20 pin end lead shoulder width is a vendor option, either half or full width.

10.63 / 9.97 TYP

A

PIN 1 ID
AREA

1

18X 1.27

20

13.0
12.6
NOTE 3

2X
11.43

10

11

B

7.6
7.4

NOTE 4

20X 0.51 / 0.31

⊕ 0.25 Ⓜ C A B

C

SEATING PLANE

� 0.1 C

2.65 MAX

0.33 / 0.10 TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

1.27
0.40

0.3
0.1

DETAIL A
TYPICAL

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

SYMM
¢

1

20

20X (0.6)

18X (1.27)

SYMM
¢

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
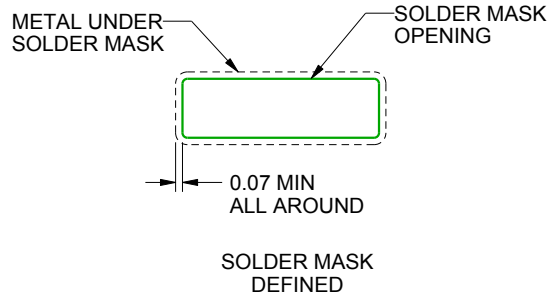
SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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20X (2)

1

20X (0.6)

18X (1.27)

SYMM

20

SYMM

10   11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.