

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

DESCRIPTION/ORDERING INFORMATION

This 16-bit transparent D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH162373 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. This device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. \overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

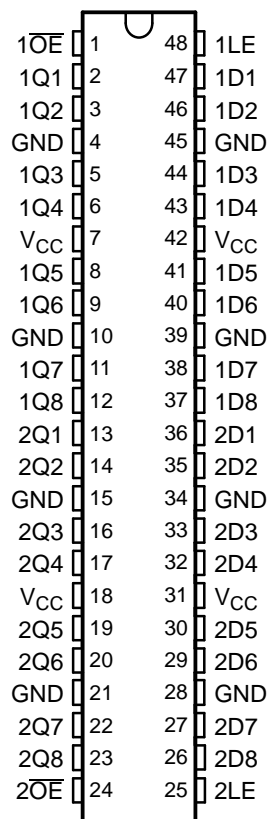
The outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP - DL	Tube	SN74ALVCH162373DL	ALVCH162373
		Tape and reel	SN74ALVCH162373LR	
	TSSOP - DGG	Tape and reel	SN74ALVCH162373GR	ALVCH162373
	VFBGA - GQL	Tape and reel	SN74ALVCH162373KR	VH2373

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DGG OR DL PACKAGE
(TOP VIEW)



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SN74ALVCH162373

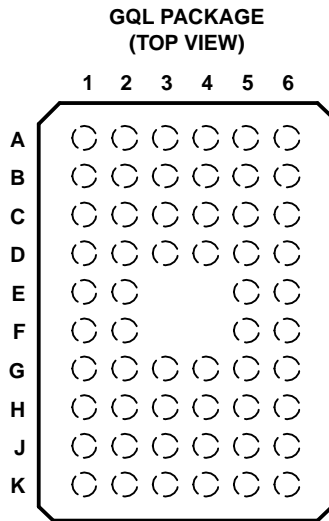
16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES583A—JULY 2004—REVISED OCTOBER 2004

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.



TERMINAL ASSIGNMENTS⁽¹⁾

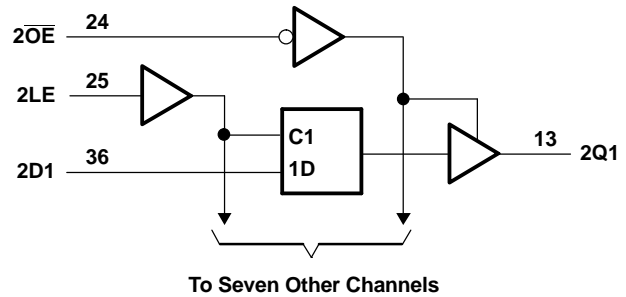
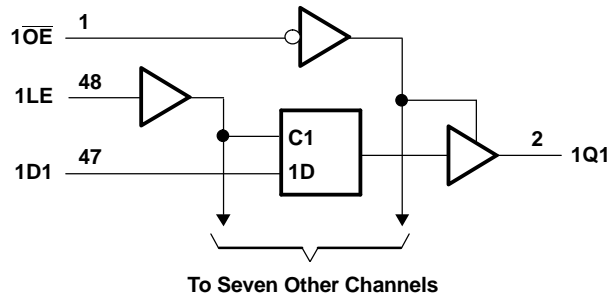
	1	2	3	4	5	6
A	$\overline{1OE}$	NC	NC	NC	NC	1LE
B	1Q2	1Q1	GND	GND	1D1	1D2
C	1Q4	1Q3	V_{CC}	V_{CC}	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
H	2Q5	2Q6	V_{CC}	V_{CC}	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	$\overline{2OE}$	NC	NC	NC	NC	2LE

(1) NC - No internal connection

FUNCTION TABLE (each 8-bit section)

INPUTS			OUTPUT Q
\overline{OE}	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG and DL packages.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	4.6	V
V _I	Input voltage range ⁽²⁾	-0.5	4.6	V
V _O	Output voltage range ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50 mA
I _{OK}	Output clamp current	V _O < 0		-50 mA
I _O	Continuous output current			±50 mA
Continuous current through each V _{CC} or GND				±100 mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DGG package		70
		DL package		63
		GQL package		42
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	1.65	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.65 × V _{CC}
		V _{CC} = 2.3 V to 2.7 V		1.7
		V _{CC} = 2.7 V to 3.6 V		2
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0
		V _{CC} = 2.3 V to 2.7 V		0.35 × V _{CC}
		V _{CC} = 2.7 V to 3.6 V		0.7
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V		-2
		V _{CC} = 2.3 V		-6
		V _{CC} = 2.7 V		-8
		V _{CC} = 3 V		-12
I _{OL}	Low-level output current	V _{CC} = 1.65 V		2
		V _{CC} = 2.3 V		6
		V _{CC} = 2.7 V		8
		V _{CC} = 3 V		12
Δt/Δv	Input transition rise or fall rate			10 ns/V
T _A	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74ALVCH162373
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

SCES583A—JULY 2004—REVISED OCTOBER 2004

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2			V
	I _{OH} = -2 mA	1.65 V	1.2			
	I _{OH} = -4 mA	2.3 V	1.9			
	I _{OH} = -6 mA	2.3 V	1.7			
		3 V	2.4			
	I _{OH} = -8 mA	2.7 V	2			
I _{OH} = -12 mA	3 V	2				
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 2 mA	1.65 V	0.45			
	I _{OL} = 4 mA	2.3 V	0.4			
	I _{OL} = 6 mA	2.3 V	0.55			
		3 V	0.55			
	I _{OL} = 8 mA	2.7 V	0.6			
I _{OL} = 12 mA	3 V	0.8				
I _I	V _I = V _{CC} or GND	3.6 V	±5			μA
I _{I(hold)}	V _I = 0.58 V	1.65 V	25			μA
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
	V _I = 1.7 V	2.3 V	-45			
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	-75			
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±10			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	40			μA
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	750			μA
C _i	Control inputs	V _I = V _{CC} or GND	3			pF
	Data inputs		6			
C _o	Outputs	V _O = V _{CC} or GND	7			pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high or low	3.3		3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE↓	1.1		1.1		1.1		1.1		ns
t _h	Hold time, data after LE↓	1.1		1.1		1.1		1.1		ns

SWITCHING CHARACTERISTICS

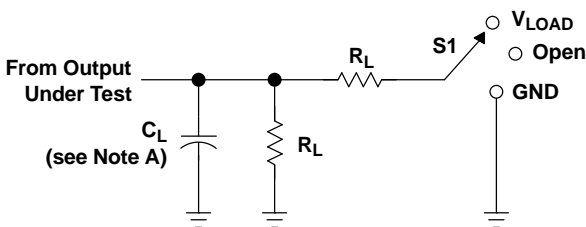
over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	1	6.3	1	5.3	1	4.5	1.1	4	ns
	LE		1	6.6	1	5.6	1	5	1	4.2	
t_{en}	\overline{OE}	Q	1	7.2	1	6.5	1.5	6	1	5	ns
t_{dis}	\overline{OE}	Q	1	6.5	1	5.6	1.5	5.5	1.4	4.5	ns
$t_{sk(o)}$				1		0.5		0.5		0.5	ns

OPERATING CHARACTERISTICS
 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}, f = 10\text{ MHz}$	20	22	26	pF
	Outputs disabled		6	6.5	8	

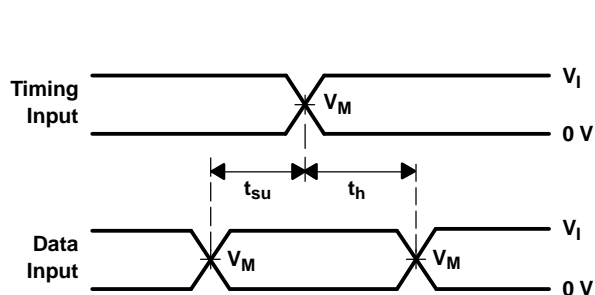
PARAMETER MEASUREMENT INFORMATION



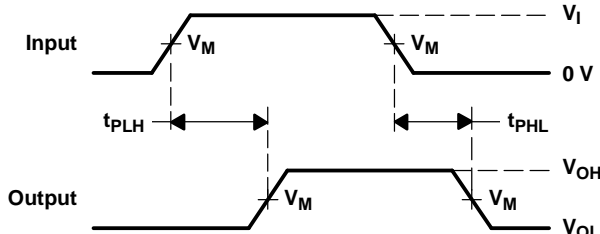
LOAD CIRCUIT

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open V_{LOAD} GND

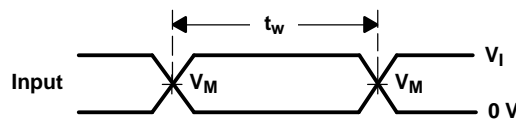
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
1.8 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 V \pm 0.2 V$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3 V \pm 0.3 V$	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



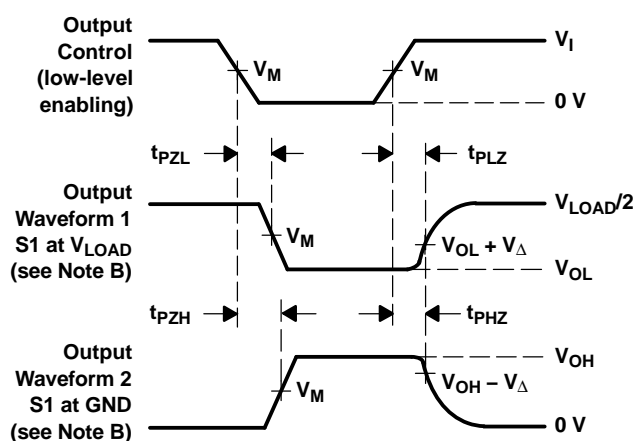
VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74ALVCH162373DLG4	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162373	Samples
SN74ALVCH162373DL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162373	Samples
SN74ALVCH162373GR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162373	Samples
SN74ALVCH162373LR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162373	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH162373GR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ALVCH162373LR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



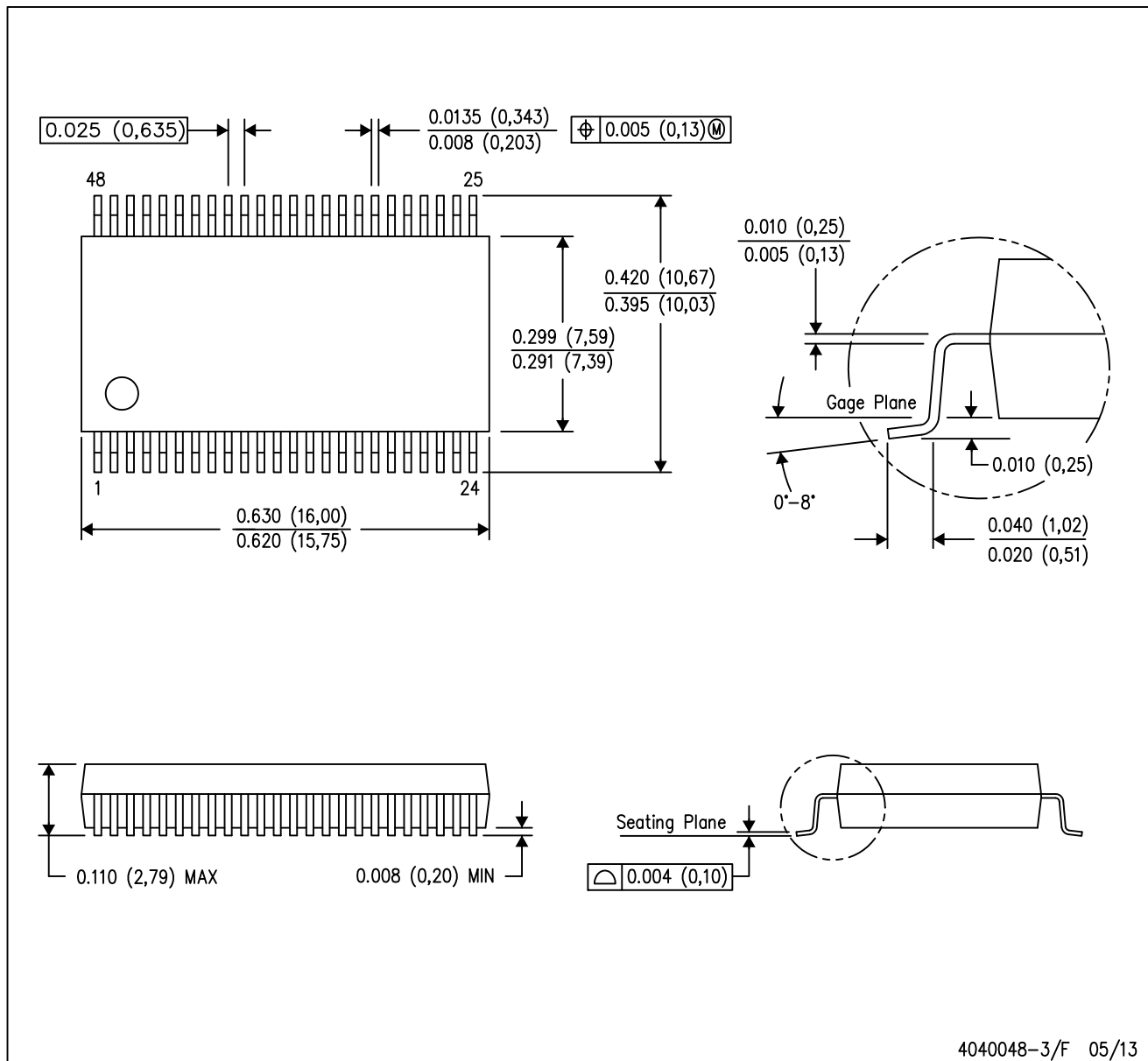
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH162373GR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ALVCH162373LR	SSOP	DL	48	1000	367.0	367.0	55.0

MECHANICAL DATA

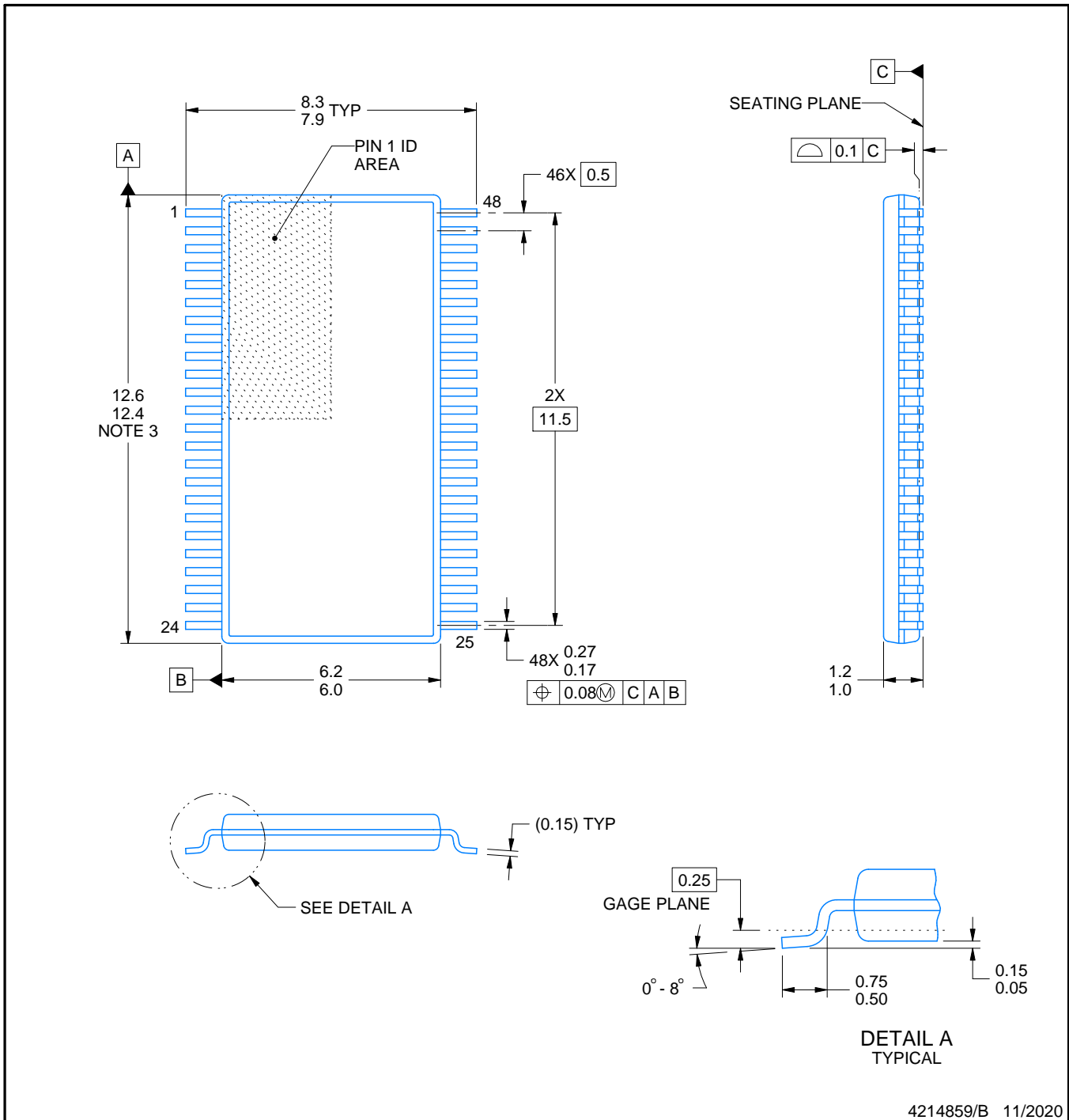
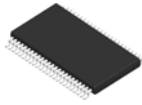
DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



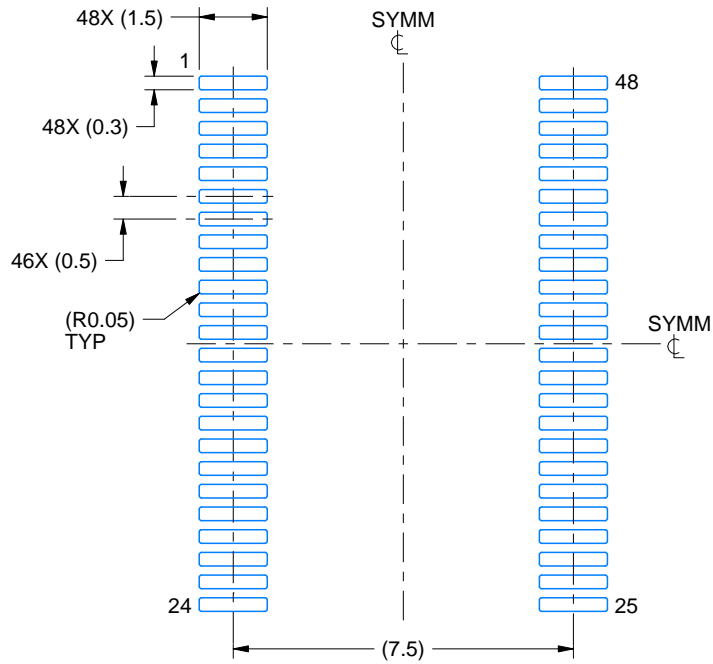
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EXAMPLE BOARD LAYOUT

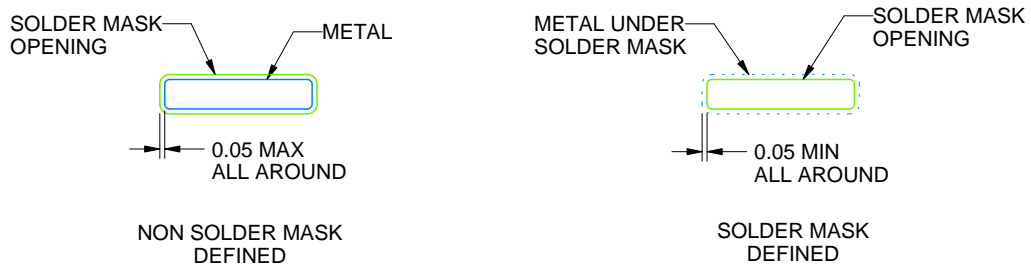
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

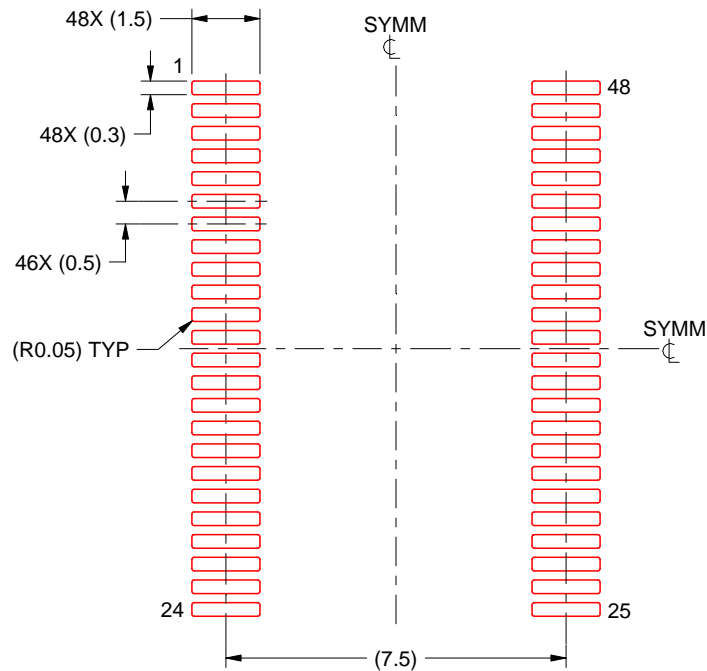
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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