TEXAS INSTRUMENTS

SN74LVC2G74
SCES203Q – APRIL 1999 – REVISED SEPTEMBER 2021

SN74LVC2G74 Single Positive-Edge-Triggered D-Type Flip-Flop With Clear and Preset

1 Features

- Available in the Texas Instruments NanoFree™ package
- Supports 5 V V_{CC} operation
- Inputs accept voltages to 5.5 V
- Maximum t_{pd} of 5.9 ns at 3.3 V
- Low power consumption, 10 µA maximum I_{CC}
- ±24 mA output drive at 3.3 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} supports live insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100 mA Per JESD 78, class II
- ESD protection exceeds JESD 22
  – 2000 V human-body model
  – 200 V machine model
  – 1000 V charged-device model

2 Applications

- Servers
- LED displays
- Network switch
- Telecom infrastructure
- Motor drivers
- I/O expanders

3 Description

This single positive-edge-triggered D-type flip-flop is designed for 1.65 V to 5.5 V V_{CC} operation.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.
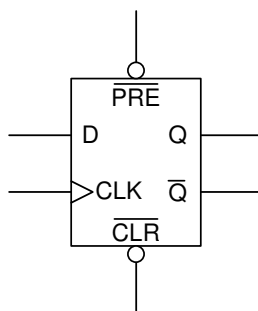
A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) input sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE
SN74LVC2G74	SM8 (8)	2.95 mm × 2.80 mm
	VSSOP (8)	2.30 mm × 2.00 mm
	DSBGA (8)	1.91 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

5 Pin Configuration and Functions
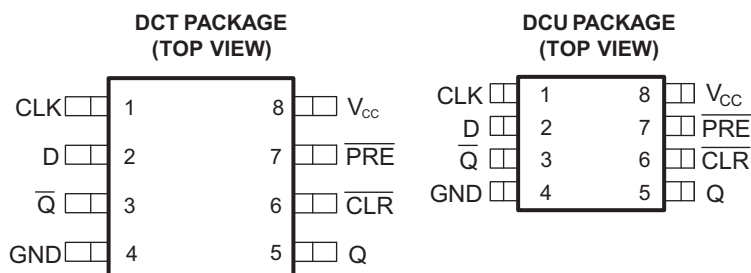
**DCT PACKAGE
(TOP VIEW)**

```
CLK   1        8    Vcc
D     2        7    PRE
Q̄     3        6    CLR
GND   4        5    Q
```

**DCU PACKAGE
(TOP VIEW)**

```
CLK   1        8    Vcc
D     2        7    PRE
Q̄     3        6    CLR
GND   4        5    Q
```

See mechanical drawings for dimensions.

Figure 5-1. DCT 8-Pin SM8 and DCU 8-Pin VSSOP Package Top View

```
          1        2

D       GND       Q

C        Q̄       CLR

B        D        PRE

A       CLK      VCC
```
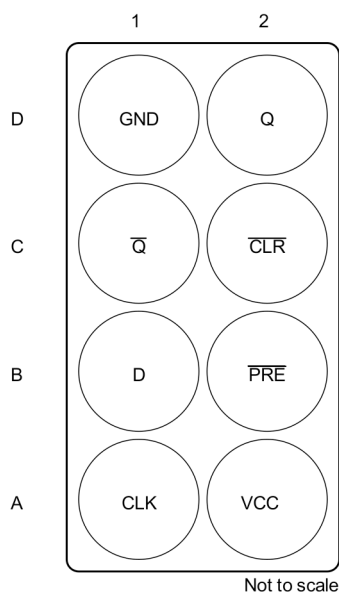
Not to scale

See mecahnical drawings for dimensions.

Figure 5-2. YZP Package 8-Pin DSBGA Bottom View

Table 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	VSSOP, SM8	DSBGA		
CLK	1	A1	I	Clock input
CLR	6	C2	I	Clear input – Pull low to set Q output low
D	2	B1	I	Input
GND	4	D1	—	Ground
PRE	7	B2	I	Preset input – Pull low to set Q output high
Q	5	D2	O	Output
Q̄	3	C1	O	Inverted output
V_{CC}	8	A2	—	Supply

Product Folder Links: *SN74LVC2G74*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	6.5	V
V_I	Input voltage[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2] [3]		−0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		−65	150	°C

(1)   Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Section 6.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2)   The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3)   The value of V_{CC} is provided in *Section 6.3* table.

6.2 ESD Ratings

PARAMETER		DEFINITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	1000	

(1)   JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)   JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Product Folder Links: *SN74LVC2G74*

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	$0.7 \times V_{CC}$		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		$0.3 \times V_{CC}$	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		−4	mA
		V_{CC} = 2.3 V		−8	
		V_{CC} = 3 V		−16	
				−24	
		V_{CC} = 4.5 V		−32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature		−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]	SN74LVC2G74			UNIT
	DCT	DCU	YZP	
	8 PINS			
$R_{\theta JA}$ Junction-to-ambient thermal resistance[2]	220	227	102	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	−40°C to +85°C			−40°C to +125°C Recommended			UNIT
				MIN	TYP[1]	MAX	MIN	TYP	MAX	
V_{OH}		$I_{OH} = -100$ μA	1.65 V to 5.5 V	$V_{CC} - 0.1$			$V_{CC} - 0.1$			V
		$I_{OH} = -4$ mA	1.65 V	1.2			1.2			
		$I_{OH} = -8$ mA	2.3 V	1.9			1.85			
		$I_{OH} = -16$ mA	3 V	2.4			2.4			
		$I_{OH} = -24$ mA		2.3			2.3			
		$I_{OH} = -32$ mA	4.5 V	3.8			3.8			
V_{OL}		$I_{OL} = 100$ μA	1.65 V to 5.5 V			0.1			0.1	V
		$I_{OL} = 4$ mA	1.65 V			0.45			0.45	
		$I_{OL} = 8$ mA	2.3 V			0.3			0.3	
		$I_{OL} = 16$ mA	3 V			0.4			0.4	
		$I_{OL} = 24$ mA				0.55			0.55	
		$I_{OL} = 32$ mA	4.5 V			0.55			0.55	
I_I	Data or control inputs	V_I = 5.5 V or GND	0 to 5.5 V			±5			±5	μA
I_{off}		V_I or V_O = 5.5 V	0			±10			±10	μA
I_{CC}		V_I = 5.5 V or GND, $I_O = 0$	1.65 V to 5.5 V			10			10	μA
ΔI_{CC}		One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500			500	μA
C_i		$V_I = V_{CC}$ or GND	3.3 V		5			5		pF

(1)   All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Timing Requirements, –40°C to +85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM	TO	−40°C to +85°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}				80		175		175		200	MHz
t_w		CLK	6.2		2.7		2.7		2		ns
		$\overline{PRE}$ or $\overline{CLR}$ low	6.2		2.7		2.7		2		
t_{su}		Data	2.9		1.7		1.3		1.1		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	1.9		1.4		1.2		1		
t_h			0		0.3		1.2		0.5		ns

6.7 Timing Requirements, –40°C to +125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM	TO	−40°C to +125°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}				80		120		120		140	MHz
t_w		CLK	6.2		3.5		3.5		3.3		ns
		$\overline{PRE}$ or $\overline{CLR}$ low	6.2		3.5		3.5		3.3		
t_{su}		Data	2.9		2.3		1.9		1.7		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	1.9		2		1.8		1.6		
t_h			0		0.3		0.5		0.5		ns

6.8 Switching Characteristics, –40°C to +85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM	TO	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			80		175		175		200		MHz
t_{pd}	CLK	Q	4.8	13.4	2.2	7.1	2.2	5.9	1.4	4.1	ns
		$\overline{Q}$	6	14.4	3	7.7	2.6	6.2	1.6	4.4	
	$\overline{PRE}$ or $\overline{CLR}$ low	Q or Q	4.4	12.9	2.3	7	1.7	5.9	1.6	4.1	

6.9 Switching Characteristics, –40°C to +125°C

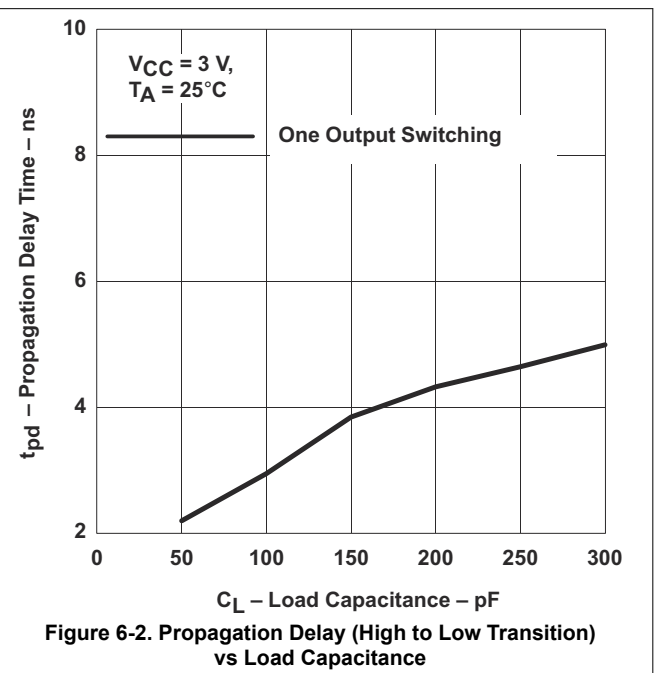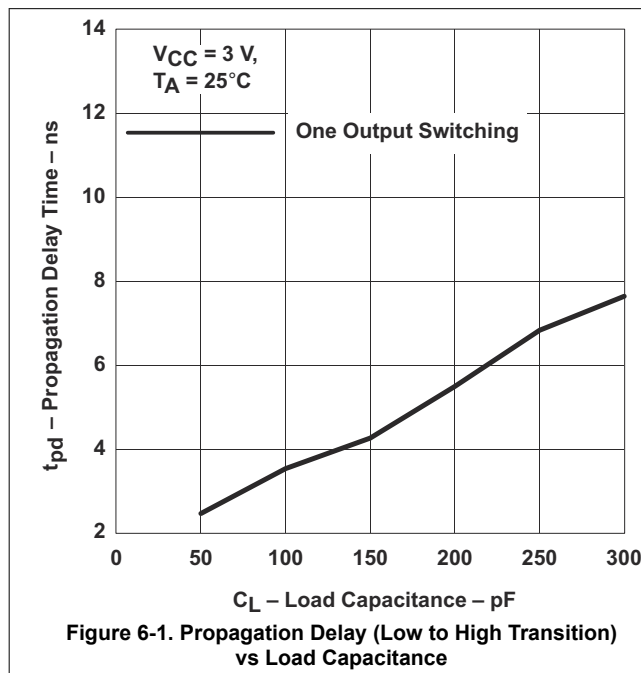over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM	TO	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			80		120		120		140		MHz
t_{pd}	CLK	Q	4.8	14.4	2.2	8.1	2.2	6.9	1.4	5.1	ns
		$\overline{Q}$	6	16	3	9.7	2.6	7.2	1.6	5.4	
	$\overline{PRE}$ or $\overline{CLR}$ low	Q or Q	4.4	14.9	2.3	9.5	1.7	7.9	1.6	6.1	

6.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	35	35	37	40	pF

6.11 Typical Characteristics

Figure 6-1. Propagation Delay (Low to High Transition)
vs Load Capacitance

Figure 6-2. Propagation Delay (High to Low Transition)
vs Load Capacitance

Product Folder Links: SN74LVC2G74

7 Parameter Measurement Information

LOAD CIRCUIT
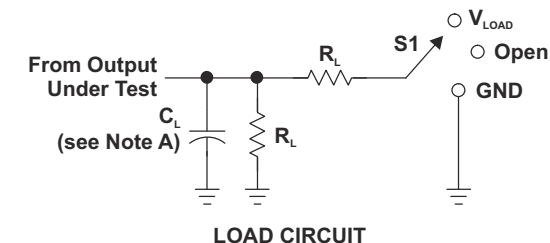
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V

**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
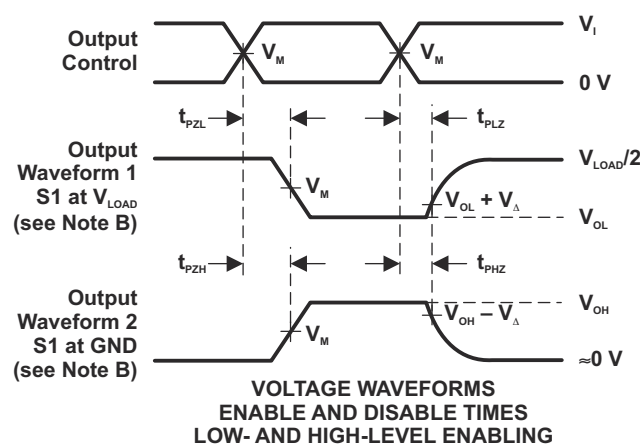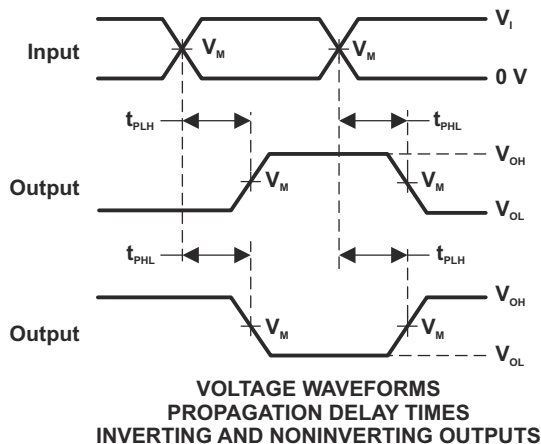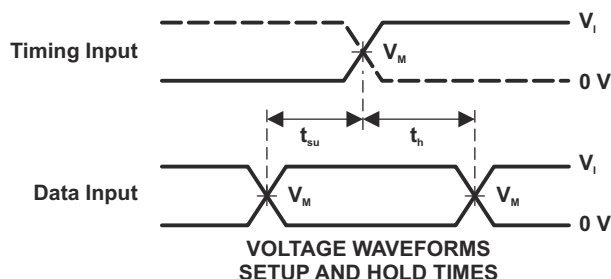PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**
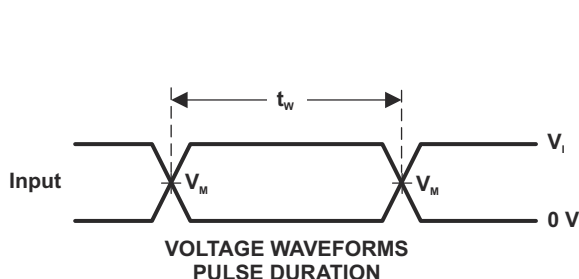
NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 F. t_{PZL} and t_{PZH} are the same as t_{en}.
 G. t_{PLH} and t_{PHL} are the same as t_{pd}.
 H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram
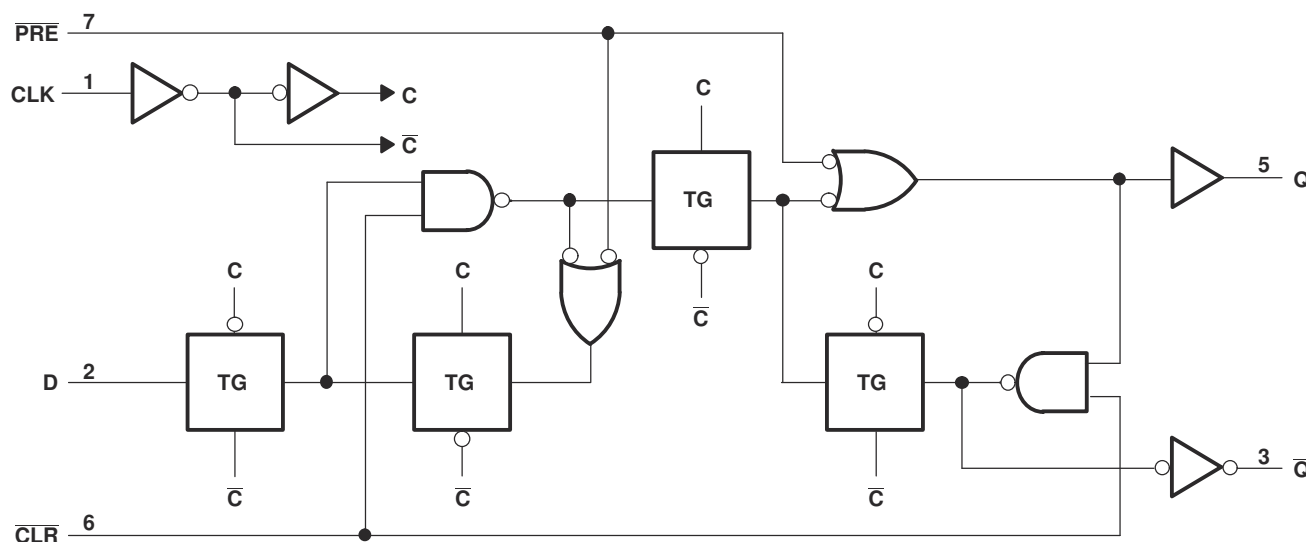
8.3 Feature Description

- Allows down voltage translation
  - 5 V to 3.3 V
  - 5 V or 3.3 V to 1.8 V
- Inputs accept voltage levels up to 5.5 V
- I_{off} Feature
  - Can prevent backflow current that can damage device when powered down.

8.4 Device Functional Modes

Table 8-1 shows the functional modes of SN74LVC2G74.

Table 8-1. Function Table

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H[1]	H[1]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

(1) This configuration is non-stable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

9 Application and Implementation

> **Note**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) input sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The 330 Ω resistor and 22 pF capacitor shown in Figure 9-1 produce enough delay to meet the hold time requirement of the D input. To calculate the delay for a particular RC combination, use Equation 1. The delay with this RC combination is 5.03 ns

$$t_{delay} = -RC \ln(0.5) \approx 0.693 \ RC \qquad (1)$$

To ensure proper operation, check that the transition time of the RC circuit meets the transition time requirements of the device inputs listed in the Recommended Operating Conditions table. Transition time for an RC can be approximated with Equation 2.

$$t_t \approx 2.2 \ RC \qquad (2)$$

In this case, transition time is 18.15 ns, which equates to a 4.54 ns / V input transition rate at VCC = 5 V, and is below the 5 ns / V maximum requirement for recommended operation.
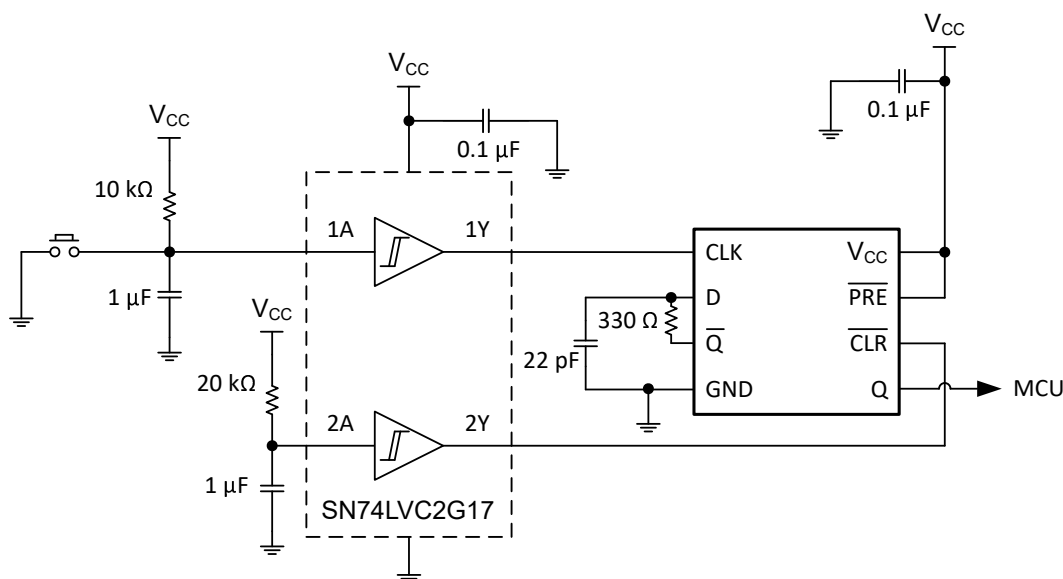
9.2 Typical Power Button Circuit

Figure 9-1. Device Power Button Circuit
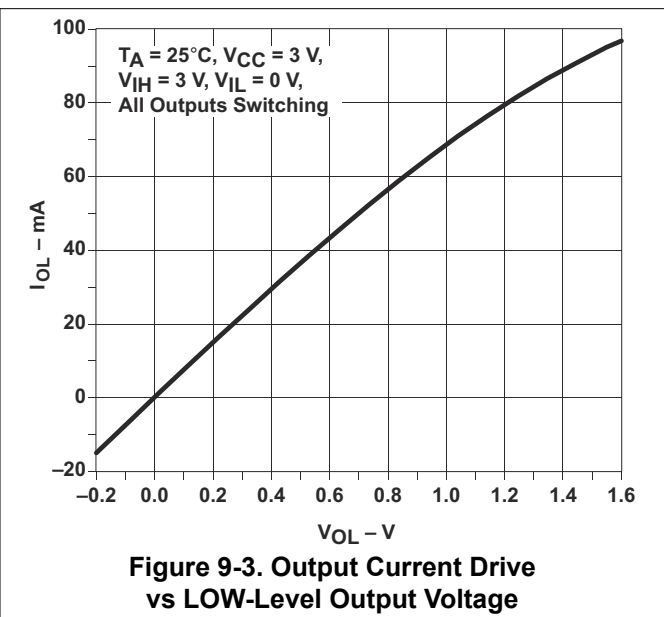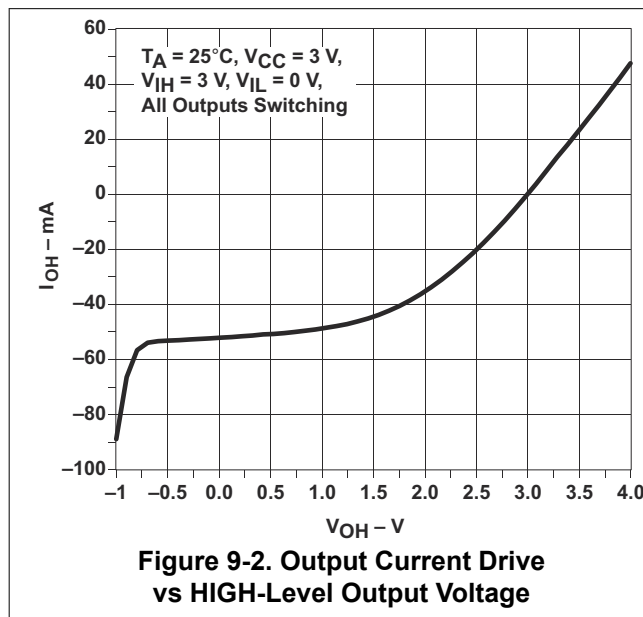
Product Folder Links: *SN74LVC2G74*

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   * For rise time and fall time specifications, see ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
   * For specified high and low levels, see (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   * Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
2. Recommend Output Conditions:
   * Load currents should not exceed 50 mA per output and 100 mA total for the part.
   * Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

9.2.3 Application Curves

Figure 9-2. Output Current Drive vs HIGH-Level Output Voltage

Figure 9-3. Output Current Drive vs LOW-Level Output Voltage

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended and if there are multiple V_{CC} terminals then .01-µF or .022-µF capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 11-1 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.
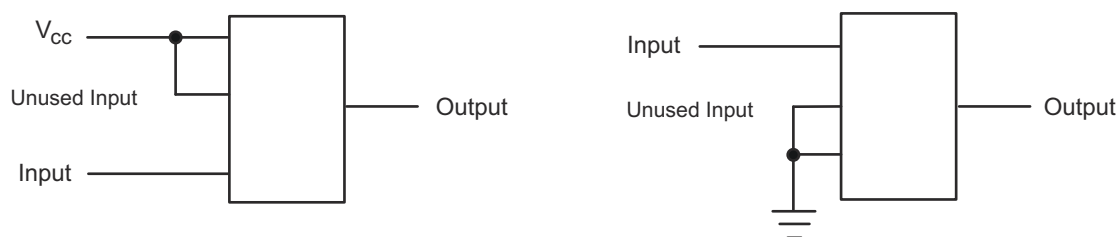
11.2 Layout Example

Figure 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC2G74DCT3	ACTIVE	SM8	DCT	8	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 125	C74 Z	Samples
SN74LVC2G74DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74 Z	Samples
SN74LVC2G74DCTRE4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74 Z	Samples
SN74LVC2G74DCTRE6	ACTIVE	SM8	DCT	8	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 125	C74 Z	Samples
SN74LVC2G74DCTRG4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74 Z	Samples
SN74LVC2G74DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(74, C74J, C74Q, C 74R) CZ	Samples
SN74LVC2G74DCURE4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74R	Samples
SN74LVC2G74DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74R	Samples
SN74LVC2G74DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C74J, C74Q, C74R)	Samples
SN74LVC2G74DCUTE4	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74R	Samples
SN74LVC2G74DCUTG4	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74R	Samples
SN74LVC2G74YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CPN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC2G74 :

• Automotive : SN74LVC2G74-Q1

• Enhanced Product : SN74LVC2G74-EP

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G74DCT3	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G74DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G74DCTRE6	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G74DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G74DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3
SN74LVC2G74DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G74DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G74DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G74YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G74DCT3	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G74DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G74DCTRE6	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G74DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC2G74DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
SN74LVC2G74DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G74DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC2G74DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G74YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

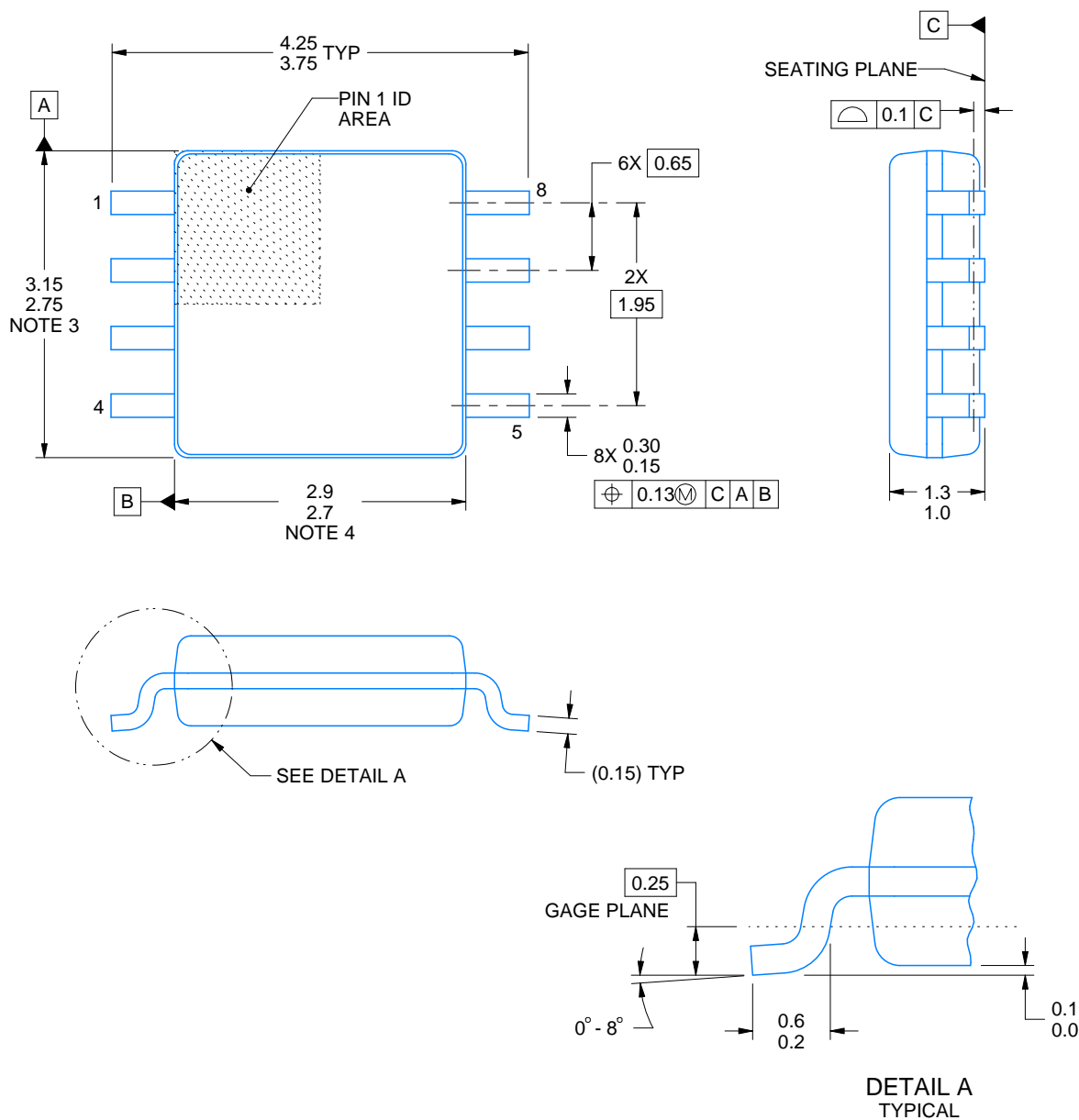DCU (R−PDSO−G8)   PLASTIC SMALL−OUTLINE PACKAGE (DIE DOWN)

4200503/F 07/05

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   Falls within JEDEC MO−187 variation CA.
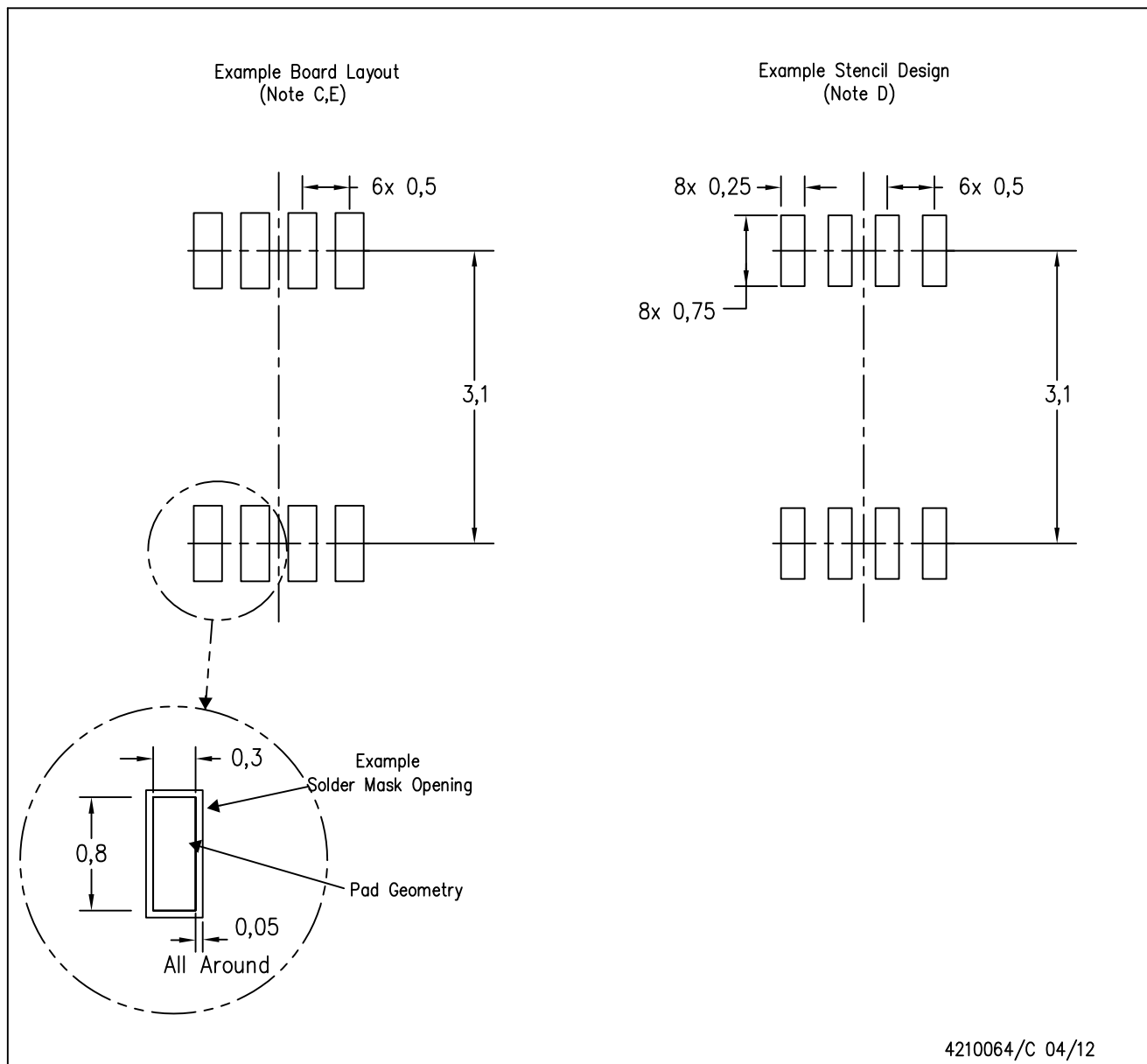
TEXAS
INSTRUMENTS
www.ti.com

DCU (S—PDSO—G8)   PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)

Example Board Layout
(Note C,E)

6x 0,5

3,1

0,3

0,8

0,05

All Around

Example
Solder Mask Opening

Pad Geometry

Example Stencil Design
(Note D)

8x 0,25

6x 0,5

8x 0,75

3,1

4210064/C 04/12

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC—7351 is recommended for alternate designs.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC—7525 for other stencil recommendations.
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

4.25 / 3.75 TYP

PIN 1 ID AREA

A

1

8

6X 0.65

2X 1.95

3.15 / 2.75 NOTE 3

4

5

8X 0.30 / 0.15

⊕ 0.13 Ⓜ C A B

B

2.9 / 2.7 NOTE 4

C

SEATING PLANE

⌒ 0.1 C

1.3 / 1.0

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0° - 8°

0.6 / 0.2

0.1 / 0.0

DETAIL A
TYPICAL

4220784/C   06/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
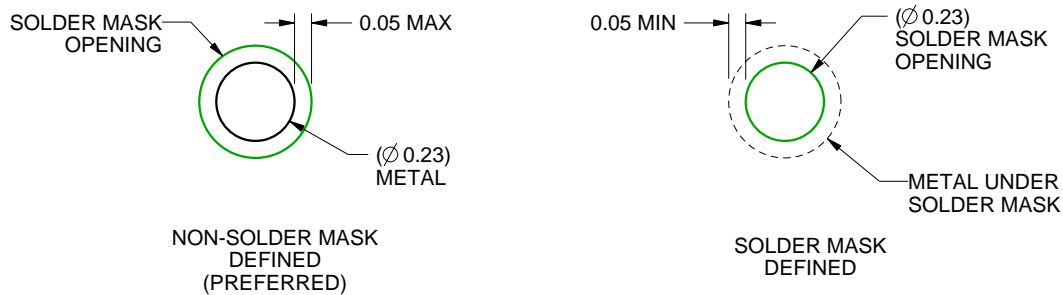2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

8X (1.1)

1

SYMM

(R0.05)
TYP

8

8X (0.4)

SYMM

6X (0.65)

4

5

(3.8)
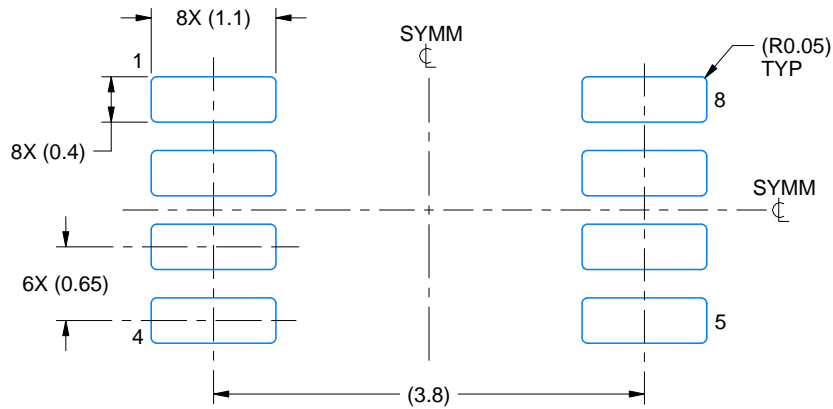
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ALL AROUND

**NON SOLDER MASK
DEFINED**

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ALL AROUND

**SOLDER MASK
DEFINED**
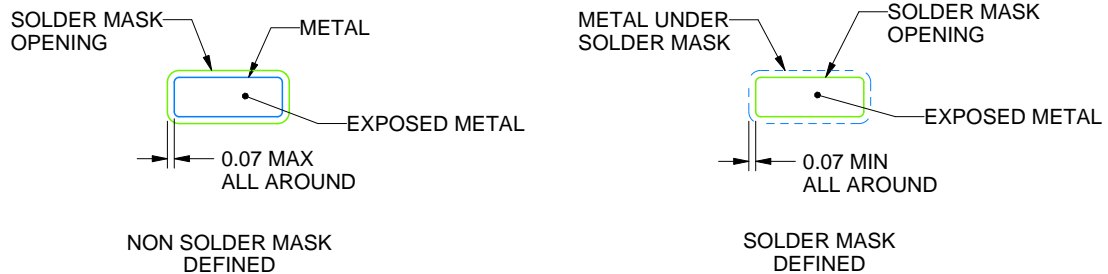
SOLDER MASK DETAILS

4220784/C   06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (1.1)

SYMM

1

8X (0.4)

8

SYMM

6X (0.65)

4

5

(3.8)
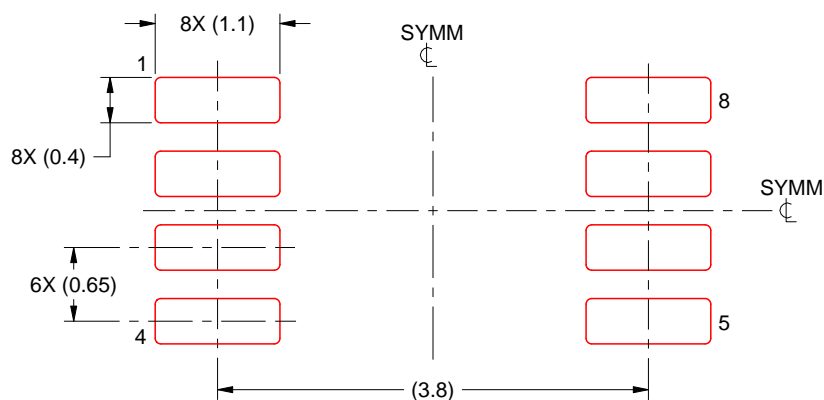
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C   06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
8. Board assembly site may have different recommendations for stencil design.

BALL A1
CORNER

B ◄── E ──► A

D

0.5 MAX

0.19
0.15

C

SEATING PLANE

⌓ 0.05 C

BALL TYP

0.5 TYP

D

C

SYMM
₵

1.5
TYP

B

0.5
TYP

A

D: Max = 1.919 mm, Min =1.858 mm

E: Max = 0.918 mm, Min =0.857 mm

1   2

8X ⌀ 0.25
      0.21

⊕ 0.015Ⓜ C A B

SYMM
₵
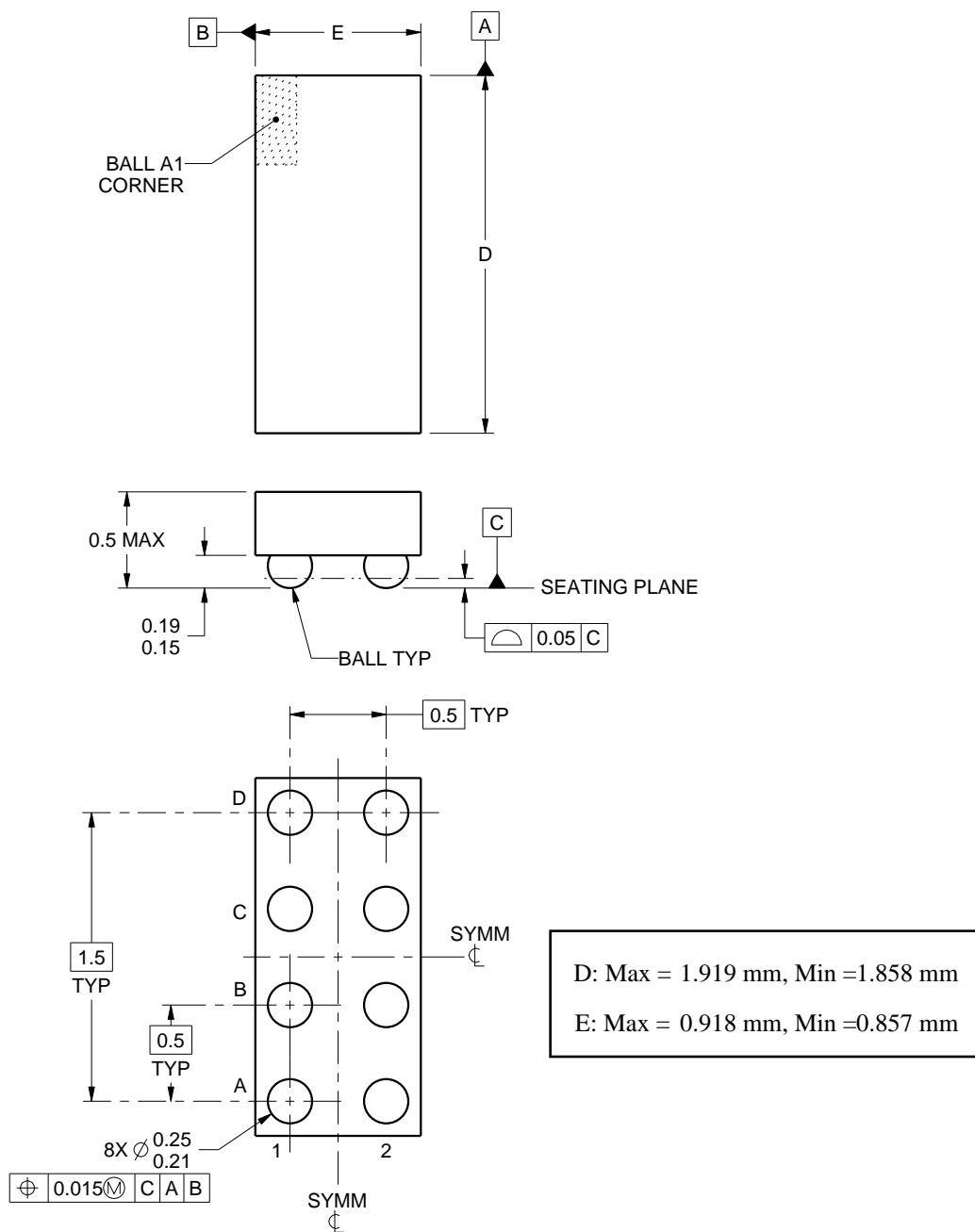
4223082/A   07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.

8X (∅ 0.23)

(0.5) TYP

(0.5) TYP

SYMM ℄

SYMM ℄

LAND PATTERN EXAMPLE
SCALE:40X

SOLDER MASK
OPENING

0.05 MAX

(∅ 0.23)
METAL

NON-SOLDER MASK
DEFINED
(PREFERRED)

0.05 MIN

(∅ 0.23)
SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4223082/A   07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).
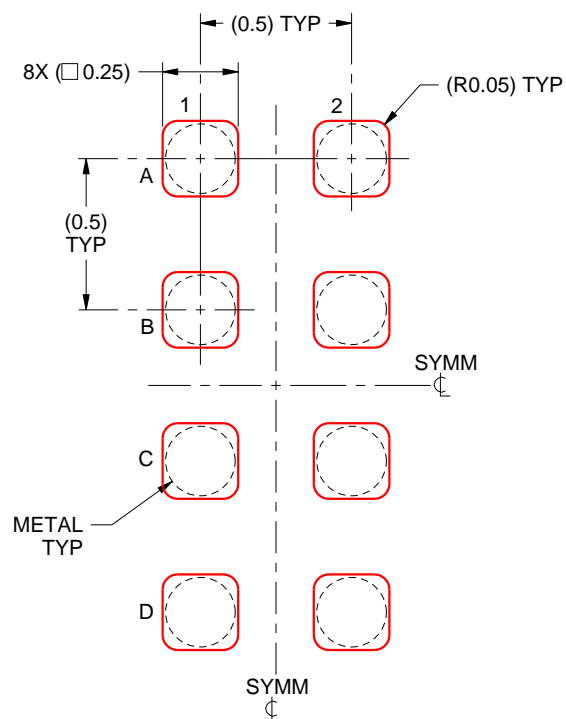
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A   07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.