TEXAS INSTRUMENTS

LMV931-N
LMV932-N, LMV934-N

SNOS993P – NOVEMBER 2001 – REVISED APRIL 2017

LMV93x-N Single, Dual, Quad 1.8-V, RRIO Operational Amplifiers

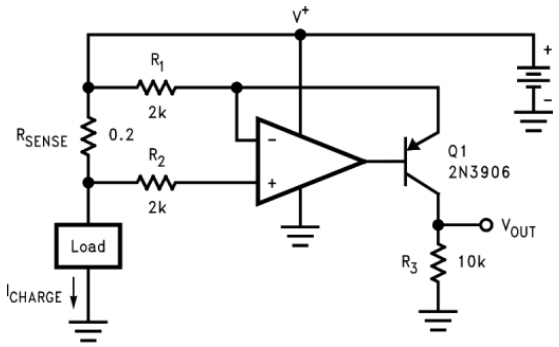
1 Features

- Typical 1.8-V Supply Values; Unless Otherwise Noted
- Specified at 1.8 V, 2.7 V and 5 V
- Output Swing
  - With 600-Ω Load 80 mV from Rail
  - With 2-kΩ Load 30 mV from Rail
- V_{CM} 200 mV Beyond Rails
- Supply Current (per Channel) 100 μA
- Gain Bandwidth Product 1.4 MHz
- Maximum V_{OS} 4 mV
- Ultra Tiny Packages
- Temperature Range −40°C to +125°C
- Create a Custom Design Using the LMV93x-N With the WEBENCH® Power Designer

2 Applications

- Phones
- Tablets
- Wearables
- Health Monitoring
- Portable and Battery-Powered Electronic Equipment
- Battery Monitoring

High-Side Current Sense Amplifier



$$V_{OUT} = \frac{R_{SENSE} \bullet R_3}{R_1} \bullet I_{Charge} = 1\,\Omega \bullet I_{Charge}$$

3 Description

The LMV93x-N family (LMV931-N single, LMV932-N dual and LMV934-N quad) are low-voltage, low-power operational amplifiers. The LMV93x-N family operates from 1.8-V to 5.5-V supply voltages and have rail-to-rail input and output. The input common-mode voltage extends 200 mV beyond the supplies which enables user enhanced functionality beyond the supply voltage range. The output can swing rail-to-rail unloaded and within 105 mV from the rail with 600-Ω load at 1.8-V supply. The LMV93x-N devices are optimized to work at 1.8 V, which make them ideal for portable two-cell, battery-powered systems and single-cell Li-Ion systems.

LMV93x-N devices exhibit an excellent speed-power ratio, achieving 1.4-MHz gain bandwidth product at 1.8-V supply voltage with very low supply current. The LMV93x-N devices can drive a 600-Ω load and up to 1000-pF capacitive load with minimal ringing. These devices also have a high DC gain of 101 dB, making them suitable for low-frequency applications.

The single LMV93x-N is offered in space-saving 5-pin SC70 and SOT-23 packages. The dual LMV932-N are in 8-pin VSSOP and SOIC packages and the quad LMV934-N are in 14-pin TSSOP and SOIC packages. These small packages are ideal solutions for area constrained PC boards and portable electronics such as mobile phones and tablets.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV931-N	SOT-23 (5)	2.90 mm × 1.60 mm
	SC-70 (5)	2.00 mm × 1.25 mm
LMV932-N	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.91 mm
LMV934-N	TSSOP (8)	5.00 mm × 4.40 mm
	SOIC (14)	8.60 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (December 2014) to Revision P — **Page**

- Deleted information specific to automotive grade - created separate automotive data sheet SNOSD49 ... 1
- Added links for WEBENCH ... 1
- Moved storage temperature to *Abs Max* table and changed *Handling Ratings* tables to *ESD Ratings* tables per new format ... 4
- Changed values in the *Thermal Information* table to align with JEDEC standards ... 4
- Changed Slew Rate vs Supply Voltage title to reflect LMV931 and LMV934 only ... 14
- Added Slew Rate vs Supply graph for LMV932 only ... 14
- Added *Receiving Notification of Documentation Updates* and *Community Resources* subsections ... 25

Changes from Revision N (June 2014) to Revision O — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout* , *Device and Documentation Support* , and *Mechanical, Packaging, and Orderable Information* sections ... 1

Changes from Revision M (November 2013) to Revision N — **Page**

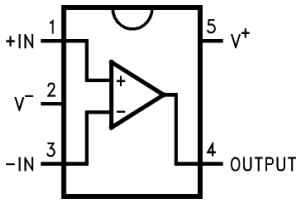
- Complete rewrite for GDS standard. ... 1
- Added LMV934-N-Q1. The other Q grades were added in previous revision. ... 1

Changes from Revision L (March 2013) to Revision M — **Page**

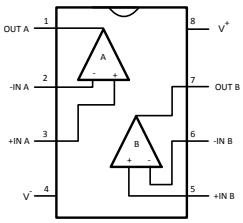
- Added Automotive Q Grade. ... 1

5 Pin Configuration and Functions

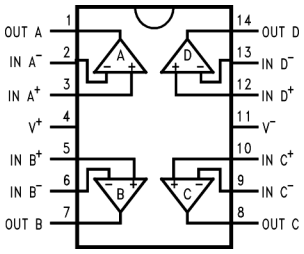
DBV and DCK Package
5-Pin SC-70 and SOT-23
LMV931-N Top View



DGK and D Package
8-Pin VSSOP and SOIC
LMV932-N Top View



DGK and D Package
14-Pin TSSOP and SOIC
LMV934-N Top View



Pin Functions: LMV931

PIN		I/O	DESCRIPTION
NAME	LMV931 DBV, DCK		
+IN	1	I	Noninverting Input
-IN	3	I	Inverting Input
OUT	4	O	Output
V-	2	P	Negative Supply
V+	5	P	Positive Supply

Pin Functions: LMV932 and LMV934

PIN			I/O	DESCRIPTION
NAME	LMV932 D, DGK	LMV934 D, PW		
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	—	10	I	Noninverting input, channel C
+IN D	—	12	I	Noninverting input, channel D
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	—	9	I	Inverting input, channel C
–IN D	—	13	I	Inverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	—	8	O	Output, channel C
OUT D	—	14	O	Output, channel D
V+	8	4	P	Positive (highest) power supply
V–	4	11	P	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2).

	MIN	MAX	UNIT
Supply voltage ($V^+ – V^-$)	–0.3	6	V
Differential input voltage	V^-	V^+	V
Voltage at input/output pins	(V^-) - 0.3	(V^+) + 0.3	V
Junction temperature(3)	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not specified. For specifications and the test conditions, see the *Electrical Characteristics*.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}–T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board.

6.2 ESD Ratings (Commercial)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	
		Machine model (MM)(3)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Machine model, 200 Ω in series with 100 pF.

6.3 Recommended Operating Ratings

See(1).

	MIN	MAX	UNIT
Supply voltage range ($V^+ – V^-$)	1.8	5.5	V
Ambient temperature	−40	125	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not specified. For specifications and the test conditions, see the *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC(1)		LMV931-N		LMV932-N		LMV934-N		UNIT
		DBV (SOT-23)	DCK (SC70)	D (SOIC)	DGK (VSSOP)	D (SOIC)	PW (TSSOP)	
		5 PINS	5 PINS	8 PINS	8 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	197.2	285.9	125.9	184.5	94.4	124.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	156.7	115.9	70.2	74.3	52.5	51.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.6	63.7	66.5	105.1	48.9	67.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	41.4	4.5	19.8	13.1	14.3	6.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55	62.9	65.9	103.6	48.6	66.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 DC Electrical Characteristics 1.8 V

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 1.8 V, V^- = 0 V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
V_{OS}	Input Offset Voltage	LMV931 (Single)	25°C		1	4	mV
			Full Range			6	
		LMV932 (Dual), LMV934 (Quad)	25°C		1	5.5	mV
			Full Range			7.5	
TCV_{OS}	Input Offset Voltage Average Drift		Full Range		5.5		µV/°C
I_B	Input Bias Current		25°C		15	35	nA
			Full Range			50	
I_{OS}	Input Offset Current		25°C		13	25	nA
			Full Range			40	
I_S	Supply Current (per channel)		25°C		103	185	µA
			Full Range			205	
CMRR	Common-Mode Rejection Ratio	LMV931, 0 ≤ V_{CM} ≤ 0.6 V 1.4 V ≤ V_{CM} ≤ 1.8 V (2)	25°C	60	78		dB
			Full Range	55			
		LMV932 and LMV934 0 ≤ V_{CM} ≤ 0.6 V 1.4 V ≤ V_{CM} ≤ 1.8 V (2)	25°C	55	76		dB
			Full Range	50			
		−0.2 V ≤ V_{CM} ≤ 0 V 1.8 V ≤ V_{CM} ≤ 2.0 V	25°C	50	72		dB
PSRR	Power Supply Rejection Ratio	1.8 V ≤ V^+ ≤ 5 V	25°C	75	100		dB
			Full Range	70			
CMVR	Input Common-Mode Voltage Range	For CMRR Range ≥ 50dB	25°C	V^- − 0.2	−0.2 to 2.1	V^+ + 0.2	V
			−40°C to 85°C	V^-		V^+	
			125°C	V^- + 0.2		V^+ − 0.2	
A_V	Large Signal Voltage Gain LMV931-N (Single)	R_L = 600 Ω to 0.9 V, V_O = 0.2 V to 1.6 V, V_{CM} = 0.5 V	25°C	77	101		dB
			Full Range	73			
		R_L = 2 kΩ to 0.9 V, V_O = 0.2 V to 1.6 V, V_{CM} = 0.5 V	25°C	80	105		dB
			Full Range	75			
	Large Signal Voltage Gain LMV932-N (Dual) LMV934-N (Quad)	R_L = 600 Ω to 0.9 V, V_O = 0.2 V to 1.6 V, V_{CM} = 0.5 V	25°C	75	90		dB
			Full Range	72			
		R_L = 2 kΩ to 0.9 V, V_O = 0.2 V to 1.6 V, V_{CM} = 0.5 V	25°C	78	100		dB
			Full Range	75			
V_O	Output Swing	R_L = 600 Ω to 0.9 V V_{IN} = ±100 mV	25°C	1.65	1.72		V
					0.077	0.105	
			Full Range	1.63		0.120	
		R_L = 2 kΩ to 0.9 V V_{IN} = ±100 mV	25°C	1.75	1.77		V
					0.024	0.035	
			Full Range	1.74		0.04	

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(2) For specified temperature ranges, see the CMVR parameter in *DC Electrical Characteristics 1.8 V* for the input common-mode voltage specifications.

DC Electrical Characteristics 1.8 V (continued)

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 1.8 V, V^- = 0 V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
I_O	Output Short Circuit Current (3)	Sourcing, V_O = 0 V V_{IN} = 100 mV	25°C	4	8		mA
			Full Range	3.3			
		Sinking, V_O = 1.8 V V_{IN} = −100 mV	25°C	7	9		mA
			Full Range	5			

(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

6.6 AC Electrical Characteristics 1.8 V

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 1.8 V, V^- = 0 V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
SR	Slew Rate	See (2).		0.35		V/μs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			67		deg
G_m	Gain Margin			7		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, V_{CM} = 0.5 V		60		nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		pA/√Hz
THD	Total Harmonic Distortion	f = 1 kHz, A_V = +1 R_L = 600 Ω, V_{IN} = 1 V_{PP}		0.023%		
	Amplifier-to-Amplifier Isolation	See (3)		123		dB

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(2) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.
(3) Input referred, R_L = 100 kΩ connected to $V^+/2$. Each amplifier excited in turn with 1 kHz to produce V_O = 3 V_{PP} (For supply voltages < 3 V, V_O = V^+).

6.7 DC Electrical Characteristics 2.7 V

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 2.7 V, V^- = 0 V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
V_{OS}	Input Offset Voltage	LMV931 (Single)	25°C		1	4	mV
			Full Range			6	
		LMV932 (Dual) LMV934 (Quad)	25°C		1	5.5	mV
			Full Range			7.5	
TCV_{OS}	Input Offset Voltage Average Drift		Full Range		5.5		μV/°C
I_B	Input Bias Current		25°C		15	35	nA
			Full Range			50	
I_{OS}	Input Offset Current		25°C		8	25	nA
			Full Range			40	
I_S	Supply Current (per channel)		25°C		105	190	μA
			Full Range			210	

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

DC Electrical Characteristics 2.7 V (continued)

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 2.7 V, V^- = 0 V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
CMRR	Common-Mode Rejection Ratio	LMV931, 0 ≤ V_{CM} ≤ 1.5 V 2.3 V ≤ V_{CM} ≤ 2.7 V(2)	25°C	60	81		dB
			Full Range	55			
		LMV932 and LMV934 0 ≤ V_{CM} ≤ 1.5 V 2.3 V ≤ V_{CM} ≤ 2.7 V(2)	25°C	55	80		dB
			Full Range	50			
		−0.2 V ≤ V_{CM} ≤ 0 V 2.7 V ≤ V_{CM} ≤ 2.9 V	25°C	50	74		dB
PSRR	Power Supply Rejection Ratio	1.8 V ≤ V^+ ≤ 5 V V_{CM} = 0.5 V	25°C	75	100		dB
			Full Range	70			
V_{CM}	Input Common-Mode Voltage Range	For CMRR Range ≥ 50 dB	25°C	V^- − 0.2	−0.2 to 3.0	V^+ + 0.2	V
			−40°C to 85°C	V^-		V^+	
			125°C	V^- + 0.2		V^+ − 0.2	
A_V	Large Signal Voltage Gain LMV931-N (Single)	R_L = 600 Ω to 1.35 V, V_O = 0.2 V to 2.5 V	25°C	87	104		dB
			Full Range	86			
		R_L = 2 kΩ to 1.35 V, V_O = 0.2 V to 2.5 V	25°C	92	110		dB
			Full Range	91			
	Large Signal Voltage Gain LMV932-N (Dual) LMV934-N (Quad)	R_L = 600 Ω to 1.35 V, V_O = 0.2 V to 2.5 V	25°C	78	90		dB
			Full Range	75			
		R_L = 2 kΩ to 1.35 V, V_O = 0.2 V to 2.5 V	25°C	81	100		dB
			Full Range	78			
V_O	Output Swing	R_L = 600 Ω to 1.35 V V_{IN} = ±100 mV	25°C	2.55	2.62		V
					0.083	0.110	
			Full Range	2.53		0.130	
		R_L = 2 kΩ to 1.35 V V_{IN} = ±100 mV	25°C	2.65	2.675		V
					0.025	0.04	
			Full Range	2.64		0.045	
I_O	Output Short Circuit Current(3)	Sourcing, V_O = 0 V V_{IN} = +100 mV	25°C	20	30		mA
			Full Range	15			
		Sinking, V_O = 2.7 V V_{IN} = −100 mV	25°C	18	25		mA
			Full Range	12			

(2) For specified temperature ranges, see the CMVR parameter in *DC Electrical Characteristics 1.8 V* for the input common-mode voltage specifications.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

6.8 AC Electrical Characteristics 2.7 V

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1.0 V, V_O = 1.35 V and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
SR	Slew Rate	See(2)		0.4		V/µs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			70		deg
G_m	Gain Margin			7.5		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, V_{CM} = 0.5 V		57		nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		pA/√Hz

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(2) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.

AC Electrical Characteristics 2.7 V (continued)

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1.0 V, V_O = 1.35 V and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
THD	Total Harmonic Distortion	f = 1 kHz, A_V = +1 R_L = 600 Ω, V_{IN} = 1 V_{PP}		0.022%		
	Amp-to-Amp Isolation	See (3)		123		dB

(3) Input referred, R_L = 100 kΩ connected to $V^+/2$. Each amplifier excited in turn with 1 kHz to produce V_O = 3 V_{PP} (For supply voltages < 3 V, V_O = V^+).

6.9 Electrical Characteristics 5 V DC

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 5 V, V^- = 0 V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
V_{OS}	Input Offset Voltage	LMV931 (Single)	25°C		1	4	mV
			Full Range			6	
		LMV932 (Dual) LMV934 (Quad)	25°C		1	5.5	mV
			Full Range			7.5	
TCV_{OS}	Input Offset Voltage Average Drift				5.5		µV/°C
I_B	Input Bias Current		25°C		14	35	nA
			Full Range			50	
I_{OS}	Input Offset Current		25°C		9	25	nA
			Full Range			40	
I_S	Supply Current (per channel)		25°C		116	210	µA
			Full Range			230	
CMRR	Common-Mode Rejection Ratio	0 ≤ V_{CM} ≤ 3.8 V 4.6 V ≤ V_{CM} ≤ 5 V (2)	25°C	60	86		dB
			Full Range	55			
		−0.2 V ≤ V_{CM} ≤ 0 V 5 V ≤ V_{CM} ≤ 5.2 V	25°C	50	78		dB
PSRR	Power Supply Rejection Ratio	1.8 V ≤ V^+ ≤ 5 V V_{CM} = 0.5 V	25°C	75	100		dB
			Full Range	70			
CMVR	Input Common-Mode Voltage Range	For CMRR Range ≥ 50 dB	25°C	V^- − 0.2	−0.2 to 5.3	V^+ + 0.2	V
			−40°C to 85°C	V^-		V^+	
			125°C	V^- + 0.3		V^+ − 0.3	
A_V	Large Signal Voltage Gain LMV931-N (Single)	R_L = 600 Ω to 2.5 V, V_O = 0.2 V to 4.8 V	25°C	88	102		dB
			Full Range	87			
		R_L = 2 kΩ to 2.5 V, V_O = 0.2 V to 4.8 V	25°C	94	113		dB
			Full Range	93			
	Large Signal Voltage Gain LMV932-N (Dual) LMV934-N (Quad)	R_L = 600 Ω to 2.5 V, V_O = 0.2 V to 4.8 V	25°C	81	90		dB
			Full Range	78			
		R_L = 2 kΩ to 2.5 V, V_O = 0.2 V to 4.8 V	25°C	85	100		dB
			Full Range	82			
V_O	Output Swing	R_L = 600 Ω to 2.5 V V_{IN} = ±100 mV	25°C	4.855	4.890		V
					0.120	0.160	
			Full Range	4.835		0.180	
		R_L = 2 kΩ to 2.5 V V_{IN} = ±100 mV	25°C	4.945	4.967		V
					0.037	0.065	
			Full Range	4.935		0.075	
I_O	Output Short Circuit Current (3)	LMV931, Sourcing, V_O = 0 V V_{IN} = +100 mV	25°C	80	100		mA
			Full Range	68			
		Sinking, V_O = 5 V V_{IN} = −100 mV	25°C	58	65		mA
			Full Range	45			

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(2) For specified temperature ranges, see the CMVR parameter in *DC Electrical Characteristics 1.8 V* for the input common-mode voltage specifications.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

6.10 AC Electrical Characteristics 5 V

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/2, V_O = 2.5 V and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
SR	Slew Rate	See .(2)		0.42		V/µs
GBW	Gain-Bandwidth Product			1.5		MHz
Φ_m	Phase Margin			71		deg
G_m	Gain Margin			8		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, V_{CM} = 1 V		50		nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		pA/√Hz
THD	Total Harmonic Distortion	f = 1 kHz, A_V = 1 R_L = 600 Ω, V_O = 1 V_{PP}		0.022%		
	Amplifier-to-Amplifier Isolation	See(3)		123		dB

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(2) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.
(3) Input referred, R_L = 100 kΩ connected to V^+/2. Each amplifier excited in turn with 1 kHz to produce V_O = 3 V_{PP} (For supply voltages < 3 V, V_O = V^+).

6.11 Typical Characteristics

Unless otherwise specified, V_S = 5 V, single-supply, T_A = 25°C.

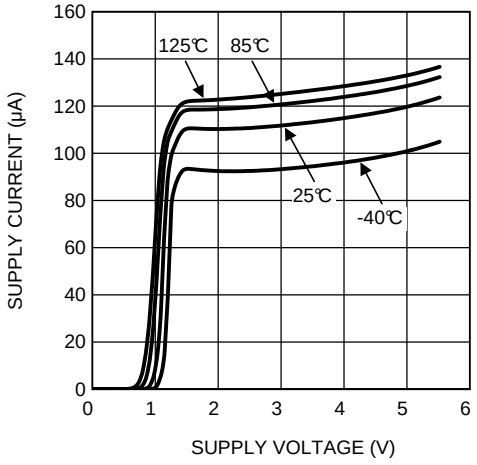


Figure 1. Supply Current vs Supply Voltage (LMV931-N)

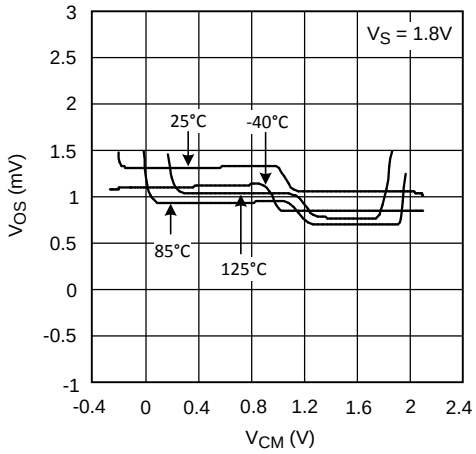


Figure 2. Offset Voltage vs Common-Mode Range

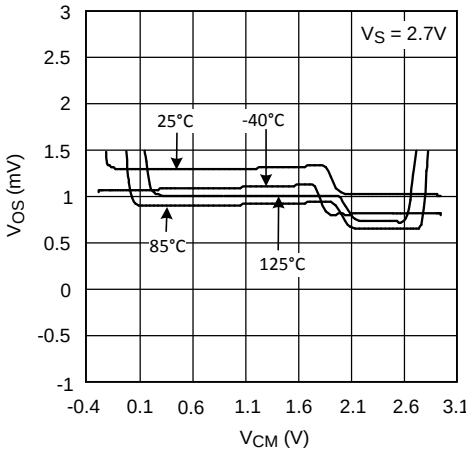


Figure 3. Offset Voltage vs Common-Mode Range

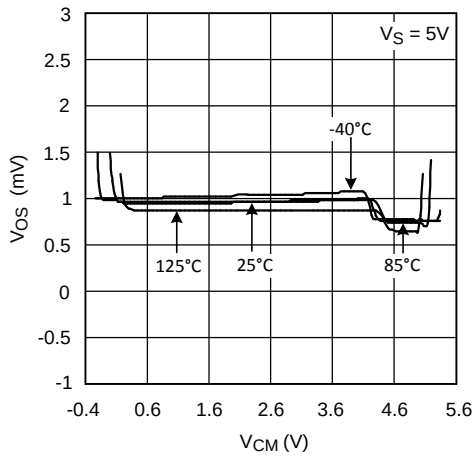


Figure 4. Offset Voltage vs Common-Mode Range

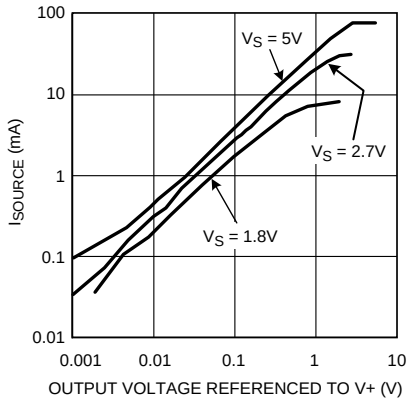


Figure 5. Sourcing Current vs Output Voltage

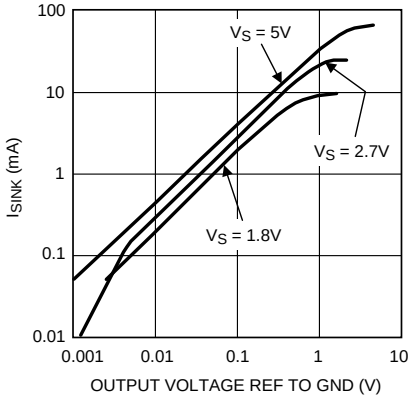


Figure 6. Sinking Current vs Output Voltage

Typical Characteristics (continued)

Unless otherwise specified, V_S = 5 V, single-supply, T_A = 25°C.

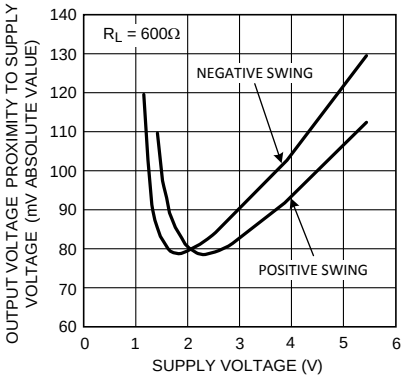


Figure 7. Output Voltage Swing vs Supply Voltage

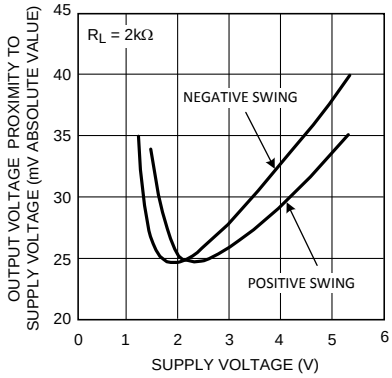


Figure 8. Output Voltage Swing vs Supply Voltage

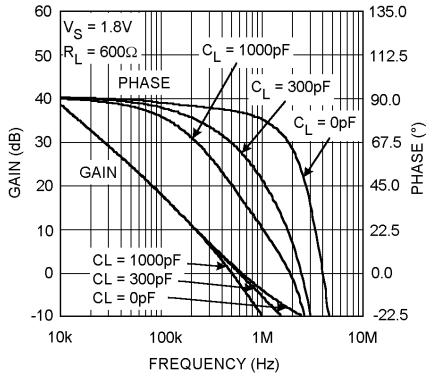


Figure 9. Gain and Phase vs Frequency

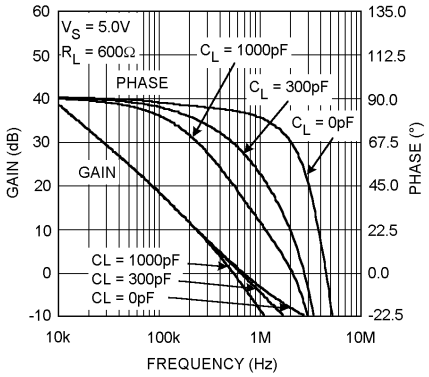


Figure 10. Gain and Phase vs Frequency

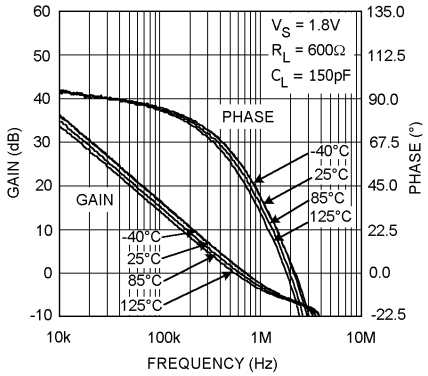


Figure 11. Gain and Phase vs Frequency

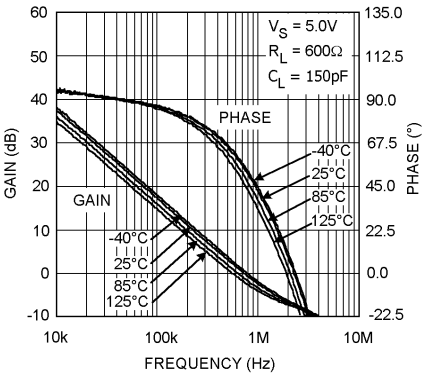


Figure 12. Gain and Phase vs Frequency

Typical Characteristics (continued)

Unless otherwise specified, V_S = 5 V, single-supply, T_A = 25°C.

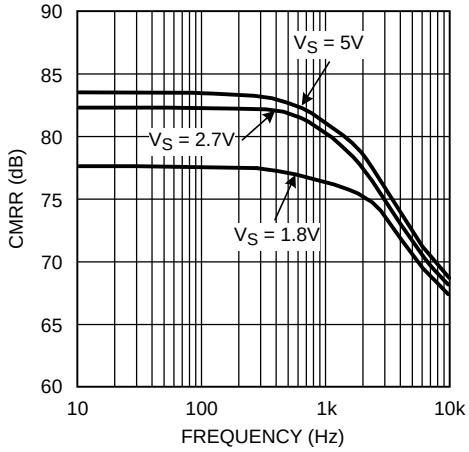


Figure 13. CMRR vs Frequency

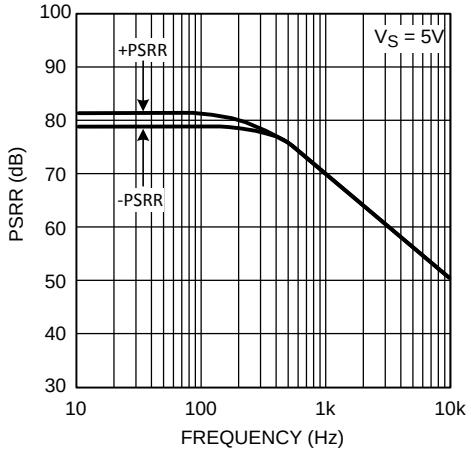


Figure 14. PSRR vs Frequency

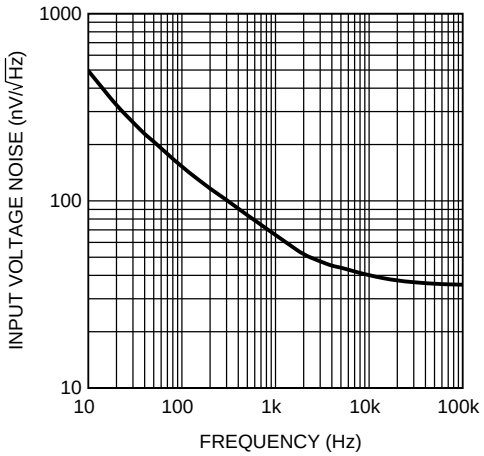


Figure 15. Input Voltage Noise vs Frequency

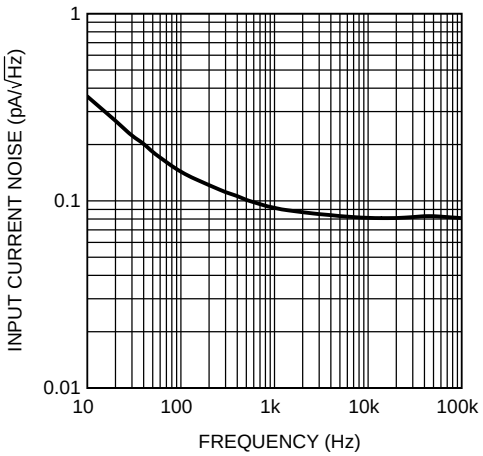


Figure 16. Input Current Noise vs Frequency

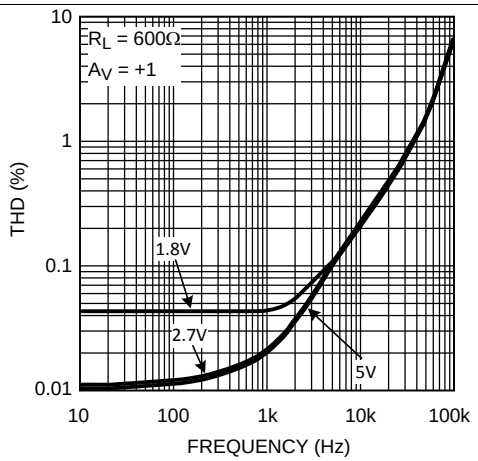


Figure 17. THD vs Frequency

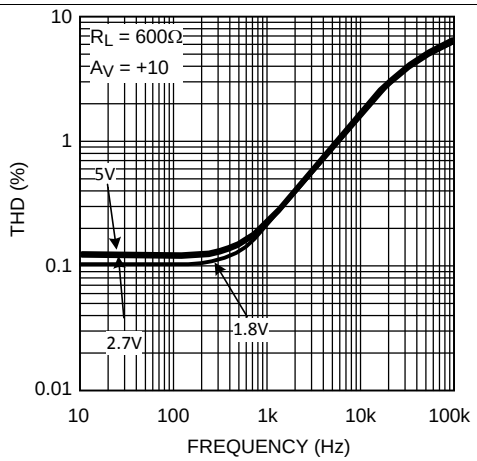


Figure 18. THD vs Frequency

Typical Characteristics (continued)

Unless otherwise specified, V_S = 5 V, single-supply, T_A = 25°C.

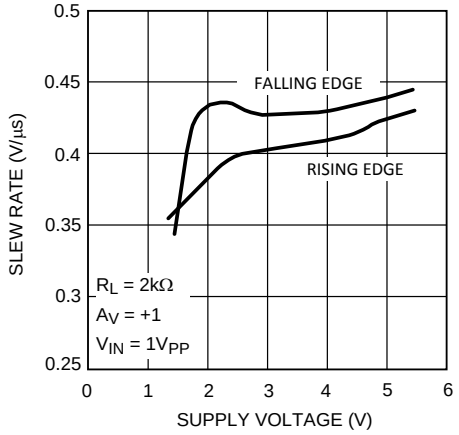


Figure 19. Slew Rate vs Supply Voltage LMV931 and LMV934

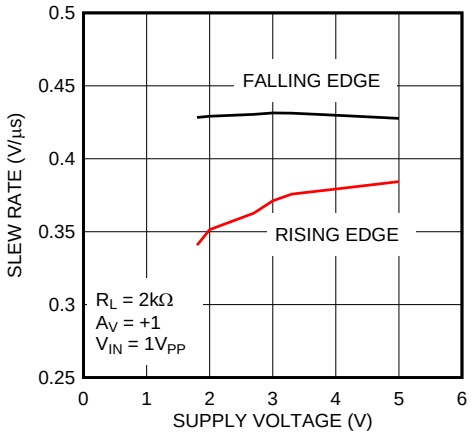


Figure 20. Slew Rate vs Supply Voltage LMV932 Only

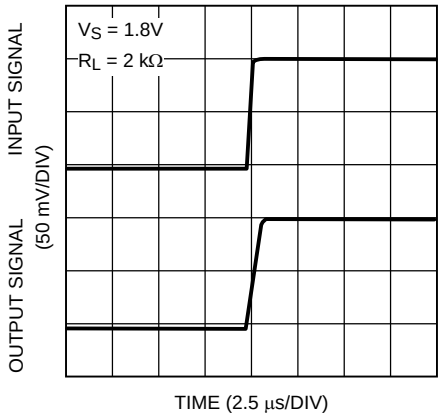


Figure 21. Small Signal Noninverting Response

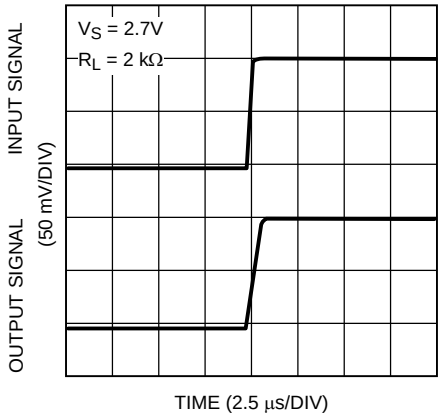


Figure 22. Small Signal Noninverting Response

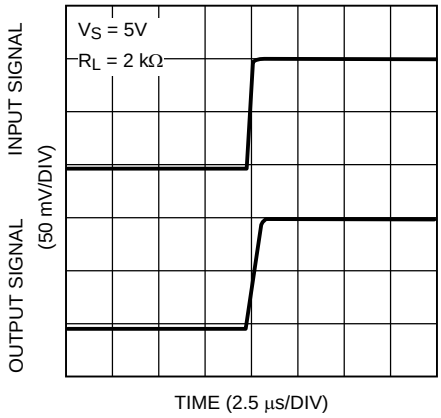


Figure 23. Small Signal Noninverting Response

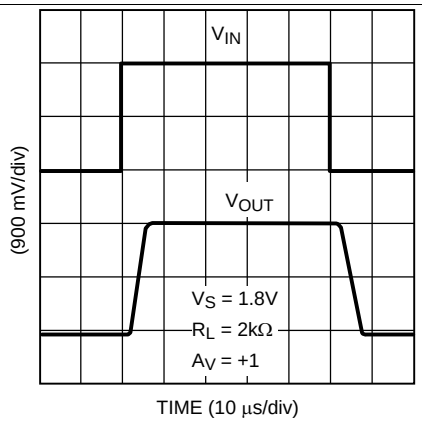


Figure 24. Large Signal Noninverting Response

Typical Characteristics (continued)

Unless otherwise specified, V_S = 5 V, single-supply, T_A = 25°C.

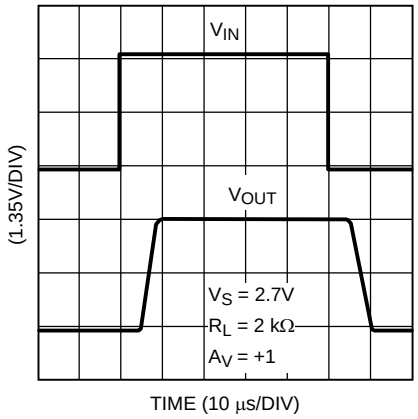


Figure 25. Large Signal Noninverting Response

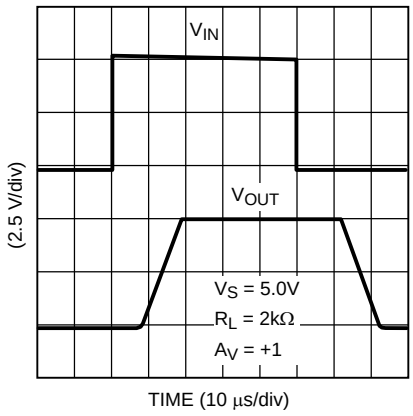


Figure 26. Large Signal Noninverting Response

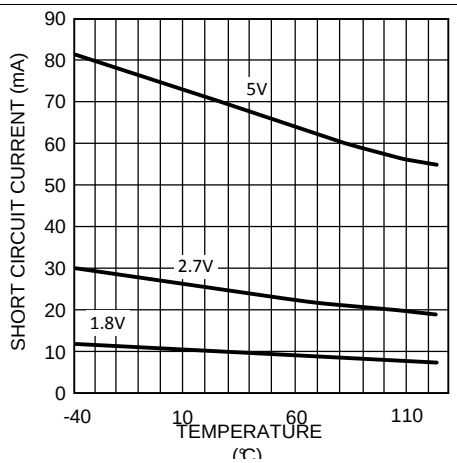


Figure 27. Short Circuit Current vs Temperature (Sinking)

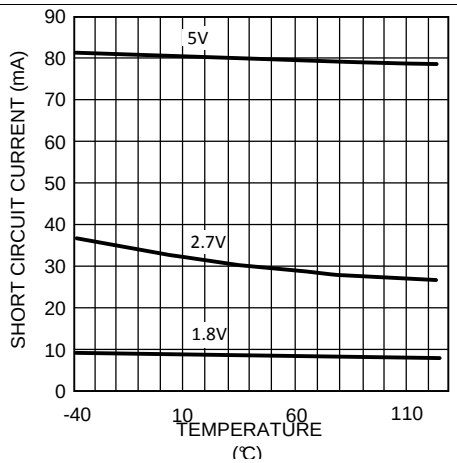


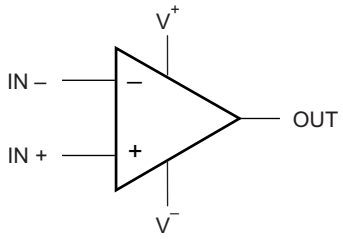
Figure 28. Short Circuit Current vs Temperature (Sourcing)

7 Detailed Description

7.1 Overview

The LMV93x-N are low-voltage, low-power operational amplifiers (op-amp) operating from 1.8-V to 5.5-V supply voltages and have rail-to-rail input and output. LMV93x-N input common-mode voltage extends 200 mV beyond the supplies which enables user enhanced functionality beyond the supply voltage range.

7.2 Functional Block Diagram



(Each Amplifier)

7.3 Feature Description

The differential inputs of the amplifier consist of a noninverting input (+IN) and an inverting input (–IN). The amplifer amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by Equation 1:

$$V_{OUT} = A_{OL} (IN^+ - IN^-) \quad (1)$$

where

- A_{OL} is the open-loop gain of the amplifier, typically around 100 dB (100,000x, or 10 µV per volt).

7.4 Device Functional Modes

7.4.1 Input and Output Stage

The rail-to-rail input stage of this family provides more flexibility for the designer. The LMV93x-N use a complimentary PNP and NPN input stage in which the PNP stage senses common-mode voltage near V^- and the NPN stage senses common-mode voltage near V^+. The transition from the PNP stage to NPN stage occurs 1 V below V^+. Because both input stages have their own offset voltage, the offset of the amplifier becomes a function of the input common-mode voltage and has a crossover point at 1 V below V^+.

Device Functional Modes (continued)

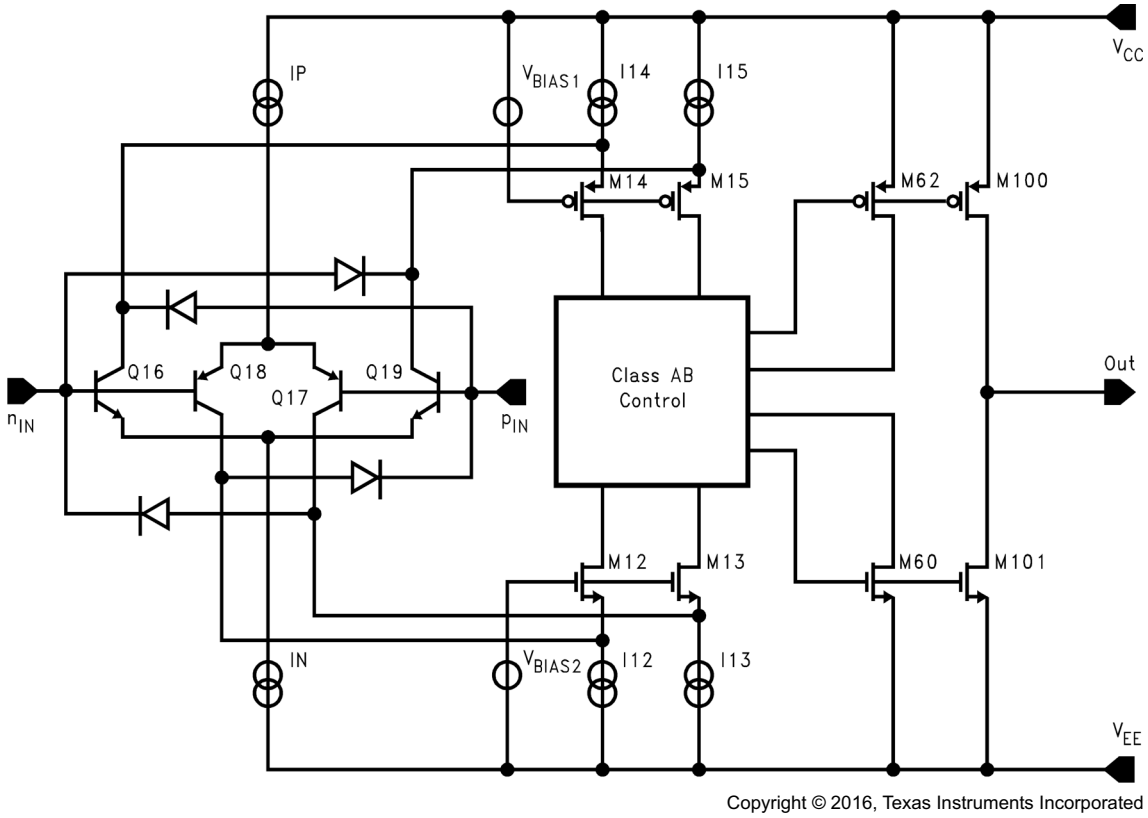


Figure 29. Simplified Schematic Diagram

This V_{OS} crossover point can create problems for both DC− and AC-coupled signals if proper care is not taken. Large input signals that include the V_{OS} crossover point will cause distortion in the output signal. One way to avoid such distortion is to keep the signal away from the crossover. For example, in a unity gain buffer configuration with V_S = 5 V, a 5-V peak-to-peak signal will contain input-crossover distortion while a 3-V peak-to-peak signal centered at 1.5 V will not contain input-crossover distortion as it avoids the crossover point. Another way to avoid large signal distortion is to use a gain of −1 circuit which avoids any voltage excursions at the input terminals of the amplifier. In that circuit, the common-mode DC voltage can be set at a level away from the V_{OS} cross-over point. For small signals, this transition in V_{OS} shows up as a V_{CM} dependent spurious signal in series with the input signal and can effectively degrade small signal parameters such as gain and common-mode rejection ratio. To resolve this problem, the small signal should be placed such that it avoids the V_{OS} crossover point. In addition to the rail-to-rail performance, the output stage can provide enough output current to drive 600-Ω loads. Because of the high-current capability, take care not to exceed the 150°C maximum junction temperature specification.

7.4.2 Input Bias Current Consideration

The LMV93x-N family has a complementary bipolar input stage. The typical input bias current (I_B) is 15 nA. The input bias current can develop a significant offset voltage. This offset is primarily due to I_B flowing through the negative feedback resistor, R_F. For example, if I_B is 50 nA and R_F is 100 kΩ, then an offset voltage of 5 mV will develop (V_{OS} = I_B x R_F). Using a compensation resistor (R_C), as shown in Figure 30, cancels this effect. But the input offset current (I_{OS}) will still contribute to an offset voltage in the same manner.

Device Functional Modes (continued)

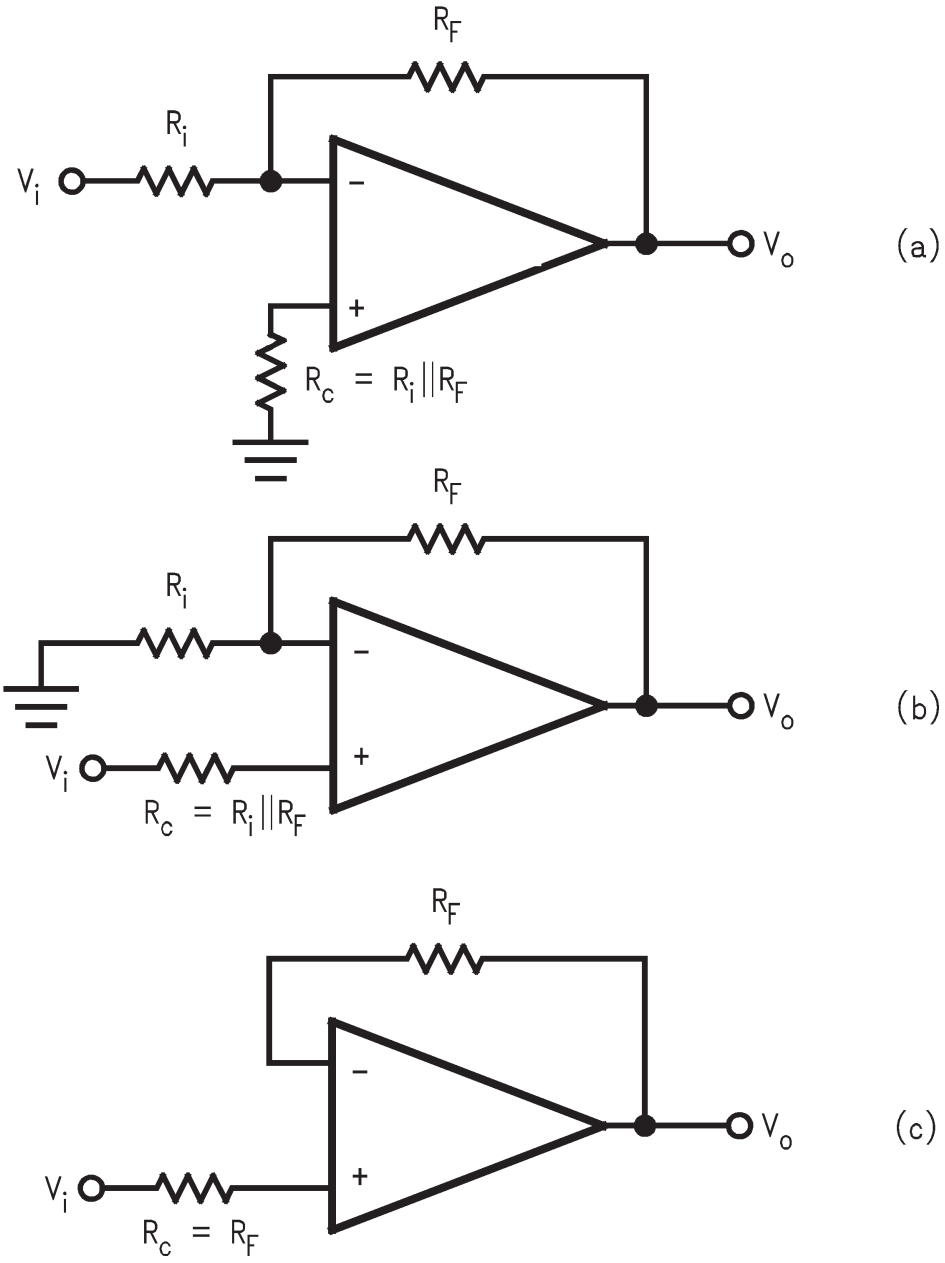


Figure 30. Canceling the Offset Voltage due to Input Bias Current

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV93x-N devices bring performance, economy and ease-of-use to low-voltage, low-power systems. They provide rail-to-rail input and rail-to-rail output swings into heavy loads.

8.2 Typical Applications

8.2.1 High-Side Current-Sensing Application

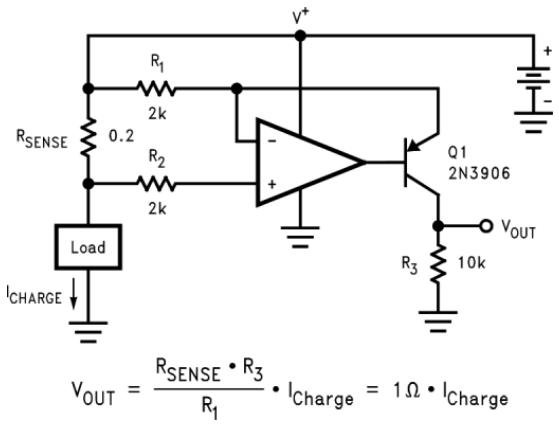


Figure 31. High-Side Current Sensing

8.2.1.1 Design Requirements

The high-side current-sensing circuit (Figure 31) is commonly used in a battery charger to monitor charging current to prevent overcharging. A sense resistor R_{SENSE} is connected to the battery directly. This system requires an op amp with rail-to-rail input. The LMV93x-N are ideal for this application because its common-mode input range extends up to the positive supply.

8.2.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMV93x-N device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

As seen in Figure 31, the I_{CHARGE} current flowing through sense resistor R_{SENSE} develops a voltage drop equal to V_{SENSE}. The voltage at the negative sense point will now be less than the positive sense point by an amount proportional to the V_{SENSE} voltage.

The low-bias currents of the LMV93x cause little voltage drop through R_2, so the negative input of the LMV93x amplifier is at essentially the same potential as the negative sense input.

The LMV93x will detect this voltage error between its inputs and servo the transistor base to conduct more current through Q1, increasing the voltage drop across R_1 until the LMV93x inverting input matches the noninverting input. At this point, the voltage drop across R_1 now matches V_{SENSE}.

I_G, a current proportional to I_{CHARGE}, will flow according to the following relation:

$$I_G = V_{RSENSE} / R_1 = (R_{SENSE} * I_{CHARGE}) / R_1 \quad (2)$$

I_G also flows through the gain resistor R_3 developing a voltage drop equal to:

$$V_3 = I_G * R_3 = (V_{RSENSE} / R_1) * R_3 = ((R_{SENSE} * I_{CHARGE}) / R_2) * R_3 \quad (3)$$

Typical Applications (continued)

$V_{OUT} = (R_{SENSE} * I_{CHARGE}) * G$

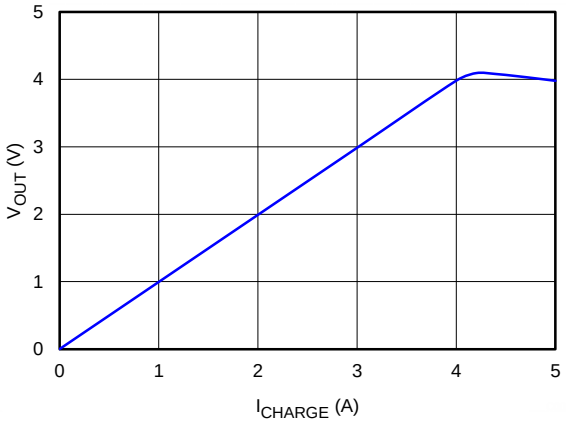
where

- $G = R_3 / R_1$ (4)

The other channel of the LMV93x may be used to buffer the voltage across R3 to drive the following stages.

8.2.1.3 Application Curve

Figure 32 shows the results of the example current sense circuit.



NOTE: the error after 4 V where transistor Q1 runs out of headroom and saturates, limiting the upper output swing.

Figure 32. Current Sense Amplifier Results

8.2.2 Half-Wave Rectifier Applications

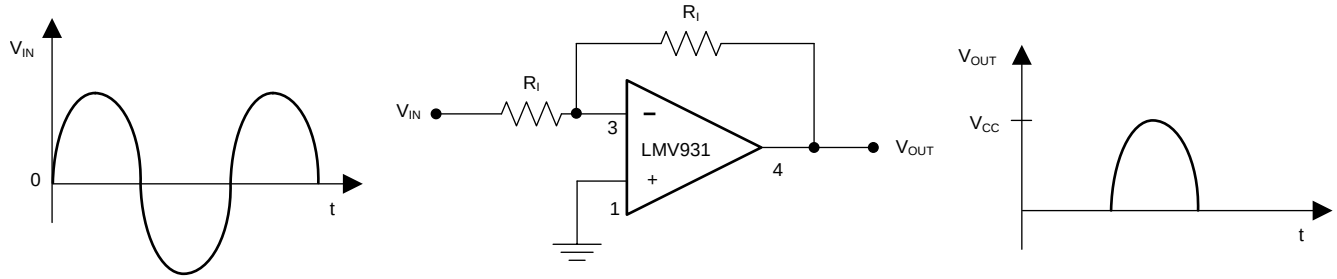


Figure 33. Half-Wave Rectifier With Rail-To-Ground Output Swing Referenced to Ground

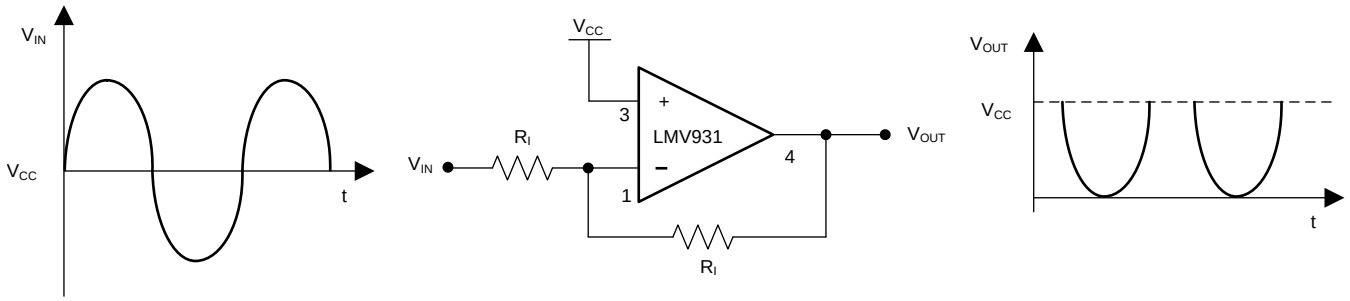


Figure 34. Half-Wave Rectifier With Negative-Going Output Referenced to V_{CC}

Typical Applications (continued)

8.2.2.1 Design Requirements

Because the LMV931-N, LMV932-N, LMV934-N input common-mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction is an easy task. All that is needed are two external resistors; there is no need for diodes or matched resistors. The half-wave rectifier can have either positive or negative going outputs, depending on the way the circuit is arranged.

8.2.2.2 Detailed Design Procedure

In Figure 33 the circuit is referenced to ground, while in Figure 34 the circuit is biased to the positive supply. These configurations implement the half-wave rectifier because the LMV93x-N can not respond to one-half of the incoming waveform. It can not respond to one-half of the incoming because the amplifier cannot swing the output beyond either rail therefore the output disengages during this half cycle. During the other half cycle, however, the amplifier achieves a half wave that can have a peak equal to the total supply voltage. R_l should be large enough not to load the LMV93x-N.

8.2.2.3 Application Curve

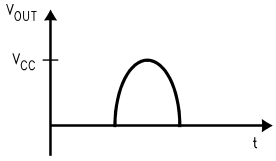


Figure 35. Output of Ground-to-Rail Circuit

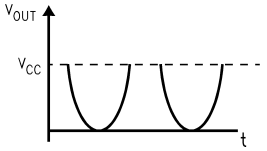


Figure 36. Output of Rail-to-Ground Circuit

8.2.3 Instrumentation Amplifier With Rail-to-Rail Input and Output Application

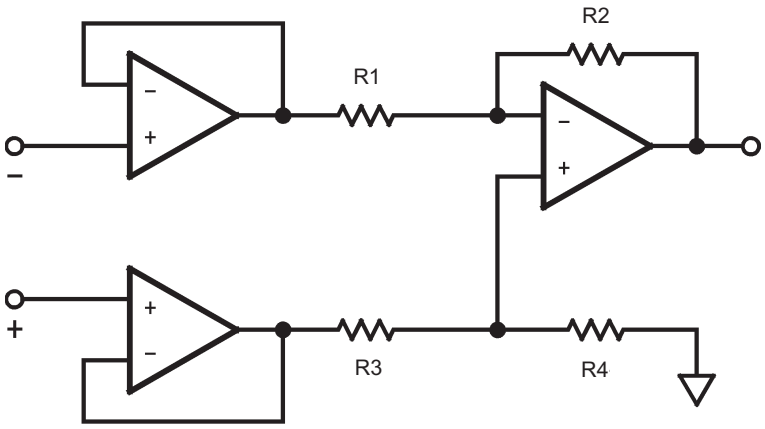


Figure 37. Rail-to-Rail Instrumentation Amplifier

8.2.3.1 Design Requirements

Using three of the LMV93x-N amplifiers, an instrumentation amplifier with rail-to-rail inputs and outputs can be made as shown in Figure 37.

8.2.3.2 Detailed Design Procedure

In this example, amplifiers on the left side act as buffers to the differential stage. These buffers assure that the input impedance is very high. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMRR set by the matching R_1-R_2 with R_3-R_4. The gain is set by the ratio of R_2/R_1 and R_3 should equal R_1 and R_4 equal R_2. With both rail-to-rail input and output ranges, the input and output are only limited by the supply voltages. Remember that even with rail-to-rail outputs, the output can not swing past the supplies so the combined common-mode voltages plus the signal should not be greater that the supplies or limiting will occur.

Typical Applications (continued)

8.2.3.3 Application Curve

Figure 38 shows the results of the instrumentation amplifier with R_1 and R_3 = 1 K, and R_2 and R_4 = 100 kΩ, for a gain of 100, running on a single 5-V supply with a input of $V_{CM} = V_S/2$. The combined effects of the individual offset voltages can be seen as a shift in the offset of the curve.

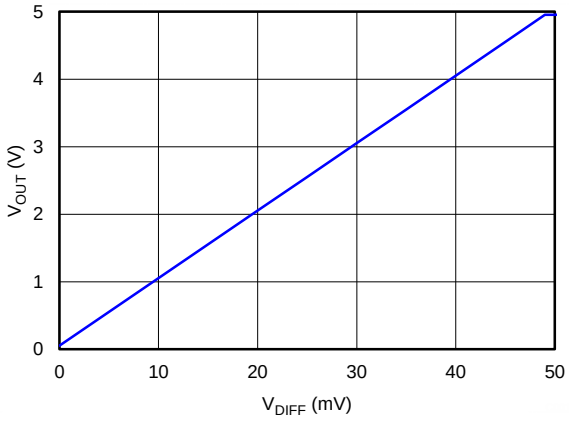


Figure 38. Instrumentation Amplifier Output Results

8.3 Dos and Don'ts

Do properly bypass the power supplies.

Do add series resistence to the output when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do add series current limiting resistors and external schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1 mA or less (1 kΩ per volt).

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, TI recommends that 10-nF capacitors be placed as close as possible to the op amp power supply pins. For single-supply, place a capacitor between V^+ and V^- supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

10 Layout

10.1 Layout Guidelines

The V^+ pin must be bypassed to ground with a low-ESR capacitor.

The optimum placement is closest to the V^+ and ground pins.

Take care to minimize the loop area formed by the bypass capacitor connection between V^+ and ground.

The ground pin must be connected to the PCB ground plane at the pin of the device.

The feedback components should be placed as close as possible to the device minimizing strays.

10.2 Layout Example

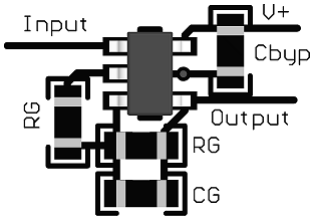


Figure 39. SOT-23 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMV93x-N device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.1.2 Development Support

LMV931 PSPICE Model (also applicable to the LMV932 and LMV934), http://www.ti.com/lit/zip/snom028

TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

DIP Adapter Evaluation Module, http://www.ti.com/tool/dip-adapter-evm

TI Universal Operational Amplifier Evaluation Module, http://www.ti.com/tool/opampevm

TI Filterpro Software, http://www.ti.com/tool/filterpro

11.2 Documentation Support

11.2.1 Related Documentation

For additional applications, see

AN-31 Op Amp Circuit Collection

11.3 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV931-N	Click here	Click here	Click here	Click here	Click here
LMV932-N	Click here	Click here	Click here	Click here	Click here
LMV934-N	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV931MF	NRND	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Call TI	-40 to 125	A79A	
LMV931MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A79A	Samples
LMV931MFX	NRND	SOT-23	DBV	5	3000	Non-RoHS & Green	Call TI	Call TI	-40 to 125	A79A	
LMV931MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A79A	Samples
LMV931MG	NRND	SC70	DCK	5	1000	Non-RoHS & Green	Call TI	Call TI	-40 to 125	A74	
LMV931MG/NOPB	ACTIVE	SC70	DCK	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A74	Samples
LMV931MGX/NOPB	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A74	Samples
LMV932MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV9 32MA	Samples
LMV932MAX	NRND	SOIC	D	8	2500	Non-RoHS & Green	Call TI	Call TI	-40 to 125	LMV9 32MA	
LMV932MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV9 32MA	Samples
LMV932MM	NRND	VSSOP	DGK	8	1000	Non-RoHS & Green	Call TI	Call TI	-40 to 125	A86A	
LMV932MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	A86A	Samples
LMV932MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	A86A	Samples
LMV934MA	NRND	SOIC	D	14	55	Non-RoHS & Green	Call TI	Call TI	-40 to 125	LMV934MA	
LMV934MA/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV934MA	Samples
LMV934MAX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV934MA	Samples
LMV934MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMV93 4MT	Samples
LMV934MTX	NRND	TSSOP	PW	14	2500	Non-RoHS & Green	Call TI	Call TI	-40 to 125	LMV93 4MT	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV934MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMV93 4MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LMV931-N, LMV932-N, LMV934-N :

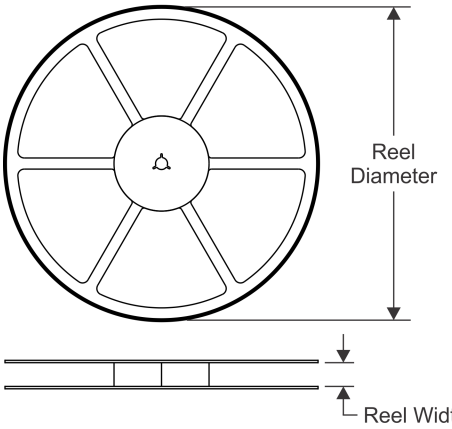
- Automotive : LMV931-N-Q1, LMV932-N-Q1, LMV934-N-Q1

NOTE: Qualified Version Definitions:

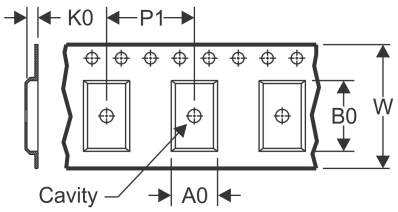
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

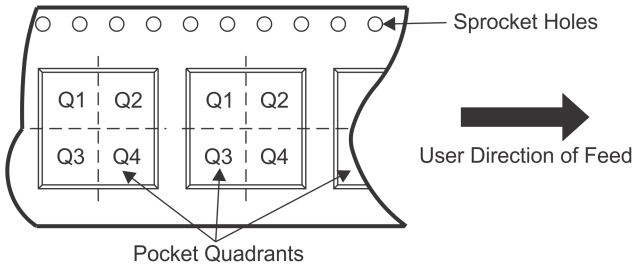


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

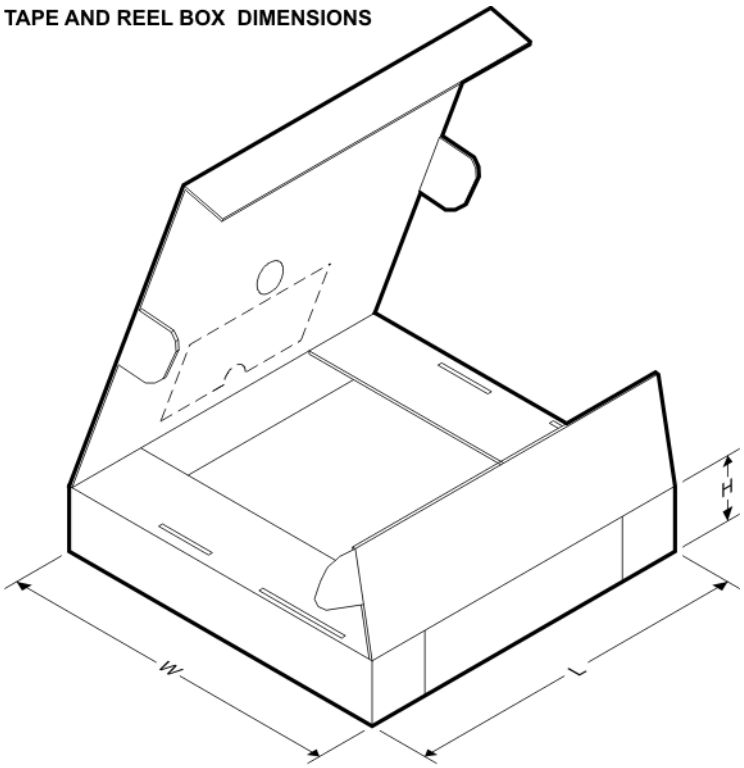
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV931MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV931MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV931MFX	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV931MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV931MG	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV931MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV931MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV932MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV932MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV932MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV932MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV932MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV934MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV934MTX	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LMV934MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LMV934MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

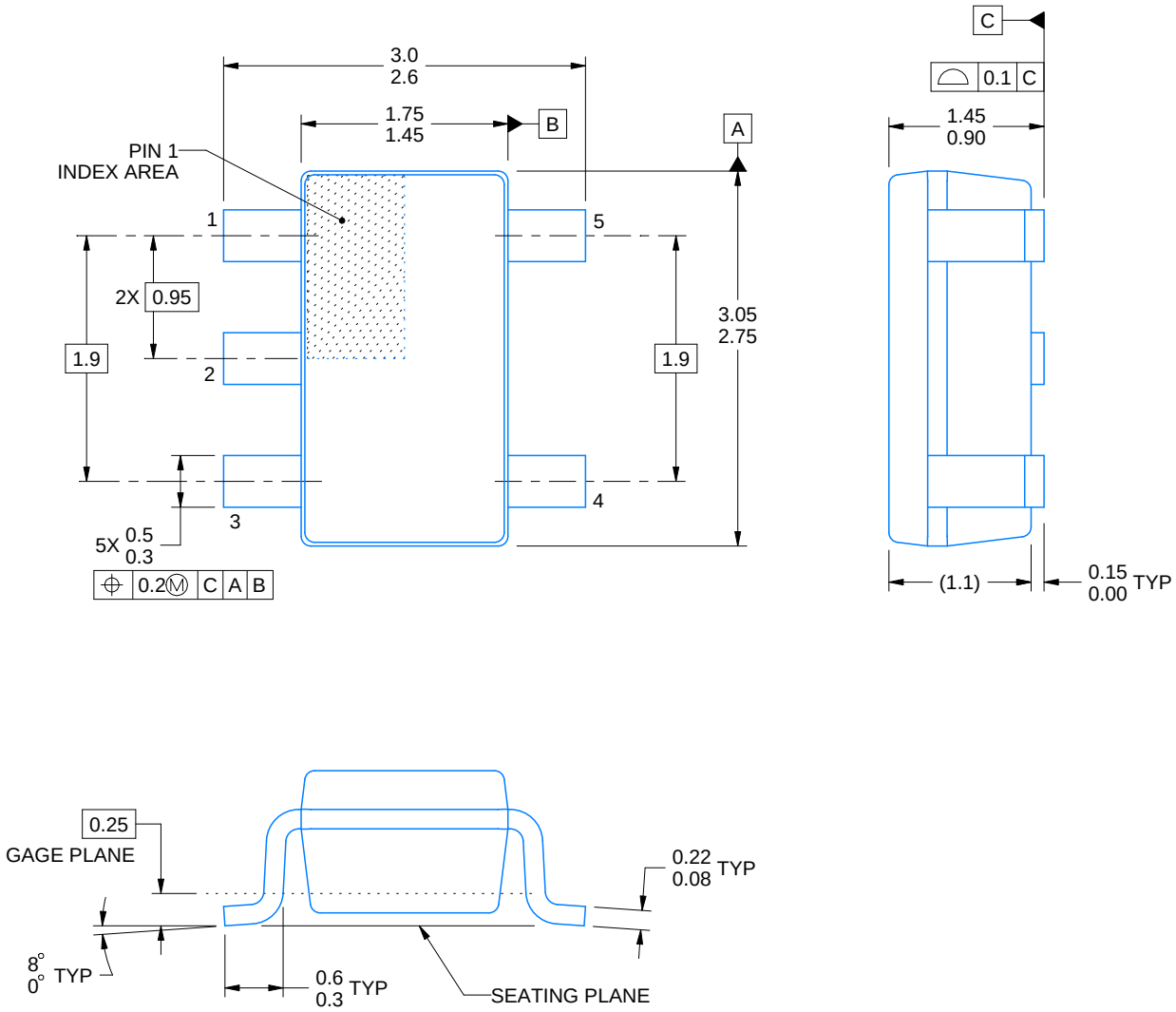
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV931MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV931MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV931MFX	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV931MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV931MG	SC70	DCK	5	1000	210.0	185.0	35.0
LMV931MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV931MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV932MAX	SOIC	D	8	2500	367.0	367.0	35.0
LMV932MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV932MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV932MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV932MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV934MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMV934MTX	TSSOP	PW	14	2500	367.0	367.0	35.0
LMV934MTX/NOPB	TSSOP	PW	14	2500	853.0	449.0	35.0
LMV934MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

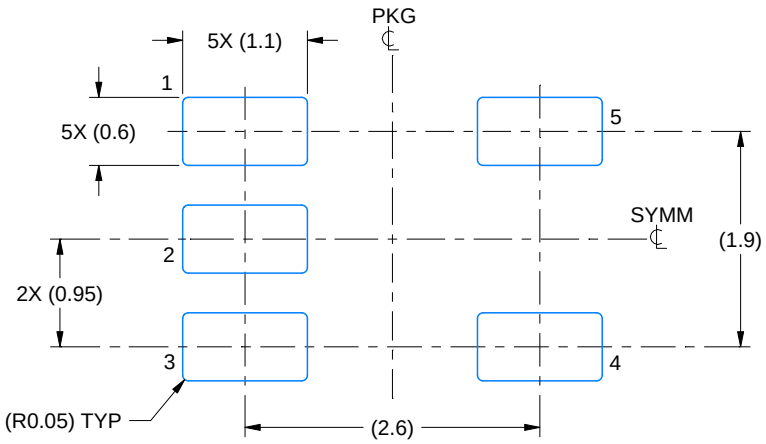
SMALL OUTLINE TRANSISTOR



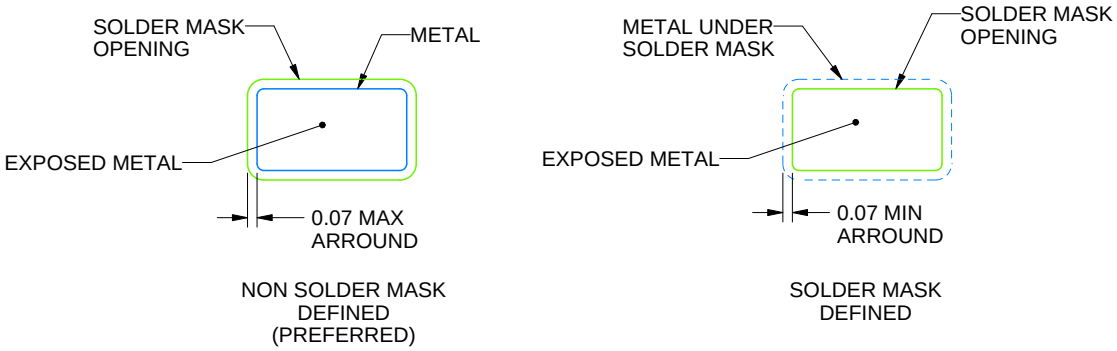
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

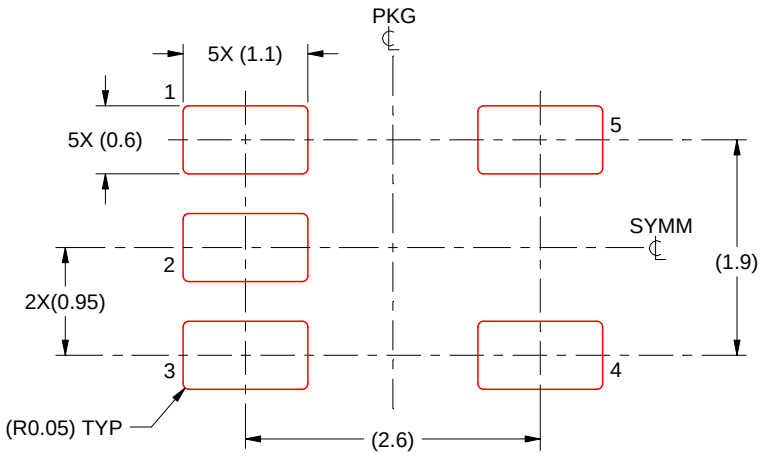


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

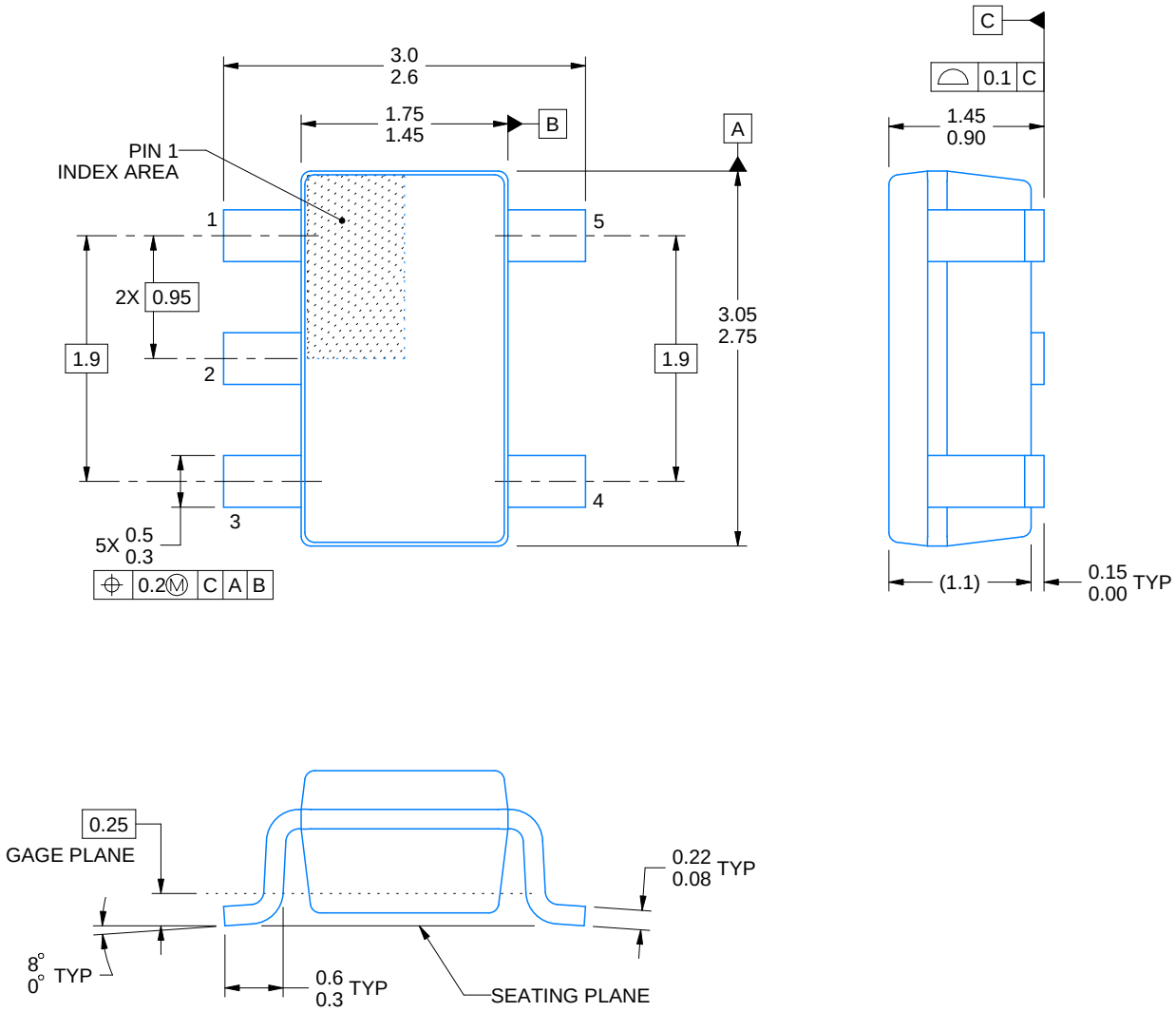
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

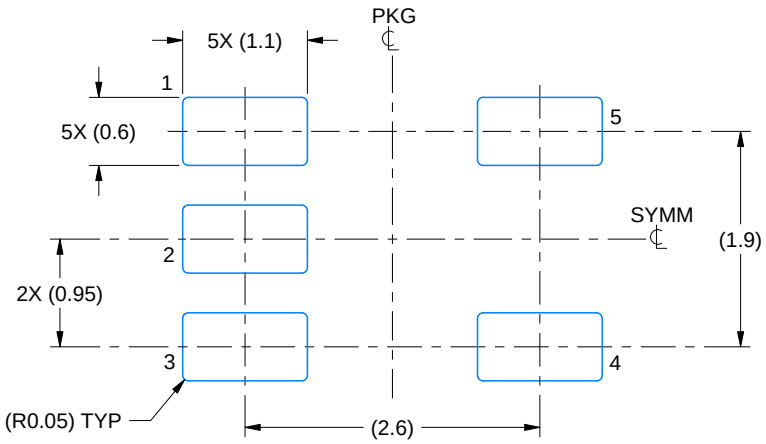
SMALL OUTLINE TRANSISTOR



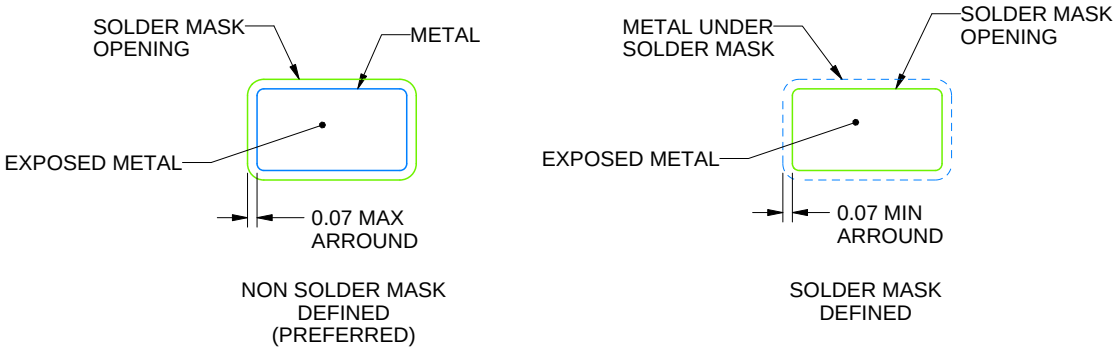
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

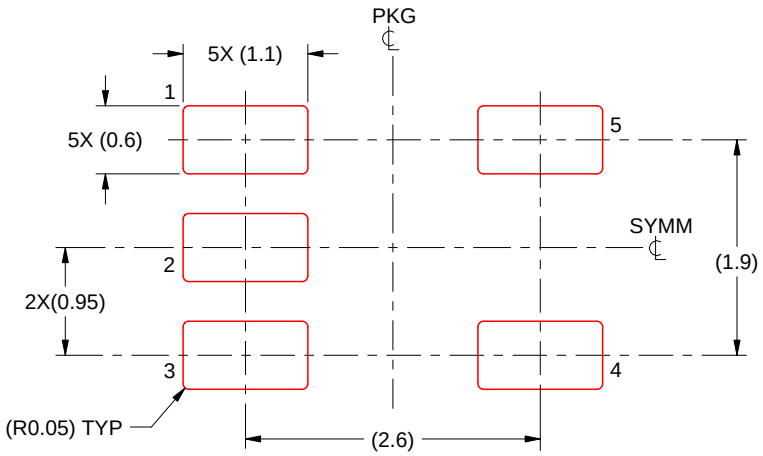


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



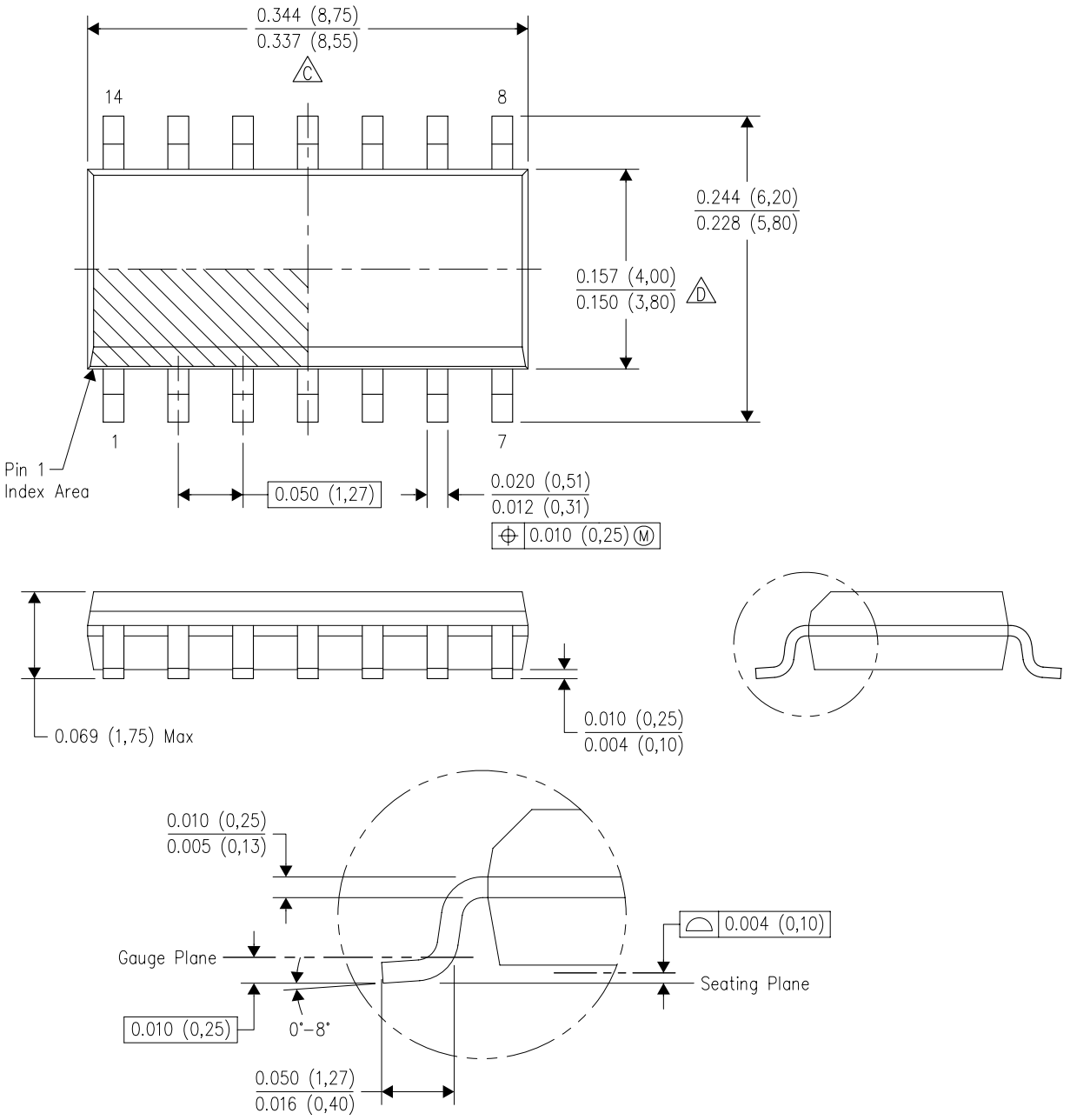
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

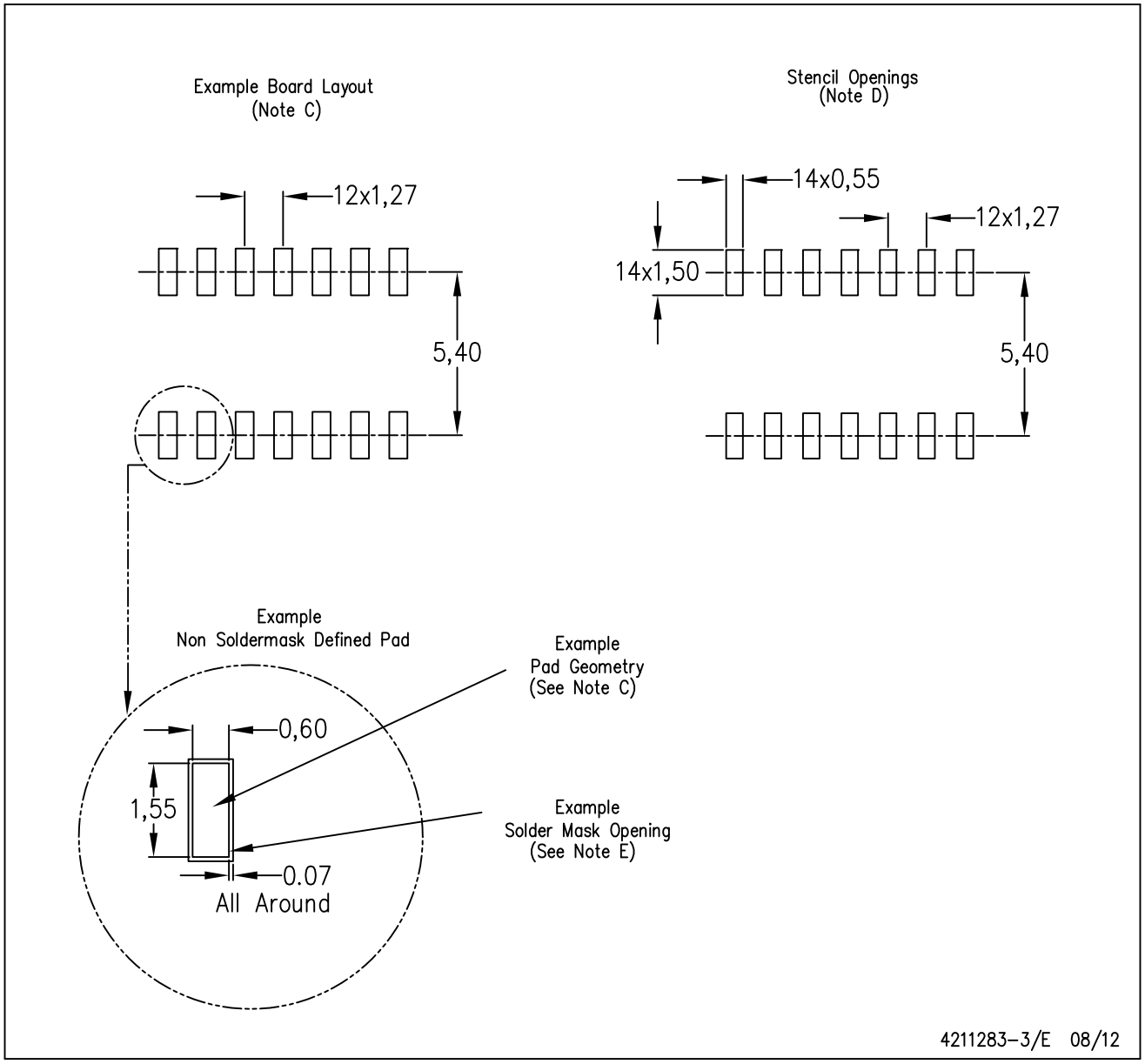
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

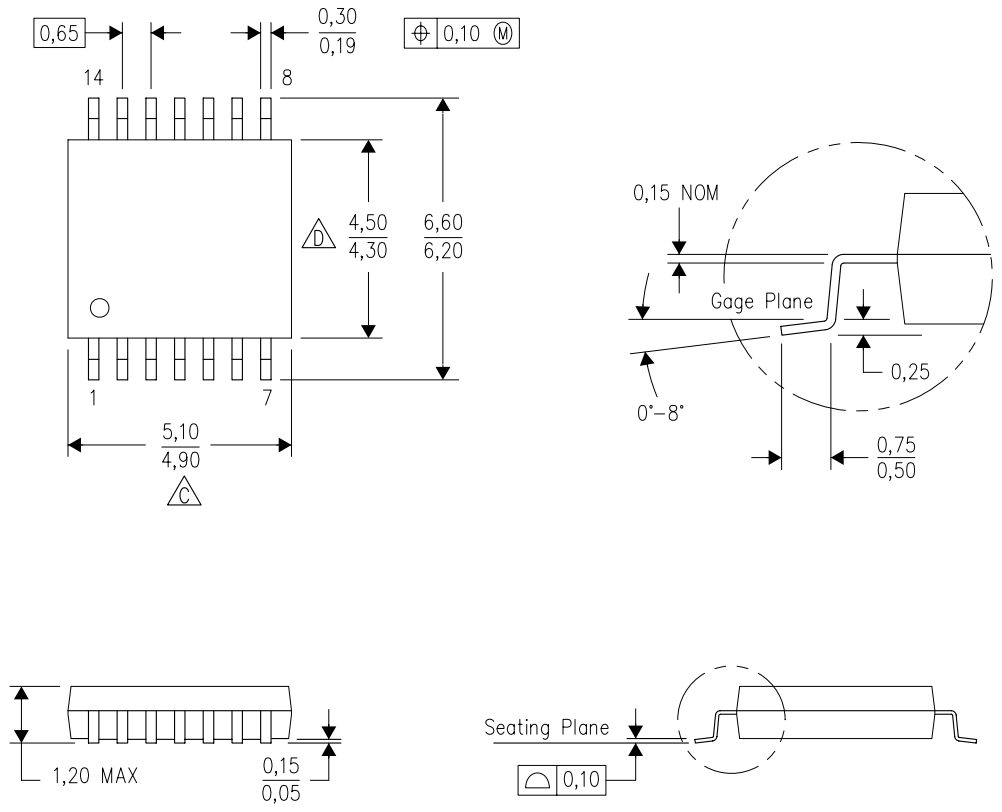
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

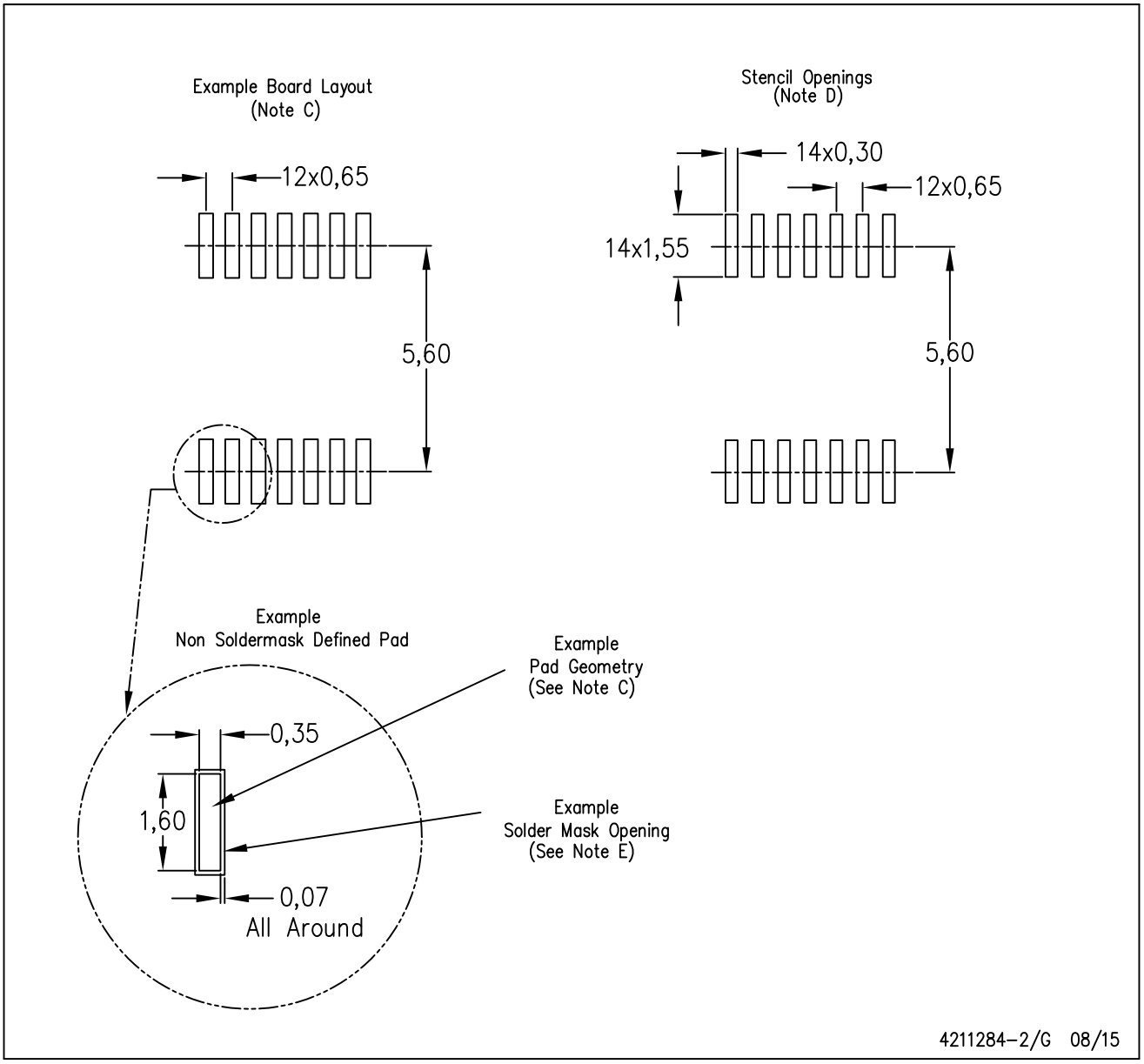
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



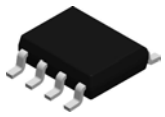
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

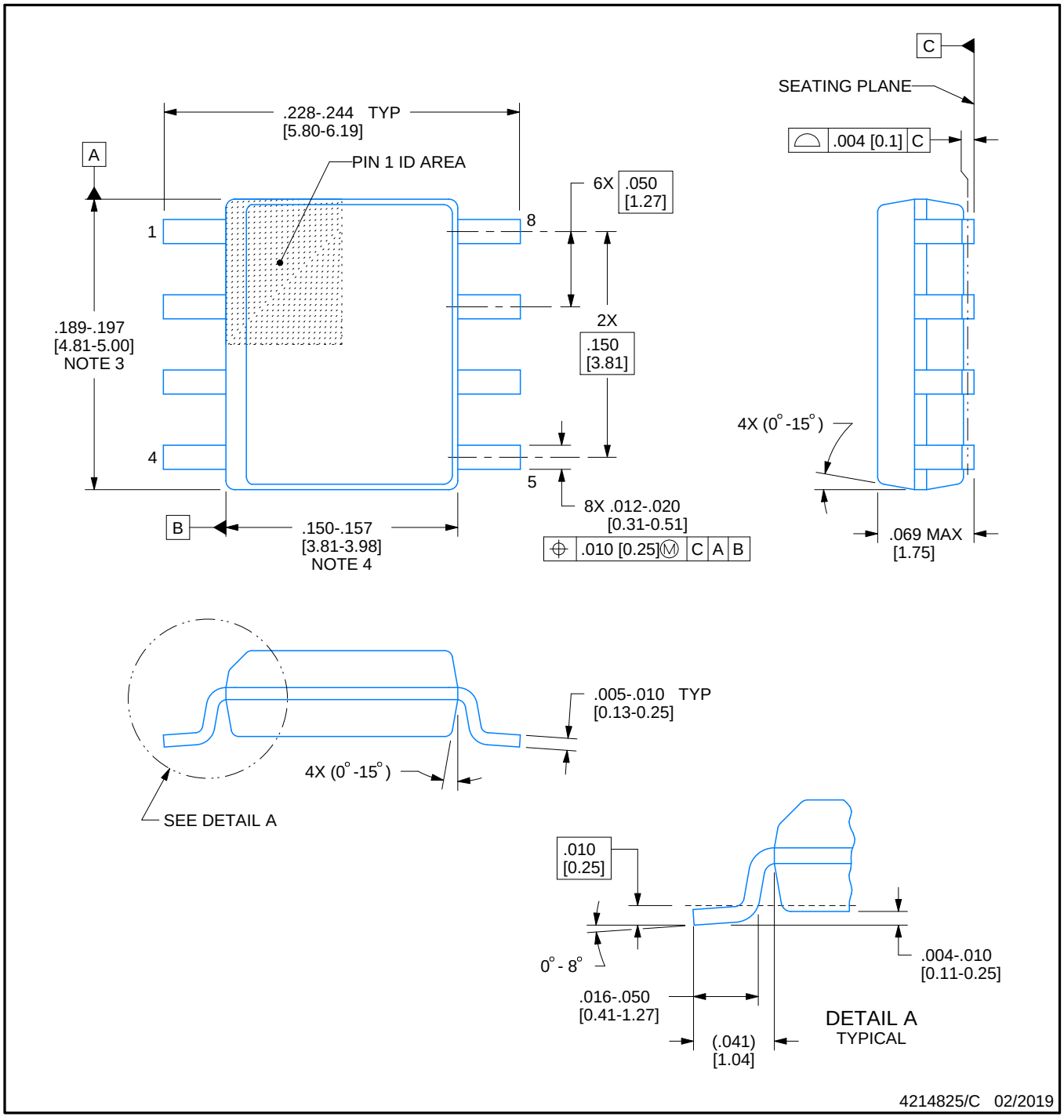


PACKAGE OUTLINE

D0008A

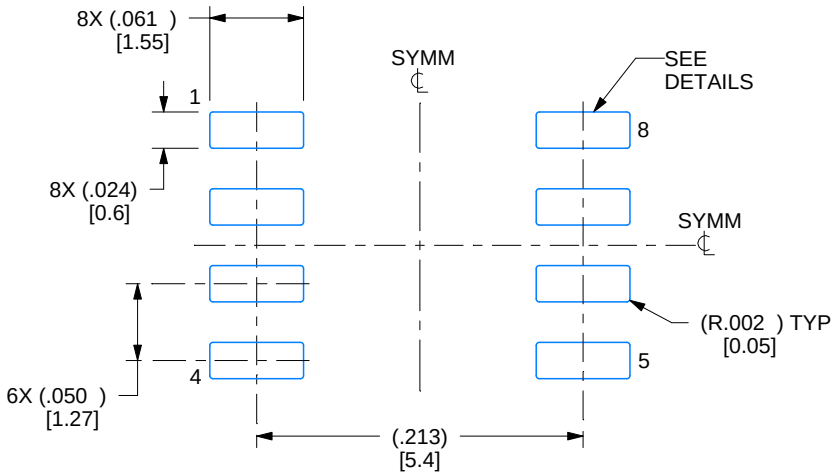
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

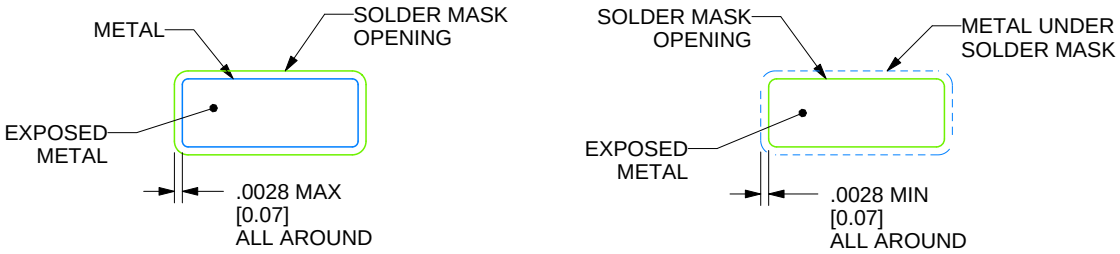


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

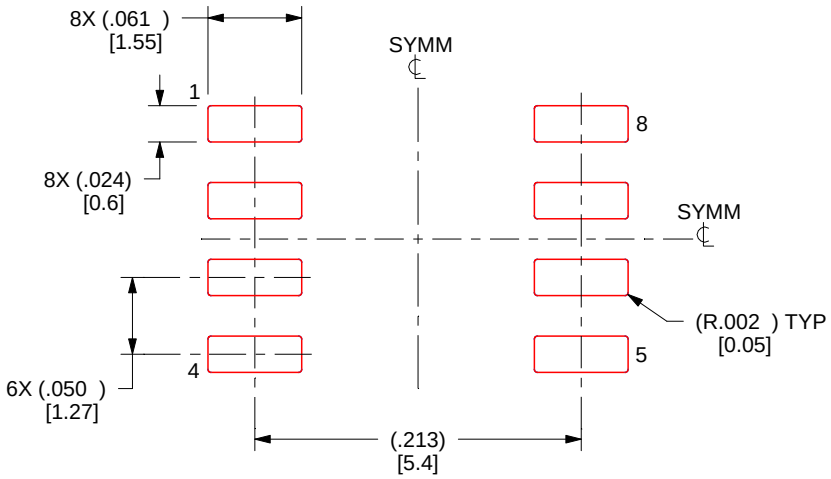
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



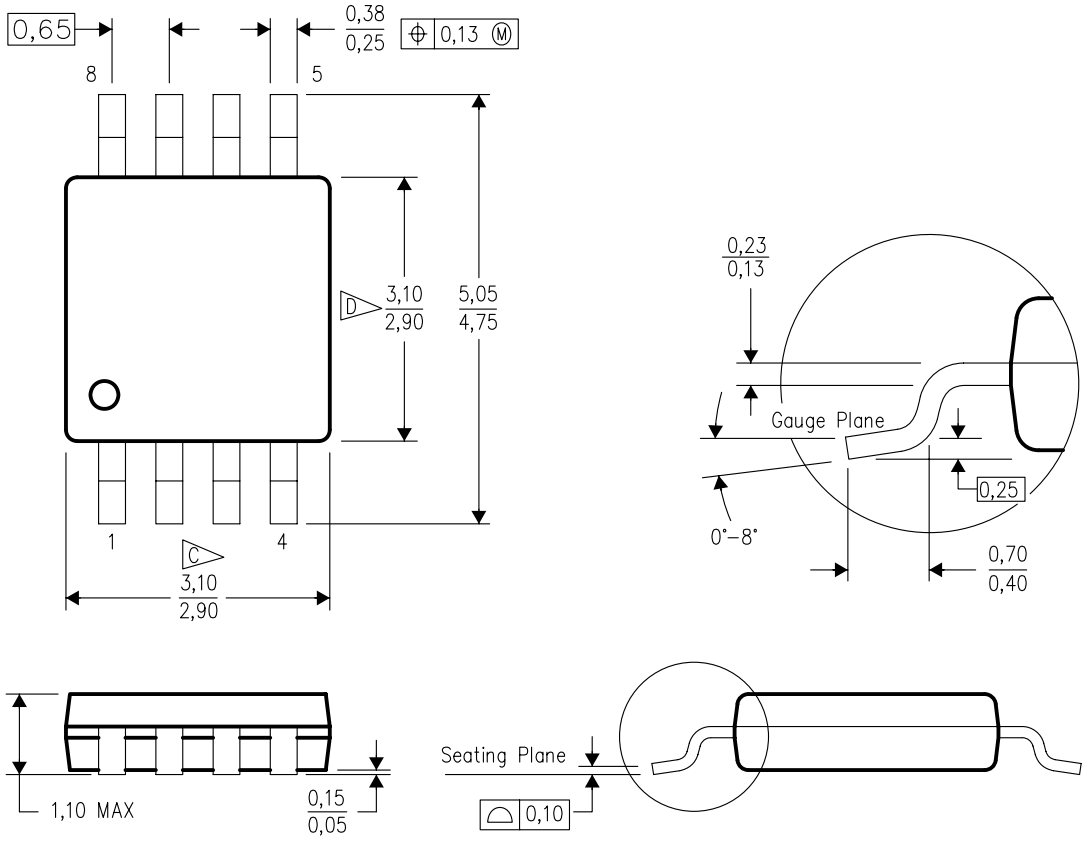
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

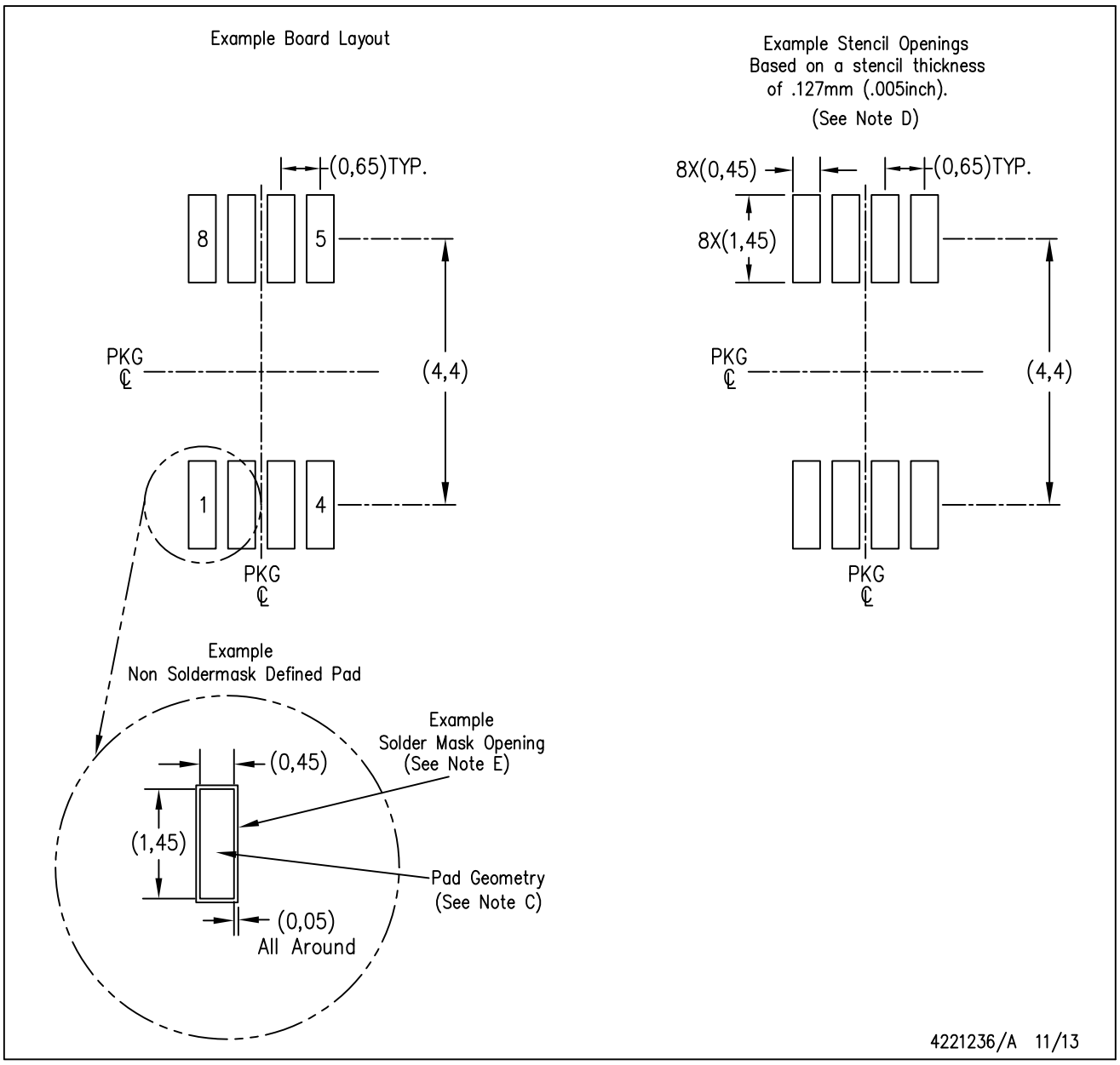
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

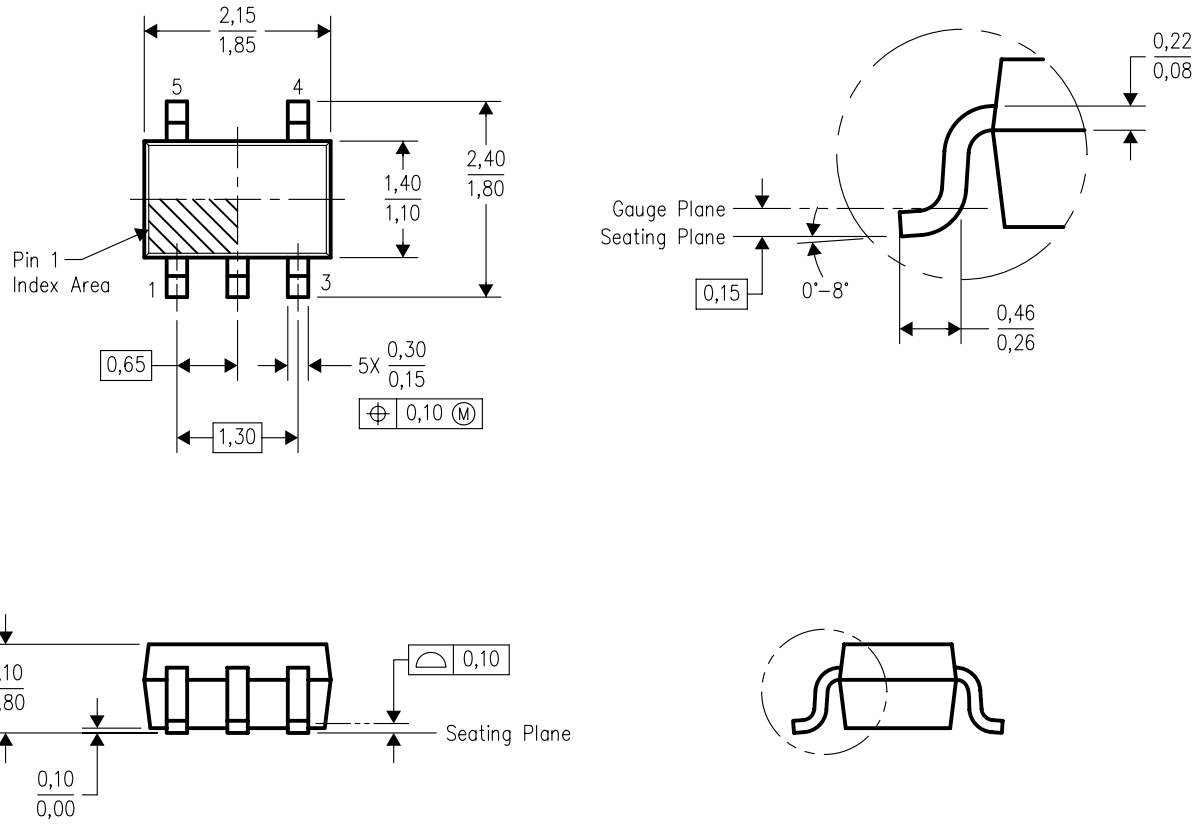
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

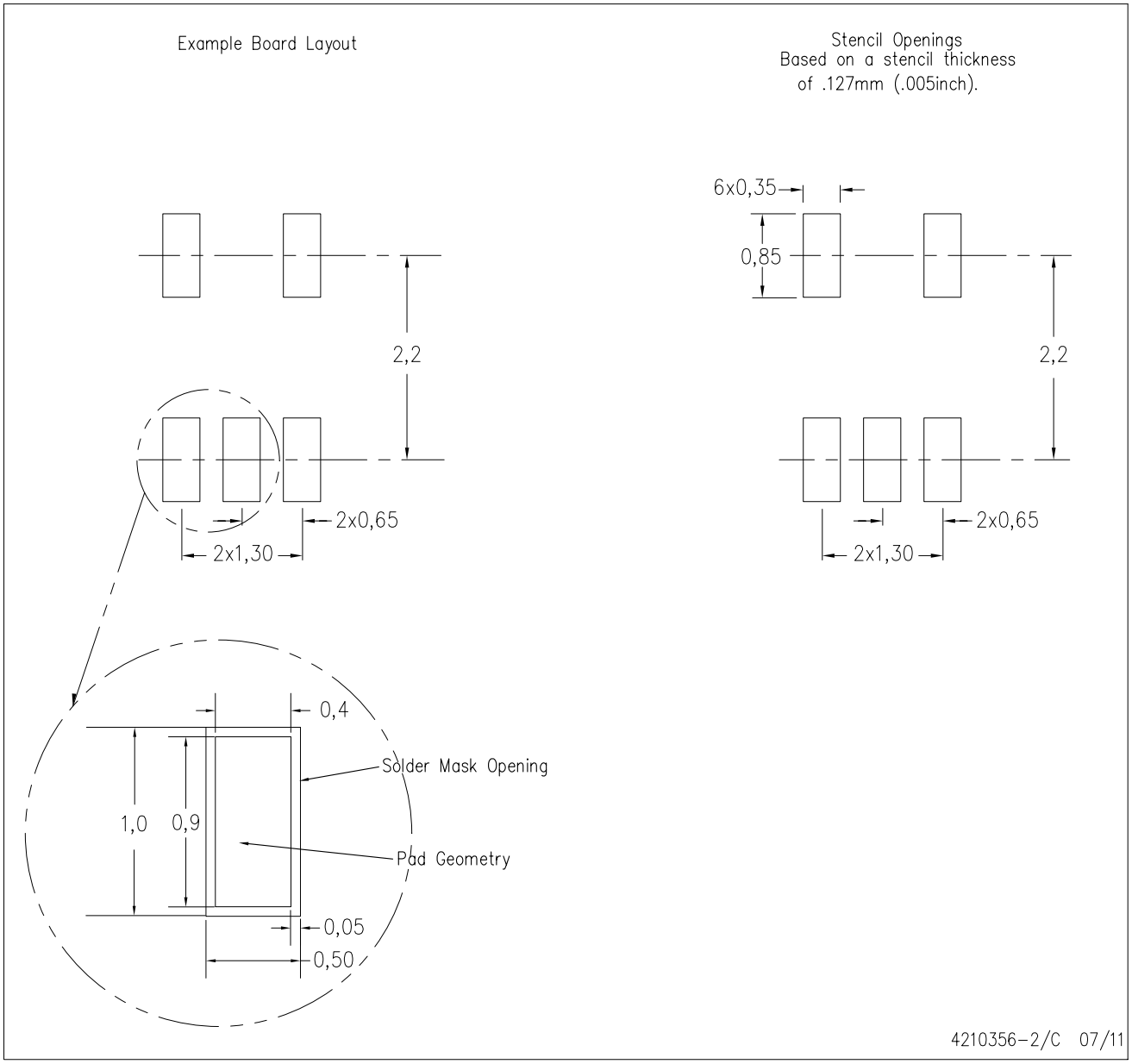
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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