

LM49251 Boomer® Audio Power Amplifier Series **Stereo Audio Subsystem with Class G Headphone Amplifier and Class D Speaker Amplifier with Speaker Protection**

Check for Samples: [LM49251](#)

FEATURES

- **Class G Ground Referenced Headphone Outputs**
- **E²S Class D Amplifier**
- **No Clip Function**
- **Power Limiter Speaker Protection**
- **I²C Volume and Mode Control**
- **Advanced Click-and-Pop Suppression**
- **Micro-Power Shutdown**

APPLICATIONS

- **Feature Phones**
- **Smart Phones**

KEY SPECIFICATIONS

- **Class G Headphone Amplifier, $HPV_{DD} = 1.8V$, $R_L = 32\Omega$**
 - **IDDQ_{HP}: 1.15 mA (Typ)**
 - **Output Power, THD+N ≤ 1%: 20 mW (Typ)**
- **Stereo Class D Speaker Amplifier $R_L = 8\Omega$**
 - **Output Power, THD+N ≤ 1%, $LSV_{DD} = 5.0V$: 1.37 W (Typ)**
 - **Output Power, THD+N ≤ 1%, $LSV_{DD} = 3.6V$: 680 mW (Typ)**
 - **Efficiency: 90% (Typ)**

DESCRIPTION

The LM49251 is a fully integrated audio subsystem designed for portable handheld applications such as cellular phones. Part of TI's PowerWise family of products, the LM49251 utilizes a high efficiency class G headphone amplifier topology as well as a high efficiency class D loudspeaker.

The headphone amplifiers feature TI's class G ground referenced architecture that creates a ground-referenced output with dynamic supply rails for optimum efficiency. The stereo class D speaker amplifier provides both a no-clip feature and speaker protection. The Enhanced Emission Suppression (E²S) outputs feature a patented, ultra low EMI PWM architecture that significantly reduces RF emissions.

The LM49251 features separate volume controls for the mono and stereo inputs. Mode selection, shutdown control, and volume are controlled through an I²C compatible interface.

Click and pop suppression eliminates audible transients on power-up/down and during shutdown. The LM49251 is available in an ultra-small 30-bump DSBGA package (2.55mmx3.02mm)



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Simplified Block Diagram

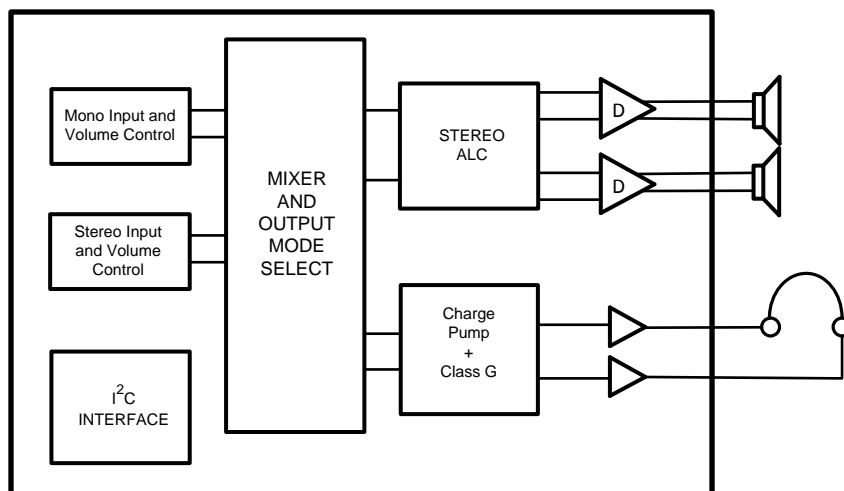


Figure 1. LM49251 Simplified Block Diagram

Typical Application

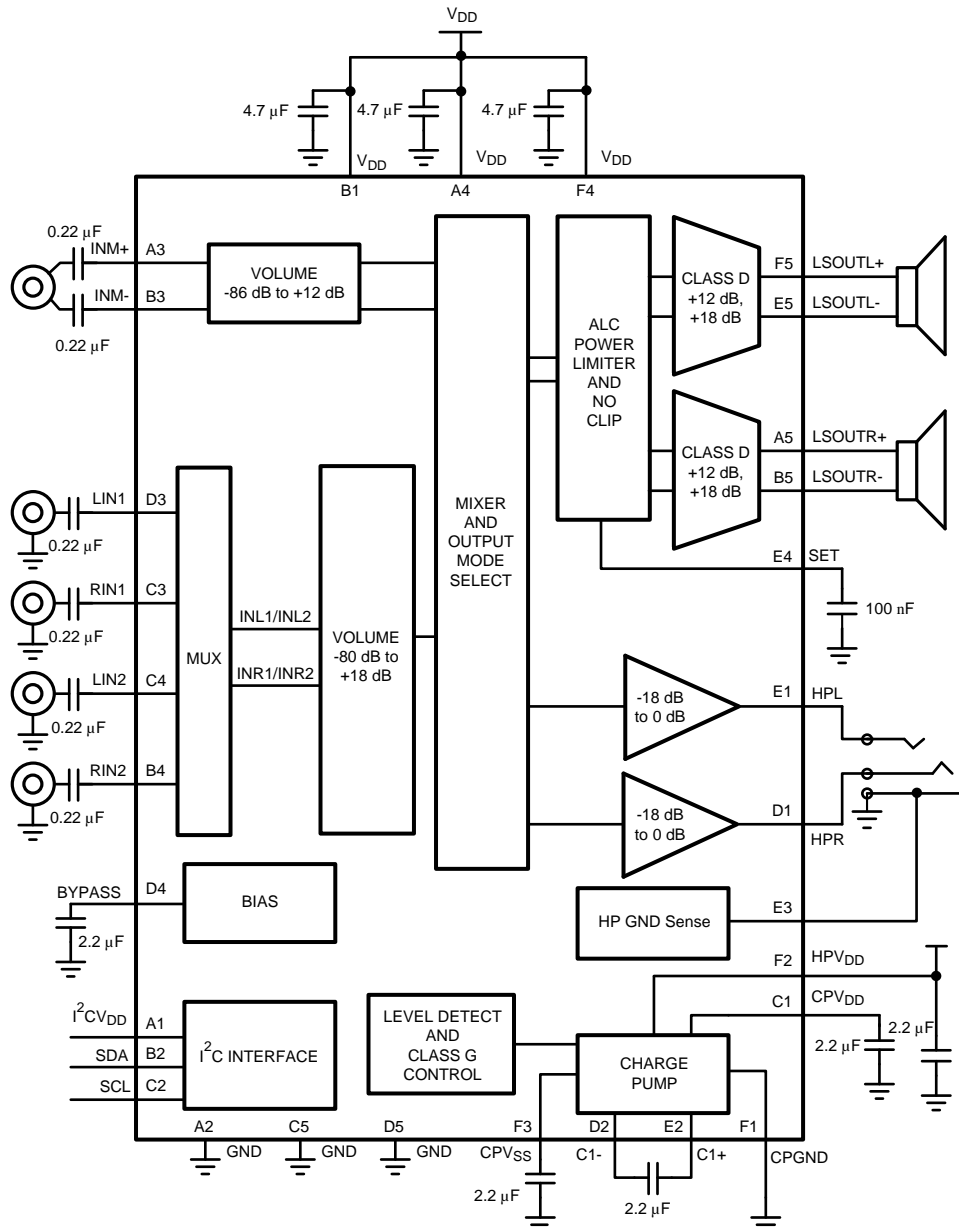


Figure 2. Typical Audio Amplifier Application Circuit

Connection Diagram

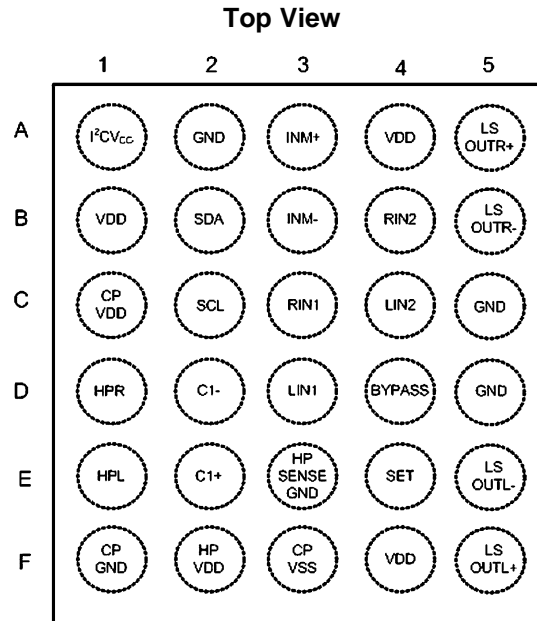


Figure 3. DSBGA Package
See Package Number YZR0030

Table 1. Bump Description

| Bump | Name | Description |
|------|---------------------------------|--|
| A1 | İ ² CV _{DD} | İ ² C Power Supply |
| A2 | GND | Ground |
| A3 | INM+ | Mono Channel Non-Inverting Input |
| A4 | V _{DD} | Loudspeaker Power Supply |
| A5 | LSOUTR+ | Right Loudspeaker Non-Inverting Output |
| B1 | V _{DD} | Loudspeaker Power Supply |
| B2 | SDA | İ ² C Serial Data Input |
| B3 | INM- | Mono Channel Inverting Input |
| B4 | RIN2 | Right Channel Input 2 |
| B5 | LSOUTR- | Right Loudspeaker Inverting Output |
| C1 | CPV _{DD} | Charge Pump Supply (internally generated) |
| C2 | SCL | İ ² C Serial Clock Input |
| C3 | RIN1 | Right Channel Input 1 |
| C4 | LIN2 | Left Channel Input 2 |
| C5 | GND | Ground |
| D1 | HPR | Right Channel Headphone Output |
| D2 | C1- | Charge Pump Flying Capacitor Negative Terminal |
| D3 | LIN1 | Left Channel Input 1 |
| D4 | BYPASS | Mid-Rail Bias Bypass Node |
| D5 | GND | Ground |
| E1 | HPL | Left Channel Headphone Output |
| E2 | C1+ | Charge Pump Flying Capacitor Positive Terminal |
| E3 | HP SENSE GND | Headphone Ground Sense |
| E4 | SET | ALC Timing Set |

Table 1. Bump Description (continued)

| Bump | Name | Description |
|------|-------------------|---------------------------------------|
| E5 | LSOUTL- | Left Loudspeaker Inverting Output |
| F1 | CPGND | Charge Pump Ground |
| F2 | HPV _{DD} | Headphone Power Supply |
| F3 | CPV _{SS} | Charge Pump Output |
| F4 | V _{DD} | Loudspeaker Power Supply |
| F5 | LSOUTL+ | Left Loudspeaker Non-Inverting Output |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾

| | | |
|---|---|--------------------------------|
| Supply Voltage ⁽¹⁾ | V _{DD} , I ² CV _{DD} | 6V |
| | HPV _{DD} | 3V |
| Storage Temperature | | -65°C to +150°C |
| Input Voltage | | -0.3V to V _{DD} +0.3V |
| Power Dissipation ⁽⁴⁾ | | Internally Limited |
| ESD HBM ⁽⁵⁾ | | 2000V |
| ESD MM ⁽⁶⁾ | | 150V |
| ESD CDM ⁽⁷⁾ | | 750V |
| Junction Temperature | | 150°C |
| Thermal Resistance | θ _{JA} (TLA30B1A) | 90°C/W |
| Soldering Information: See AN-1112 (Literature Number SNVA009) | | |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The Electrical Characteristics tables list specified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is P_{DMAX} = (T_{JMAX} - T_A) / θ_{JA} or the number given in *Absolute Maximum Ratings*, whichever is lower.
- (5) Human body model, applicable std. JESD22-A114C.
- (6) Machine model, applicable std. JESD22-A115-A.
- (7) Charge device model, applicable std. JESD22-C101D.

Operating Ratings

| | | |
|---|--------------------------------|---|
| Temperature Range (T _{MIN} ≤ T _A ≤ T _{MAX}) | | -40°C ≤ T _A ≤ +85°C |
| Supply Voltage | V _{DD} | 2.7V ≤ V _{DD} ≤ 5.5V |
| | HPV _{DD} | 1.6V ≤ HPV _{DD} ≤ 2.0V |
| | I ² C _{DD} | 1.7V ≤ I ² CV _{DD} ≤ 5.5V |

Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾

The following specifications apply for $A_V = 0\text{dB}$, $R_L = 15\mu\text{H} + 8\Omega + 15\mu\text{H}$ (Loudspeaker), $R_L = 32\Omega$ (Headphone), $C_{\text{SET}} = 100\text{nF}$, $f = 1\text{kHz}$, ALC off, unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

| Parameter | | Test Conditions | LM49251 | | Units (Limits) |
|---------------------|---|---|--------------------|----------------------|----------------------|
| | | | Typ ⁽⁴⁾ | Limit ⁽⁵⁾ | |
| I_{DD} | Quiescent Power Supply Current ($LSV_{\text{DD}} + V_{\text{DD}}$) | $V_{\text{IN}} = 0$, No Load | | | |
| | | LS Mode (stereo input), mode 2 | 5.6 | 6.25 | mA (max) |
| | | LS Mode (mono input), mode 3 | 5.3 | 6.0 | mA (max) |
| | | HP Mode (stereo input), mode 6 | 2.1 | 2.4 | mA (max) |
| | | HP Mode (mono input), mode 4 | 1.8 | 2.0 | mA (max) |
| | | LS+HP Mode (stereo input), mode 8 | 6.1 | 6.8 | mA (max) |
| | | LS+HP Mode (mono input), mode 5 | 5.8 | 6.5 | mA (max) |
| | | LS Mode (stereo input, ALC on), mode 2 | 5.9 | | |
| $I_{\text{DD(HP)}}$ | Quiescent Power Supply Current (HPV_{DD}) | $V_{\text{IN}} = 0$, No Load, Mode 6 | 1.15 | 1.45 | mA (max) |
| | Operating Power Supply Current (HPV_{DD}) | $P_{\text{OUT}} = 0.5\text{mW}$, $G_{\text{AMP_SD}} = 0$, $R_L = 32\Omega$, Mode 6 | 4.3 | 4.6 | mA (max) |
| | | $P_{\text{OUT}} = 1\text{mW}$, $G_{\text{AMP_SD}} = 0$, $R_L = 32\Omega$, Mode 6 | 5.8 | 6.15 | mA (max) |
| I_{SD} | Shutdown Current | | 0.02 | 1 | μA (max) |
| V_{OS} | Output Offset Voltage | $V_{\text{IN}} = 0$ | | | |
| | | Mode 3, mono input, $A_V = 6\text{dB}$ | 12 | | mV (max) |
| | | Mode 4, mono input | 1.1 | | mV (max) |
| | | Mode 2, stereo input, $A_V = 6\text{dB}$ | 12 | | mV (max) |
| | | Mode 6, stereo input | 1.1 | | mV (max) |
| T_{WU} | Wake Up Time | HP mode, $C_{\text{BYPASS}} = 2.2\mu\text{F}$ | | | |
| | | Normal turn on time | 31 | | ms |
| | | Fast turn on time | 16 | | ms |
| A_{VOL} | Volume Control | Minimum Gain Setting (mono input), Mode 3 | -86 | | dB (max) dB (min) |
| | | Maximum Gain Setting (mono input), Mode 3 | 12 | 13 11.5 | dB (max) dB (min) |
| | | Minimum Gain Setting (stereo input), Mode 6 | -80 | | dB (max) dB (min) |
| | | Maximum Gain Setting (stereo input), Mode 6 | 18 | 19 17.5 | dB (max) dB (min) |
| | Volume Control Step Error | | ± 0.2 | | dB |

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- (2) The Electrical Characteristics tables list specified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Loudspeaker R_L is a resistive load in series with two inductors to simulate an actual speaker load. For $R_L = 8\Omega$, the load is $15\mu\text{H} + 8\Omega + 15\mu\text{H}$. For $R_L = 4\Omega$, the load is $15\mu\text{H} + 4\Omega + 15\mu\text{H}$.
- (4) Typical values represent most likely parametric norms at $T_A = +25^\circ\text{C}$, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (5) Datasheet min/max specification limits are ensured by test or statistical analysis.

Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾ (continued)

The following specifications apply for $A_V = 0\text{dB}$, $R_L = 15\mu\text{H} + 8\Omega + 15\mu\text{H}$ (Loudspeaker), $R_L = 32\Omega$ (Headphone), $C_{\text{SET}} = 100\text{nF}$, $f = 1\text{kHz}$, ALC off, unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

| Parameter | | Test Conditions | LM49251 | | Units (Limits) |
|----------------------|-----------------------------------|--|--------------------|----------------------|--------------------------------------|
| | | | Typ ⁽⁴⁾ | Limit ⁽⁵⁾ | |
| A_V | Gain | LS Mode | | | |
| | | Gain 0 | 12 | 11.5 12.5 | dB (min) dB (max) |
| | | Gain 1 | 18 | 17.5 19 | dB (min) dB (max) |
| | | HP Mode | | | |
| | | Gain 0 | 0 | -0.5 0.5 | dB (min) dB (max) |
| | | Gain 1 | -1.7 | | dB |
| | | Gain 2 | -3 | | dB |
| | | Gain 3 | -6 | | dB |
| | | Gain 4 | -9 | | dB |
| | | Gain 5 | -12 | | dB |
| | | Gain 6 | -15 | | dB |
| $A_{V(\text{MUTE})}$ | Mute Attenuation | LS Output | -93 | | dB |
| | | HP Output | -98 | | dB |
| R_{IN} | Input Resistance | MONO, R_{IN} , L_{IN} inputs | | | |
| | | Maximum Gain Setting | 13 | 9.5 15.5 | k Ω (min) k Ω (max) |
| | | Minimum Gain Setting | 110 | 97 122 | k Ω (min) k Ω (max) |
| P_O | Output Power | Mode 3, $A_V = 18\text{dB}$, $R_L = 8\Omega$ | | | |
| | | $LSV_{\text{DD}} = 3.3\text{V}$ | 570 | | mW |
| | | $LSV_{\text{DD}} = 3.6\text{V}$ | 680 | 600 | mW (min) |
| | | $LSV_{\text{DD}} = 4.2\text{V}$ | 955 | | mW |
| | | $LSV_{\text{DD}} = 5.0\text{V}$ | 1370 | | mW |
| | | Mode 6 | | | |
| | | $R_L = 16\Omega$ | 20 | | mW |
| $R_L = 32\Omega$ | 20 | 16 | mW (min) | | |
| THD+N | Total Harmonic Distortion + Noise | $f = 1\text{kHz}$, Mode 3 Mono Input, $P_O = 250\text{mW}$ | 0.02 | | % |
| | | $f = 1\text{kHz}$, Mode 6 Stereo Input, $P_O = 12\text{mW}$ | 0.02 | | % |
| PSRR | Power Supply Rejection Ratio | $f = 217\text{Hz}$, $V_{\text{RIPPLE}} = 200\text{mV}_{\text{P-P}}$, Inputs AC GND, $C_B = 2.2\mu\text{F}$ | | | |
| | | Mode 3, mono input, $A_V = 6\text{dB}$ | 77 | | dB |
| | | Mode 2, stereo input, $A_V = 6\text{dB}$ | 65 | | dB |
| | | Mode 4, ripple on V_{DD} , mono input | 93 | | dB |
| | | Mode 4, ripple on HPV_{DD} , mono input | 83 | | dB |
| | | Mode 6, ripple on V_{DD} , stereo input | 80 | | dB |
| | | Mode 6, ripple on HPV_{DD} , stereo input | 80 | | dB |
| CMRR | Common Mode Rejection Ratio | $V_{\text{RIPPLE}} = 1\text{V}_{\text{P-P}}$, $f_{\text{RIPPLE}} = 217\text{Hz}$, mono input | | | |
| | | Mode 3 | 52 | | dB |
| | Mode 4 | 63 | | dB | |
| η | Efficiency | LS Mode, $P_O = 680\text{mW}$ | 90 | | % |
| X_{TALK} | Crosstalk | $P_O = 12\text{mW}$, $f = 1\text{kHz}$, Mode 6 | 84 | | dB |

Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾ (continued)

The following specifications apply for $A_V = 0\text{dB}$, $R_L = 15\mu\text{H} + 8\Omega + 15\mu\text{H}$ (Loudspeaker), $R_L = 32\Omega$ (Headphone), $C_{\text{SET}} = 100\text{nF}$, $f = 1\text{kHz}$, ALC off, unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

| Parameter | | Test Conditions | LM49251 | | Units (Limits) |
|------------------------|-----------------------|--|--------------------|----------------------|-------------------|
| | | | Typ ⁽⁴⁾ | Limit ⁽⁵⁾ | |
| ϵ_{OS} | Output Noise | A-weighted, Inputs AC GND | | | |
| | | Mode 3, mono input | 44 | | μV |
| | | Mode 2, stereo input | 45 | | μV |
| | | Mode 4, mono input | 8 | | μV |
| | | Mode 6, stereo input | 10.2 | | μV |
| SNR | Signal-To-Noise-Ratio | Mode 3, $P_O = 680\text{mW}$ | 94 | | dB |
| | | Mode 6, $P_O = 20\text{mW}$ | 98 | | dB |
| t_A | Attack Time | Step 1, Mode 1 | 0.75 | | ms |
| t_R | Release Time | Step 1, Mode 1 | 1 | | s |
| V_{LIMIT} | Output Voltage Limit | Mode 3, $\text{THD} + \text{N} \leq 1\%^{(6)}$ | | | |
| | | Voltage Level | | | |
| | | Step 1 001 | 3.9 | | $V_{\text{P-P}}$ |
| | | Step 2 010 | 4.7 | | $V_{\text{P-P}}$ |
| | | Step 3 011 | 5.4 | | $V_{\text{P-P}}$ |
| | | Step 4 100 | 6.2 | | $V_{\text{P-P}}$ |
| | | Step 5 101 | 7.0 | | $V_{\text{P-P}}$ |
| Step 6 110 | 7.8 | | $V_{\text{P-P}}$ | | |

(6) The LM49251 ALC limits the output power to which ever is lower, the supply voltage or output power limit.

I²C Interface Characteristics $V_{\text{DD}} = 5\text{V}$, $2.2\text{V} \leq I^2\text{C}V_{\text{DD}} \leq 5.5\text{V}^{(1)(2)}$

The following specifications apply for $A_V = 0\text{dB}$, $R_L = 8\Omega$, $f = 1\text{kHz}$, unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

| Parameter | | Test Conditions | LM49251 | | Units (Limits) |
|-----------------|----------------------|-----------------|--------------------|--------------------------------------|---------------------|
| | | | Typ ⁽³⁾ | Limit ⁽⁴⁾ | |
| t_1 | SCL Period | | | 2.5 | μs (min) |
| t_2 | SDA Set-up Time | | | 100 | ns (min) |
| t_3 | SDA Stable Time | | | 0 | ns (min) |
| t_4 | Start Condition Time | | | 100 | ns (min) |
| t_5 | Stop Condition Time | | | 100 | ns (min) |
| t_6 | SDA Hold time | | | 100 | ns (min) |
| V_{IH} | Input High Voltage | | | $0.7 \cdot I^2\text{C}V_{\text{DD}}$ | V (min) |
| V_{IL} | Input Low Voltage | | | $0.3 \cdot I^2\text{C}V_{\text{DD}}$ | V (max) |

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- (4) Datasheet min/max specification limits are ensured by test or statistical analysis.

I²C Interface Characteristics $V_{DD} = 5V, 1.8V \leq I^2CV_{DD} \leq 2.2V$ ⁽¹⁾⁽²⁾

The following specifications apply for $A_V = 0dB$, $R_L = 8\Omega$, $f = 1kHz$, unless otherwise specified. Limits apply for $T_A = 25^\circ C$.

| Parameter | | Test Conditions | LM49251 | | Units (Limits) |
|-----------|----------------------------|-----------------|--------------------|------------------------|----------------|
| | | | Typ ⁽³⁾ | Limit ⁽⁴⁾ | |
| t_1 | SCL Period | | | 2.5 | μs (min) |
| t_2 | SDA Set-up Time | | | 250 | ns (min) |
| t_3 | SDA Stable Time | | | 0 | ns (min) |
| t_4 | Start Condition Time | | | 250 | ns (min) |
| t_5 | Stop Condition Time | | | 250 | ns (min) |
| t_6 | SDA Hold Time | | | 250 | ns (min) |
| V_{IH} | Digital Input High Voltage | | | $0.7 \cdot I^2CV_{DD}$ | V (min) |
| V_{IL} | Digital Input Low Voltage | | | $0.3 \cdot I^2CV_{DD}$ | V (max) |

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Typical Performance Characteristics

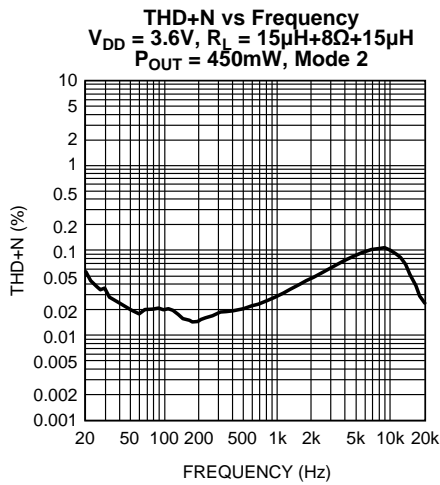


Figure 4.

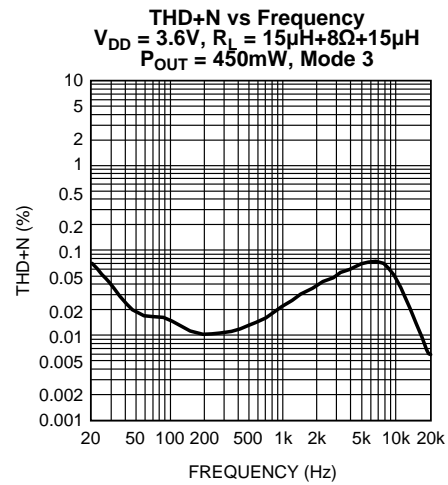


Figure 5.

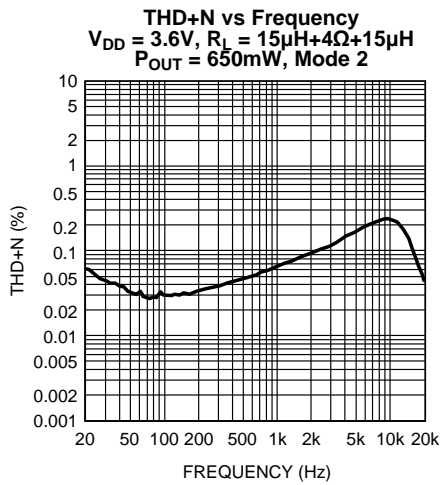


Figure 6.

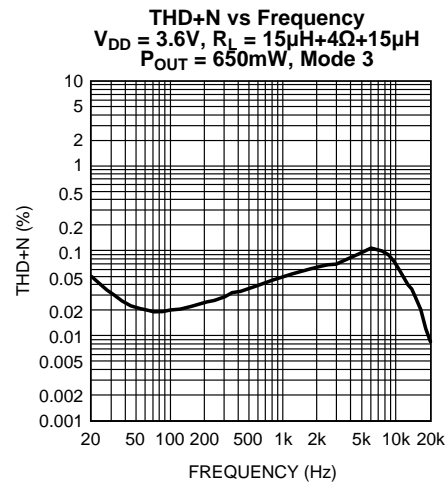


Figure 7.

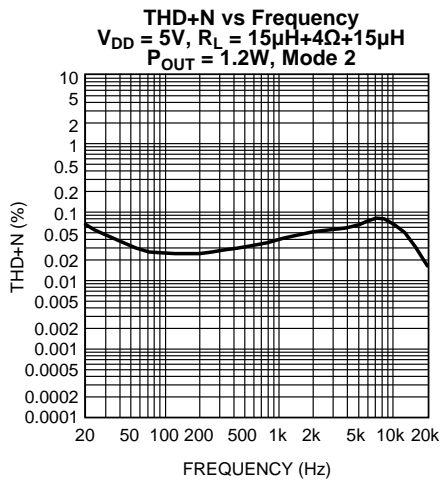


Figure 8.

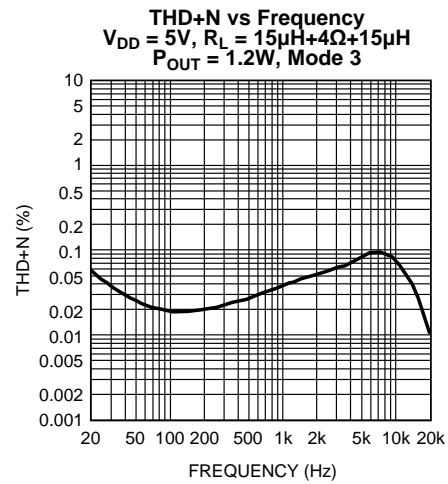


Figure 9.

Typical Performance Characteristics (continued)

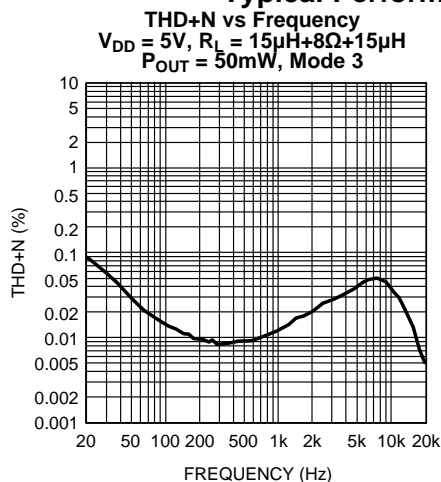


Figure 10.

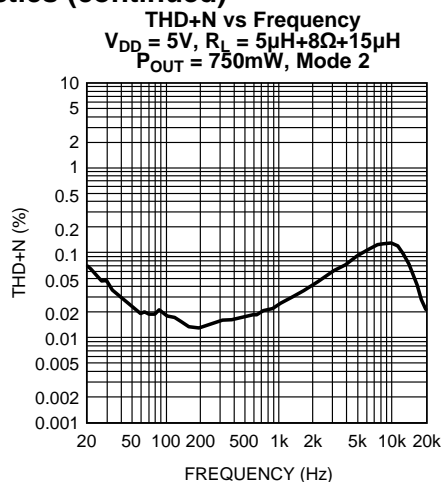


Figure 11.

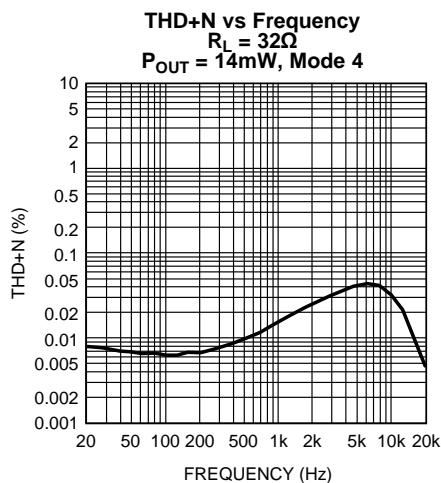


Figure 12.

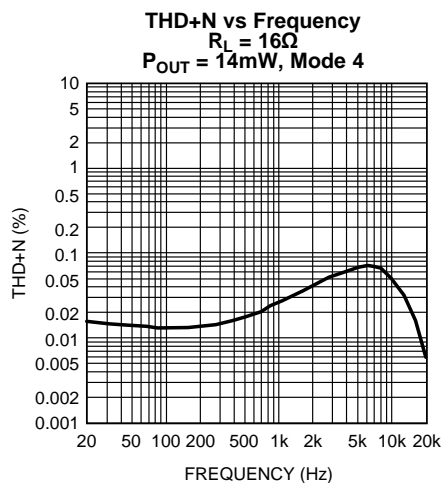


Figure 13.

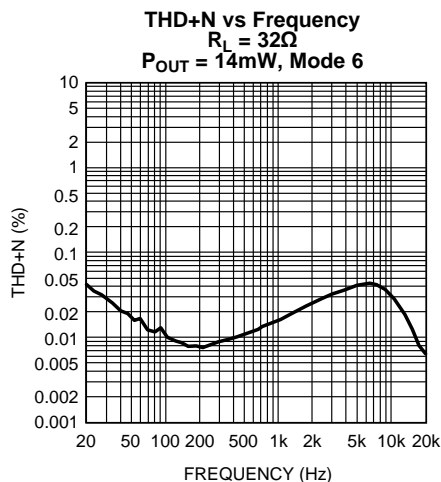


Figure 14.

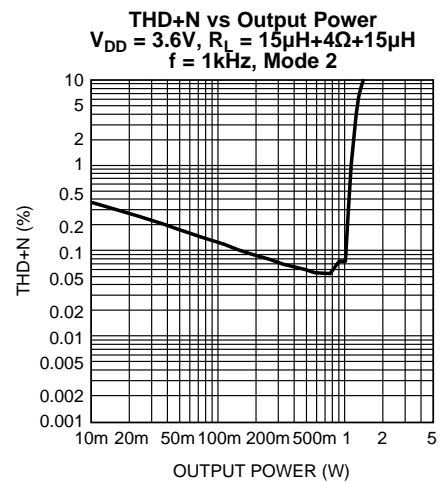


Figure 15.

Typical Performance Characteristics (continued)

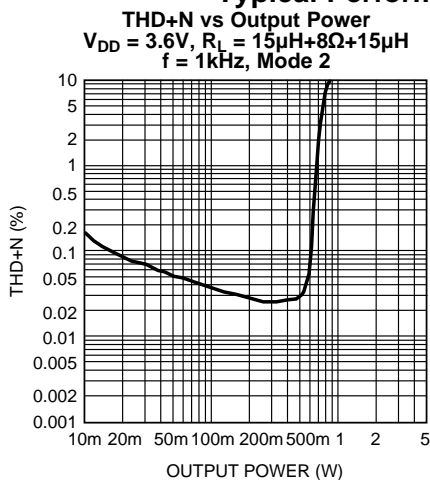


Figure 16.

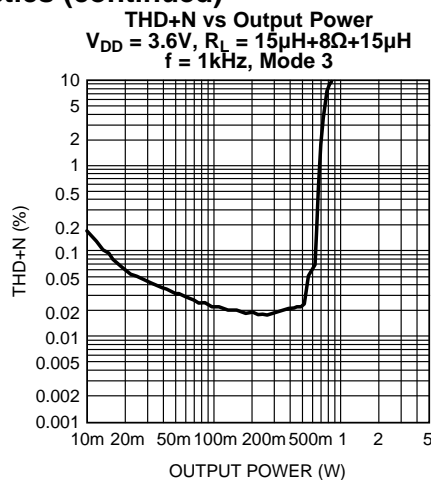


Figure 17.

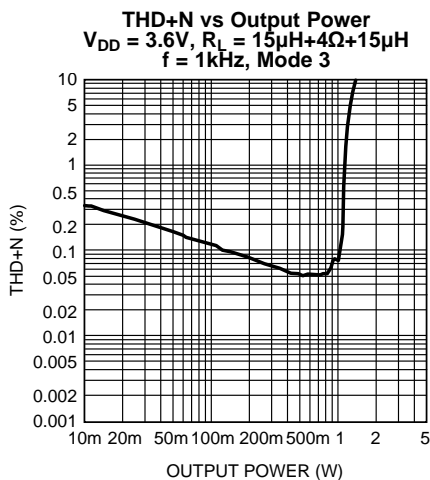


Figure 18.

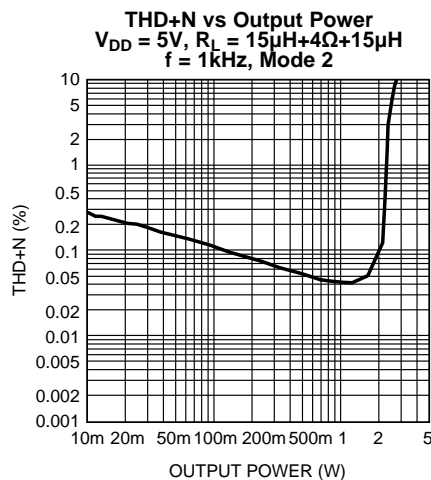


Figure 19.

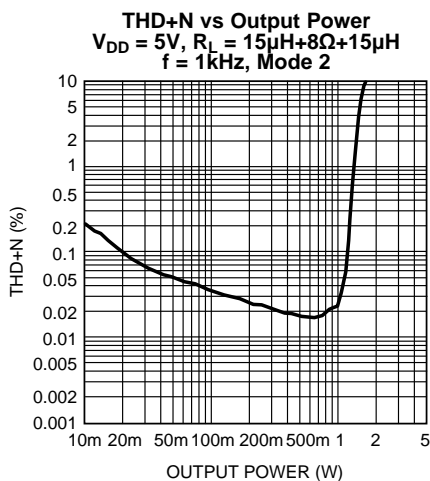


Figure 20.

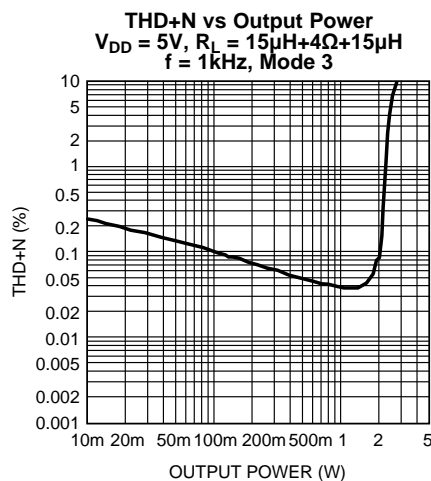


Figure 21.

Typical Performance Characteristics (continued)

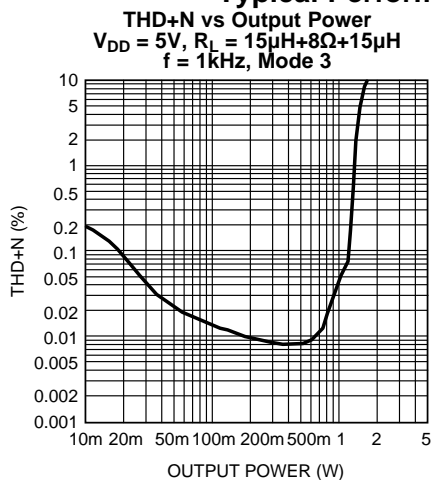


Figure 22.

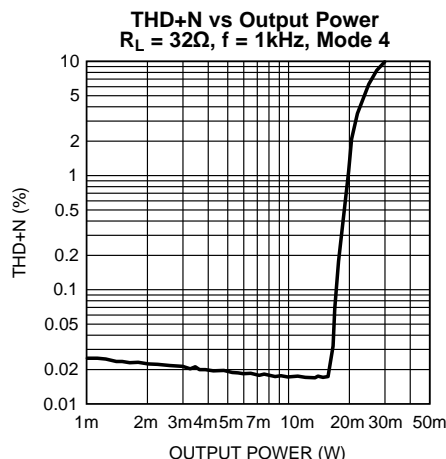


Figure 23.

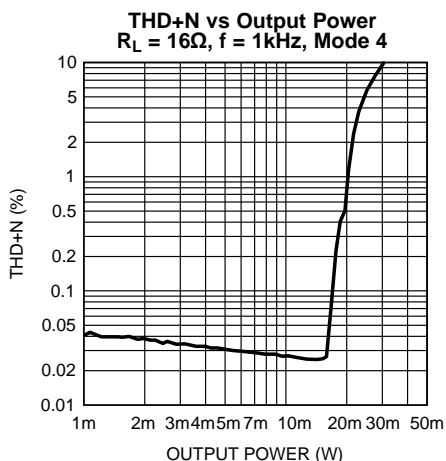


Figure 24.

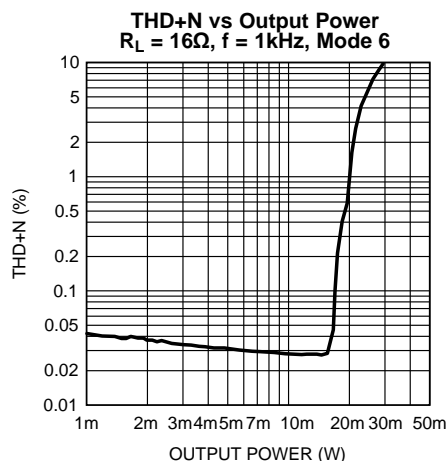


Figure 25.

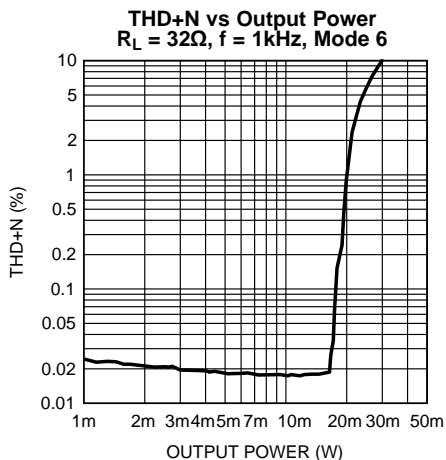


Figure 26.

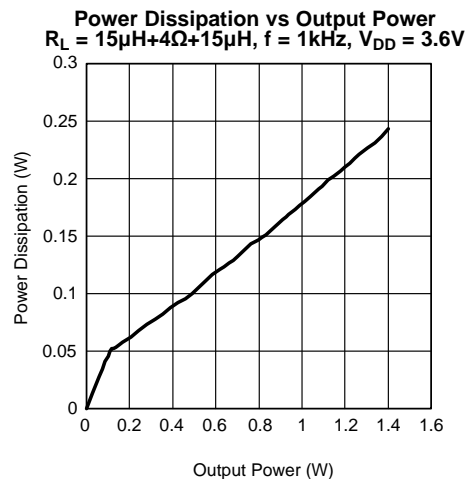
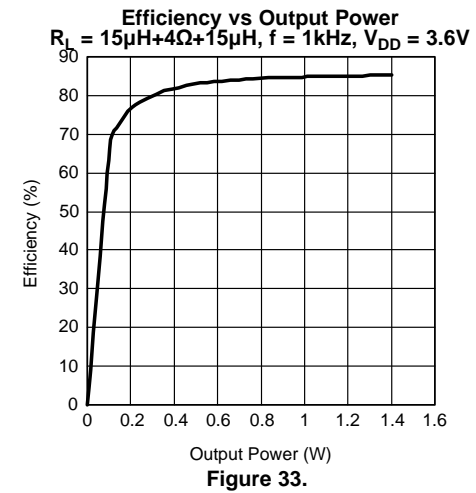
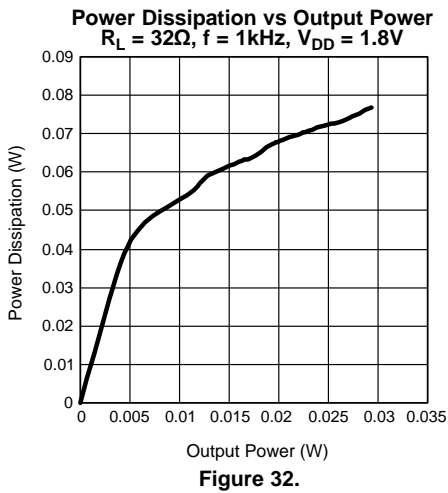
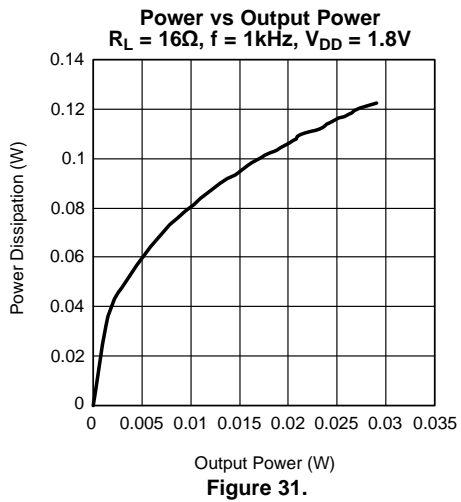
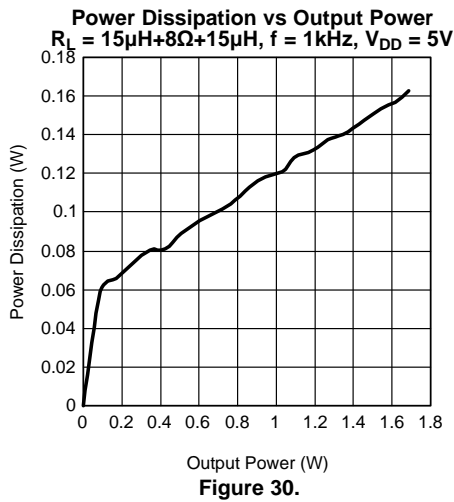
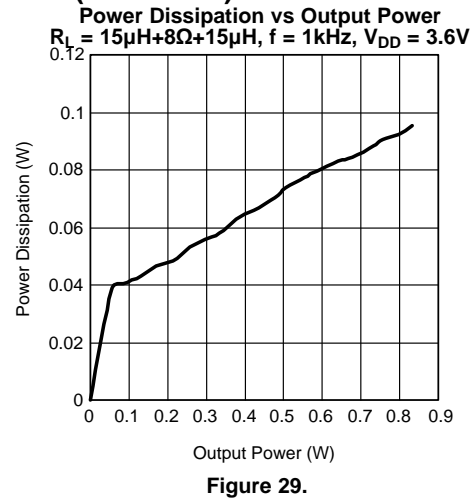
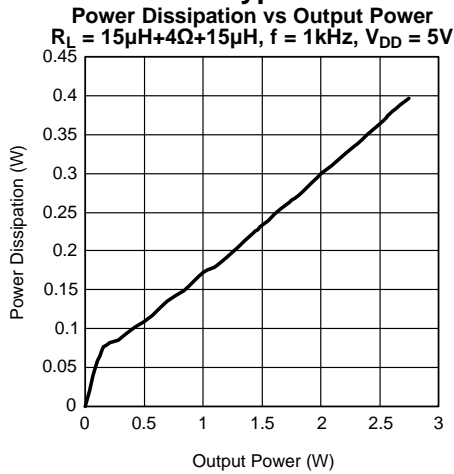


Figure 27.

Typical Performance Characteristics (continued)



Typical Performance Characteristics (continued)

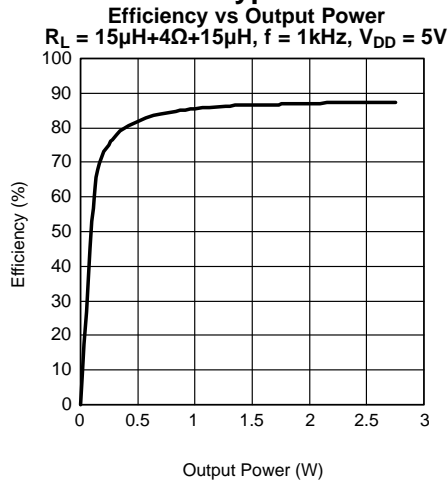


Figure 34.

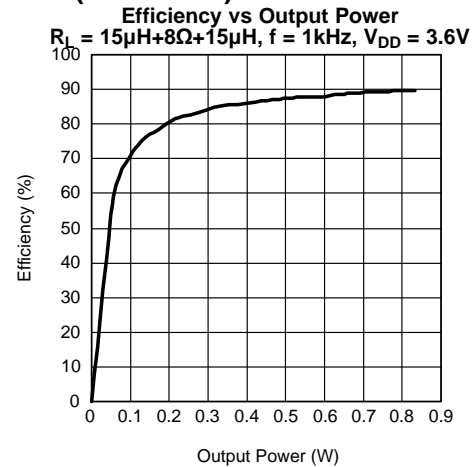


Figure 35.

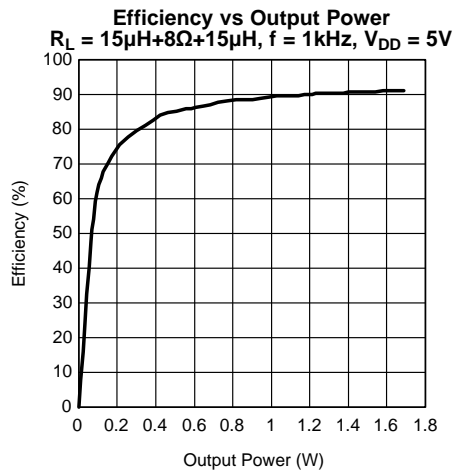


Figure 36.

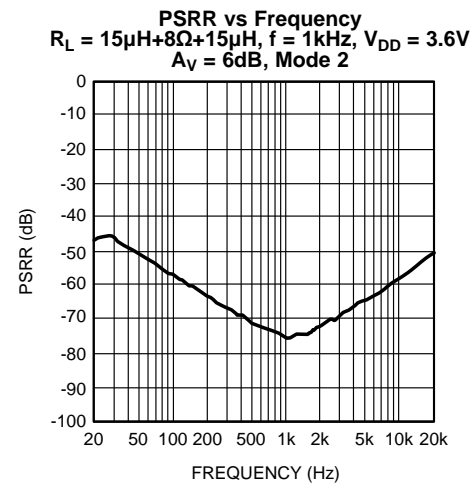


Figure 37.

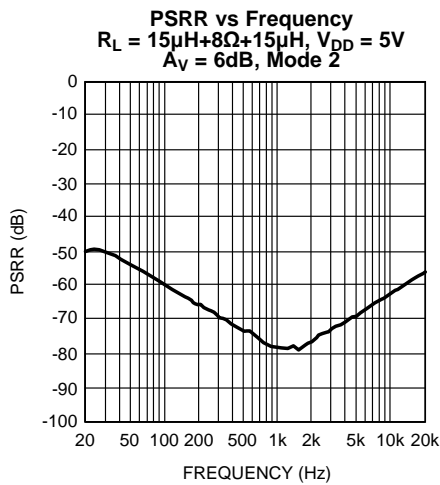


Figure 38.

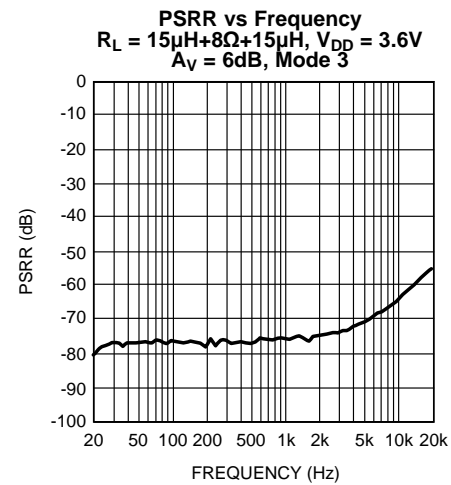


Figure 39.

Typical Performance Characteristics (continued)

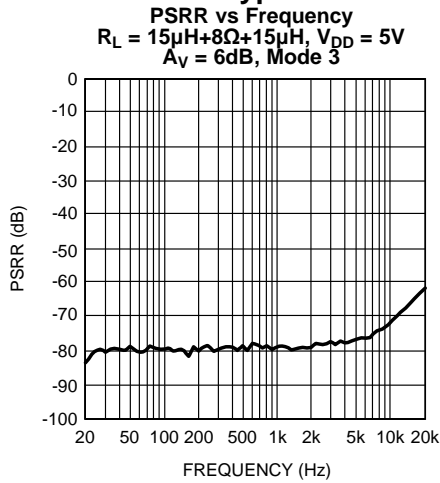


Figure 40.

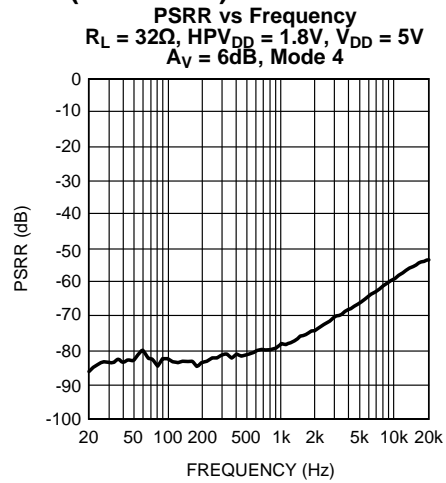


Figure 41.

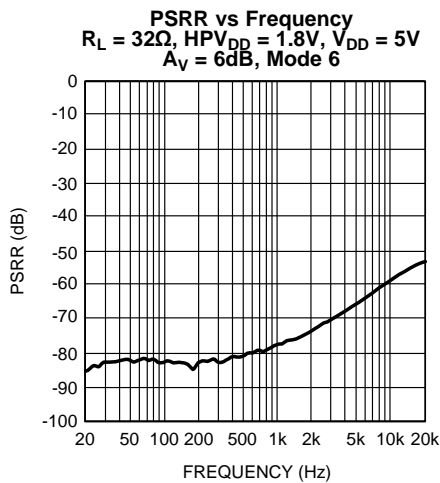


Figure 42.

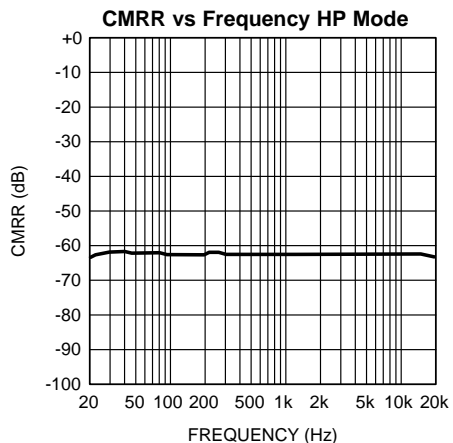


Figure 43.

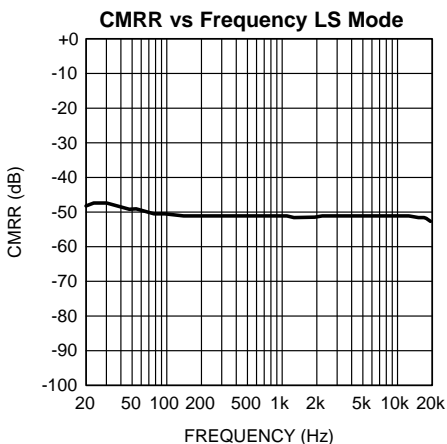


Figure 44.

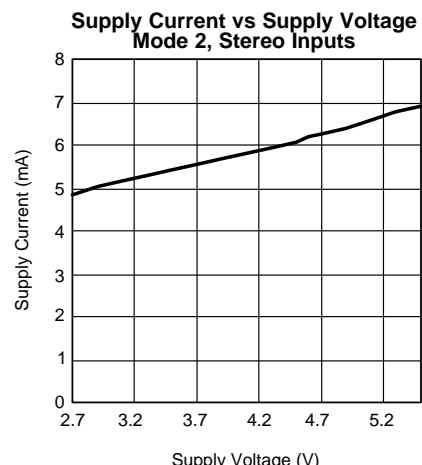


Figure 45.

Typical Performance Characteristics (continued)

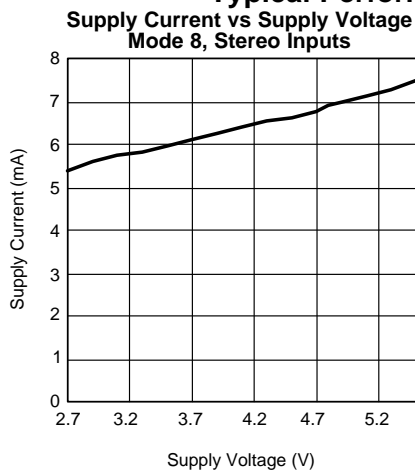


Figure 46.

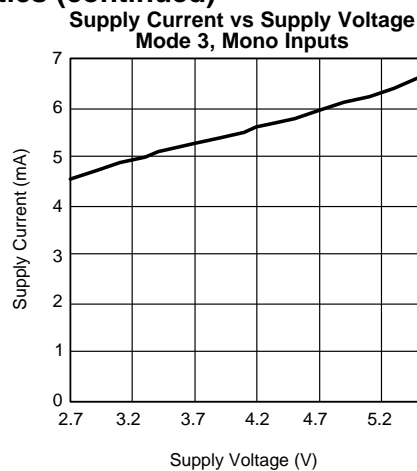


Figure 47.

System Control

I²C SIGNALS

In I²C mode the LM49251 pin SCL is used for the I²C clock SCL and the pin SDA is used for the I²C data signal SDA. Both of these signals need a pull-up resistor according to I²C specification. The 7-bits I²C slave address for LM49251 is 1111100.

I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when SCL is LOW.

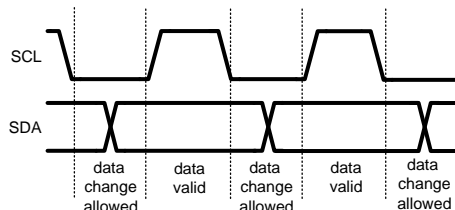


Figure 48. I²C Signals: Data Validity

I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

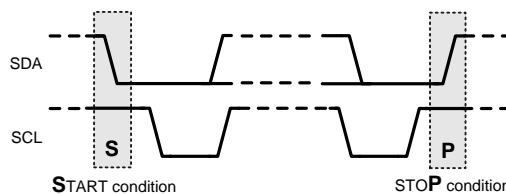


Figure 49. I²C Start and Stop Conditions

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received. After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eight bit which is a data direction bit (R/W). The LM49251 address is 11111000. For the eighth bit, a "0" indicates a WRITE and a "1" indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.



Figure 50. I²C Chip Address

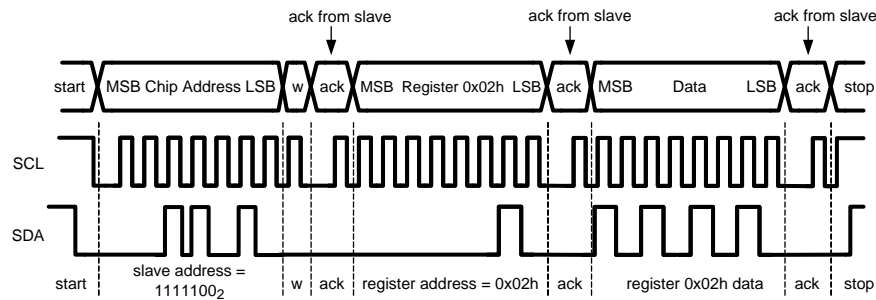
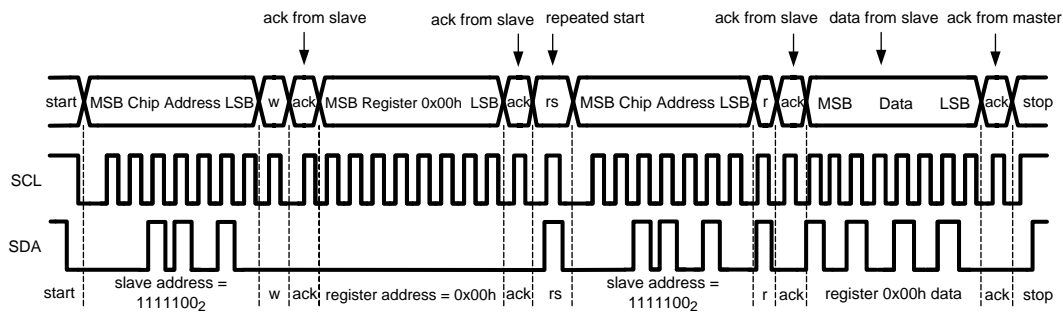


Figure 51. Example I²C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.



w = write (SDA = "0")
 r = read (SDA = "1")
 ack = acknowledge (SDA pulled down by slave)
 rs = repeated start

Figure 52. Example I²C Read Cycle

Table 2. Device Address

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----------------|----|----|----|----|----|----|----|----|
| Device Address | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

Table 3. I²C Control Registers

| Register Name | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----------------------|----|----|----|---------|---------|---------|------------|-----------------|
| SHUTDOWN CONTROL | 0 | 0 | 0 | 1 | GAMP_ON | HPR_SD | Class G_SD | \overline{SD} |
| MODE CONTROL | 0 | 0 | 1 | HP_ST | HP_M | SPK_L+R | SPK_ST | SPK_M |
| POWER LIMITER CONTROL | 0 | 1 | 0 | ATK1 | ATK0 | PLEV2 | PLEV1 | PLEV0 |
| NO CLIP CONTROL | 0 | 1 | 1 | RLT1 | RLT0 | OCP2 | OCP1 | OCP0 |
| GAIN CONTROL | 1 | 0 | 0 | LSGAINL | LSGAINR | HPGAIN2 | HPGAIN1 | HPGAIN0 |
| MONO VOLUME CONTROL | 1 | 0 | 1 | MG4 | MG3 | MG2 | MG1 | MG0 |
| STEREO VOLUME CONTROL | 1 | 1 | 0 | SG4 | SG3 | SG2 | SG1 | SG0 |

Table 3. I²C Control Registers (continued)

| Register Name | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----------------|----|----|----|----|----|------------------------------------|----------|--------------|
| CLASS D CONTROL | 1 | 1 | 1 | 0 | 0 | 0 | ER_CNTRL | SS_EN |
| LS CONTROL | 1 | 1 | 1 | 0 | 1 | 0 | ST_SEL | LSR_SD |
| CLASS G CONTROL | 1 | 1 | 1 | 1 | 0 | 0 | TLEV1 | TLEV2 |
| OTHER CONTROL | 1 | 1 | 1 | 1 | 1 | I ² CV _{DD} SD | RAIL_SW | TURN_ON TIME |

Table 4. Shutdown Control

| BIT | NAME | VALUE | DESCRIPTION |
|-----|------------|---|------------------------------------|
| B3 | GAMP_ON | This disables the gain amplifiers that are not in use to minimize I _{DD} . | |
| | | 0 | Normal Operation |
| | | 1 | Unused gain amplifiers disabled |
| B2 | HPR_SD | This disables the right headphone output. | |
| | | 0 | Normal operation |
| | | 1 | Right headphone amplifier disabled |
| B1 | Class G_SD | This disables the Class G. | |
| | | 0 | Class G enabled |
| | | 1 | Class G disabled |
| B0 | SD | LM49251 Shutdown | |
| | | 0 | LM49251 Disabled |
| | | 1 | LM49251 Enabled |

Table 5. Output Mode Selection

| HP (ST) | HP (M) | SPK (L+R) | SPK (ST) | SPK (M) | SPK(L) | SPK(R) | HP(L) | HP(R) | Datasheet |
|---------|--------|-----------|----------|---------|---------------|---------------|--------|---------|-----------|
| 0 | 0 | 0 | 0 | 0 | SD | SD | SD | SD | Mode 0 |
| 0 | 0 | 1 | 1 | 0 | GST X (L + R) | GST X (L + R) | SD | SD | Mode 1 |
| 0 | 0 | 0 | 1 | 0 | GST X L | GST X R | SD | SD | Mode 2 |
| 0 | 0 | 0 | 0 | 1 | GM X M | GM X M | SD | SD | Mode 3 |
| 0 | 1 | 0 | 0 | 0 | SD | SD | GM X M | GM X M | Mode 4 |
| 0 | 1 | 0 | 0 | 1 | GM X M | GM X M | GM X M | GM X M | Mode 5 |
| 1 | 0 | 0 | 0 | 0 | SD | SD | GSTX L | GST X R | Mode 6 |
| 1 | 0 | 1 | 1 | 0 | GST X (L + R) | GST X (L + R) | GSTX L | GST X R | Mode 7 |
| 1 | 0 | 0 | 1 | 0 | GST X L | GST X R | GSTX L | GST X R | Mode 8 |

Table 6. Voltage Limit Control Register

| BIT | NAME | VALUE | | | DESCRIPTION |
|-------|-------------------------|----------|------------------------|----|---|
| B4:B3 | ATK1 ATK2 | B4 | | B3 | Sets Attack Time based on C _{SET} and R _{SET} t _{ATK} 1.3 x t _{ATK} 2 x t _{ATK} 2.7 x t _{ATK} |
| | | 0 | | 0 | |
| | | 0 | | 1 | |
| | | 1 | | 0 | |
| B2:B0 | PLEV2 PLEV1 PLEV0 | B2 B1 B0 | | | Sets output power limit level |
| | | 0 | 0 | 0 | Voltage Limit disabled |
| | | 0 | 0 | 1 | V _{TH(VLIM)} = 3.9V _{P-P} |
| | | 0 | 1 | 0 | V _{TH(VLIM)} = 4.7V _{P-P} |
| | | 0 | 1 | 1 | V _{TH(VLIM)} = 5.4V _{P-P} |
| | | 1 | 0 | 0 | V _{TH(VLIM)} = 6.2V _{P-P} |
| | | 1 | 0 | 1 | V _{TH(VLIM)} = 7.0V _{P-P} |
| | | 1 | 1 | 0 | V _{TH(VLIM)} = 7.8V _{P-P} |
| 1 | 1 | 1 | Voltage Limit disabled | | |

Table 7. No Clip Control Register

| BIT | NAME | VALUE | | | DESCRIPTION |
|-------|----------------------|----------|---|---|--|
| B2:B0 | OCP2 OCP1 OCP0 | B2 B1 B0 | | | This sets the output clip limit level |
| | | 0 | 0 | 0 | NO_CLIP = disabled, OUTPUT_CLIP = disabled |
| | | 0 | 0 | 1 | Test Mode |
| | | 0 | 1 | 0 | NO_CLIP = enabled, OUTPUT_CLIP = disabled |
| | | 0 | 1 | 1 | low |
| | | 1 | 0 | 0 | medium |
| | | 1 | 0 | 1 | medium high |
| | | 1 | 1 | 0 | high |
| B4:B3 | RLT1 RTL0 | B1 B0 | | | This sets the release time of the automatic limiter control circuit. |
| | | 0 | 0 | | 1s |
| | | 0 | 1 | | 0.8s |
| | | 1 | 0 | | 0.65s |
| | | 1 | 1 | | 0.4s |

Table 8. Gain Control Register

| BIT | NAME | VALUE | DESCRIPTION |
|-----|---------|-------|-----------------------|
| B4 | LSGAINL | 0 | 6dB Loudspeaker gain |
| | | 1 | 12dB Loudspeaker gain |
| B3 | LSGAINR | 0 | 6dB Loudspeaker gain |
| | | 1 | 12dB Loudspeaker gain |

Table 8. Gain Control Register (continued)

| BIT | NAME | VALUE | | | DESCRIPTION |
|-------|--|-------|----|----|-----------------------|
| | | B2 | B1 | B0 | |
| B2:B0 | HPGAIN2 (B2) HPGAIN1 (B1) HPGAIN0 (B0) | 0 | 0 | 0 | Headphone Gain 0dB |
| | | 0 | 0 | 1 | -1.5dB |
| | | 0 | 1 | 0 | -3dB |
| | | 0 | 1 | 1 | -6dB |
| | | 1 | 0 | 0 | -9dB |
| | | 1 | 0 | 1 | -12dB |
| | | 1 | 1 | 0 | -15dB |
| | | 1 | 1 | 1 | -18dB |

General Amplifier Function**Table 9. Volume Control Table**

| VOLUME STEP | _G4 | _G3 | _G2 | _G1 | _G0 | GAIN (dB) |
|-------------|-----|-----|-----|-----|-----|-----------|
| 1 | 0 | 0 | 0 | 0 | 0 | -80 |
| 2 | 0 | 0 | 0 | 0 | 1 | -46.5 |
| 3 | 0 | 0 | 0 | 1 | 0 | -40.5 |
| 4 | 0 | 0 | 0 | 1 | 1 | -34.5 |
| 5 | 0 | 0 | 1 | 0 | 0 | -30 |
| 6 | 0 | 0 | 1 | 0 | 1 | -27 |
| 7 | 0 | 0 | 1 | 1 | 0 | -24 |
| 8 | 0 | 0 | 1 | 1 | 1 | -21 |
| 9 | 0 | 1 | 0 | 0 | 0 | -18 |
| 10 | 0 | 1 | 0 | 0 | 1 | -15 |
| 11 | 0 | 1 | 0 | 1 | 0 | -13.5 |
| 12 | 0 | 1 | 0 | 1 | 1 | -12 |
| 13 | 0 | 1 | 1 | 0 | 0 | -10.5 |
| 14 | 0 | 1 | 1 | 0 | 1 | -9 |
| 15 | 0 | 1 | 1 | 1 | 0 | -7.5 |
| 16 | 0 | 1 | 1 | 1 | 1 | -6 |
| 17 | 1 | 0 | 0 | 0 | 0 | -4.5 |
| 18 | 1 | 0 | 0 | 0 | 1 | -3 |
| 19 | 1 | 0 | 0 | 1 | 0 | 1.5 |
| 20 | 1 | 0 | 0 | 1 | 1 | 0 |
| 21 | 1 | 0 | 1 | 0 | 0 | 1.5 |
| 22 | 1 | 0 | 1 | 0 | 1 | 3 |
| 23 | 1 | 0 | 1 | 1 | 0 | 4.5 |
| 24 | 1 | 0 | 1 | 1 | 1 | 6 |
| 25 | 1 | 1 | 0 | 0 | 0 | 7.5 |
| 26 | 1 | 1 | 0 | 0 | 1 | 9 |
| 27 | 1 | 1 | 0 | 1 | 0 | 10.5 |
| 28 | 1 | 1 | 0 | 1 | 1 | 12 |
| 29 | 1 | 1 | 1 | 0 | 0 | X |
| 30 | 1 | 1 | 1 | 0 | 1 | X |
| 31 | 1 | 1 | 1 | 1 | 0 | X |
| 32 | 1 | 1 | 1 | 1 | 1 | X |

Table 10. Class D Control

| BIT | NAME | VALUE | DESCRIPTION |
|-----|----------|---------------------------------|----------------------------|
| B1 | ER_CNTRL | This enables edge rate control. | |
| | | 0 | Edge Rate Control Disabled |
| | | 1 | Edge Rate Control Enabled |
| B0 | SS_EN | This enables Spread Spectrum. | |
| | | 0 | Spread Spectrum Disabled |
| | | 1 | Spread Spectrum Enabled |

Table 11. Loudspeaker (LS) Control

| BIT | NAME | VALUE | DESCRIPTION |
|-----|--------|--|---------------------------|
| B1 | ST_SEL | This allows selection between two Stereo Inputs. | |
| | | 0 | LIN1/RIN1 |
| | | 1 | LIN2/RIN2 |
| B0 | LSR_SD | This disables the Left Loudspeaker. | |
| | | 0 | Left Loudspeaker enabled |
| | | 1 | Left Loudspeaker disabled |

Table 12. Class G Control

| BIT | NAME | VALUE | | DESCRIPTION |
|-------|----------------|---------------------------|----|----------------|
| | | B1 | B0 | |
| B1:B0 | TLEV1 TLEV0 | This sets the Trip Level. | | |
| | | 0 | 0 | High (default) |
| | | 0 | 1 | High-Medium |
| | | 1 | 0 | Low-Medium |
| | | 1 | 1 | Low |

Table 13. Other Control

| BIT | NAME | VALUE | DESCRIPTION |
|-----|--------------|---|---------------------|
| B1 | RAIL_SW | This switches between two HP voltage rails ⁽¹⁾ | |
| | | 0 | High Rail |
| | | 1 | Low Rail |
| B0 | TURN_ON_TIME | This allows fast turn on time | |
| | | 0 | Normal Turn-On Time |
| | | 1 | Fast Turn-On Time |

(1) This option is only available when the Class G is disabled.

APPLICATION INFORMATION

DIFFERENTIAL AMPLIFIER EXPLANATION

The LM49251 features a differential input stage, which offers improved noise rejection compared to a single-ended input amplifier. Because a differential input amplifier amplifies the difference between the two input signals, any component common to both signals is cancelled. An additional benefit of the differential input structure is the possible elimination of the DC input blocking capacitors. Since the DC component is common to both inputs, and thus cancelled by the amplifier, the LM49251 can be used without input coupling capacitors when configured with a differential input signal.

INPUT MIXER/MULTIPLEXER

The LM49251 includes a comprehensive mixer multiplexer controlled through the I²C interface. The mixer/multiplexer allows any input combination to appear on any output of LM49251. [Table 5](#) (MODE CONTROL) shows how the input signals are routed together for each possible input selection.

SHUTDOWN FUNCTION

The LM49251 features the following shutdown controls: Bit B4 (GAMP_SD) of the SHUTDOWN CONTROL register controls the gain amplifiers. When GAMP_SD = 1, it disables the gain amplifiers that are not in use. For example, in Modes 1, 4 and 5, the Mono inputs are in use, so the Left and Right input gain amplifiers are disabled, causing the I_{DD} to be minimized. Bit B0 (PWR_ON) of the SHUTDOWN CONTROL register is the global shutdown control for the entire device. Set PWR_ON = 0 for normal operation. PWR_ON = 1 overrides any other shutdown control bit.

CLASS D AMPLIFIER

The LM49251 features a mono class D audio power amplifier with a filterless modulation scheme that reduces external component count, conserving board space and reducing system cost. With no signal applied, the outputs (LSOUT+ and LSOUT-) switch between V_{DD} and GND with 50% duty cycle, in phase, causing the two outputs to cancel. This cancellation results in no net voltage across the speaker, thus there is no current to the load in the idle state.

With an input signal applied, the duty cycle (pulse width) of the class D output changes. For increasing output voltage, the duty cycle of LSOUT+ increases, while the duty cycle of LSOUT- decreases. For decreasing output voltages, the converse occurs. The difference between the two pulse widths yields the differential output voltage.

ENHANCED EMISSIONS SUPPRESSION (E²S)

The LM49251 class D amplifier features TI's patent-pending E²S system that reduces EMI, while maintaining high quality audio reproduction and efficiency. The E²S system features selectable spread spectrum and advanced edge rate control (ERC). The LM49251 class D ERC greatly reduces the high frequency components of the output square waves by controlling the output rise and fall times, slowing the transitions to reduce RF emissions, while maximizing THD+N and efficiency performance.

FIXED FREQUENCY

The LM49251 class D amplifier features two modulation schemes, a fixed frequency mode and a spread spectrum mode. Select the fixed frequency mode by setting bit B0 (SS_EN) of the SS Control register to 0. In fixed frequency mode, the loudspeaker outputs switch at a constant 300kHz. The output spectrum consists of the 300kHz fundamental and its associated harmonics.

SPREAD SPECTRUM

The selectable spread spectrum mode minimizes the need for output filters, ferrite beads or chokes. In spread spectrum mode, the switching frequency varies randomly by 30% about a 300kHz center frequency, reducing the wideband spectral content, improving EMI emission radiated by the speaker and associated cables and traces. Where a fixed frequency class D exhibits large amounts of spectral energy at multiples of the switching frequency, the spread spectrum architecture spreads that energy over a larger bandwidth. The cycle-to-cycle variation of the switching period does not affect the audio reproduction, efficiency, or PSRR. Set bit B0 (SS_EN) of the SS Control register to 1 to enable spread spectrum mode.

GROUND REFERENCED HEADPHONE AMPLIFIER

The LM49251 features a low noise inverting charge pump that generates an internal negative supply voltage. This allows the headphone outputs to be biased about GND instead of a nominal DC voltage, like traditional headphone amplifiers. Because there is no DC component, the large DC blocking capacitors (typically 220 μ F) at the headphone outputs are not necessary. The coupling capacitors are replaced by two small ceramic charge pump capacitors, saving board space and cost. Eliminating the output coupling capacitors also improves low frequency response. In traditional headphone amplifiers, the headphone impedance and the output capacitor form a high-pass filter that not only blocks the DC component of the output, but also attenuates low frequencies, impacting the bass response. Because the LM49251 does not require the output coupling capacitors, the low frequency response of the device is not degraded by external components. In addition to eliminating the output coupling capacitors, the ground referenced output nearly doubles the available dynamic range of the LM49251 headphone amplifiers when compared to a traditional headphone amplifier operating from the same supply voltage.

CLASS G OPERATION

The LM49251 features a ground referenced class G headphone amplifier for increased efficiency and decreased power dissipation. This particular architecture creates a ground-referenced output with dynamic supply rails for optimum efficiency. Music and voice signals have a high peak-to-mean ratio with the majority of the signal content at low levels, class G amplifiers take advantage of this behavior. Class G amplifiers have multiple voltage supplies to decrease power dissipation. The LM49251 has two discrete supply rails: ± 0.9 V and ± 1.8 V. The device switches from ± 0.9 V to ± 1.8 V when the output signal reaches the selectable threshold level to switch to the higher voltage rails. When the output falls below the required voltage for a set period of time, it will switch back to the lower rail until the next time the threshold is reached. The threshold level has 4 selectable levels that can be set through the Class G Control I²C control register <B1:B2>. With this topology power dissipation is reduced for typical music or voice sources. Figure 53 below shows how a music output may look.

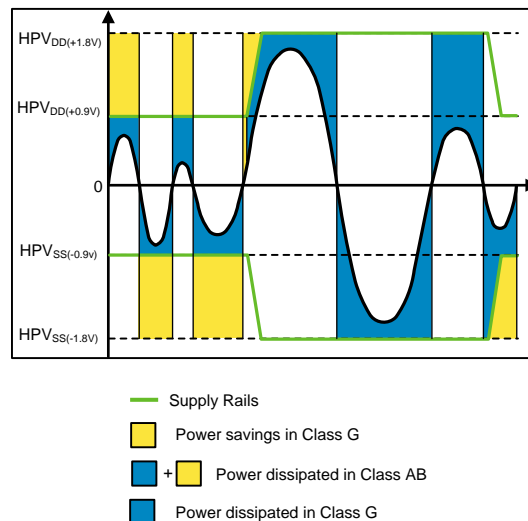


Figure 53. Class G Operation

Disabling the Class G

The Class G feature can be disabled via I²C Shutdown Control Register B1. When the Class G is disabled the headphone supply rails are selectable. In the Other Control register B1 = 0 sets the headphone supply rails at ± 1.8 V (high) and B1 = 1 sets the supply to ± 0.9 V (low). Figure 54 below shows a curve of THD+N vs Output Power for the two supply rails.

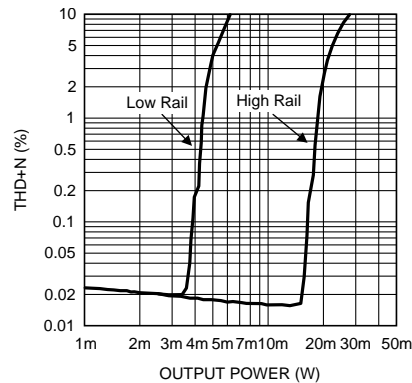


Figure 54. Class G Disabled (Low/High Supply Rails)

AUTOMATIC LIMITER CONTROL (ALC)

When enabled, the ALC continuously monitors and adjusts the gain of the loudspeaker amplifier signal path if necessary. The ALC serves two functions: voltage limiter/speaker protection and output clip prevention (No-Clip) with three clip controls levels. The voltage limiter/speaker protection prevents an output overload condition by maintaining the loudspeaker output signal below a preset amplitude (See [VOLTAGE LIMITER](#) section). The No Clip feature monitors the output signal and maintains audio quality by preventing the loudspeaker output from exceeding the amplifier's headroom (see [NO CLIP/OUTPUT CLIP CONTROL](#) section). The voltage limiter thresholds, clip control levels, attack and release times are configured through the I²C interface.

VOLTAGE LIMITER

The voltage limiter function of the ALC monitors and prevents the audio signal from exceeding the voltage limit threshold. The voltage limit threshold ($V_{TH(VLIM)}$) is set by bits B2:B0 in the "Voltage Limit Threshold Register" (see [Table 6](#)). Although the ALC reduces the gain of the speaker path to maintain the audio signal below the voltage limit threshold, it is still possible to overdrive the speaker output in which case loudspeaker output will exceed the voltage limit threshold and cause clipping on the output, and speaker damage is possible. Please see the [ALC HEADROOM](#) section for further details.

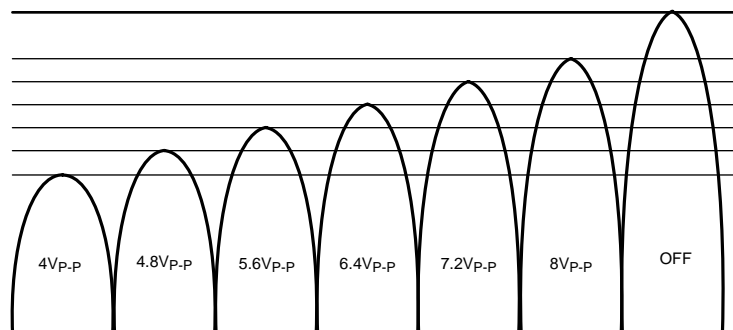


Figure 55. Voltage Limit Output Level

NO CLIP/OUTPUT CLIP CONTROL

The LM49251 No Clip circuitry detects when the loudspeaker output is near clipping and reduces the signal gain to prevent output clipping and preserve audio quality ([Figure 54](#)). Although the ALC reduces the gain of the speaker path to prevent output clipping, it is still possible to overdrive the speaker output. Please see the [ALC HEADROOM](#) section for further details.

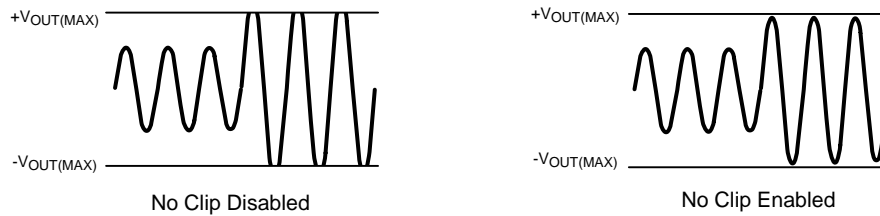


Figure 56. No Clip Function

The LM49251 also features an output clip control that allows a certain amount of clipping at the output in order to increase the loudspeaker output power. The clip level is set by B2:B0 in the No Clip Control Register (see Table 7). The clip control works by allowing the output to enter clipping before the ALC turns on and maintains the output level. The clip control has three levels: low, medium, and high. The low and max clip level control settings give the lowest distortion and highest distortion respectively on the output (see Figure 57). The actual output level of the device will depend upon the supply voltage, and the output power will depend upon the load impedance.

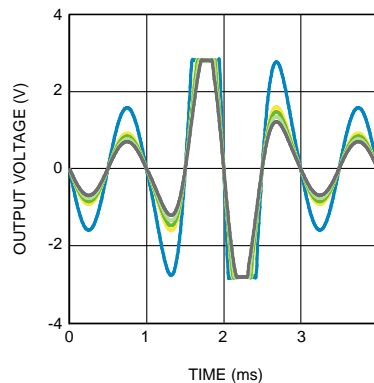


Figure 57. Clip Control Levels
 $V_{DD} = 3.3V$, $V_{IN} = 8V_{PP}$ Shaped Burst, 1kHz
 Blue = No Clip Disabled, Gray = Low, Light Green = Medium
 Green = High, Yellow = Max

ALC HEADROOM

When either voltage limiter or no clip is enabled, it is still possible to drive LM49251 into clipping by over driving the input volume stage of the signal path beyond its output dynamic range. In this case, clipping occurs at the input volume stage, and although ALC is active, the gain reduction will have no effect on the output clipping. The maximum input that can safely pass through the input volume stage can be calculated by following formula:

$$V_{IN} \leq \frac{V_{DD}}{A_v \text{ (volume gain)}} \quad (1)$$

So in the case of 0 dB volume gain, audio input has to be less than V_{DD} for both voltage limiter or No clip settings.

When voltage limiter is enabled, ALC can reach its max attenuation for lower voltage limit levels as shown in Figure 58. Typically, after the ALC started working, with 6 dB of audio input change ALC is well within its regulation. Voltage limiter Input headroom can be increased by switching to the LS_GAIN to 18dB in the Gain Control Register (see Table 8).

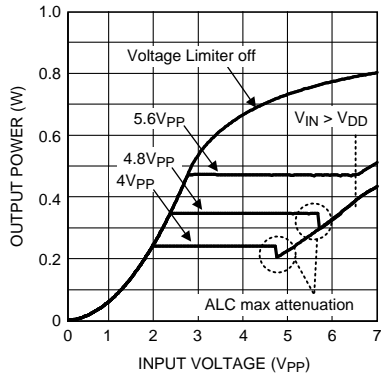


Figure 58. Voltage Limiter Function
 $V_{DD} = 3.3V$, $R_L = 15\mu H + 8\Omega + 15\mu H$
 $f_{IN} = 1kHz$, $LS_GAIN = 0$

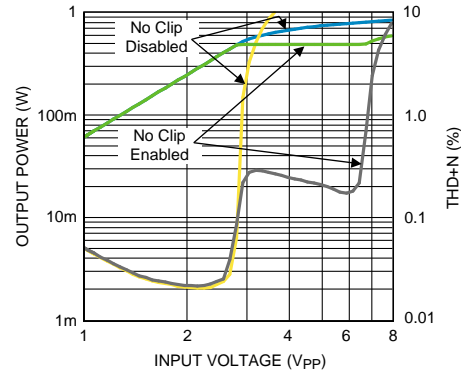


Figure 59. No Clip Function
 $V_{DD} = 3.3V$, $R_L = 15\mu H + 8\Omega + 15\mu H$
 $f_{IN} = 1kHz$, $LS_GAIN = 0$
 Blue, Green = Output Power vs Input Voltage
 Gray, Yellow = THD+N vs Input Voltage

When No Clip is enabled, class D speaker output reduces when it's about to enter clipping region and power stay constant as long as V_{IN} is less than V_{DD} for 0 dB volume gain (see Figure 58). For example, in the case of $V_{DD} = 3.3V$, there is a 6 dB of headroom for the change in input. Please see the ALC typical performance curves for additional plots relating to different supply voltages and LS_GAIN settings for specific application parameters.

ATTACK TIME

Attack time (t_{ATK}) is the time it takes for the gain to be reduced by 6dB ($LS_GAIN=0$) once the audio signal exceeds the ALC threshold. Fast attack times allow the ALC to react quickly and prevent transients such as symbol crashes from being distorted. However, fast attack times can lead to volume pumping, where the gain reduction and release becomes noticeable, as the ALC cycles quickly. Slower attack times cause the ALC to ignore the fast transients, and instead act upon longer, louder passages. Selecting an attack time that is too slow can lead to increased distortion in the case of the No Clip function, and possible output overload conditions in the case of the Voltage limiter. The attack time is set by a combination of the value of C_{SET} and the attack time coefficient as given by Equation 2:

$$t_{ATK} = 20k\Omega C_{SET} / \alpha_{ATK}(s) \quad (2)$$

Where α_{ATK} is the attack time coefficient (Table 14) set by bits B4:B3 in the Voltage Limit Control Register (see Table 6). The attack time coefficient allows the user to set a nominal attack time. The internal 20k Ω resistor is subject to temperature change, and it has tolerance between -11% to +20%.

Table 14. Attack Time Coefficient

| B4 | B3 | α_{ATK} |
|----|----|----------------|
| 0 | 0 | 2.667 |
| 0 | 1 | 2 |
| 1 | 0 | 1.333 |
| 1 | 1 | 1 |

RELEASE TIME

Release time (t_{RL}) is the time it takes for the gain to return from 6dB ($LS_GAIN=0$) to its normal level once the audio signal returns below the ALC threshold. A fast release time allows the ALC to react quickly to transients, preserving the original dynamics of the audio source. However, similar to a fast attack time, a fast release time contributes to volume pumping. A slow release time reduces the effect of volume pumping. The release time is set by a combination of the value of C_{SET} and release time coefficient as given by Equation 3:

$$t_{RL} = 20M\Omega C_{SET} / \alpha_{RL}(s) \quad (3)$$

where α_{RL} is the release time coefficient (Table 15) set by bits B4:B3 in the No Clip Control Register. The release time coefficient allows the user to set a nominal release time. The internal 20M Ω is subject to temperature change, and it has tolerance between -11% to +20%.

Table 15. Release Time Coefficient

| B4 | B3 | α_{RL} |
|----|----|---------------|
| 0 | 0 | 2 |
| 0 | 1 | 2.5 |
| 1 | 0 | 3 |
| 1 | 1 | 5 |

A-WEIGHTED FILTER

The human ear is sensitive for acoustic signals within a frequency range from about 20Hz to 20kHz. Within this range the sensitivity of the human ear is not equal for each frequency. To approach the hearing response, weighting filters are introduced. One of those filters is the A-weighted filter.

The A-weighted filter is used in signal to noise measurements, where the wanted audio signal is compared to device noise and distortion.

The use of this filter improves the correlation of the measured values to the way these ratios are perceived by the human ear.

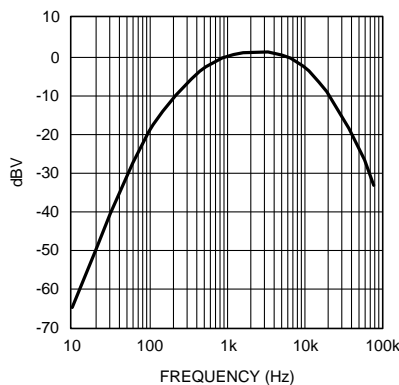


Figure 60. A-Weighted Filter

PROPER SELECTION OF EXTERNAL COMPONENTS

ALC Timing (C_{SET}) Capacitor Selection

The recommended range value of C_{SET} is between $.01\mu\text{F}$ to $1\mu\text{F}$. Lowering the value below $.01\mu\text{F}$ can increase the attack time but LM49251 ALC ability to regulate its output can be disrupted and approaches the hard limiter circuit. This in turn increases the THD+N and audio quality will be severely affected.

Charge Pump Capacitor Selection

Use low ESR ceramic capacitors (less than $100\text{m}\Omega$) for optimum performance.

Charge Pump Flying Capacitor (C_1)

The flying capacitor (C_1), see [Figure 2](#), affects the load regulation and output impedance of the charge pump. A C_1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C_1 improves load regulation and lowers charge pump output impedance to an extent. Above $2.2\mu\text{F}$, the $RDS_{(ON)}$ of the charge pump switches and the ESR of C_1 and CPV_{SS} dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Charge Pump Hold Capacitor (CPV_{SS})

The value and ESR of the hold capacitor (CPV_{SS}) directly affects the ripple on CPV_{SS} (see [Figure 2](#)). Increasing the value of CPV_{SS} reduces output ripple. Decreasing the ESR of CPV_{SS} reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Input Capacitor Selection

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM49251. The input capacitors create a high-pass filter with the input resistors R_{IN} . The -3dB point of the high-pass filter is found using [Equation 4](#) below.

$$f = 1 / 2\pi R_{IN} C_{IN} (\text{Hz}) \quad (4)$$

Where the value of R_{IN} is given in the [Electrical Characteristics Table](#).

High-pass filtering the audio signal helps protect the speakers. When the LM49251 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

Demo Board User Guide

Quick Start Guide:

1. Connect a shunt across pin 1 and pin 2 of JUI to provide 3.3V to $I^2C_{V_{DD}}$.
2. Connect a shunt across JU3 to provide 1.8V to V_{DDHP} from on board regulator.
3. Connect a 4Ω or 8Ω speaker across LSOUTL (left loudspeaker output) and LSOUTR (right loudspeaker output).
4. Connect stereo headphones to the headphone jack J1.
5. Connect a 3.6V power supply to the V_{DD} pin of J3 and the ground source to the GND pin.
6. Apply audio input signal to any of the stereo (IN1/IN2) or mono (MONO_IN) inputs.
7. Turn on power supply.
8. Connect the mini USB cable to J29 and the other end of the cable to a PC.
9. Open the LM49251 I²C control software.
10. Verify that the device has been acknowledged by looking at bottom left corner of GUI (see [Figure 61](#) and [Figure 62](#)).
11. On GUI:
 - a. Set POWER: on
 - b. Set MODE SELECT to desired position (see [Table 16](#)).
 - c. Set all VOLUME CONTROL to 0dB by clicking on Set 0dB button.

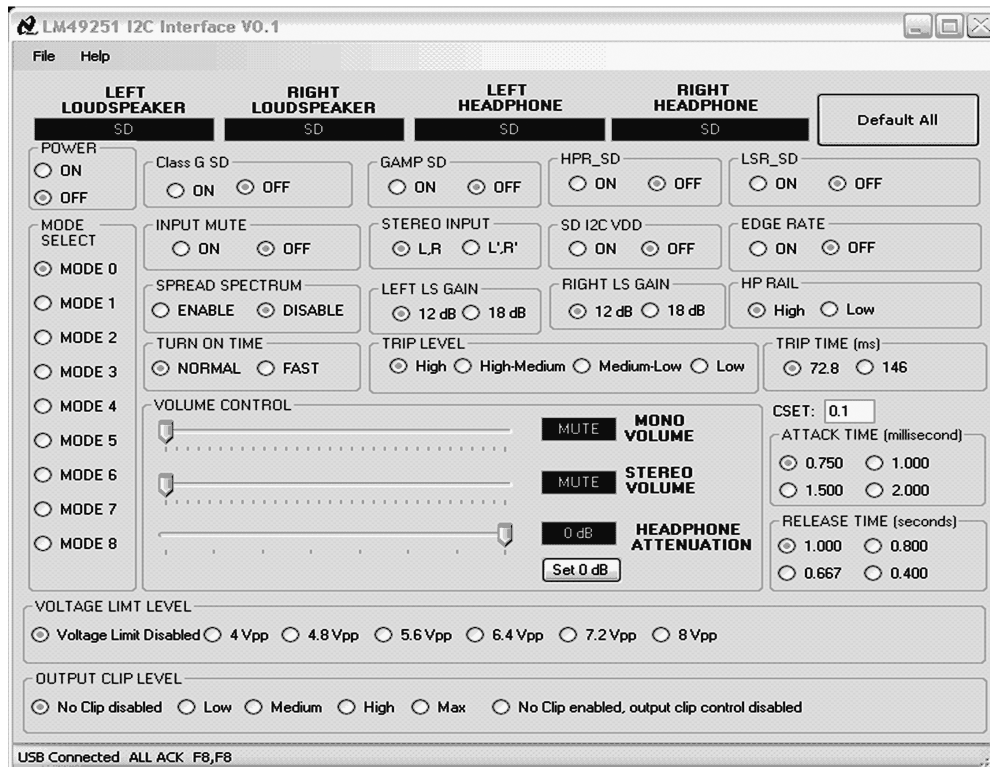


Figure 61. Software Graphic user Interface (GUI)

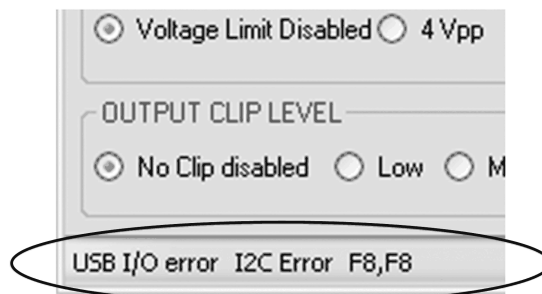


Figure 62. Error Message displayed on GUI if device is NOT acknowledged (I²C Error) or if there is an USB error (USB I/O error)

Table 16. Mode Table

| SPK(L) | SPK(R) | HP(L) | HP(R) | Datasheet |
|---------------------------|---------------------------|---------------------|---------------------|-----------|
| SD | SD | SD | SD | Mode 0 |
| G _{ST} X (L + R) | G _{ST} X (L + R) | SD | SD | Mode 1 |
| G _{ST} X L | G _{ST} X R | SD | SD | Mode 2 |
| G _M X M | G _M X M | SD | SD | Mode 3 |
| SD | SD | G _M X M | G _M X M | Mode 4 |
| G _M X M | G _M X M | G _M X M | G _M X M | Mode 5 |
| SD | SD | G _{ST} X L | G _{ST} X R | Mode 6 |
| G _{ST} X (L + R) | G _{ST} X (L + R) | G _{ST} X L | G _{ST} X R | Mode 7 |
| G _{ST} X L | G _{ST} X R | G _{ST} X L | G _{ST} X R | Mode 8 |

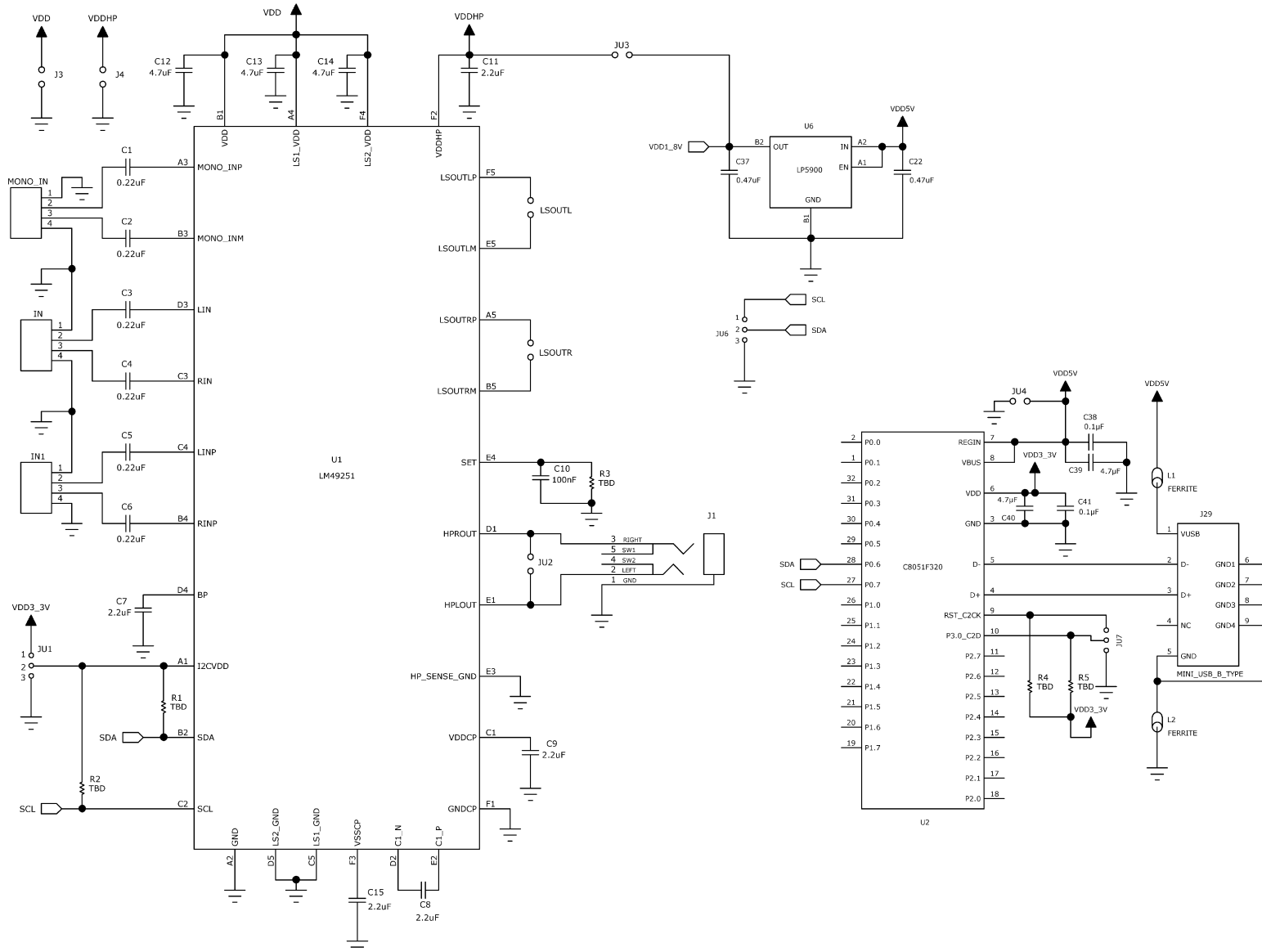
Table 17. Board Connectors

| Designator | Function | Comments |
|------------|--|--|
| J1 | (HPOUT) Headphone Output | Ring - Right Channel, Tip - Left Channel |
| J3 | (V _{DD} /GND) Loudspeaker Power Supply | |
| J4 | (V _{DD} HP/GND) Headphone Power Supply | Apply voltage on J4 when JU3 is open. DO NOT apply voltage if JU3 is closed |
| J29 | Mini USB | |
| JU1 | I ² CV _{DD} Select | Pin 1 = 3.3V, Pin 2 = I ² CV _{DD} , Pin 3 = GND Short Pin 1 and Pin 2 for I ² CV _{DD} = 3.3V |
| JU2 | (HPOUT) Headphone Output | Left and Right Channel |
| JU3 | V _{DD} HP = 1.8V | Short JU3 for V _{DD} HP = 1.8V from on board regulator |
| JU4 | 5V | Access to 5V from USB |
| JU6 | I ² C Clock/Data | GND, SDA, SCL connections |
| JU7 | | To program USB controller |
| LSOUTL | Left Loudspeaker Out | |
| LSOUTR | Right Loudspeaker Out | |
| MONO_IN | Mono Input | |
| IN1 | Stereo Input 1 | |
| IN2 | Stereo Input 2 | |

Bill of Materials**Table 18. Bill of Materials**

| Ref Designator | Part Description | Manufacturer | Part Number |
|---------------------------------|---|--------------|--------------------|
| | LM49251TL DEMO BOARD PCB, RevA | TI | |
| U1 | LM49251TL | TI | LM49251TL |
| U2 | USB, 25 MIPS, 16 kB Flash, 10-Bit ADC, 32-Pin Mixed-Signal MCU | Silicon Labs | C8051F320-GQ |
| U3 | Ultra Low Noise, 150mA Linear Regulator for RF/Analog Circuits Requires No Bypass Capacitor | TI | LP5900TL-1.8/NOPB |
| C12, C13, C14, C39, C40 | CAP CER 4.7UF 10V X5R 0603 10% | Taiyo Yuden | LMK107BJ475KA-T |
| C10, C38, C41 | CAP .1UF 25V CERAMIC X7R 0603 5% | Kemet | C0603C104J3RACTU |
| R3 | NO LOAD | NO LOAD | NO LOAD |
| C11, C9, C15, C8, C7 | CAP CER 2.2UF 10V X7R 0603 10% | Murata | GRM188R71A225KE15D |
| L1, L2 | FERRITE CHIP 30 OHM 2200MA 0402 | Murata | BLM15PD300SN1D |
| C22, C37 | CAP CERM .47UF 16V X7R 0603 10% | Kemet | C0603C474K4RACTU |
| C1, C2, C3, C4, C5, C6 | CAP CER .22UF 10V 10% X7R 0603 | Murata | GRM188R71A224KA01D |
| R1, R2 R4, R5 | RES 10.0K OHM 1/10W 1% 0603 SMD | Panasonic | ERJ-3EKF1002V |
| J29 | CONN RECEPT MINI USB2.0 5POS | Hirose | UX60-MB-5ST |
| JU1, JU6, JU7 | CONN HEADR BRKWAY .100 03POS STR | Tyco | 9-146285-0-03 |
| J3, J4, JU2, LSOUTL, LSOUTR, Jw | CONN HEADR BRKWAY .100 02POS STR | Tyco | 9-146285-0-02 |
| Mono_IN, In, In1 | CONN HDR BRKWAY .100 04POS VERT | Tyco | 9-146282-0-04 |
| J1 | CONN JACK STEREO 3.5MM HORIZONTAL | Switchcraft | 35RAPC4BH3 |
| JU3, JU7, JU1, | Jumper Shunt w/handle, 30µin gold plated, 0.100in pitch | Tyco/AMP | 881545-2 |

Demo Board Schematic Diagram



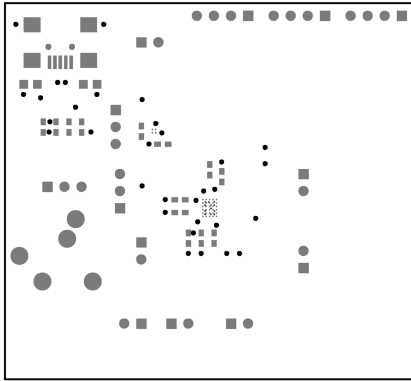


Figure 69. Paste Mask Top Layer

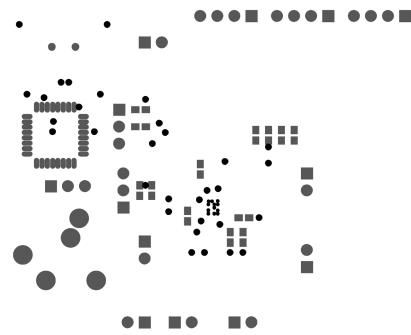


Figure 70. Past Mask Bottom Layer

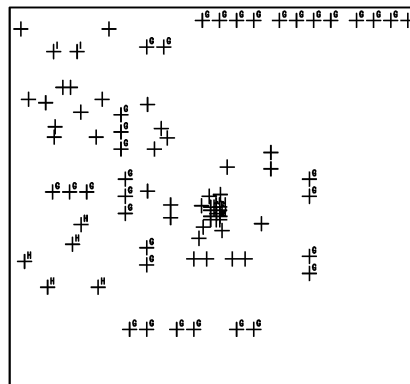


Figure 71. Drill Drawing

Revision History

| Rev | Date | Description |
|------------|-------------|--|
| 1.0 | 02/08/11 | Initial Web released. |
| A | 04/05/13 | Changed layout of National Data Sheet to TI format |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LM49251TL/NOPB | ACTIVE | DSBGA | YZR | 30 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | GN9 | Samples |
| LM49251TLX/NOPB | ACTIVE | DSBGA | YZR | 30 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | GN9 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

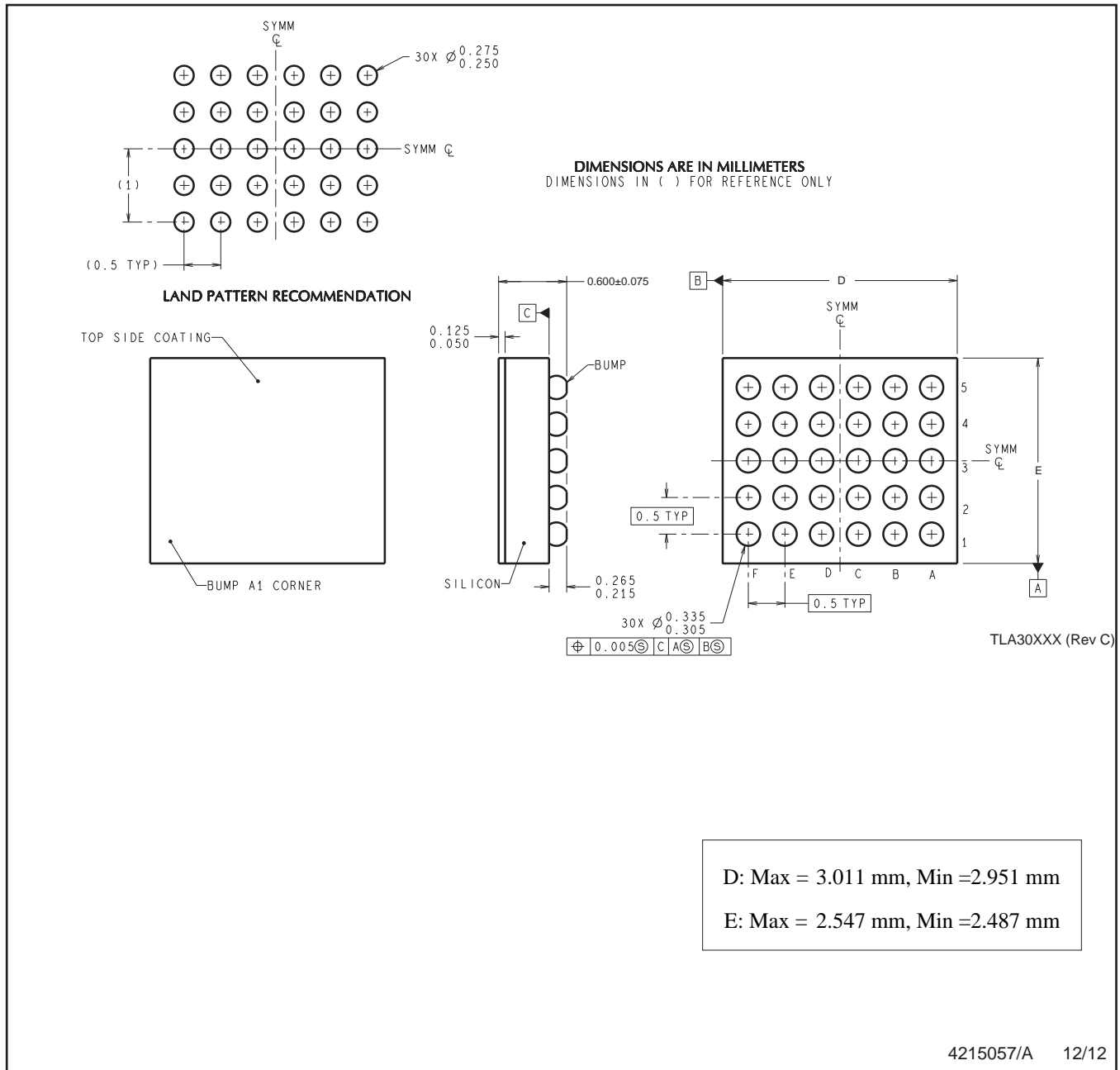
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM49251TL/NOPB | DSBGA | YZR | 30 | 250 | 178.0 | 8.4 | 2.74 | 3.15 | 0.76 | 4.0 | 8.0 | Q1 |
| LM49251TLX/NOPB | DSBGA | YZR | 30 | 3000 | 178.0 | 8.4 | 2.74 | 3.15 | 0.76 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM49251TL/NOPB | DSBGA | YZR | 30 | 250 | 210.0 | 185.0 | 35.0 |
| LM49251TLX/NOPB | DSBGA | YZR | 30 | 3000 | 210.0 | 185.0 | 35.0 |

YZR0030



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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