LMH7220 High Speed Comparator with LVDS Output

Check for Samples: LMH7220

FEATURES

- **(V_S = 5V T_A = 25°C, Typical Values unless Otherwise Specified)**
- **Propagation Delay @ 100 mV Overdrive 2.9 ns**
- **Rise and Fall Times 0.6 ns**
- **Supply Voltage 2.7V to 12V**
- **Supply Current 6.8 mA**
- **Temperature Range −40°C to 125°C**
- **LVDS Output**

APPLICATIONS

- **Acquisition Trigger**
- **Fast Differential Line Receiver**
- **Pulse Height Analyzer**
- **Peak Detector**
- **Pulse Width Modulator**
- **Remote Threshold Detection**
- **Oscilloscope Triggering**

DESCRIPTION

The LMH7220 is a high speed, low power comparator with an operating supply voltage range of 2.7V to 12V. The LMH7220 has a differential, LVDS output, driving 325 mV into a 100Ω symmetrical transmission line. The LMH7220 has a 2.9 ns propagation delay and 0.6 ns rise and fall times while the supply current is only 6.8 mA at 5V (load current excluded).

The LMH7220 inputs have a voltage range that extends 200 mV below ground, allowing ground sensing applications. The LMH7220 is available in the 6-Pin SOT package. This package is ideal where space is a critical item.

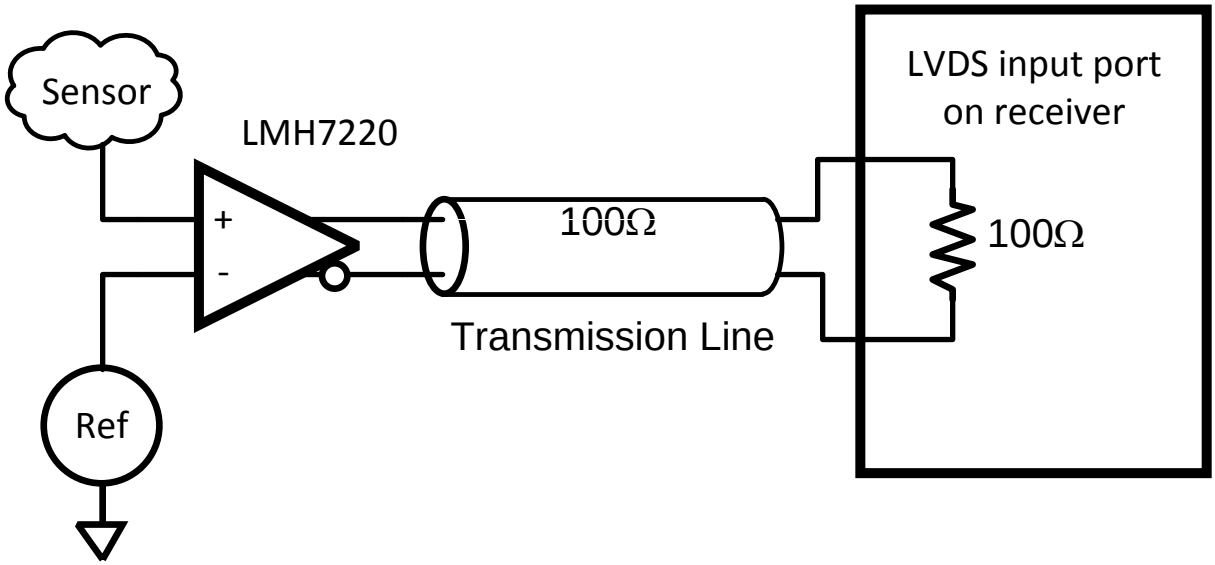

Figure 1. Typical Schematic

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

ESD Tolerance (3)	Human Body Model	2.5 kV
	Machine Model	250V
Supply Voltage (V_{CC} - GND)		13.5V
Differential Input Voltage		±13V
Output Shorted to GND (4)		Continuous
Output Shorted Together (4)		Continuous
Storage Temperature Range		−65°C to +150°C
Voltage on any I/O Pin		GND−0.2V to V_{CC}+0.2V
Junction Temperature (5)		150°C max

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Conditions indicate specifications for which the device is intended to be functional, but specific performance is not ensured. For specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC)
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

OPERATING RATINGS (1)

Temperature Range (2)		−40°C to +125°C
Supply Voltage		2.7V to 13V
Package Thermal Resistance (θ_{JA})	6-Pin SOT	189°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Conditions indicate specifications for which the device is intended to be functional, but specific performance is not ensured. For specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

+12V DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits are specified for T_J = 25°C, V_{CM} = 300 mV, −50 mV < V_{ID} < +50 mV and R_L = 100Ω. **Boldface** limits apply at the temperature extremes. (1)(2)

Symbol	Parameter	Conditions	Min(1)	Typ(3)	Max(1)	Units
I_B	Input Bias Current	V_{IN} Differential = 0	−5 **−7**	−2.1	−0.5	µA
I_{OS}	Input Offset Current	V_{IN} Differential = 0	−500		+500	nA
TC I_{OS}	Input Offset Current TC	V_{IN} Differential = 0		±2		nA/°C
V_{OS}	Input Offset Voltage		−9.5		+9.5	mV
TC V_{OS}	Input Offset Voltage TC			± 50		µV/°C
VRI	Input Voltage Range	CMRR > 50 dB	−0.2		V_{CC}−2	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0 to V_{CC}−2.2V	60	70		dB
PSRR	Power Supply Rejection Ratio		63	74		dB
A_V	Open Loop Gain			59		dB
V_O	Output Offset Voltage	V_{IN} Differential = 50 mV	1125	1225	1325	mV
ΔV_O	V_O Change Between '0' and '1'	V_{IN} Differential = ±50 mV	−25		+25	mV
V_{OH}	Output Voltage High	V_{IN} Differential = 50 mV		1390	1475	mV
V_{OL}	Output Voltage Low	V_{IN} Differential = 50 mV	925	1060		mV
V_{OD}	Output Voltage Differential	V_{IN} Differential = 50 mV	250	330	400	mV
ΔV_{OD}	V_{OD} Change between '0' to '1'	V_{IN} Differential = ±50 mV	−25		+25	mV
I_{SC}	Short Circuit Current Output to GND Pin (4)	OUT Q to GND Pin V_{IN} Differential = 50 mV			5	mA
		OUT $\overline{Q}$ to GND Pin V_{IN} Differential = 50 mV			5	
	Output Shorted Together (4)	OUT Q to OUT $\overline{Q}$ V_{IN} Differential = 50 mV			5	
I_S	Supply Current	Load Current Excluded V_{IN} Differential = 50 mV		7.5	10.0 **14.0**	mA

(1) All limits are specified by testing or statistical analysis.
(2) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See APPLICATION INFORMATION for information on temperature de-rating of this device.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

+12V AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits specified for T_J = 25°C, V_{CM} = 300 mV, −50 mV < V_{ID} < +50 mV and R_L = 100Ω. **Boldface** limits apply at the temperature extremes. (1)(2)

Symbol	Parameter	Conditions	Min(1)	Typ(3)	Max(1)	Units
TR	Toggle Rate	Overdrive = ±50 mV; C_L = 2 pF @ 50% Output Swing	860	1080		Mb/s
t_{jitter_RMS}	RMS-Random Jitter	Overdrive = 100 mV; C_L = 2 pF Center Frequency = 70 MHz Bandwidth = 10 Hz – 20 MHz		4.29		ps
t_{PDLH}	Propagation Delay $t_{PDLH} = (t_{PDH} + t_{PD\overline{L}}) / 2$ (see Figure 21 application information) Input SR = Constant V_{ID} start value = −100 mV	Overdrive 20 mV		3.56		ns
		Overdrive 50 mV		2.98		
		Overdrive 100 mV		2.7	7	
		Overdrive 1V		2.24		
t_{OD}-disp	Input Overdrive Dispersion	@Overdrive 20 - 100 mV		0.86		ns
		@Overdrive 100 mV - 1V		0.46		
t_{SR}-disp	Input Slew Rate Dispersion	0.05 V/ns to 1 V/ns Overdrive 100 mV		0.24		ns
t_{CM}-disp	Input Common Mode dispersion	SR = 4 V/ns; Overdrive 100 mV V_{CM} = 0 to 10V		0.55		ns
Δt_{PDLH}	Q to $\overline{Q}$ Time Skew $\lvert t_{PDH} - t_{PD\overline{L}} \rvert$ (4)	Overdrive = 100 mV; C_L = 2 pF		0		ns
Δt_{PDHL}	Q to $\overline{Q}$ Time Skew $\lvert t_{PDL} - t_{PD\overline{H}} \rvert$ (4)	Overdrive = 100 mV; C_L = 2 pF		0.06		ns
t_r	Output Rise Time (20% - 80%) (5)	Overdrive = 100 mV; C_L = 2 pF		0.56		ns
t_f	Output Fall Time (20% - 80%) (5)	Overdrive = 100 mV; C_L = 2 pF		0.49		ns

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(2) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See APPLICATION INFORMATION for information on temperature de-rating of this device.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Propagation Delay Skew, Δt_{PD}, is defined as the average of Δt_{PDLH} and Δt_{PDHL}.
(5) The rise or fall time is the average of the Q and $\overline{Q}$ rise or fall time.

+5V DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits specified for T_J = 25°C, V_{CM} = 300 mV, −50 mV < V_{ID} < +50 mV and R_L = 100Ω. **Boldface** limits apply at the temperature extremes. (1)(2)

Symbol	Parameter	Conditions	Min(1)	Typ(3)	Max(1)	Units
I_B	Input Bias Current	V_{IN} Differential = 0	−5 **−7**	−1.5	−0.5	µA
I_{OS}	Input Offset Current	V_{IN} Differential = 0	−500		+500	nA
TC I_{OS}	Input Offset Current TC	V_{IN} Differential = 0		± 2		nA/°C
V_{OS}	Input Offset Voltage		−9.5		+9.5	mV
TC V_{OS}	Input Offset Voltage TC			± 50		µV/°C
VRI	Input Voltage Range	CMRR > 50 dB	−0.2		V_{CC}−2	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0 to V_{CC}−2.2V	60	70		dB
PSRR	Power Supply Rejection Ratio		63	74		dB
A_V	Open Loop Gain			59		dB
V_O	Output Offset Voltage	V_{IN} Differential = 50 mV	1125	1217	1325	mV
ΔV_O	V_O Change Between '0' and '1'	V_{IN} Differential = ±50 mV	−25		+25	mV
V_{OH}	Output Voltage High	V_{IN} Differential = 50 mV		1380	1475	mV
V_{OL}	Output Voltage Low	V_{IN} Differential = 50 mV	925	1060		mV
V_{OD}	Output Voltage Differential	V_{IN} Differential = 50 mV	250	320	400	mV
ΔV_{OD}	V_{OD} Change between '0' to '1'	V_{IN} Differential = ±50 mV	−25		+25	mV
I_{SC}	Short Circuit Current Output to GND Pin (4)	OUT Q to GND Pin V_{IN} Differential = 50 mV			5	mA
		OUT $\overline{Q}$ to GND Pin V_{IN} Differential = 50 mV			5	
	Output Shorted Together (4)	OUT Q to OUT $\overline{Q}$ V_{IN} Differential = 50 mV			5	
I_S	Supply Current	Load Current Excluded V_{IN} Differential = 50 mV		6.8	9 **12.6**	mA

(1) All limits are specified by testing or statistical analysis.
(2) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See APPLICATION INFORMATION for information on temperature de-rating of this device.
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(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

+5V AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits specified for T_J = 25°C, V_{CM} = 300 mV, −50 mV < V_{ID} < +50 mV and R_L = 100Ω. **Boldface** limits apply at the temperature extremes. (1)(2)

Symbol	Parameter	Conditions	Min(1)	Typ(3)	Max(1)	Units
TR	Toggle Rate	Overdrive = ±50 mV; C_L = 2 pF @ 50% Output Swing	750	940		Mb/s
t_{jitter_RMS}	RMS-Random Jitter	Overdrive = 100 mV; C_L = 2 pF Center Frequency = 70 MHz Bandwidth = 10 Hz – 20 MHz		4.44		ps
t_{PDLH}	Propagation Delay $t_{PDLH} = (t_{PDH} + t_{PD\overline{L}}) / 2$ (see Figure 21 application information) Input SR = Constant V_{ID} start value = -100mV	Overdrive 20 mV		3.63		ns
		Overdrive 50 mV		3.09		
		Overdrive 100 mV		2.9	7	
		Overdrive 1V		2.41		
t_{OD}-disp	Input Overdrive Dispersion	@Overdrive 20 - 100 mV		0.79		ns
		@Overdrive 100 mV - 1V		0.43		
t_{SR}-disp	Input Slew Rate Dispersion	0.05 V/ns to 1 V/ns Overdrive 100 mV		0.20		ns
t_{CM}-disp	Input Common Mode Dispersion	SR = 4 V/ns; Overdrive 100 mV V_{CM} = 0 to 3V		0.21		ns
Δt_{PDLH}	Q to $\overline{Q}$ Time Skew $\lvert t_{PDH} - t_{PD\overline{L}} \rvert$ (4)	Overdrive = 100 mV; C_L = 2 pF		0.09		ns
Δt_{PDHL}	Q to $\overline{Q}$ Time Skew $\lvert t_{PDL} - t_{PD\overline{H}} \rvert$ (4)	Overdrive = 100 mV; C_L = 2 pF		0.07		ns
t_r	Output Rise Time (20% - 80%) (5)	Overdrive = 100 mV; C_L = 2 pF		0.59		ns
t_f	Output Fall Time (20% - 80%) (5)	Overdrive = 100 mV; C_L = 2 pF		0.55		ns

(1) All limits are specified by testing or statistical analysis.
(2) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See APPLICATION INFORMATION for information on temperature de-rating of this device.
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(4) Propagation Delay Skew, Δt_{PD}, is defined as the average of Δt_{PDLH} and Δt_{PDHL}.
(5) The rise or fall time is the average of the Q and $\overline{Q}$ rise or fall time.

+2.7V DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits specified for T_J = 25°C, V_{CM} = 300 mV, −50 mV < V_{ID} < +50 mV and R_L = 100Ω. **Boldface** limits apply at the temperature extremes. (1)

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
I_B	Input Bias Current	V_{IN} Differential = 0	−5 **−7**	−1.3	−0.5	µA
I_{OS}	Input Offset Current	V_{IN} Differential = 0	−500		+500	nA
TC I_{OS}	Input Offset Current TC	V_{IN} Differential = 0		±2		nA/°C
V_{OS}	Input Offset Voltage		−9.5		+9.5	mV
TC V_{OS}	Input Offset Voltage TC			± 50		µV/°C
VRI	Input Voltage Range	CMRR > 50 dB	−0.2		V_{CC}−2	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0 to V_{CC}−2.2V	56	70		dB
PSRR	Power Supply Rejection Ratio		63	74		dB
A_V	Open Loop Gain			59		dB
V_O	Output Offset Voltage	V_{IN} Differential = 50 mV	1125	1213	1325	mV
ΔV_O	V_O Change Between ‘0’ and ‘1’	V_{IN} Differential = ± 50 mV	−25		+25	mV
V_{OH}	Output Voltage High Average of ‘0’ to ‘1’	V_{IN} Differential = 50 mV		1370	1475	mV
V_{OL}	Output Voltage Low Average of ‘0’ to ‘1’	V_{IN} Differential = 50 mV	925	1060		mV
V_{OD}	Output Voltage Differential	V_{IN} Differential = 50 mV	250	315	400	mV
ΔV_{OD}	V_{OD} Change between ‘0’ to ‘1’	V_{IN} Differential = ±50 mV	−25		+25	mV
I_{SC}	Short Circuit Current Output to GND Pin (3)	OUT Q to GND Pin V_{IN} Differential = 50 mV			5	mA
		OUT $\overline{Q}$ to GND Pin V_{IN} Differential = 50 mV			5	
	Output Shorted Together (3)	OUT Q to OUT $\overline{Q}$ V_{IN} Differential = 50 mV			5	
I_S	Supply Current	Load Current Excluded V_{IN} Differential = 50 mV		6.6	9 **12.6**	mA

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

+2.7V AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits specified for T_J = 25°C, V_{CM} = 300 mV, −50 mV < V_{ID} < +50 mV and R_L = 100Ω. **Boldface** limits apply at the temperature extremes. (1)(2)

Symbol	Parameter	Conditions	Min(1)	Typ(3)	Max(1)	Units
TR	Toggle Rate	Overdrive = ±50 mV; C_L = 2 pF @ 50% Output Swing	700	880		Mb/s
t_{jitter_RMS}	RMS-Random Jitter	Overdrive = 100 mV; C_L = 2 pF Center Frequency = 70 MHz Bandwidth = 10 Hz – 20 MHz		4.82		ps
t_{PDLH}	Propagation Delay $t_{PDLH} = (t_{PDH} + t_{PD\overline{L}}) / 2$ (see Figure 21 application information) Input SR = Constant V_{ID} start value = -100mV	Overdrive 20 mV		3.80		ns
		Overdrive 50 mV		3.29		
		Overdrive 100 mV		3.0	7	
		Overdrive 1V		2.60		
t_{OD}-disp	Input Overdrive Dispersion	@Overdrive 20 - 100 mV		0.83		ns
		@Overdrive 100 mV - 1V		0.37		
t_{SR}-disp	Input Slew Rate Dispersion	0.05 V/ns to 1 V/ns Overdrive 100 mV		0.23		ns
t_{CM}-disp	Input Common Mode dispersion	SR = 4 V/ns; Overdrive 100 mV V_{CM} = 0 to 1.5V		0.16		ns
Δt_{PDLH}	Q to $\overline{Q}$ Time Skew $\lvert t_{PDH} - t_{PD\overline{L}} \rvert$ (4)	Overdrive = 100 mV; C_L = 2 pF		0.09		ns
ΔtPDHL	Q to $\overline{Q}$ Time Skew $\lvert t_{PDL} - t_{PD\overline{H}} \rvert$ (4)	Overdrive = 100 mV; C_L = 2 pF		0.09		ns
t_r	Output Rise Time (20% - 80%) (5)	Overdrive = 100 mV; C_L = 2 pF		0.64		ns
t_f	Output Fall Time (20% - 80%) (5)	Overdrive = 100 mV; C_L = 2 pF		0.59		ns

(1) All limits are specified by testing or statistical analysis.
(2) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See APPLICATION INFORMATION for information on temperature de-rating of this device.
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(4) Propagation Delay Skew, Δt_{PD}, is defined as the average of Δt_{PDLH} and Δt_{PDHL}.
(5) The rise or fall time is the average of the Q and $\overline{Q}$ rise or fall time.

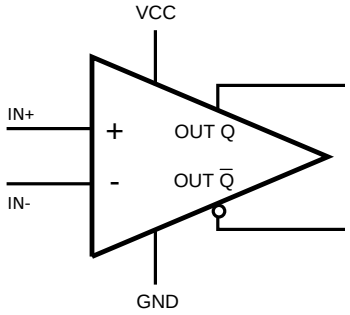


Figure 2. Schematic Diagram

Connection Diagram

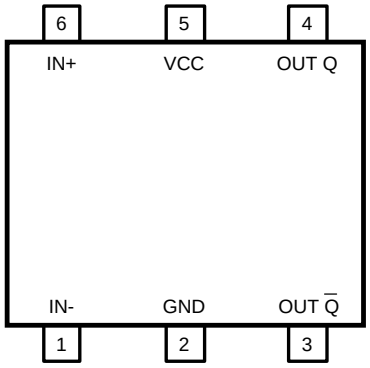


Figure 3. 6-Pin SOT Top View

TYPICAL PERFORMANCE CHARACTERISTICS

At T_J = 25°C; unless otherwise specified: V_{CM} = 0.3V, $V_{OVERDRIVE}$ = 100 mV, R_L = 100Ω.

Input Current vs. Differential Input Voltage

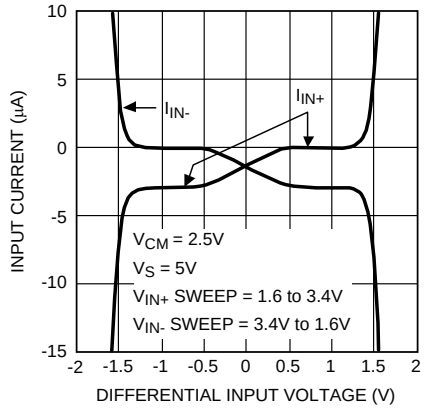


Figure 4.

Bias Current vs. Supply Voltage

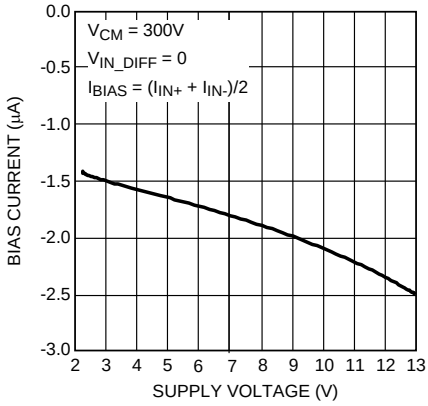


Figure 5.

Bias Current vs. Temperature

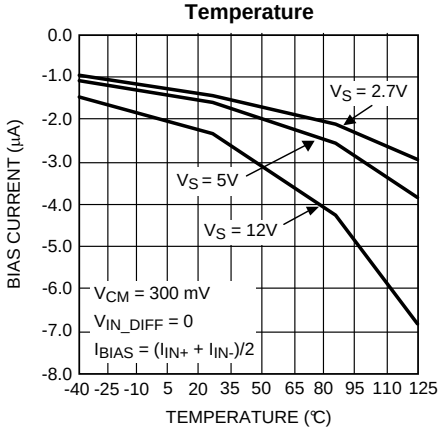


Figure 6.

Output Offset Voltage vs. Supply Voltage

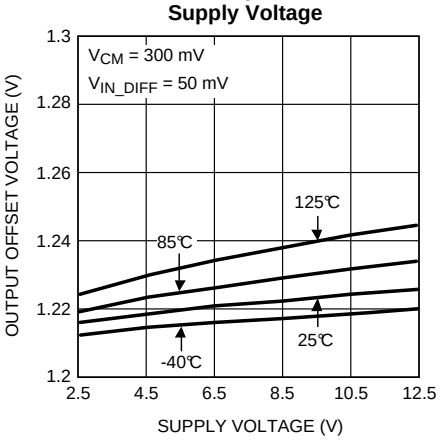


Figure 7.

Output Offset Voltage vs. Temperature

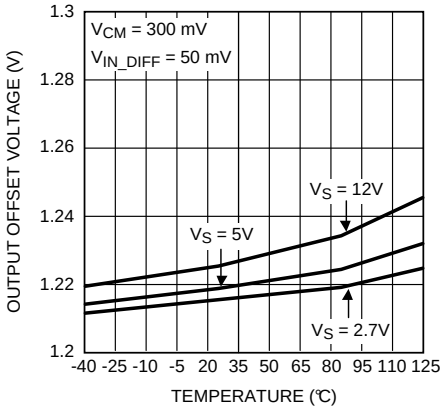


Figure 8.

Differential Output Voltage vs. Supply Voltage

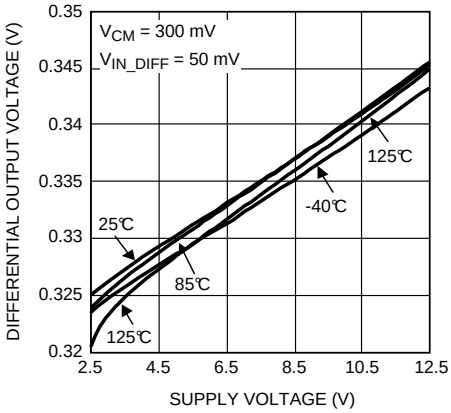


Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C; unless otherwise specified: V_{CM} = 0.3V, $V_{OVERDRIVE}$ = 100 mV, R_L = 100Ω.

Differential Output Voltage vs. Temperature

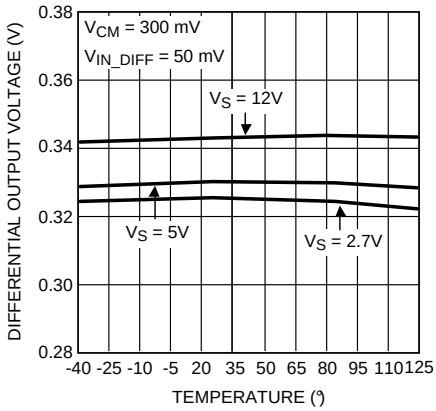


Figure 10.

Supply Current vs. Supply Voltage

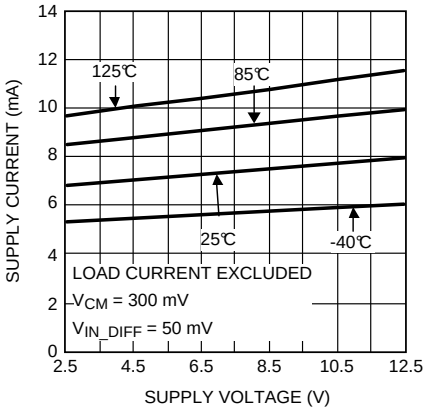


Figure 11.

Supply Current vs. Temperature

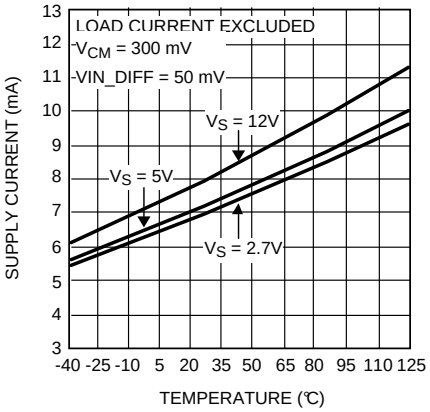


Figure 12.

Rise & Fall Time vs. Temperature

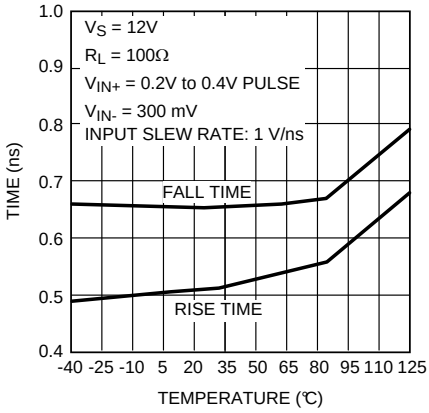


Figure 13.

Propagation Delay vs. Temperature

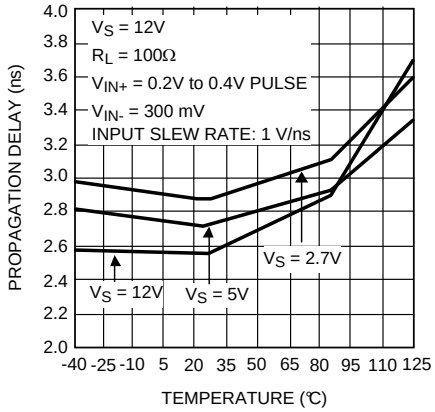


Figure 14.

Propagation Delay vs. Overdrive Voltage

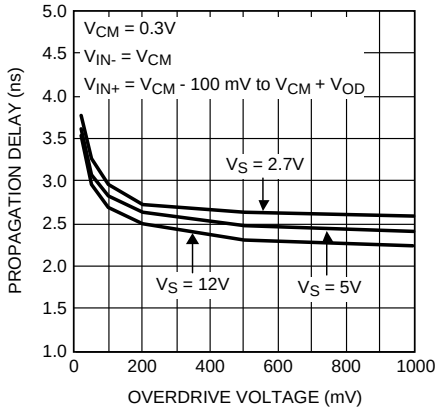


Figure 15.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C; unless otherwise specified: V_{CM} = 0.3V, $V_{OVERDRIVE}$ = 100 mV, R_L = 100Ω.

Propagation Delay vs. Common Mode Voltage

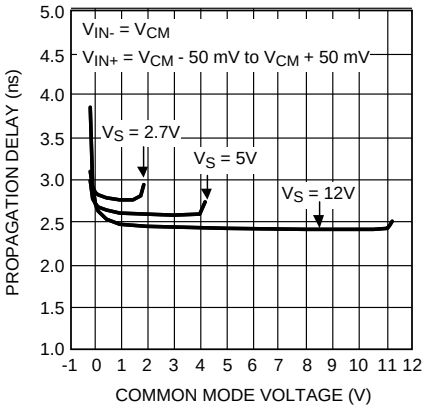


Figure 16.

Propagation Delay vs. Slew Rate

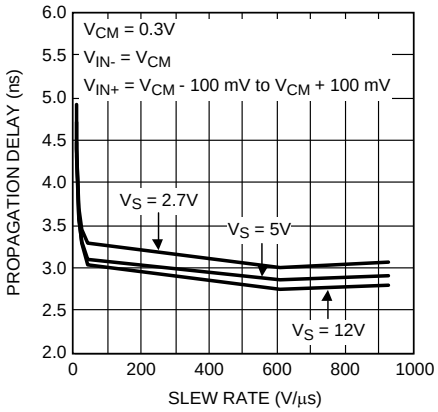


Figure 17.

Pulse Response Over Temperature

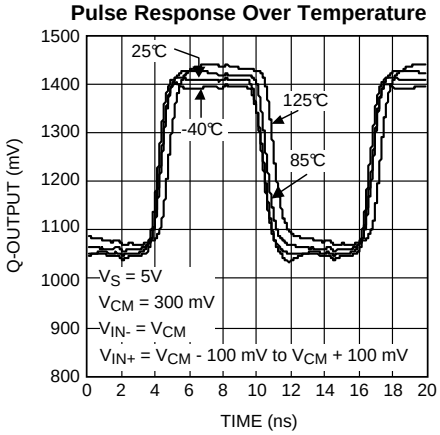


Figure 18.

APPLICATION INFORMATION

INTRODUCTION

The LMH7220 is a high speed comparator with LVDS outputs. The LVDS (Low Voltage Differential Signaling) standard uses differential outputs with a voltage swing of approximately 325 mV on each output. The most widely used setup for LVDS outputs consists of a switched current source of 3.25 mA. The output pins need to be differentially terminated with an external 100Ω resistor, producing the standardized output voltage swing of 325 mV. The common mode level of both outputs is about 1.2V, and is independent of the power supply voltage. The use of complementary outputs gives a high level of suppression for common mode noise. The very fast rise and fall times of the LMH7220 enable data transmission rates up to several hundreds of Megabits per second (Mbps). Due to the current-nature of the outputs the power consumption remains at a very low level even if the data transmission rate is rising. Power delivered to a load resistance of 100Ω is only 1.2 mW.

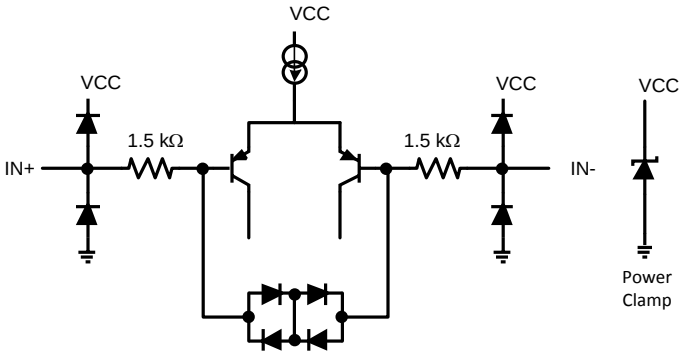
The LMH7220 inputs have a common mode voltage range that extends 200 mV below the negative supply voltage thus allowing ground sensing in case of single supply. The rise and fall times of the LMH7220 are about 0.6 ns, while the propagation delay time is about 2.7 ns. The LMH7220 can operate over the full supply voltage range of 2.7V to 12V, while using single or dual supply voltages. The LVDS outputs refer to the negative supply rail. The supply current is 6.8 mA at 5V (load current excluded). The LMH7220 is available in the 6-Pin SOT package.

In the next sections the following issues are discussed:

- In- and output topology
- Definition of terms of used specifications
- Propagation delay and dispersion
- Hysteresis and oscillations
- The output
- Applying transmission lines
- PCB layout

INPUT & OUTPUT TOPOLOGY

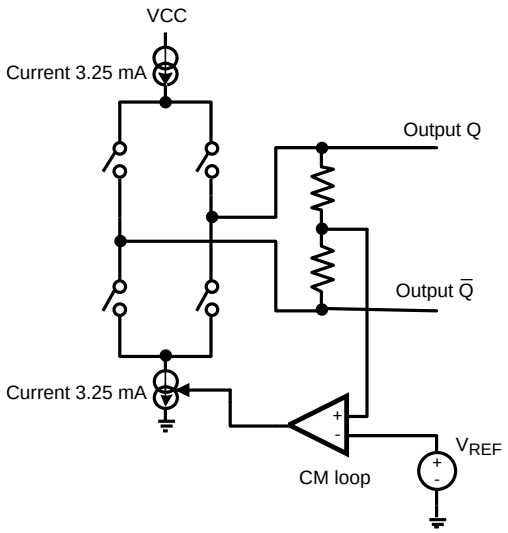
All input and output pins are protected against excessive voltages by ESD diodes. These diodes are connected from the negative supply to the positive supply. As can be seen in Figure 19, both inputs are connected to these diodes. Protection against excessive supply voltages is provided by a power clamp between V_{CC} and GND. Both inputs are also connected to the bases of the input transistors of the differential pair via 1.5 kΩ resistors. The input transistors cannot withstand high reverse voltages between bases and emitter, due to their high frequency properties. To protect the input stage against damage, both bases are connected together by a string of anti-parallel diodes. Be aware of situations in which differential input voltage level is such that these diodes are conducting. In this case the input current is raised far above the normal value stated in the datasheet tables.



Equivalent Input Circuitry

Figure 19. Equivalent Input Circuitry

The output can be seen as a bridge configuration in which switches are crosswise closed, producing the differential LVDS logic high and low levels (see Figure 20). The output switches are fed at top and bottom by two current sources. The top one is fixed and determines the differential voltage across the external load resistor. The other one is regulated and determines the common-mode voltage on the outputs. It is essential to keep the output common-mode voltage at the defined standardized LVDS level under all circumstances. To realize this, both outputs are internally connected together via two equal resistors. At the midpoint this produces the common mode output voltage, which is made equal to V_{REF} (1.2V) by means of the CM feedback loop.



Equivalent Output Circuitry

Figure 20. Equivalent Output Circuitry

DEFINITIONS

For a good understanding of many parameters of the LMH7220 it is necessary to perform a lot of measurements. All of those parameters are listed in the data tables in the first part of the datasheet. There are different tables for several supply voltages containing a separate set of data per supply voltage. In the table below is a list of abbreviations of the measured parameters and a short description of the conditions which are applied for measuring them . Following this table several parameters are highlighted to explain more clearly what it means exactly and what effects such a phenomena can have for any applied electronic circuit.

Symbol	Text	Description
I_B	Input Bias Current	Current flowing in or out the input pins, when both biased at 0.3 Volt above GND
I_{OS}	Input Offset Current	Difference between the positive- and the negative input currents needed to make the outputs change state, averaged for H to L and L to H transitions
TC I_{OS}	Average Input Offset Current Drift	Temperature Coefficient of I_{OS}
V_{OS}	Input Offset Voltage	Voltage difference needed between IN^+ and IN^- to make the outputs change state, averaged for H to L and L to H transitions
TC V_{OS}	Average Input Offset Voltage Drift	Temperature Coefficient of V_{OS}
CMRR	Common Mode Rejection Ratio	Ratio of input offset voltage change and input common mode voltage change
VRI	Input Voltage Range	Upper and lower limits of the input voltage are defined as where CMRR drops below 50 dB.
PSRR	Power Supply Rejection Ratio	Ratio of input offset voltage change and supply voltage change from $V_{S\text{-}MIN}$ to $V_{S\text{-}MAX}$
V_O	Output Offset Voltage	Output Common Mode Voltage averaged for logic '0' and logic '1' levels (See Figure 30)

Symbol	Text	Description
ΔV_O	Change in Output Offset Voltage	Difference in Output Common Mode Voltage between logic '0' and logic '1' levels (See Figure 31)
V_{OH}	Output Voltage High	High state single ended output voltage ($\overline{Q}$ or Q) (See Figure 30)
V_{OL}	Output Voltage Low	Low state single ended output voltage ($\overline{Q}$ or Q) (See Figure 30)
V_{ODH}	Output Differential Voltage logic '1'	$V_{OH(Q)} - V_{OL(\overline{Q})}$ (logic level '1') (See Figure 31)
V_{ODL}	Output Differential Voltage logic '0'	$V_{OH(\overline{Q})} - V_{OL(Q)}$ (logic level '0') (See Figure 31)
V_{OD}	Average of V_{ODH} and V_{ODL}	$(V_{ODH} + V_{ODL}) / 2$
ΔV_{OD}	Change in V_{OD} between '0' and '1'	$\lvert V_{ODH} - V_{ODL} \rvert$ (See Figure 31)
Hyst	Hysteresis	Difference in input switching levels for L to H and H to L transitions. (See Figure 29)
I_{SQG}, $I_{S\overline{Q}G}$	Short Circuit Current one output to GND	Current that flows from one output to GND if shorted single ended
$I_{SQ\overline{Q}}$	Short Circuit Current outputs together	Current flowing between output Q and output $\overline{Q}$ if shorted differentially
TR	Maximum Toggle Rate	Maximum frequency at which the outputs can toggle before V_{OD} drops under 50% of the nominal value.
PW	Pulse Width	Time from 50% of the rising edge of a signal to 50% of the falling edge
t_{PDH} resp t_{PDL}	Propagation Delay	Delay time between the moment the input signal crosses the switching level L to H and the moment the output signal crosses 50% of the rising edge of Q output (t_{PDH}), or delay time between the moment the input signal crosses the switching level H to L and the moment the output signal crosses 50% of the falling edge of Q output (t_{PDL})
$t_{PD\overline{L}}$resp $t_{PD\overline{H}}$		Delay time between the moment the input signal crosses the switching level L to H and the moment the output signal crosses 50% of the falling edge of $\overline{Q}$ output ($t_{PD\overline{L}}$), or delay time between the moment the input signal crosses the switching level H to L and the moment the output signal crosses 50% of the rising edge of $\overline{Q}$ output ($t_{PD\overline{H}}$)
t_{PDLH}		Average of t_{PDH} and $t_{PD\overline{L}}$
t_{PDHL}		Average of t_{PDL} and $t_{PD\overline{H}}$
t_{PD}		Average of t_{PDLH} and t_{PDHL}
t_{PDHd} resp t_{PDLd}		Delay time between the moment the input signal crosses the switching level L to H and the zero crossing of the rising edge of the differential output signal (t_{PDHd}), or delay time between the moment the input signal crosses the switching level H to L and the zero crossing of the falling edge of the differential output signal (t_{PDLd})
Δt_{PDLH} resp Δt_{PDHL}	Q to $\overline{Q}$ time skew	Time skew between 50% levels of rising edge of Q output and falling edge of $\overline{Q}$ output (Δt_{PDLH}), or time skew between 50% levels of falling edge of Q output and rising edge of $\overline{Q}$ output (Δt_{PDHL})
Δt_{PD}	Average Q to $\overline{Q}$ time skew	Average of t_{PDLH} and t_{PDHL} for L to H and H to L transients
Δt_{PDd}	Average diff. time skew	Average of t_{PDHd} and t_{PDLd} for L to H and H to L transients
$t_{OD\text{-}disp}$	Input overdrive dispersion	Change in t_{PD} for different overdrive voltages at the input pins
$t_{SR\text{-}disp}$	Input slew rate dispersion	Change in t_{PD} for different slew rates at the input pins
$t_{CM\text{-}disp}$	Input Common Mode dispersion	Change in t_{PD} for different common mode voltages at the input pins
t_r / t_{rd}	Output rise time (20% - 80%)	Time needed for the (single ended or differential) output voltage to change from 20% of its nominal value to 80%
t_f / t_{fd}	Output fall time (20% - 80%)	Time needed for the (single ended or differential) output voltage to change from 80% of its nominal value to 20%

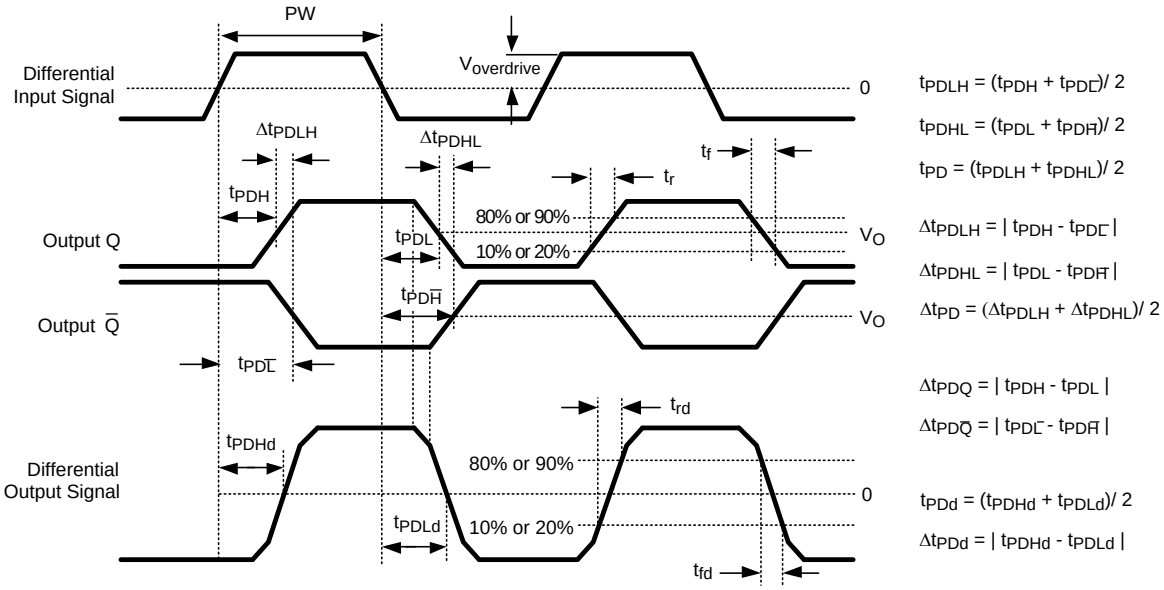


Figure 21. Propagation Delay Definition

DELAY AND DISPERSION

Comparators are widely used to connect the analog world to the digital one. The accuracy of a comparator is dictated by its DC properties such as offset voltage and hysteresis and by its timing aspects such as rise and fall times and delay. For low frequency applications most comparators are much faster than the analog input signals they handle. The timing aspects are less important here than the accuracy of the input switching levels. The higher the frequency, the more important the timing properties of the comparator become, because the response of the comparator can give e.g. a noticeable change in time frame or duty cycle. A designer has to know these effects in order to deal with them. In order to predict what the output signal will do compared to the input signal, several parameters are defined which describe the behavior of the comparator. For a good understanding of the timing parameters discussed in the following section, a brief explanation is given and several timing diagrams are shown for clarification.

PROPAGATION DELAY

The propagation delay parameter is defined as the time it takes for the comparator to change the output level halfway in its transition from L to H or H to L, in reaction to the moment the input signal crosses the switching level. Due to this definition there are two parameters, t_{PDH} and t_{PDL} (Figure 22). Both parameters don't necessarily have the same value. It is possible that differences will occur due to a different response of the internal circuitry. As a result of this effect another parameter is defined: Δt_{PD}. This parameter is defined as the absolute value of the difference between t_{PDH} and t_{PDL}.

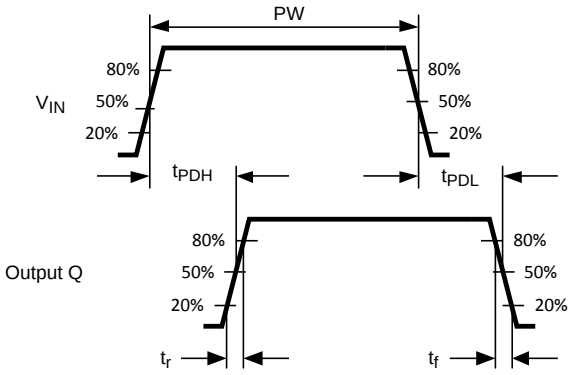


Figure 22. Pulse Parameter

If Δt_{PD} isn't zero, duty cycle distortion will occur. For example when applying a symmetrical waveform (e.g. a sinewave) at the input, it is expected that the comparator produces a symmetrical square wave at the output with a duty cycle of 50%. In case of different t_{PDH} and t_{PDL} the duty cycle of the output signal will not remain at 50%, but will be lower or higher. In addition to the propagation delay parameters for single ended outputs discussed before, there are other parameters in case of complementary outputs. These parameters describe the delay from input to each of the outputs and the difference between both delay times (see Figure 23). When the differential input signal crosses the reference level from L to H, both outputs will switch to their new state with some delay. This is defined as t_{PDH} for the Q output and $t_{PD\overline{L}}$ for the $\overline{Q}$ output, while the difference between both signals is defined as ΔtP_{DLH}. similar definitions for the falling slope of the input signal can be seen in Figure 21.

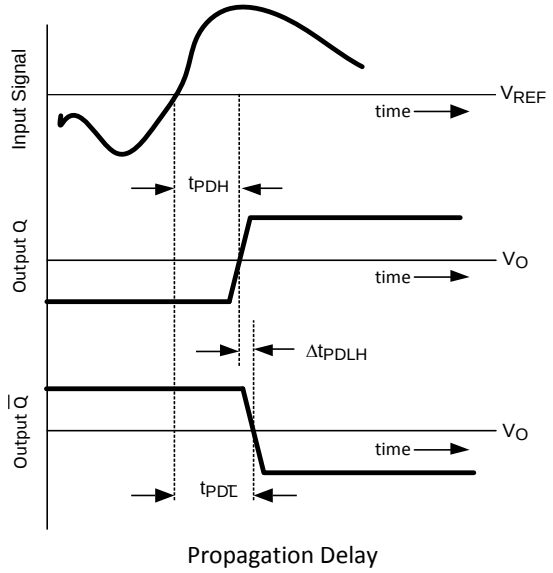


Figure 23. Propagation Delay

Both output circuits should be symmetrical. At the moment one output is switching 'on' the other is switching 'off' with ideally no skew between them. The design of the LMH7220 is optimized to minimize this timing difference. Propagation delay t_{PD} is defined as the average delay of both outputs at both slopes: $(t_{PDLH} + t_{PDHL}) / 2$.

DISPERSION

There are several circumstances that will produce a variation of the propagation delay time. This effect is called dispersion.

Amplitude Overdrive Dispersion

One of the parameters that causes dispersion is the amplitude variation of the input signal. Figure 24 shows the dispersion due to a variation of the input overdrive voltage. The overdrive is defined as the 'goto' differential voltage applied to the inputs. Figure 24 shows the impact it has on the propagation delay time if overdrive is varied from 10 millivolts to 100 millivolts. This parameter is measured with a constant slew rate of the input signal.

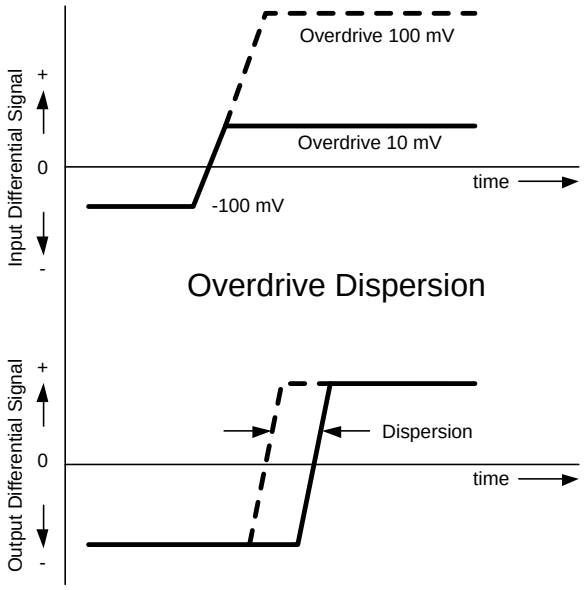


Figure 24. Overdrive Dispersion

The overdrive dispersion is caused by the fact that switching currents in the input stage depend on the level of the differential input signal.

Slew Rate Dispersion

The slew rate is another parameter that affects propagation delay. The higher the input slew rate, the faster the input stage switches (Figure 25).

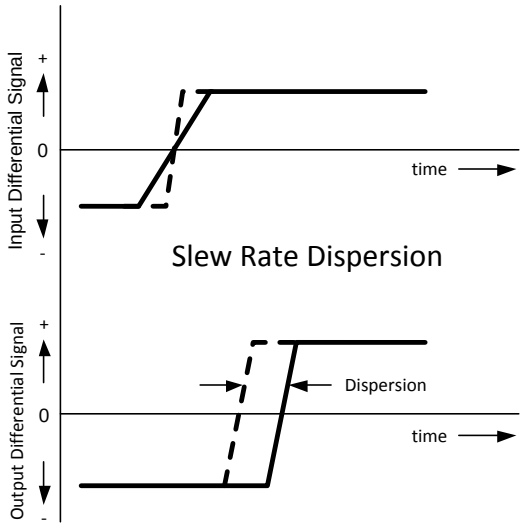


Figure 25. Slew Rate Dispersion

A combination of overdrive- and slew rate dispersion occurs when applying signals with different amplitude at constant frequency. A small amplitude will produce a small voltage change per time unit (dV/dt) but also a small maximum switching current (overdrive) in the input transistors. High amplitudes produce a high dV/dt and a bigger overdrive.

Common Mode Dispersion

Dispersion will also occur when changing the common mode level of the input signal (Figure 26). When V_{REF} is swept through the CMVR (Common Mode Voltage Range), this results in a variation of the propagation delay time. This variation is called Common Mode Dispersion.

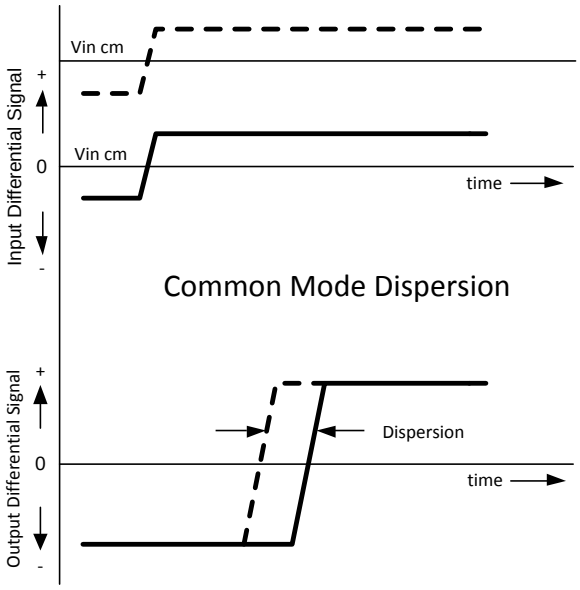


Figure 26. Common Mode Dispersion

All of the dispersion effects discussed before influence the propagation delay. In practice the dispersion is often caused by a combination of more than one varied parameter. It is good to realize this if there is the need to predict how much dispersion a circuit will show.

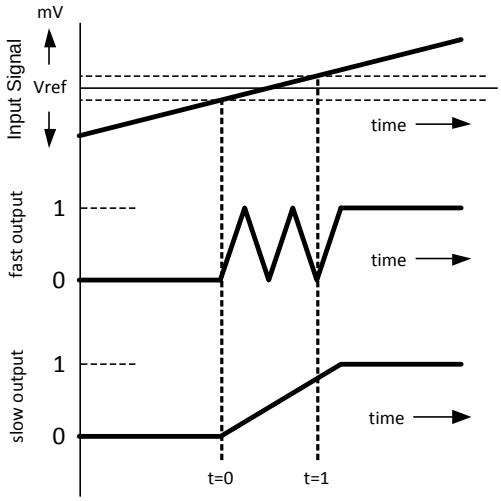
HYSTERESIS & OSCILLATIONS

In contrast to an op amp, the output of a comparator has only two defined states '0' or '1'. Due to finite comparator gain however, there will be a small band of input differential voltage where the output is in an undefined state. An input signal with fast slopes will pass this band very quickly without problems. During slow slopes however, passing the band of uncertainty can be relatively long. This enables the comparator outputs to switch back and forth several times between '0' and '1' on a single slope. The comparator will switch on its input noise, ground bounce (possible oscillations), ringing etc. Noise in the input signal will also contribute to these undesired switching effects.

In the next sections an explanation follows about these phenomena in situations where no hysteresis is applied, and the possible improvement hysteresis can give.

Using No Hysteresis

In Figure 27 can be seen what happens when the input signal rises from just under the threshold V_{REF} to a level just above it. From the moment the input reaches the lowest dotted line around V_{REF} at t=0, the output toggles on noise etc. Toggling ends when the input signal leaves the undefined area at t=1. In this example the output was fast enough to toggle three times. Due to this behavior digital circuitry connected to the output will count a wrong number of pulses. One way to prevent this is to choose a very slow comparator with an output that is not able to switch more than once between '0' and '1' during the time the input state is undefined.



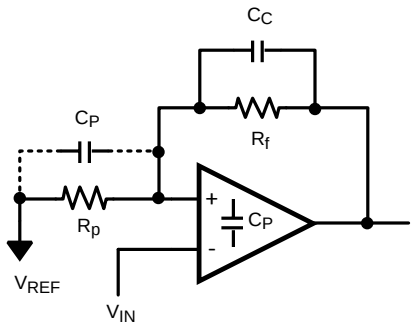
Oscillations & Noise

Figure 27. Oscillations & Noise

In most circumstances this is not an option because the slew rate of the input signal will vary.

Using Hysteresis

A good way to avoid oscillations and noise during slow slopes is the use of hysteresis. For this purpose a threshold is introduced that pushes the input switching level back at the moment the output switches (See Figure 28). In this simple setup, a comparator with a single output and a resistive divider to the positive input is drawn.



Simplified Schematic

Figure 28. Simplified Schematic

The divider R_F-R_P feeds back a portion of the output voltage to the positive input. Only a small part of the output voltage is needed, just enough to avoid the area at which the input is in an undefined state. Assuming this is only a few millivolts, it is sufficient to add (plus or minus) 10 mV to the positive input to prevent the circuit from oscillations. If the output switches between 0V and 5V and the choice for one of the resistors is done the other can be calculated. Assume R_P is 50Ω then R_F is 25 kΩ for 10 mV threshold on the positive input. The situation of Figure 29 is now created.

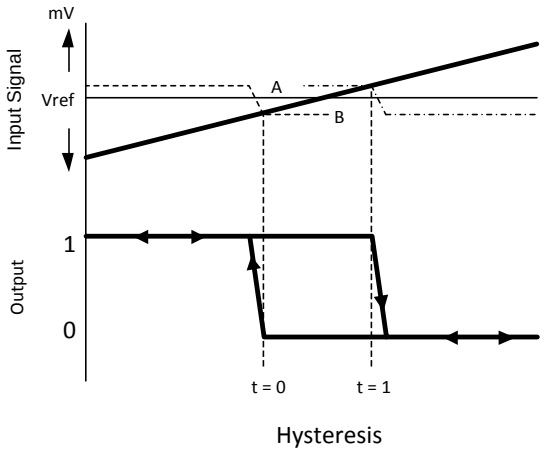


Figure 29. Hysteresis

In this picture there are two dotted lines, A and B, both indicating the resulting level at the positive input. When the signal at the negative input is low, the state of the input stage is well defined with the negative input much lower than the positive input. As a result the output will be in the high state. The positive input is at level A. With the input signal sloping up, this situation remains until V_{IN} crosses level A at t=1. Now the output toggles, and the voltage at the positive input is lowered to level B. So before the output has the possibility to toggle again, the difference between both inputs is made sufficient to have a stable situation again. When the input signal comes down from high to low, the situation is stable until level B is reached at t=0. At this moment the output will toggle back, and the circuit is back in the start situation with the negative input at a much lower level than the positive one. In the situation without hysteresis, the output would toggle exactly at V_{REF}. With hysteresis this happens at the introduced levels A and B, as can be seen in Figure 29. Varying the levels A and B will also vary the timing of t=0 and t=1. When designing a circuit be aware of this effect. Introducing hysteresis will cause some time shifts between output and input (e.g. duty cycle variations), but eliminates undesired switching of the output.

Parasitic Capacitors

In the simple schematic of Figure 28 some capacitors are drawn. The capacitors C_P. represent the parasitic (board) capacitance at the input of the part. This capacity will slow down the change of the level of the positive input in reaction to the changing output voltage. As a result of this, the output may have the time to switch over more than once. Actually the parasitic capacity represented by C_P makes the attenuation circuit of R_F and R_P frequency dependent. The only action to take is to create a frequency independent circuit. This is simply done by placing the compensation capacitor C_C in parallel with R_F. The capacitor C_C can be calculated with the formula $R_F * C_C = R_P * C_P$; this means that both of the time constants must be the same to create a frequency independent network. A simple example gives the following assuming that C_P is in total 2.5 pF and as already calculated R_F = 25 kΩ in combination with R_P = 50Ω. These input data gives:

$$C_C = R_P * C_P/R_F \quad (1)$$

$$C_C = 50*2.5e\text{-}12/25e3 \quad (2)$$

$$C_C = 5e\text{-}15 = 0.005 \text{ pF} \quad (3)$$

This is not a practical value and different conclusions are possible:

- No capacitor C_C needed

- Place a capacitor C_C of 1 pF and accept a big overshoot at the positive input being sure that the input stage is in a secure new position
- Place an extra C_P of such a value that C_C has a realistic value of say 1 pF (extra C_P = ±500 pF).

Position of Feedback Resistors

Another important issue while using positive feedback is the placement of the resistors R_P and R_F. These resistors must be placed as near as possible to the positive input, because this input is most sensitive for picking up spurious signals, noise etc. This connection must be very clean for the best performance of the overall circuit. With raising speeds the total PCB design becomes more and more critical, the LMH7220 comparator doesn't have built in hysteresis, so the input signal must meet minimum requirements to make the output switch over properly. In the following sections some aspects concerning the load connected to the outputs and transmission lines will be discussed.

THE OUTPUT SWING PROPERTIES

LVDS has differential outputs which means that both outputs have the same swing but in opposite direction (Figure 30). Both outputs swing around a voltage called the common mode output voltage (V_O). This voltage can be measured at the midpoint of two equal resistors connected to both outputs as discussed in INPUT & OUTPUT TOPOLOGY. The absolute value of the difference between both voltages is called V_{OD}. LVDS outputs cannot be held at the V_O level because of their digital nature. They only cross this level during a transition. Due to the symmetrical structure of the circuit, both output voltages cross at V_O regardless if the output changes from '0' to '1' or vise versa.

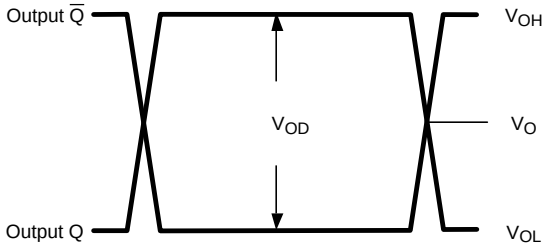


Figure 30. LVDS Output Signals

In case the outputs aren't symmetrical or are a-symmetrically loaded, the output voltages differ from the situation of Figure 30. For this non-ideal situation there are two additional parameters defined, ΔV_O and ΔV_{OD}, as can be seen in Figure 31.

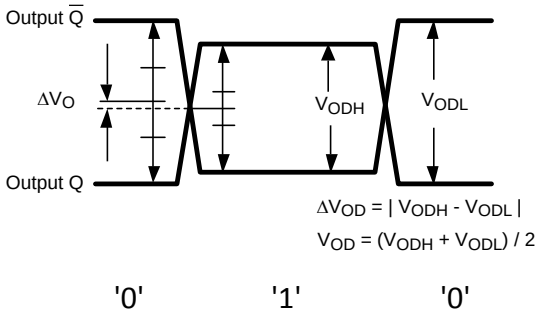


Figure 31. LVDS Output Signals with Different Amplitude

ΔV_O is the difference in V_O between the '1' state and the '0' state. This variation is acceptable if it is below 50 mV following the ANSI/TIA/EIA-644 LVDS standard. It is also possible that V_{OD} in the '1' state isn't the same as in the '0' state. This parameter is specified as ΔV_{OD}, and is calculated as the absolute value of the difference of V_{ODH} and V_{ODL}.

LOADING THE OUTPUT

The output structure creates a current (I_{LOOP} see Figure 32) through an external differential load resistor of 100Ω nominal. This results in a differential output voltage of 325 mV. The outputs of the comparator are connected to tracks on a PCB. These tracks can be seen as a differential transmission line. The differential load resistor acts as a high frequency termination at the end of the transmission line. This means that for a proper signal behavior the PCB tracks have to be dimensioned for a characteristic impedance of 100Ω as well. Changing the load resistor also implies a change of the transmission line impedance. More about transmission lines and termination can be found in the next section. The signal across the 100Ω termination resistor is fed into the inputs of subsequent circuitry that processes the data. Any connection to input circuitry of course draws current from the comparator's outputs. In the case of a balanced input connected to the load resistance, current I_P is drawn from both output connection points to ground. Keep in mind that the LMH7220's ability to source currents is much higher than to sink them. The connected input circuitry also forms a differential load to the outputs of the comparator (see Figure 32). This will cause the voltage across the termination resistor to differ from its nominal value.

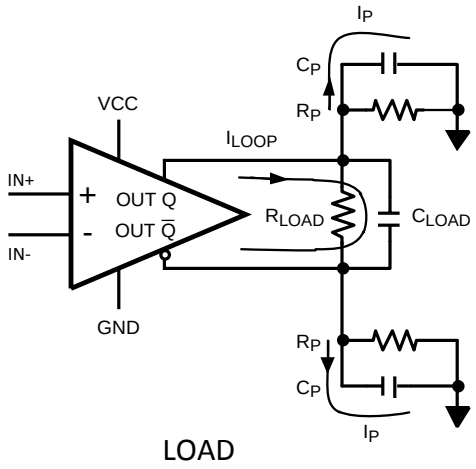


Figure 32. Load

In general one single connection only draws a few µA's, and doesn't have much effect on the LVDS output voltage. For multiple inputs on one output pair, load currents must not exceed the specified limits, as described in the ANSI or IEEE LVDS standards. Below a specified value of V_{OD}, the functioning of subsequent circuitry becomes uncertain. However under normal conditions there is no need to worry. Another point of practice is load capacitances. Capacitances are applied differentially (C_{LOAD}) and also to ground (C_P). All of these capacitors will disturb the pulse shape. The edges of the output pulse become slower, and in reaction the detection of the transition comes at a later moment. Be aware of this effect when measuring with probes. Both single ended and differential probes have these capacitances. A standard probe commonly has a load capacity of about 8 to 10 pF. This will cause some degradation of the pulse shape and will add some time delay.

TRANSMISSION LINES & TERMINATION TECHNOLOGIES

The LMH7220 uses LVDS technology. LVDS is a way to communicate data using low voltage swing and low power consumption. Nowadays data rates are growing, requiring increasing speed. Data isn't only connected to other IC's on a single PCB board but in many cases there are interconnections from board to board or from equipment to equipment. Distances can be short or long but it is always necessary to have a reliable connection, consume low power and to be able to handle high data rates. LVDS is a differential signal protocol. The advantage over single ended signal transmission is its higher immunity to common mode noise. Common mode signals are signals that are equally apparent on both lines and because the receiver only looks at the difference between both lines, this noise is canceled.

Maximum Bitrates

A very important specification in high speed circuits are the rise and fall times. In fact these determine the maximum toggle rate (TR) of the part. The LVDS standard specifies them at 0.26 ns to 1.5 ns. Rise and fall times are normally specified at 20% and 80% of the signal amplitude (60% difference). TR is defined as the bitrate at which the differential output voltage drops to 50% of its nominal value.

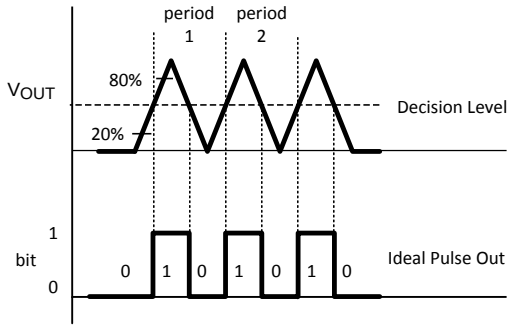


Figure 33. Bitrate

Need for Terminated Transmission Lines

During the '80's and '90's TI fabricated the 100k ECL logic family. The rise and fall time specification was 0.75 ns which was very fast and will easily introduce errors in digital circuits if insufficient care has been taken to the transmission lines and terminations used for these signals. To be helpful to designers that use ECL with "old" PCB-techniques, the 10k ECL family was introduced with a rise and fall time specification of 2 ns. This was much slower and more easy to use. LVDS signals have transition times that exceed the fastest ECL family. A careful PCB design is needed using RF techniques for transmission and termination. Transmission lines can be formed in several ways. The most commonly used types are the coaxial cable and the twisted pair telephony cable (Figure 34).

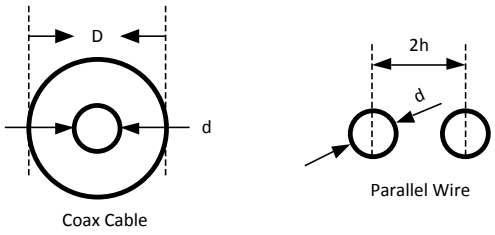


Figure 34. Cable Configuration

These cables have a characteristic impedance determined by their geometric parameters. Widely used impedances for the coaxial cable are 50Ω and 75Ω. Twisted pair cables have impedances of about 120Ω to 150Ω.

Other types of transmission lines are the strip line and the micro strip. These last types are used on PCB boards. They have the characteristic impedance dictated by the physical dimensions of a track placed over a metal ground plane (See Figure 35).

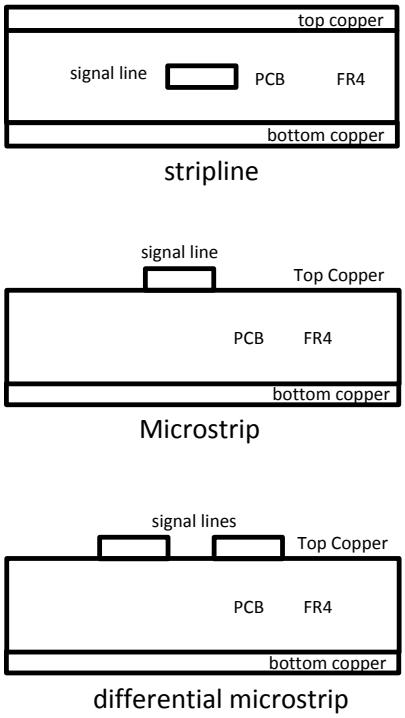


Figure 35. PCB Transmission Lines

Differential Microstrip Line

The transmission line which is ideally suited for LVDS signals is the differential micro strip line. This is a double micro strip line with a narrow space in between. This means both lines have a strong coupling and this determines mainly the characteristic impedance. The fact that they are routed above a copper plane doesn't affect differential impedance, only CM-capacitance is added. Each of the structures above has its own geometric parameters so for each structure there is another formula to calculate the right impedance. For calculations of these transmission lines visit the Texas Instruments website or feel free to order the RAPIDESIGNER. For some formula's given in the 'LVDS owners manual' see chapter 3 (see INTRODUCTION for the URL). At the end of the transmission line there must be a termination having the same impedance as of the transmission line itself. It doesn't matter what impedance the line has, if the load has the same value no reflections will occur. When designing a PCB board with transmission lines on it, space becomes an important item especially on high density boards. With a single micro strip line, line width is fixed for given impedance and a board material. Other line widths will result in different impedances.

Advantage of Differential Microstrip

Impedances of transmission lines are always dictated by their geometric parameters. This is also true for differential micro strip lines. Using this type of transmission lines, track distance determines mainly the resulting impedance. So, if the PCB manufacturer can produce reliable boards with narrow track spacing the track width for a given impedance is also small. The wider the spacing, the wider tracks are needed for a certain impedance. For example two tracks of 0.2 mm width and 0.1 mm spacing have the same impedance as two tracks of 0.8 mm width and 0.4 mm spacing. With high-end PCB processes, it is possible to design very narrow differential microstrip transmission lines. It is desirable to use these phenomena to create optimal connections to the receiving part or the terminating resistor, in accordance with their physical dimensions. Seen from the comparator, the termination resistor must be connected at the far end of the line. Open connections after the termination resistor (e.g. to an input of a receiver) must be as short as possible. The allowed length of such connections varies with the received transients. The faster the transients the shorter open lines must be to prevent signal degradation.

PCB LAYOUT CONSIDERATIONS AND COMPONENT VALUES SELECTION

High frequency designs require that both active- and passive components are selected that are specially designed for this purpose. For reliable high speed design it is highly recommended also to use small surface mount passive components because these packages have low parasitic capacitance and low inductance simply because they have no leads to connect them to the PCB. It is possible to amplify signals at frequencies of several hundreds of MHz using standard through- hole resistors. Surface mount devices however are better suited for this purpose. Another important issue is the PCB itself, which is no longer a simple carrier for all the parts and a medium to interconnect them. The PCB becomes a real component itself and consequently contributes its own high frequency properties to the overall performance of the circuit. Practice dictates that a high frequency design at least has one ground plane, providing a low impedance path for all decoupling capacitors and other ground connections. Care should be taken especially that on-board transmission lines have the same impedance as the cables to which they are connected. Most single ended applications have 50Ω impedance (75Ω for video and cable TV applications). On PCBs, such low impedance single ended microstrip transmission lines usually require much wider traces (2 to 3 mm) on a standard double sided PCB board than needed for a ‘normal’ trace. Another important issue is that inputs and outputs shouldn’t ‘see’ each other. This occurs if input- and output tracks are routed in parallel over the PCB with only a small amount of physical separation, and particularly when the difference in signal level is high. Furthermore components should be placed as flat and low as possible on the surface of the PCB. For higher frequencies a long lead can act as a coil, a capacitor or an antenna. A pair of leads can even form a transformer. Careful design of the PCB minimizes oscillations, ringing and other unwanted behavior. For ultra high frequency designs only surface mount components will give acceptable results. (for more information see OA-15 [SNOA367]).

TI suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization.

LMH730220 / 551012993-002 Rev A

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	26

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH7220MK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	C29A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

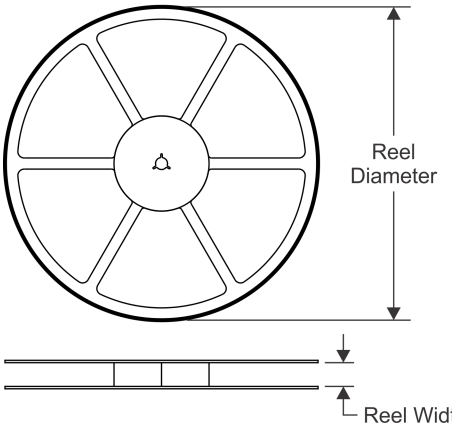
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

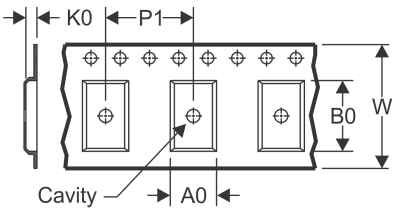
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

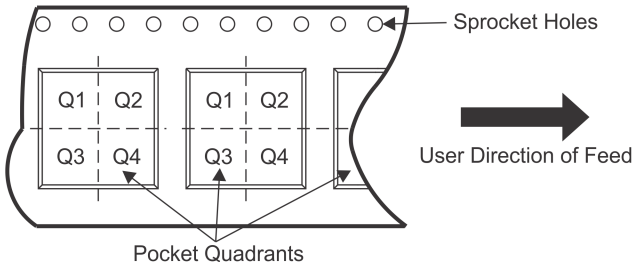


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

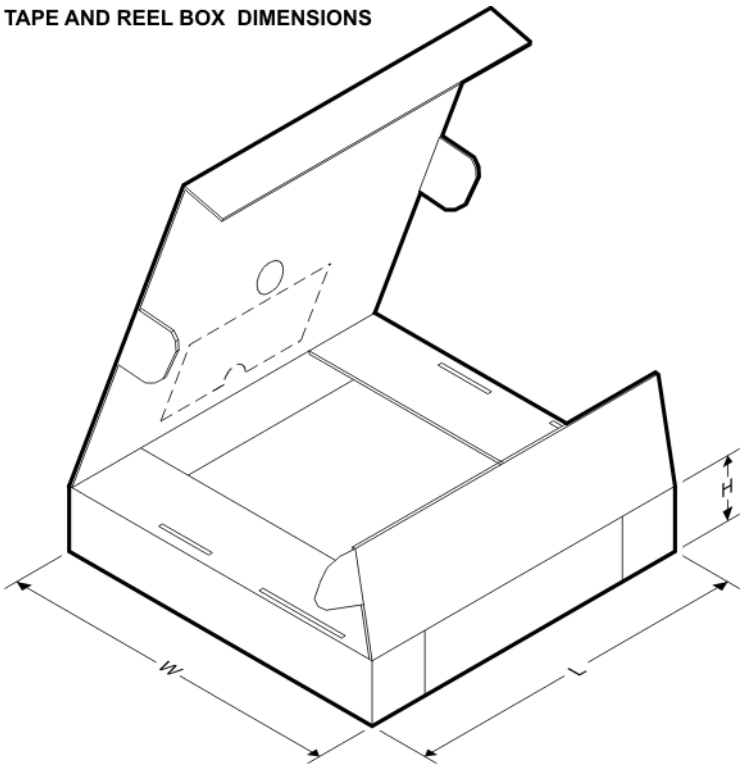
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH7220MK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

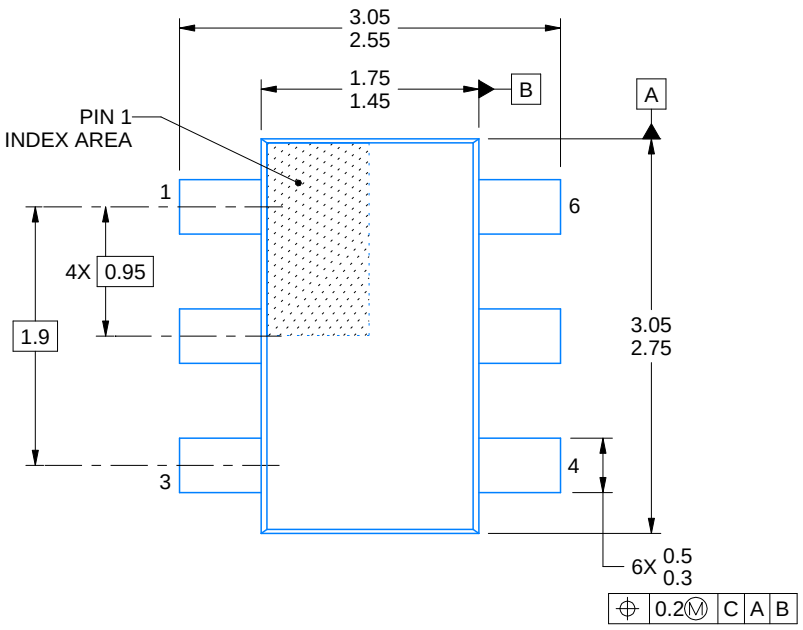
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH7220MK/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0

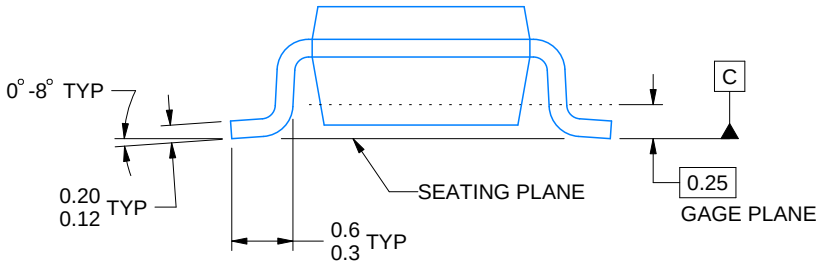
PACKAGE OUTLINE

DDC0006A

SOT - 1.1 max height

SOT





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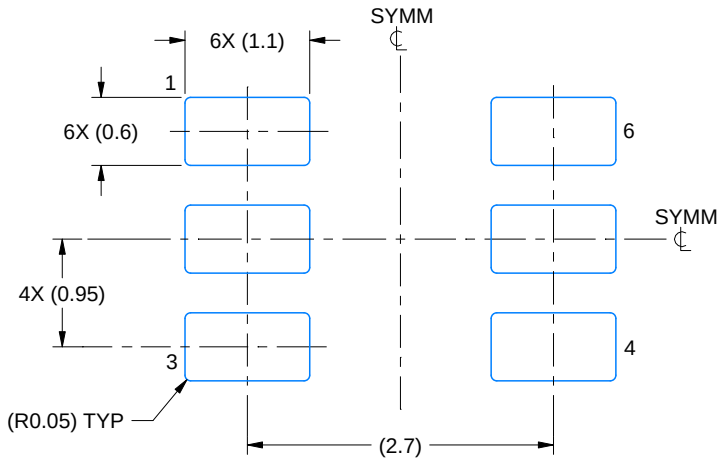
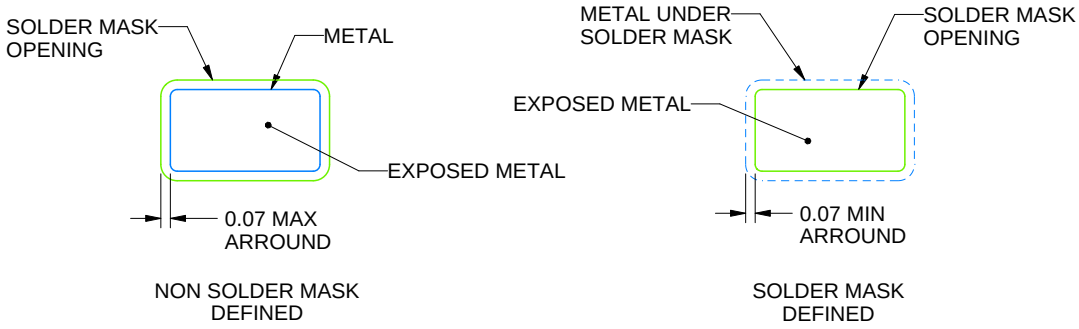
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

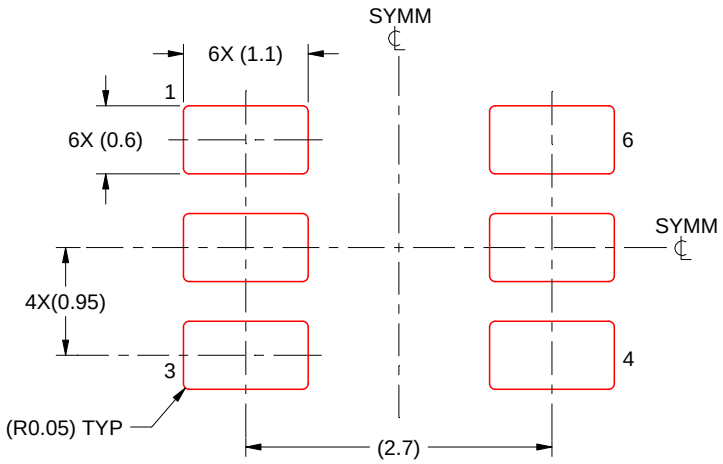


SOLDERMASK DETAILS

4214841/B 11/2020

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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