EiceDRIVER™ 1ED34x1Mc12M Enhanced

Datasheet

Single-channel 5.7 kV (rms) isolated gate driver IC with adjustable DESAT and soft-off

Features

- 650 V, 1200 V, 1700 V, 2300 V IGBTs, SiC, and Si MOSFETs
- 40 V absolute maximum output supply voltage
- ±3 A, ±6 A, and ±9 A typical sinking and sourcing peak output current
- Separate source and sink outputs for hard switching and with active Miller clamp/clamp driver
- Adjustment pins for parameter configuration from input side
- Precise V_{CEsat} detection (DESAT) with fault output and adjustable filter time and leading edge blanking time with resistor at *ADJB* pin
- Adjustable IGBT soft turn-off after desaturation detection with resistor at *ADJA* pin
- Operation at high ambient temperature up to 125 °C with over-temperature shut down at 160 °C (±10 °C)
- Tight IC-to-IC propagation delay matching ($t_{PDD,max}$ = 30 ns)
- Undervoltage lockout protection with hysteresis for input and output side with active shut-down
- High common-mode transient immunity CMTI = 200 kV/µs
- Small space-saving DSO-16 fine-pitch package with large creepage distance (>8 mm)
- Safety certification
  - UL 1577 recognized (File E311313) with $V_{ISO,test}$ = 6840 V (rms) for 1 s, V_{ISO} = 5700 V (rms) for 60 s
  - VDE 0884-11 approval (Certificate no. 40053980) with V_{IORM} = 1767 V (peak, reinforced)
- Evaluation board available EVAL-1ED3491MX12M

Potential applications

- Industrial motor drives - compact, standard, premium, servo drives
- Solar inverters
- UPS systems
- Welding
- Commercial and agricultural vehicles (CAV)
- Commercial air-conditioning (CAC)
- High-voltage isolated DC-DC converters
- Isolated switch mode power supplies (SMPS)

PG-DSO-16

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Device information

Product type	Output current	CLAMP type[1]	Isolation class	Marking	OPN
1ED3431MC12M	3 A (typ)	CLAMP	reinforced	3431MC12	1ED3431MC12MXUMA1
1ED3461MC12M	6 A (typ)	CLAMPDRV	reinforced	3461MC12	1ED3461MC12MXUMA1
1ED3491MC12M	9 A (typ)	CLAMPDRV	reinforced	3491MC12	1ED3491MC12MXUMA1
1ED3431MU12M	3 A (typ)	CLAMP	UL 1577	3431MU12	1ED3431MU12MXUMA1
1ED3461MU12M	6 A (typ)	CLAMPDRV	UL 1577	3461MU12	1ED3461MU12MXUMA1
1ED3491MU12M	9 A (typ)	CLAMPDRV	UL 1577	3491MU12	1ED3491MU12MXUMA1

1) Please refer to Chapter 4.5.4.1 for circuit connection to avoid damage to the gate driver IC

Description

The 1ED34x1Mc12M family (X3 Analog) consists of galvanically isolated single channel gate driver ICs in a small PG-DSO-16 package with a large creepage and clearance of 8 mm. The gate driver ICs provide a typical peak output current of 3 A, 6 A, and 9 A.

Adjustable control and protection functions are included to simplify the design of highly reliable systems. All parameter adjustments are done from the input side, including adjustable DESAT filter time, leading edge blanking time, and soft-off current level with only two resistors..

All logic I/O pins are supply voltage dependent 3.3 V or 5 V CMOS compatible and can be directly connected to a microcontroller.

The data transfer across the galvanic isolation is realized by the integrated coreless transformer technology.

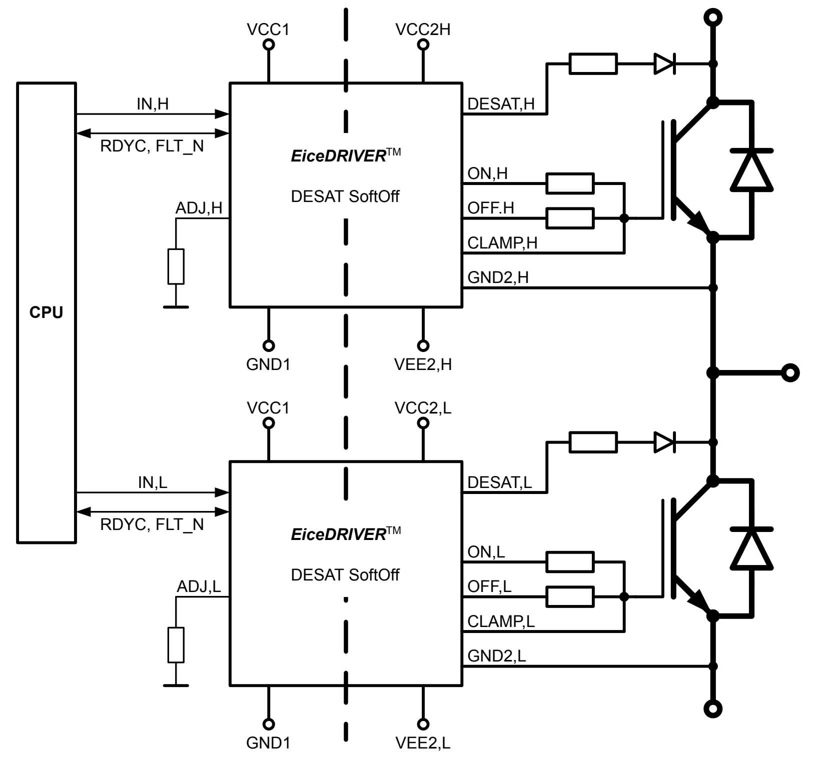

Figure 1 **Typical application**

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1 Block diagram

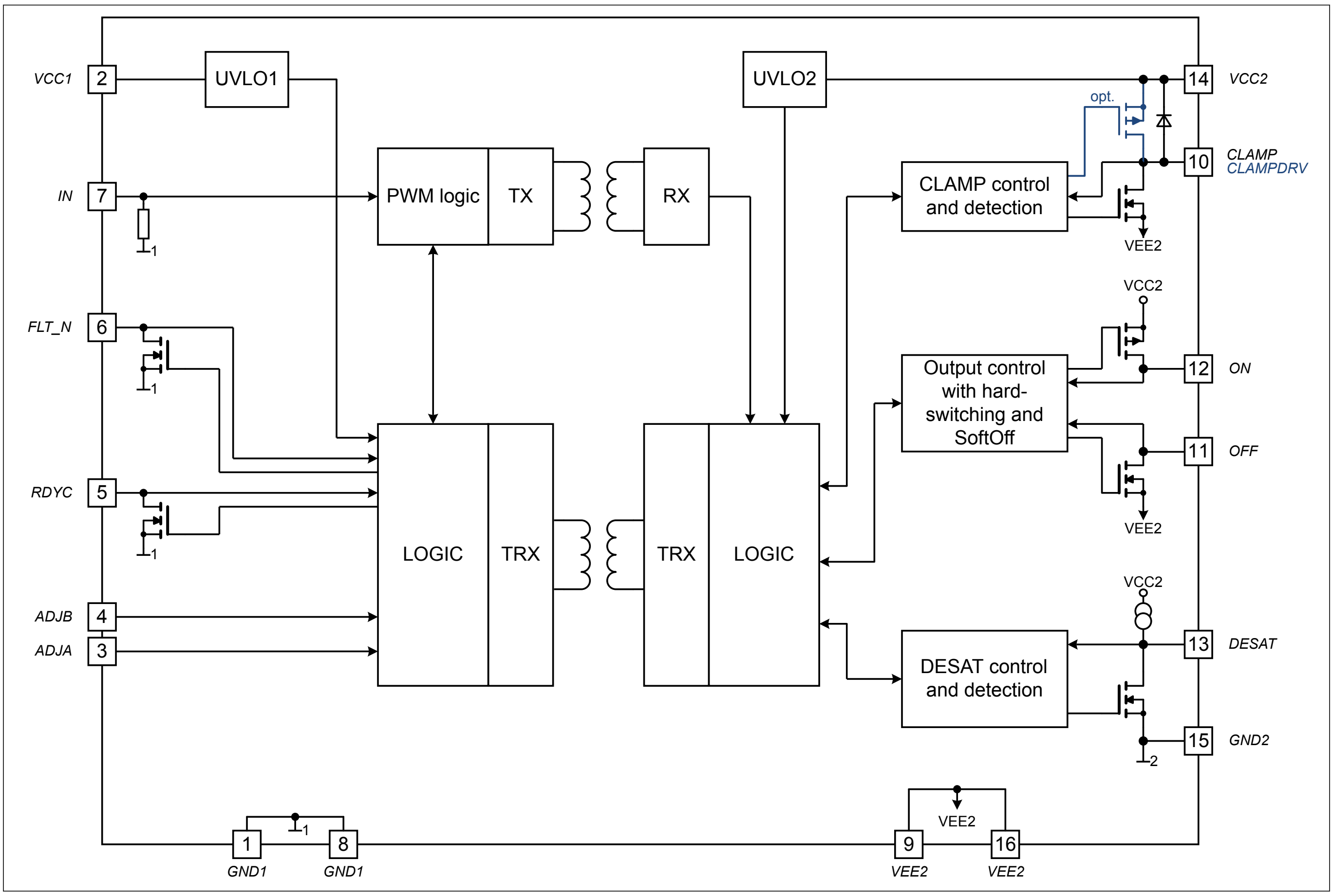

Figure 2 Block diagram

2 Related products

Note: *Please consider the gate driver IC power dissipation and insulation requirements for the selected power switch and operating condition.*

Product group	Product name	Description
TRENCHSTOP™ IGBT Discrete	IKQ75N120CS6	High Speed 1200 V, 75 A IGBT with anti-parallel diode in TO247-3
	IKW15N120BH6	High Speed 1200 V, 15 A IGBT with anti-parallel diode in TO247
	IHW40N120R5	Reverse conducting 1200 V, 40 A IH IGBT with integrated diode in TO247
CoolSiC™ SiC MOSFET Discrete	IMBF170R650M1	1700 V, 650 mΩ SiC MOSFET in TO263-7 package
	IMBG120R045M1H	1200 V, 45 mΩ SiC MOSFET in TO263-7 package
	IMZ120R350M1H	1200 V, 350 mΩ SiC MOSFET in TO247-4 package
CoolSiC™ SiC MOSFET Module	FS45MR12W1M1_B11	EasyPACK™ 1B 1200 V / 45 mΩ sixpack module
	FF23MR12W1M1_B11	EasyDUAL™ 1B 1200 V, 23 mΩ half-bridge module
	FF6MR12W2M1_B11	EasyDUAL™ 2B 1200 V, 6 mΩ half-bridge module
	F3L11MR12W2M1_B74	EasyPACK™ 2B 1200 V, 11 mΩ 3-Level module in Advanced NPC (ANPC) topology
	F4-23MR12W1M1_B11	EasyPACK™ 1B 1200 V, 23 mΩ fourpack module
TRENCHSTOP™ IGBT Modules	F4-100R17N3E4	EconoPACK™ 3 1700 V, 100 A fourpack IGBT module
	F4-200R17N3E4	EconoPACK™ 3 1700 V, 200 A fourpack IGBT module
	FS150R17N3E4	EconoPACK™ 3 1700 V, 150 A sixpack IGBT module
	FF650R17IE4	PrimePACK™ 3 1700 V, 650 A half-bridge dual IGBT module
	FF1000R17IE4	PrimePACK™ 3 1700 V, 1000 A half-bridge dual IGBT module
	FF1200R17IP5	PrimePACK™ 3+ 1700 V, 1200 A dual IGBT module
	FF1500R17IP5	PrimePACK™ 3+ 1700 V, 1500 A dual IGBT module
	FF1500R17IP5R	PrimePACK™ 3 1700 V, 1500 A dual IGBT module
	FF1800R17IP5	PrimePACK™ 3+ 1700 V, 1800 A dual IGBT module
	FP10R12W1T7_B11	EasyPIM™ 1B 1200 V, 10 A three phase input rectifier PIM IGBT module
	FS100R12W2T7_B11	EasyPACK™ 2B 1200 V, 100 A sixpack IGBT module
	FP150R12KT4_B11	EconoPIM™ 3 1200V three-phase PIM IGBT module
	FS200R12KT4R_B11	EconoPACK™ 3 1200 V, 200 A sixpack IGBT module

3 Pin configuration and functionality

The pin assignment at the gate driver IC generally differentiates between the input side and the output side.

Table 1 General pin assignment

Pins	**Designation**
1 to 8	input side, input logic signal side, or low voltage side
9 to 16	output side, driver power side, or high voltage side

For simplicity reasons the driver is described as an IGBT driver. For use with MOSFETs and other power switches simply replace any mentioning of collector and emitter with their corresponding pin names.

3.1 Pin configuration

Table 2 Pin configuration table abbreviations

Abbreviation	**Description**
Pin type	
PWR	Power supply and gate current output pins
I/O	Digital input and output pin
I	Digital input pin
GND	Ground reference pin
AI	Analog input pin
Buffer type	
OD	Open drain output
CMOS	CMOS compatible input threshold levels
PP	Push/pull output buffer
special	Special output/input function, see individual description
Pull device	
PD	Pull-down resistor
CS	Current source

Table 3 Pin configuration

Pin no.	**Pin name**	**Pin type**	**Buffer type**	**Pull device**	**Function**
1	*GND1*	GND	–	–	Ground input side
2	*VCC1*	PWR	–	–	Positive power supply input side
3	*ADJA*	AI	special	CS	Parameter adjust set A
4	*ADJB*	AI	special	CS	Parameter adjust set B
5	*RDYC*	I/O	OD, CMOS	–	Combined ready output, high active and fault clear input and soft-off input, low active
6	*FLT_N*	I/O	OD, CMOS	–	Fault output, low active and soft- off input, low active
7	*IN*	I	CMOS	PD, 40 kΩ	Non inverted driver input

(table continues...)

Table 3 (continued) Pin configuration

Pin no.	Pin name	Pin type	Buffer type	Pull device	Function
8	*GND1*	GND	–	–	Ground input side
9	*VEE2*	GND	–	–	Negative power supply output side
10	*CLAMP*	PWR	OD	–	Active Miller clamping, open drain to VEE2 (1ED3431M only)
10	*CLAMPDRV*	PWR	PP	–	Active miller clamping, clamp driver for external MOSFET (1ED3461M, 1ED3491M)
11	*OFF*	PWR, AI	OD	–	Driver sink output
12	*ON*	PWR, AI	OD	–	Driver source output
13	*DESAT*	AI	special	CS, 500 µA	Enhanced desaturation protection
14	*VCC2*	PWR	–	–	Positive power supply output side
15	*GND2*	AI	–	–	Signal ground output side
16	*VEE2*	GND	–	–	Negative power supply output side

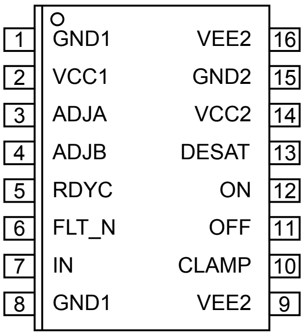

Figure 3 PG-DSO-16 (top view) with CLAMP

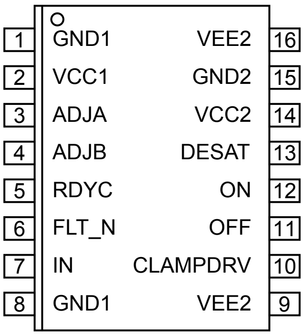

Figure 4 PG-DSO-16 (top view) with CLAMPDRV

3.2 Pin functionality

GND1

Reference ground of the input side. Connect direct to input signal ground.

VCC1

Positive power supply terminal of the input side, connect to 5 V or 3.3 V for proper operation. Place a decoupling capacitor close to this pin and *GND1*.

ADJA and *ADJB* parameter adjust input for set A or B

The pins *ADJA* and *ADJB* are used to adjust two sets of independent parameters of output functions.

Connect a resistor between 1.33 kΩ and 28.0 kΩ to *GND1* to adjust each parameter. All valid resistor values belong to the E96-series with 1% tolerance.

Connecting *ADJA* to *GND1* uses a default value for soft switch-off. Connecting it to *VCC1* is disabling the gate driver IC.

Connecting *ADJB* to *GND1* is disabling the gate driver IC. Connecting it to *VCC1* is setting the function to minimum values.

RDYC ready status output, fault-off input and fault-clear input

Open-drain output reports the correct operation of the device, ready output is high active. Fault-clear input and fault-off input clears a gate driver fault or switch the gate driver output to off with fault-off function, input is low active. Connect to a microcontroller with 5 V or 3.3 V I/O with an external pull-up resistor to *VCC1*. A typical value for this resistor is 2.2 kΩ. The *RDCY* signal is referenced to *GND1*.

FLT_N fault output and fault-off input

Open-drain output reports the failures related to operating of the inverter system to the microcontroller, fault output is active low. Fault-off input switch the gate driver output to off with fault-off function, input is low active. Connect to a microcontroller with 5 V or 3.3 V I/O with an external pull-up resistor to *VCC1*. A typical value for this resistor is 2.2 kΩ. The *FLT_N* signal is referenced to *GND1*.

IN non inverting gate driver input

IN input controls the output of the gate driver IC, the IGBT is turned on if *IN* is set to high. Connect to a PWM output of the microcontroller with 5 V or 3.3 V IO. An internal pull-down resistor ensures IGBT off-state if not connected. A minimum pulse width of typical 103 ns is defined to make the gate driver IC robust against glitches at *IN*.

VEE2

Negative power supply terminal of the output side. Connect to a voltage of 0 V to -25 V referenced to *GND2* for proper operation. Place a decoupling capacitor close to the following pins:

- *VCC2* and *VEE2*
- *GND2* and *VEE2*

If no negative supply voltage is used, all *VEE2* pins have to be connected to *GND2*.

CLAMP Miller clamp output, *CLAMPDRV* Miller clamp pre-driver output

CLAMP: High-current clamp output to hold the gate voltage low during collector-emitter-voltage rise. Connect directly to the gate of the IGBT.

CLAMPDRV: Clamp pre-driver output for the use of an external clamp switch. Connect directly to the gate of a n-channel MOSFET.

OFF driver output

High-current driver sink output to discharge the gate of the external IGBT.The gate driver IC also sinks the Soft-off current at this pin. Connect to the gate of the IGBT via a chosen turn-off gate resistor.

ON driver output

High-current driver source output to charge the gate of the external IGBT and turn it on and sense input for the CLAMP function. Connect to the gate of the IGBT via a chosen turn-on gate resistor.

DESAT enhanced desaturation detection input

Desaturation detection input to monitor the IGBT collector-emitter voltage (V_{CE}) to detect desaturation caused by short circuit events. Connect to the collector of the driven IGBT via a series connection of a protection resistor and a high-voltage diode. The *DESAT* signal is referenced to *GND2*.

VCC2

Positive power supply terminal of the output side. Connect to sufficient supply voltage referenced to *GND2* for proper operation. Place a decoupling capacitor close to the following pins:

- *VCC2* and *VEE2*
- *VCC2* and *GND2*

GND2 reference ground

Reference ground of the output side. Connect to common voltage of a bipolar supply and the emitter of the IGBT. Place a decoupling capacitor close to the following pins:

- *VCC2* and *GND2*
- *GND2* and *VEE2*

4 Functional description

The 1ED34x1Mc12M family (X3 Analog) consists of galvanically isolated single channel gate driver ICs with adjustable feature parametrization by two simple resistors. All adjustments can be done from the low voltage input side.

To start-up the gate driver IC for normal operation both input and output sides of the gate driver IC need to be powered.

The 1ED34x1Mc12M family (X3 Analog) is designed to support various supply configurations on the input and output side. On the output side unipolar and bipolar supply is possible.

The output stage is realized as rail-to-rail. There the gate driver voltage follows the supply voltage without an additional voltage drop. In addition it provides an easy clamping of the gate voltage during short circuit of an external IGBT.

The *RDYC* status output reports correct operation of the gate driver IC like sufficient voltage supply. The *FLT_N* status output reports failures in the application like desaturation detection.

To ensure safe operation the gate driver IC is equipped with an input and output side under-voltage lockout circuit. The UVLO levels are optimized for IGBTs.

The desaturation detection circuit protects the external IGBT from destruction at a short circuit. The gate driver IC reacts on a DESAT fault by turning off the IGBT with the adjustable soft-off method.

The soft turn-off function is used to switch-off the external IGBT in overcurrent conditions in a soft-controlled manner to protect the IGBT against collector emitter over-voltages.

An active Miller clamp function protects the IGBT from parasitic turn-on in fast switching applications.

4.1 Start-up and fault clearing

For normal operation both input and output sides of the gate driver IC need to be powered. A low level at the *FLT_N* pin always indicates a fault condition. In this case the IC starts internal mechanisms for fault clearing.

Input side start-up

1. Voltage at *VCC1* reaches the input UVLO threshold: input side of gate driver IC starts operating
2. *FLT_N* follows input supply voltage
3. Records resistor programmable function from *ADJA* and *ADJB*
4. Waits until output side is powered
5. Initiates internal start-up: Transfers configured values to output side
6. Performs internal self-test

The start-up delay takes approx. 200 µs and is part of the complete start-up time t_{START1}.

Output side start-up

1. Voltage at *VCC2* reaches the output UVLO threshold: output side of gate driver IC starts operating
2. Activates OFF gate driver output: connected gate stays discharged
3. Waits until input side is powered
4. Initiates internal start-up: Receives configured values from input side
5. Performs internal self-test

The start-up delay takes approx. 200 µs and is part of the complete start-up time t_{START2}.

The gate driver IC releases *RDYC* to high to signal a successful start-up and its readiness to operate. The gate driver IC will follow the status of the *IN* signal.

Clearing a fault with *RDYC* to low cycle

1. Set *IN* to low
2. Set *RDYC* to low for a duration longer than the fault clear time t_{CLRMIN}

3. Release *RDYC* to high
    a. If the source of the fault is no longer present, *FLT_N* is released to high
    b. If another fault source is active, *FLT_N* stays low and the cycle needs to be repeated
4. Continue PWM operation

4.2 Supply

The 1ED34x1Mc12M family (X3 Analog) is designed to support various supply configurations. The input side can be used with a 3.3 V or 5 V supply.

The output side requires either an unipolar supply (*VEE2* = *GND2*) or a bipolar supply.

- Individual supply voltages between *VCC2* and *GND2* or *GND2* and *VEE2* shall not exceed 25 V.
- The total supply voltage between *VCC2* and *VEE2* shall not exceed 35 V.

To ensure safe operation of the gate driver IC, it is equipped with an input and output side undervoltage lockout circuit.

Unipolar supply

In unipolar supply configuration the gate driver IC is typically supplied with a positive voltage of 15 V at *VCC2*. *GND2* and *VEE2* are connected together and this common potential is connected to the IGBT emitter.

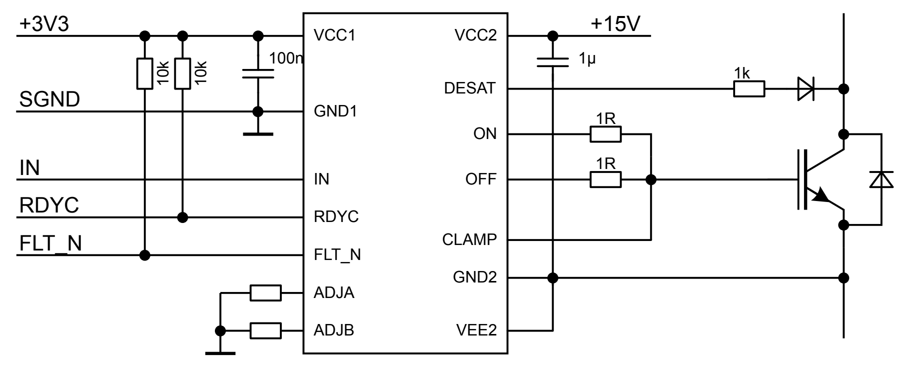

Figure 5 Application example with unipolar supply (1ED3431M)

Bipolar supply

For bipolar supply the gate driver IC is typically supplied with a positive voltage of 15 V at *VCC2* and a negative voltage of -8 V or -15 V at *VEE2* relative to *GND2*.

Between *VCC2* and *VEE2* the maximum potential difference is 35 V.

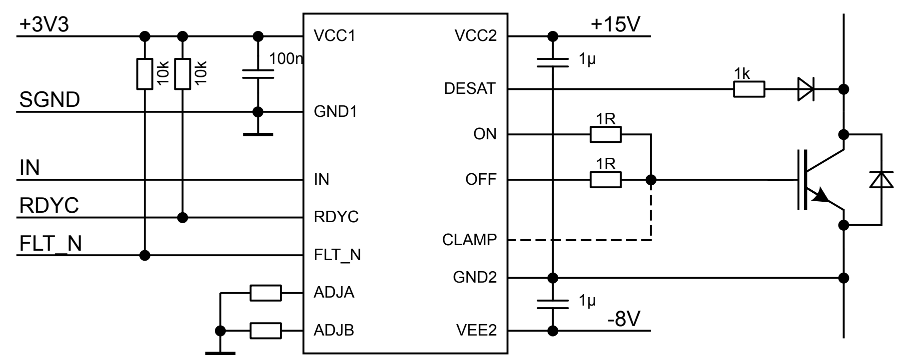

Figure 6 Application example with bipolar supply (1ED3431M)

Negative supply prevents a parasitic turn-on due to the additional voltage margin to the gate turn-on threshold.

VEE2 over GND2 supply connection check

The gate driver IC has a built-in connection check for *VEE2*. A loss of *VEE2* connection will be detected and signaled via *RDYC*.

4.2.1 Input side undervoltage lockout, *VCC1* UVLO

To ensure correct operation of the input side and safe operation of the application the gate driver IC is equipped with an input supply undervoltage lockout for *VCC1*.

UVLO behavior during start-up:

1. The voltage at the supply terminal *VCC1* reaches the V_{UVLO1H} threshold
2. The gate driver IC reads the *ADJA* and *ADJB* resistor values and transfers the configuration to the output side
3. The IC releases the *RDYC* output to **high** and is ready to operate.

The start-up delay takes approx. 200 µs and is part of the complete start-up time t_{START1}.

UVLO behavior during shut-down:

- If the supply voltage V_{VCC1} of the input side drops below V_{UVLO1L} the *RDYC* signal is switched to **low** and the output will be switched off.

The fault signal *FLT_N* follows the input supply voltage.

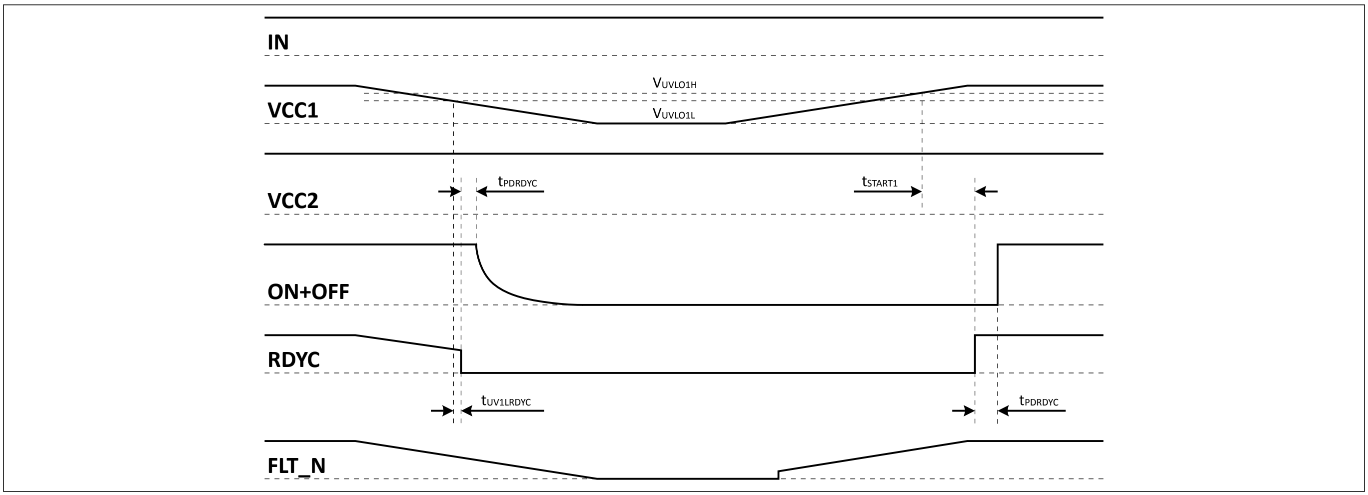

Figure 7 UVLO ***VCC1*** **behavior**

4.2.2 Output side under-voltage lockout, *VCC2* UVLO

To ensure correct operation of the output side and safe operation of the IGBT in the application, the gate driver IC is equipped with an output supply undervoltage lockout for *VCC2* versus *GND2*.

UVLO behavior during start-up:

- If the voltage at the supply terminal *VCC2* reaches the V_{UVLO2H} threshold the *RDYC* output is released to **high** and the gate driver IC is ready to operate.

The start-up delay takes approx. 200 µs and is part of the complete start-up time t_{START2}.

UVLO behavior during shut-down:

- If the supply voltage V_{VCC2} of the output side drops below V_{UVLO2L} the *RDYC* signal is switched to **low** and the output will be switched off.

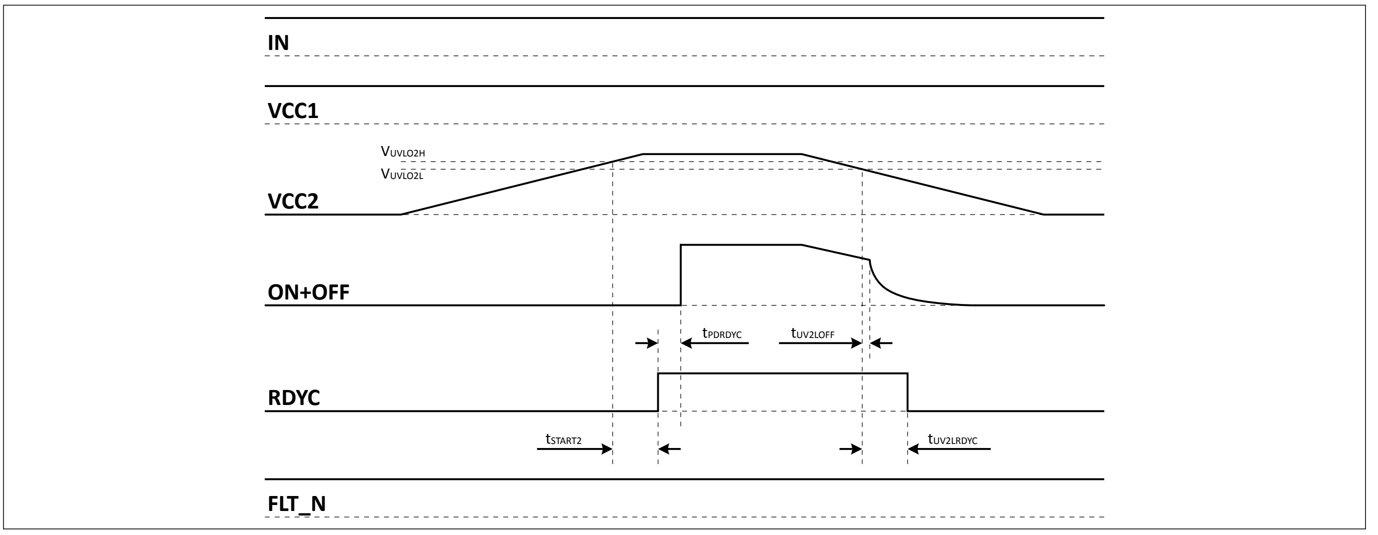

Figure 8 UVLO *VCC2* behavior

Any V_{UVLO2L} event will lead to a fault-off and a *RDYC* low level. Depending of the level of the voltage drop, the gate driver IC either stays in a not ready state and waits for the supply voltage to recover, or it will fully reset the gate driver IC. Both variants differ in the necessary delay of *RDYC* release after the supply voltage has recovered. After a reset, the gate driver IC needs to fully restart until it becomes ready again.

4.3 Input side logic

The input threshold levels are always CMOS compliant. The threshold levels are 30% of *VCC1* for low level and 70% of *VCC1* for high level.

The 1ED34x1Mc12M family (X3 Analog) has three input pins (*IN*, *ADJA*, *ADJB*) and two I/O pins (*RDYC*, *FLT_N*) at the input side.

4.3.1 IN non-inverting driver input

The input pin has a positive logic. To turn on the associated IGBT apply a logic high signal at the *IN* pin. A minimum pulse width of typical 103 ns is defined to make the IC robust against glitches at *IN*.

4.3.2 *RDYC* ready status output, fault-off and fault clear input

The *RDYC* pin is a logic input and open drain output and has three different functions:

- *RDYC* as ready status output of all ready sources
- *RDYC* as fault-off input
- *RDYC* as fault clear input

In a typical application the *RDYC* pins of all gate driver ICs in the inverter are connected together and form a single wire *RDYC* signal.

An external pull-up resistor is required to ensure *RDYC* status output during operation.

Ready sources

- the input side is properly supplied, *VCC1* supply above UVLO1 threshold
- the output side is properly supplied with a positive voltage, *VCC2* supply above UVLO2 threshold
- no *VEE2* over *GND2* failure
- Internal signal transmission is operating nominal
- the *ON* pin monitoring of the gate driver is below *VEE2* + 2 V, IGBT has to be off at start-up

4.3.2.1 *RDYC* fault-off input

Pulling *RDYC* to low disables the operation of the gate driver IC. The gate driver IC ignores *IN* signals as long as the *RDYC* pin stays low and the IC uses its fault-off function to switch-off the IGBT.

The defined minimum pulse width makes the IC robust against glitches at *RDYC*. The gate driver ignores pulses with a shorter duration.

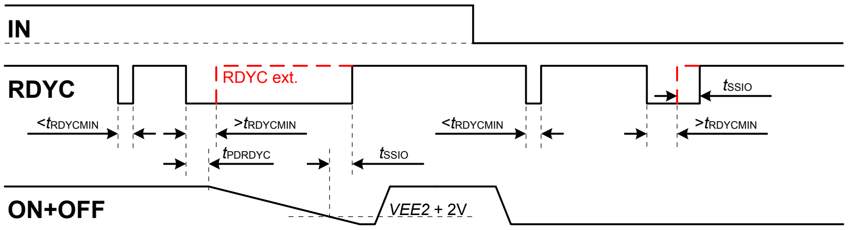

Figure 9 ***RDYC* short pulse behavior of external manipulation of the *RDYC* pin**

After an external *RDYC* low signal the IC is actively pulling *RDYC* to low until the voltage at *ON* pin falls below the *VEE2*+2 V threshold.

The *RDYC* fault-off input is active low.

4.3.2.2 *RDYC* fault clear input

Setting *RDYC* to low for longer than the fault clear time t_{CLRMIN} will reset the stored fault signal at pin *FLT_N* with the rising edge of *RDYC*. Additionally the following conditions have to be met as well:

- PWM *IN* pin level needs to be low,
- voltage at *ON* pin has dropped below the *VEE2*+2 V threshold, and
- triggering fault condition is no longer present.

The typical fault clear time t_{CLRMIN} is 1.0 µs.

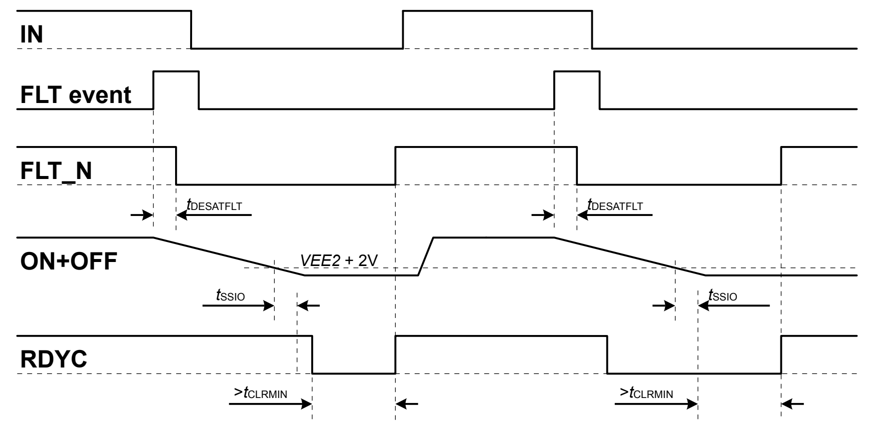

Figure 10 *RDYC* **fault clear timing**

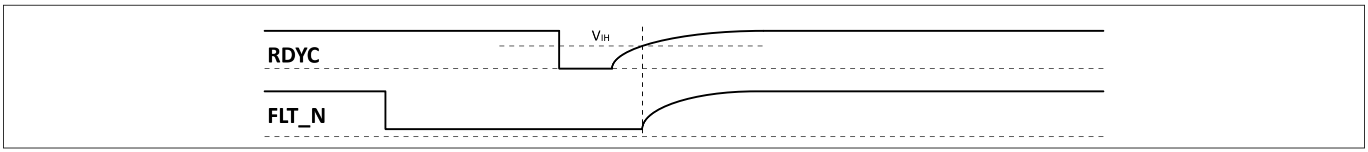

Figure 11 *RDYC* **fault clear rising edge to** ***FLT_N***

4.3.3 *FLT_N* status output and fault-off input

The *FLT_N* pin is a logic input and open drain output and has two different functions:

- *FLT_N* as fault-status output for fault sources
- *FLT_N* as fault-off input

In a typical application the *FLT_N* pins of all gate driver ICs in the inverter are connected together and form a single wire *FLT_N* signal.

An external pull-up-resistor is required to ensure *FLT_N* status output during operation.

Fault sources

The following fault sources can trigger a *FLT_N* pin to low and initiate a fault turn-off:

- desaturation detection of IGBT
- gate driver over temperature protection

4.3.3.1 *FLT_N* fault-off input

Pulling *FLT_N* to low disables the operation of the gate driver IC. The gate driver IC ignores *IN* signals as long as the *FLT_N* pin stays low and the IC uses its fault-off function to switch-off the IGBT.

The defined minimum pulse width makes the gate driver IC robust against glitches at *FLT_N*.

After a low at the *FLT_N* pin either internally or externally applied, the fault event is latched until cleared.

The *FLT_N* fault-off input is active low.

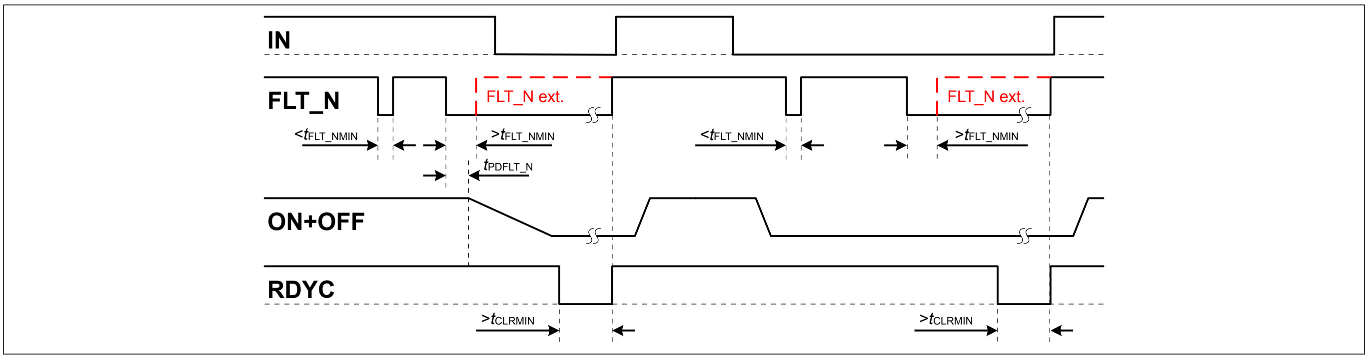

Figure 12 ***FLT_N*** **short pulse behavior of external manipulation of the** ***FLT_N*** **pin cleared by** ***RDYC***

4.4 Desaturation protection

The desaturation detection circuit protects the external IGBT from destruction at a short circuit. The desaturation protection follows the given sequence:

1. Voltage at *DESAT* pin reaches DESAT threshold level, for a period of time exceeding the filter time
2. Gate driver IC output switches the external IGBT off, using the soft-off method
3. Gate driver IC switches *FLT_N* pin to low to indicate the fault to a connected microcontroller
4. Short circuit situation is resolved
    - after the voltage at the *ON* pin has dropped below the *VEE2*+2 V threshold,
    - no other fault condition is present,
    - the input has been turned off and
    - the fault has been cleared using the RDYC low cycle method

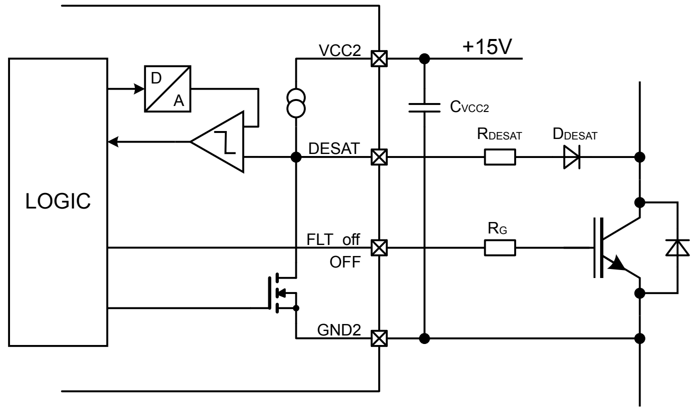

Figure 13 **DESAT circuit (only relevant pins shown)**

The 1ED34x1Mc12M family (X3 Analog) has a fixed DESAT threshold level of typical 9.18 V. If lower threshold levels are required, the DESAT resistor can be increased. Larger DESAT resistor values lead to lower DESAT threshold voltages. The threshold voltage reduction is equal to the DESAT current multiplied by the DESAT resistance.

The high-precision internal current source results in a minimum impact on the DESAT detection variation.

4.4.1 DESAT behavior

The DESAT function offers a leading edge blanking time and filters to optimize the DESAT detection for application usage.

The leading edge blanking inhibits threshold detection during an IGBT turn on phase. The typical IGBT turn on behavior starts with charging of the gate, commutation of the application load current and finally V_{CE} voltage decrease to V_{CEsat} voltage levels. To prevent the gate driver IC from detecting a false DESAT event, leading edge blanking pauses the DESAT circuit until the time $t_{DESATleb}$ has elapsed.

Following the leading edge blanking time, the gate driver IC forces the DESAT current into the external DESAT circuit. The current typically flows through a protection resistor, a fast high voltage diode and the collector-emitter path of the IGBT. The resulting voltage at the *DESAT* pin is the sum of the voltage drop across this path.

During a short circuit condition, the V_{CE} voltage increases, resulting in a reverse polarity condition of the DESAT diode. The remaining DESAT current also increases the voltage level at the *DESAT* pin and triggers the DESAT threshold. If the pin voltage level stays above the threshold for the duration of the DESAT filter time $t_{DESATfilter}$, the gate driver IC registers the DESAT event and acts accordingly.

The internal processing time after DESAT threshold crossing, filtering and beginning of fault-off is defined as $t_{DESATOUT}$. The duration of the gate discharge during fault-off is defined as $t_{FLTOFFtot}$ and is depending on the soft-off function and the gate load.

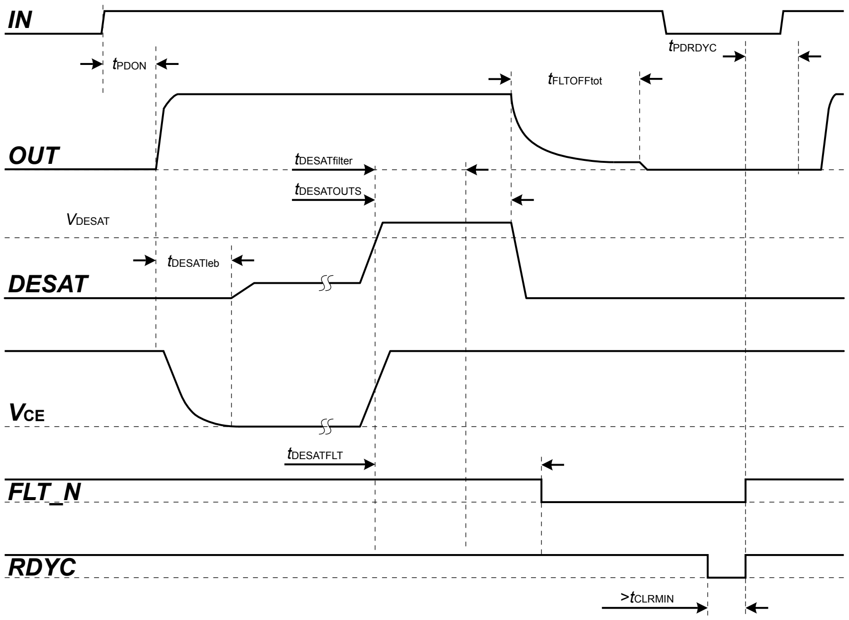

Figure 14 DESAT timing with leading edge blanking, filter and reaction times

4.4.2 DESAT filter and leading edge blanking time adjustment with *ADJB*

The *ADJB* pin configures the DESAT leading edge blanking time and DESAT filter time:

- A resistor from *ADJB* to *GND1* sets the DESAT leading edge blanking time and the DESAT filter time used during DESAT detection
- Use resistors from the E96 resistor-series with 1% tolerance values to achieve accurate parameter configuration
- The gate driver IC reads the resistor value once during start-up
- Connecting *ADJB* to *GND1* inhibits the gate driver operation and stops the start-up sequence
- Connecting *ADJB* to *VCC1* disables the filtering resulting in minimum response times

Table 4 DESAT filter timing ADJB adjustment

DESAT filter time set up	stopped	0	1	2	3	4	5	6	7
Resistance at *ADJB* to *GND1*	< 1.05 kΩ or tied to *GND1*	1.33 kΩ	1.58 kΩ	1.91 kΩ	2.26 kΩ	2.74 kΩ	3.32 kΩ	4.02 kΩ	4.87 kΩ
typ. $t_{DESATleb}$	inhibit gate driver operation	650 ns	650 ns	650 ns	650 ns	650 ns	650 ns	650 ns	650 ns
typ. $t_{DESATfilter}$		1575 ns	1775 ns	1975 ns	2375 ns	2775 ns	3175 ns	3575 ns	3975 ns

Table 4 **DESAT filter timing ADJB adjustment**

DESAT filter time set up	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**default**
Resistance at *ADJB* to *GND1*	5.90 kΩ	7.15 kΩ	8.66 kΩ	10.7 kΩ	13.7 kΩ	17.4 kΩ	23.2 kΩ	28.0 kΩ	>45.3 kΩ or tied to *VCC1*
typ. t_{DESATleb}	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	400 ns
typ. $t_{\mathrm{DESATfilter}}$	3975 ns	3575 ns	3175 ns	2775 ns	2375 ns	1975 ns	1775 ns	1575 ns	*225* ns

4.5 Gate driver output

The gate driver output side uses MOSFETs to provide a rail-to-rail output. Therefore, the gate drive voltage follows the supply voltage closely.

Due to the low internal voltage drop, the switching behavior of the IGBT is predominantly governed by the external gate resistor. The gate driver IC offers separate sink and source outputs to adapt the gate resistor for turn-on and turn-off separately without additional bypass components.

The cell value x in the following table is placeholder for high or low and indicates that this pin does not influence the resulting gate driver output state. The arrow (→) in cells indicate the transition initiated by the pin of the logic input and gate driver supply pins resulting in a transition to the gate driver output state as listed.

Table 5 Driver output state including transition behavior

Logic input and gate driver supply					**Gate driver output**	
IN	***RDYC***	***FLT_N***	***VCC1***	***VCC2***	***ON***	***OFF***
Static gate driver output state: on and off						
high	high	high	high	high	high	tri-state
low	high	high	high	high	tri-state	low
Transition to not ready and static not ready state						
x	high → low	high	high	high	→ tri-state	→ fault off
x	low	high	high	high	tri-state	low
Transition to fault and static fault state						
x	high	high → low	high	high	→ tri-state	→ fault off
x	high	low	high	high	tri-state	low
Transition with VCC1 power loss and unsupplied input side						
x	x	x	high → low	high	→ tri-state	→ fault off
x	x	x	low	high	tri-state	low
Transition with VCC2 power loss and unsupplied output side						
x	x	x	x	high → low	→ tri-state	→ fault off
x	x	x	x	low	tri-state	active shut down

4.5.1 Turn-on behavior

The 1ED34x1Mc12M family (X3 Analog) is optimized for hard switching turn-on. A turn-on command switches the *ON* pin internally to *VCC2*.

4.5.2 Turn-off and fault turn-off behavior

The gate driver IC supports different turn-off sequences to adapt to different applications and IGBT currents during normal switching operation and in the case of a fault.

Table 6 Turn-off sequences

Turn-off reason	**Turn-off sequence**		**Remark**
	Hard switching	**Soft turn-off**	
normal off	X		
fault turn-off		X	adjustable via *ADJA*

The gate driver fault turn-off behavior can be configured with the *ADJA* pin

Once started, the fault turn-off sequence cannot be interrupted by an *IN* = low turn-off signal.

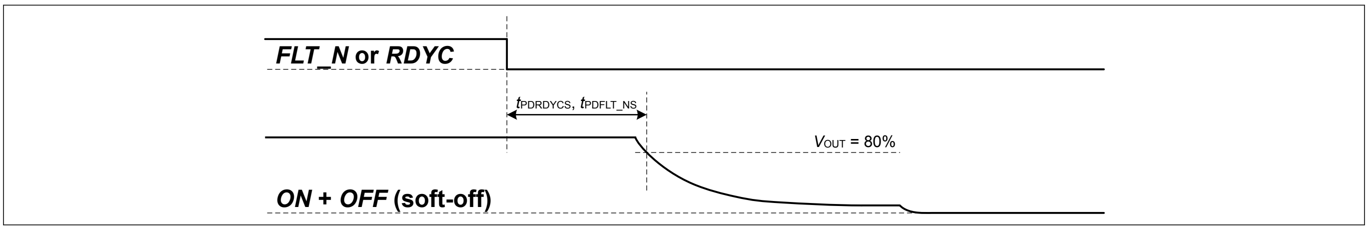

Figure 15 Fault turn-off sequence initiated by *FLT_N* or *RDYC*

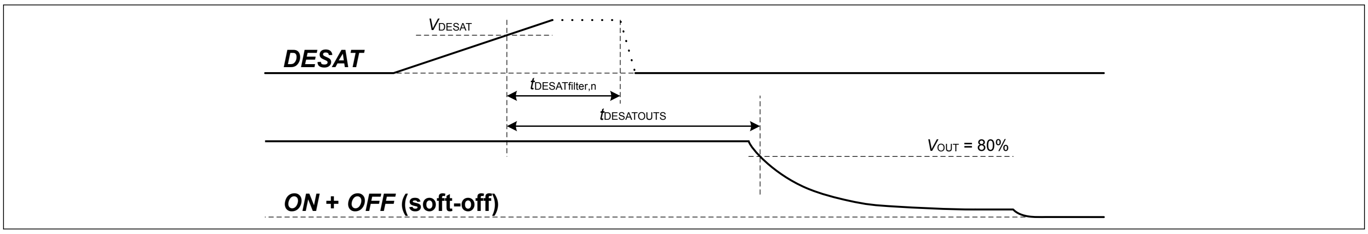

Figure 16 Fault turn-off sequence initiated by DESAT event

4.5.2.1 Hard switching turn-off

The gate driver IC supports hard switching turn-off during normal switching operation. Switching the IGBT gate off by turning on the discharge MOSFET in the output stage, the *OFF* pin is switched to *VEE2* pin.

4.5.2.2 Soft turn-off

The soft turn-off function protects the IGBT against collector-emitter overvoltage during turn off in an overcurrent condition. It turns-off the IGBT with a reduced gate current to reduce the d*i*/d*t* induced overvoltage..

The IGBT gate is connected via *OFF* to an internal current sink circuit. The discharge current is typically lower than the hard switch-off current used for normal operation. Since soft turn-off is a single event after a failure, the gate driver IC can handle the additional power dissipation internally.

Soft turn-off can be configured with the *ADJA* pin. The function is only active during fault turn-off.

The adjustable range depends on the current strength of the gate driver IC:

- 1ED3431M: 15 mA - 233 mA
- 1ED3461M: 29 mA - 466 mA
- 1ED3491M: 44 mA - 699 mA

4.5.2.2.1 Soft-off current source adjustment with *ADJA*

The *ADJA* pin configures the Soft-off function and current level:

- A resistor from *ADJA* pin to *GND1* sets the Soft-off current level for the fault-off function
- Use resistors from the E96 resistor-series with 1% tolerance values to achieve accurate parameter configuration
- The gate driver IC reads the resistor value once during start-up
- Connecting *ADJA* to *GND1* results in a Soft-off function for fault-off with a predefined value
- Connecting *ADJA* to *VCC1* inhibits the gate driver operation and stops the start-up sequence

Table 7 **Soft-off adjustment with *ADJA***

Soft-off set up	**default**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Resistance from *ADJA* to *GND1*	< 1.05 kΩ or tied to *GND1*	1.33 kΩ	1.58 kΩ	1.91 kΩ	2.26 kΩ	2.74 kΩ	3.32 kΩ	4.02 kΩ	4.87 kΩ
typ. I_{CSOFF} 1ED3431M	146 mA	15 mA	29 mA	44 mA	58 mA	73 mA	87 mA	102 mA	116 mA
typ. I_{CSOFF} 1ED3461M	291 mA	29 mA	58 mA	87 mA	116 mA	146 mA	175 mA	204 mA	233 mA
typ. I_{CSOFF} 1ED3491M	437 mA	44 mA	87 mA	131 mA	175 mA	218 mA	262 mA	306 mA	349 mA

Table 7 **Soft-off adjustment with *ADJA***

Soft-off set up	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**stopped**
Resistance from *ADJA* to *GND1*	5.90 kΩ	7.15 kΩ	8.66 kΩ	10.7 kΩ	13.7 kΩ	17.4 kΩ	23.2 kΩ	28.0 kΩ	>45.3 kΩ or tied to *VCC1*
typ. I_{CSOFF} 1ED3431M	131 mA	146 mA	160 mA	175 mA	189 mA	204 mA	218 mA	233 mA	inhibit gate driver operation
typ. I_{CSOFF} 1ED3461M	262 mA	291 mA	320 mA	349 mA	379 mA	408 mA	437 mA	466 mA	
typ. I_{CSOFF} 1ED3491M	393 mA	437 mA	480 mA	524 mA	568 mA	612 mA	655 mA	699 mA	

4.5.3 Active shut-down

The active shut-down feature ensures a safe IGBT off-state, if the output chip is not supplied. It protects the IGBT against a floating gate. The IGBT gate is always clamped via *OFF* to *VEE2*.

4.5.4 Active Miller clamp

The 1ED34x1Mc12M family (X3 Analog) is equipped with an active Miller clamp function to protect the IGBT from parasitic turn-on in fast switching applications.

After a turn-off command the gate driver IC follows the implemented sequence:

1. Discharge of the IGBT gate while monitoring the voltage level at the *ON* pin
2. Detection of a voltage at the *ON* pin less than a level of *VEE2* + 2.0 V
3. Filtering of the detection to avoid false CLAMP activation and not to influence regular turn-off behavior
4. Activating clamp function to keep IGBT gate at *VEE2* level

4.5.4.1 CLAMP output types

The CLAMP output stage offers two operating modes:

- direct gate clamping with an open drain output for medium clamping current, 1ED3431M variants
- pre-driver output, to clamp IGBT gate with external transistor for high clamping current, 1ED3461M and 1ED3491M variants

Direct gate clamping

Direct gate clamping with an open drain output is tailored for direct clamping of IGBT gate to *VEE2*. The output current capability is typically 2 A. Useful IGBT current rating for direct gate clamping is a collector current of typically smaller than 100 A. Connect the *CLAMP* pin directly to the gate with low inductive tracks.

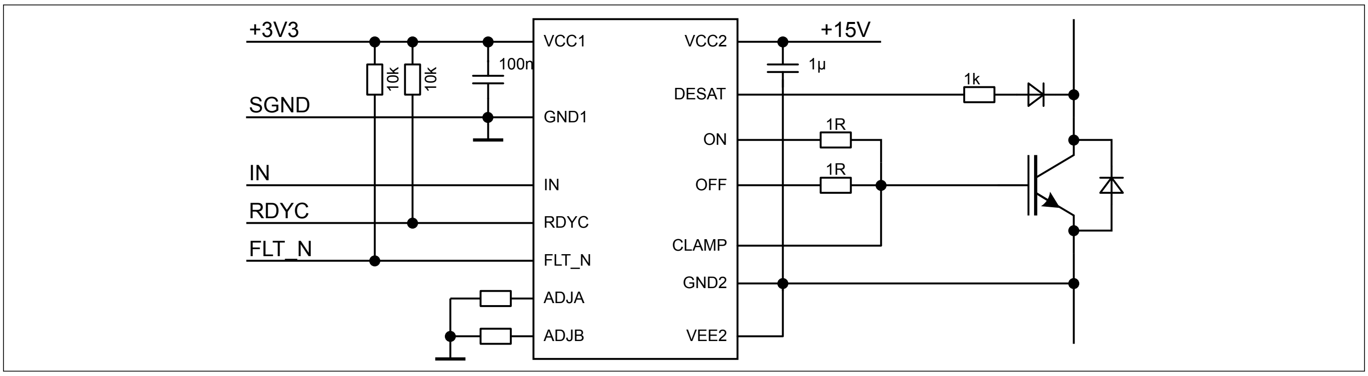

Figure 17 **Application example with unipolar supply (1ED3431M)**

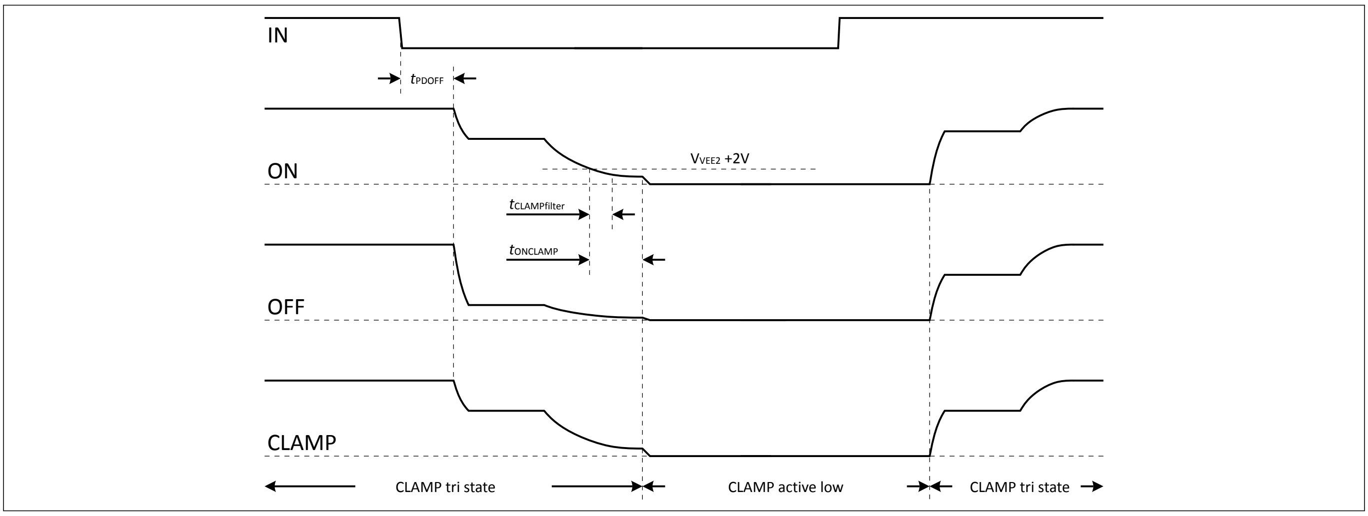

Figure 18 **Direct clamp output behavior**

Pre-driver output

Track inductance and clamp output resistance reduces the clamping capability for large IGBTs. In this case, select the pre-driver output product variant with an external MOSFET.

The external small signal n-channel MOSFET transistor in combination with the pre-driver output enables clamping of high gate currents. Connect the MOSFET between the *CLAMPDRV* output, *VEE2* pin, and IGBT gate. Due to the pre-driver configuration the clamp current is only limited by the external clamp MOSFET transistor. Depending on the external MOSFET a Miller current clamping up to 20 A can be reached. The clamping MOSFET has to be placed close to the IGBT gate to minimize track resistance and inductance.

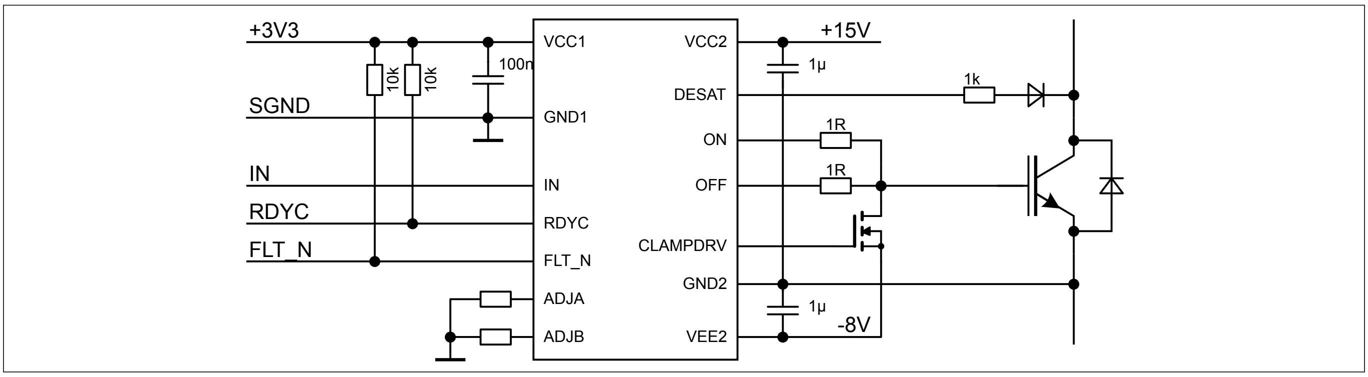

Figure 19 **Application example with bipolar supply and CLAMP pre-driver output (1ED3461M, 1ED3491M)**

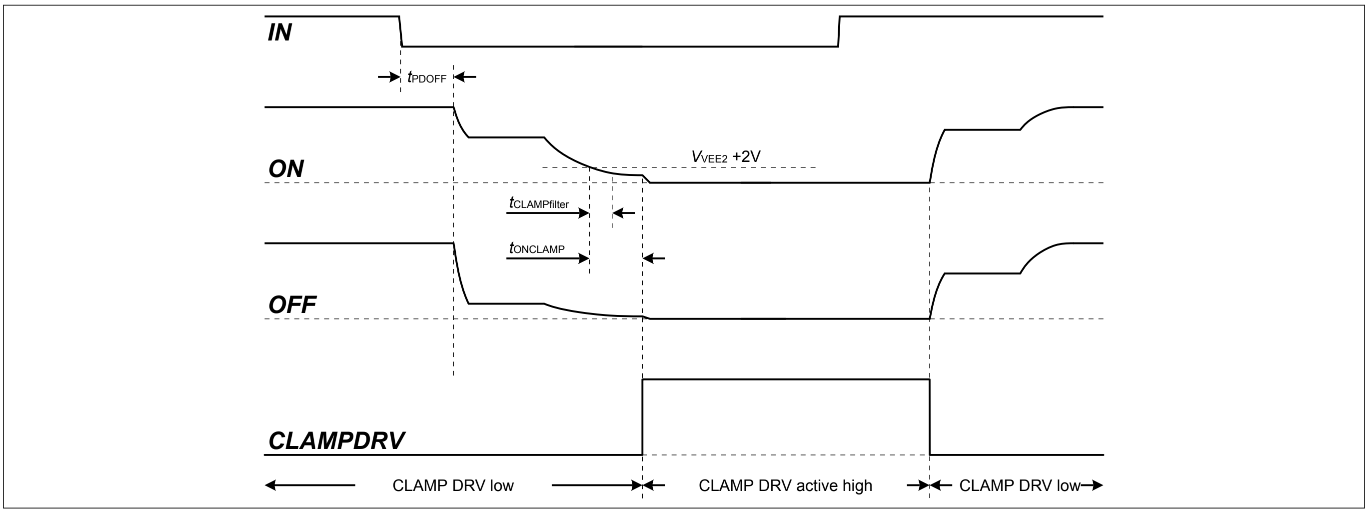

Figure 20 **Clamp pre-driver output behavior**

4.5.5 Switch-off timeout until forced switch-off

The gate driver IC is equipped with a switch-off timeout monitoring feature. In case the pin monitoring comparator has not registered an off-state within the timeout time this feature activates a forced switch-off.

The monitoring feature secures the IGBT switch-off in case of a connection failure between the *OFF* output and the IGBT gate or a faulty gate resistor. In a forced switch-off all available output switch-off paths (*OFF* and *CLAMP*/*CLAMPDRV*) will be used to hard switch-off the IGBT after such an event.

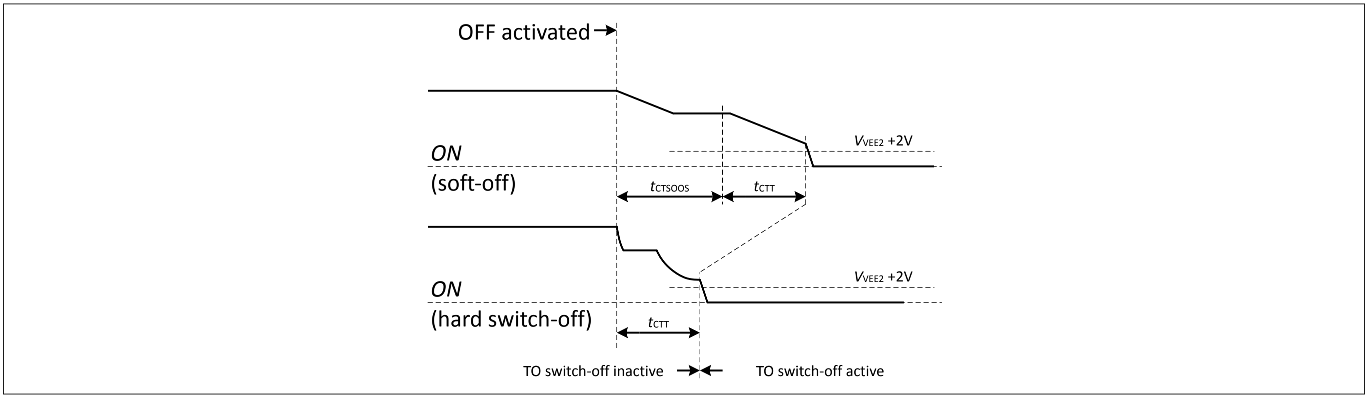

Figure 21 **Switch-off timeout behavior**

The timing diagram shows the switch-off timeout behavior from the moment of *OFF* output activation until the timeout has elapsed and the *CLAMP* output is activated.

4.6 Short circuit clamping

The integrated short circuit clamping diode limits the IGBT gate over voltage during a short circuit. The over voltage is typically triggered by the capacitive feedback of the Miller capacitance.

The internal diodes from *ON* and *CLAMP* to *VCC2* limit the gate driver voltage to a value slightly higher than the supply voltage. These diode paths are rated for a maximum current of 0.75 A and the duration of 6 µs. Add an external Schottky diode if higher currents are expected or a tighter clamping is desired. Also use an external diode if the active Miller clamping circuit uses the pre-driver output configuration.

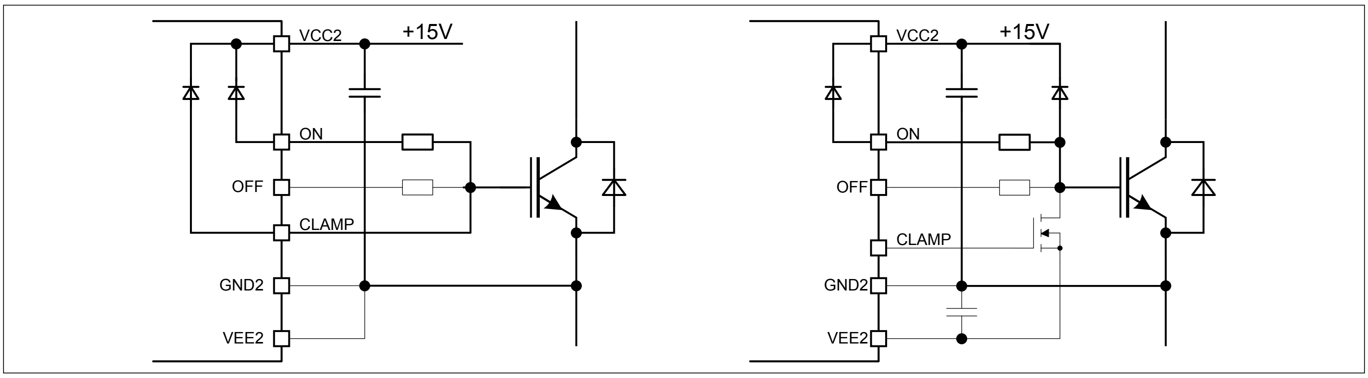

Figure 22 Short circuit clamping circuitry

5 Electrical parameters

5.1 Absolute maximum ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 1 to 8, GND2 for pins 9 to 16).

Table 8 Absolute maximum ratings

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input to output offset voltage	V_{OFFSET}	–	2300	V	$V_{VEE2,max}$-$V_{VEE2,min}$ with $V_{VEE2,max} \geq V_{GND1} \geq V_{VEE2,min}$ 1) 2)
Supply voltage input side	V_{VCC1}	-0.3	6.5	V	–
Logic input voltage (*IN*)	$V_{LogicIN}$	-0.3	6.5	V	–
Logic input voltage (*RDYC*, *FLT_N*)	$V_{LogicRF}$	-0.3	6.5	V	–
Logic input voltage (*ADJA*, *ADJB*)	$V_{LogicAD}$	-0.3	6.5	V	–
Open drain logic output current (*RDYC*, *FLT_N*)	$I_{LogicOC}$	–	10	mA	–
Positive supply voltage output side	V_{VCC2}	-0.3	40	V	–
Negative supply voltage output side	V_{VEE2}	-40	0.3	V	–
Maximum supply voltage difference output side (V_{VCC2} - V_{VEE2})	V_{max2}	–	40	V	–
DESAT input voltage	V_{DESAT}	-0.3	V_{VCC2} +0.3	V	–
CLAMP input voltage	V_{CLAMP}	V_{VEE2} -0.3	V_{VCC2} +0.3	V	3)
Maximum *CLAMP* output current	I_{CLAMP}	–	2.4	A	$t < 5$ µs
Gate driver output voltage (*ON*, *OFF*)	V_{OUT}	V_{VEE2} -0.3	V_{max2} +0.3	V	–
Maximum *CLAMP* to *VCC2* diode IGBT short circuit clamping time	t_{CLP}	–	6	µs	$I_{CLAMP/OUT}$ = 0.75 A
Junction temperature	T_J	-40	150	°C	–
Storage temperature	T_{Stg}	-55	150	°C	–
Power dissipation, input side	$P_{D,IN}$	–	100	mW	@T_A = 25 °C
Power dissipation, output side	$P_{D,OUT}$	–	700	mW	@T_A = 25°C 4)
ESD capability: Human body model	V_{ESDHBM}	–	2	kV	5)
ESD capability: Charged device model	V_{ESDCDM}	–	500	V	6)

1) for functional operation only
2) See also Chapter 6 on page 41
3) May be exceeded during short circuit clamping.
4) Derating the power above 65°C with 8 mW/°C

[5] According to ANSI/ESDA/JEDEC-JS-001-2017 (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).

[6] According to ANSI/ESDA/JEDEC-JS-002-2014 (TC = test condition in volt)

5.2 Thermal parameters

Thermal performance may change significantly with layout and heat dissipation of components in close proximity.

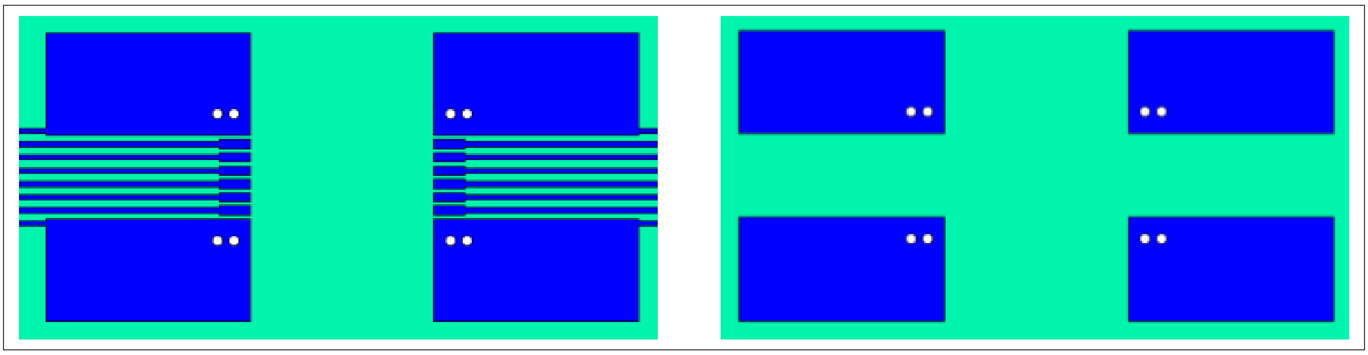

Figure 23 **Reference layout for thermal data (Two layer PCB; copper thickness 35 µm; left: top layer; right: bottom layer)**

The PCB layout represents the reference layout used for the thermal characterization. Pins 1 and 8 (*GND1*) and pins 9 and 16 (*VEE2*) require ground plane connections for achieving maximum power dissipation. The 1ED34x1Mc12M family (X3 Analog) is conceived to dissipate most of the heat generated through these pins.

Table 9 **Thermal parameters**

Parameter	Symbol	Value	Unit	Note / Test Condition
Thermal resistance junction to ambient	$R_{\mathrm{THJA,OUT}}$	122	K/W	@T_A = 65°C, $P_{\mathrm{D,\,OUT}}$ = 400 mW, $P_{\mathrm{D,\,IN}}$ = 50 mW, 4 layer test PCB, PG-DSO-16
Characterization parameter junction to package top input side	Ψ_{Jtop}	8	K/W	

5.3 Operating parameters

Note: *Within the operating range the IC operates as described in the functional description. Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 1 to 8, GND2 for pins 9 to 16).*

Table 10 **Operating parameters**

Parameter[1]	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Supply voltage input side	V_{VCC1}	3.0	5.5	V	–
Logic input voltages (*IN*, *RDYC*, *FLT_N*)	V_{LogicIN}	-0.3	5.5	V	–
Positive supply voltage output side	V_{VCC2}	13	25	V	–
Negative supply voltage output side	V_{VEE2}	-25	0	V	–

(table continues...)

Table 10 (continued) Operating parameters

Parameter[1]	**Symbol**	**Values**		**Unit**	**Note / Test Condition**
		Min.	**Max.**		
Supply voltage difference output side (V_{VCC2} - V_{VEE2})	V_{max2}	13	35	V	–
Ambient temperature	T_A	-40	125	°C	[2]
Switching frequency	f_{SW}	0	250	kHz	max P_D applies
Common mode transient immunity	$\|CMTI\|$	0	200	V/ns	$V_{OFFSET,test}$ = 1500 V

1) Parameter is not subject to production test - verified by design/characterization

2) T_J has to be below over temperature protection temperature T_{OTPOFF}

5.4 Electrical characteristics

Note: The electrical characteristics include the spread of values in supply voltages, load, and junction temperatures within the operating parameters unless specified otherwise. Typical values represent the median values at T_A = 25°C. Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 1 to 8, GND2 for pins 9 to 16).

5.4.1 Voltage supply

Table 11 Voltage supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VCC1 UVLO threshold	V_{UVLO1H}	–	2.95	3.05	V	–
	V_{UVLO1L}	2.6	2.8	–	V	–
VCC1 UVLO hysteresis (V_{UVLO1H} - V_{UVLO1L})	V_{HYS1}	0.1	0.14	–	V	–
VCC1 quiescent current	I_{Q1}	–	2.4	4.0	mA	V_{VCC1} = 3.3 V, *IN* = High, *RDYC* = High, *FLT_N* = High
VCC1 operating current	I_{O1}	–	2.4	4.0	mA	V_{VCC1} = 3.3 V, *IN* = 16 kHz, 50%, *RDYC* = High, *FLT_N* = High
VCC2 UVLO threshold	$V_{UVLO2H,0}$	–	12.0	12.6	V	
	$V_{UVLO2L,0}$	10.4	11.0	–	V	
VCC2 UVLO hysteresis ($V_{UVLO2H,0}$ - $V_{UVLO2L,0}$)	$V_{HYS2,0}$	0.75	1.0	–	V	
VEE2 not connected detection threshold	$V_{VEE2,NC}$	–	0.5	–	V	V_{VEE2} - V_{GND2}
VCC2 quiescent current	I_{Q2}	–	3.9	5	mA	V_{VCC2} = 15 V, V_{VEE2} = -8 V, *OUT* = High, *DESAT* = Low
VCC2 operating current	I_{O2}	–	3.9	5	mA	V_{VCC2} = 15 V, V_{VEE2} = -8 V, *OUT* = 16 kHz, 50%, *DESAT* = Low, C_{LOAD} = 100 pF

5.4.2 Logic input and output

Table 12 **Logic input and output**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Logic low input voltage (*IN*, *RDYC*, *FLT_N*)	V_{LogicINL}	–	–	30	%	of V_{VCC1}
Logic high input voltage (*IN*, *RDYC*, *FLT_N*)	V_{LogicINH}	70	–	–	%	of V_{VCC1}
Logic low output voltage (*RDYC*, *FLT_N*)	V_{RDYC5}, $V_{\mathrm{FLT\_N5}}$	–	–	300	mV	I_{SINK} = 5 mA
Logic input pull down resistor (*IN*)	R_{INPD}	33	40	47	kΩ	–
Logic input pull down resistor (*RDYC*, *FLT_N*)	R_{RDYCPD}, $R_{\mathrm{FLT\_NPD}}$	0.8	1.0	1.2	MΩ	–

5.4.3 Analog input

Resistor values outside of the 1% tolerance range results in the gate driver IC selecting either the lower or higher step for the corresponding function.

Table 13 **Analog input**

Parameter1)	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Analog input resistor (*ADJA*, *ADJB*)	R_{ADJx0}	–	1.33	–	kΩ	all resistor values are from the E96-series with 1% tolerance
	R_{ADJx1}	–	1.58	–		
	R_{ADJx2}	–	1.91	–		
	R_{ADJx3}	–	2.26	–		
	R_{ADJx4}	–	2.74	–		
	R_{ADJx5}	–	3.32	–		
	R_{ADJx6}	–	4.02	–		
	R_{ADJx7}	–	4.87	–		
	R_{ADJx8}	–	5.90	–		
	R_{ADJx9}	–	7.15	–		
	R_{ADJx10}	–	8.66	–		
	R_{ADJx11}	–	10.7	–		
	R_{ADJx12}	–	13.7	–		
	R_{ADJx13}	–	17.4	–		
	R_{ADJx14}	–	23.2	–		
	R_{ADJx15}	–	28.0	–		

1) Parameter is not subject to production test - verified by design/characterization

5.4.4 Gate driver

Note: *High and low level output currents are absolute values without an information of current direction.*

Table 14 **Gate driver**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High level output voltage	V_{ON0}	–	V_{VCC2} + 0.87	V_{VCC2} + 1.01	V	I_{ON} = 500 mA[1]
High level output peak current 1ED3431M	I_{ON}	2.6	3.8	–	A	[2] [3] C_{LOAD} = 33 nF
High level output on resistance 1ED3431M	$R_{DSON,H}$	0.51	1.12	2.24	Ω	I_{ON} = 67 mA[3]
Low level output peak current 1ED3431M	I_{OFF}	2.0	2.5	–	A	[2] [4] C_{LOAD} = 33 nF
Low level ouput on resistance 1ED3431M	$R_{DSON,L}$	0.31	0.82	1.64	Ω	I_{OFF} = 67 mA[4]
High level output peak current 1ED3461M	I_{ON}	5.2	7.5	–	A	[2] [3] C_{LOAD} = 68 nF
High level output on resistance 1ED3461M	$R_{DSON,H}$	0.26	0.56	1.13	Ω	I_{ON} = 133 mA[3]
Low level output peak current 1ED3461M	I_{OFF}	4.0	5.0	–	A	[2] [4] C_{LOAD} = 68 nF
Low level ouput on resistance 1ED3461M	$R_{DSON,L}$	0.16	0.41	0.83	Ω	I_{OFF} = 133 mA[4]
High Level output peak current 1ED3491M	I_{ON}	7.9	11	–	A	[2] [3] C_{LOAD} = 100 nF
High level output on resistance 1ED3491M	$R_{DSON,H}$	0.17	0.38	0.75	Ω	I_{ON} = 200 mA[3]
Low Level output peak current 1ED3491M	I_{OFF}	6.0	7.5	–	A	[2] [4] C_{LOAD} = 100 nF
Low level ouput on resistance 1ED3491M	$R_{DSON,L}$	0.11	0.28	0.55	Ω	I_{OFF} = 200 mA[4]
Active Shut Down Voltage *OFF* 1ED3431M	V_{ACTSD}[5]	–	–	V_{VEE2} +2.4	V	I_{OUT} = 67 mA,V_{VCC2} open
Active Shut Down Voltage *OFF* 1ED3461M	V_{ACTSD}[5]	–	–	V_{VEE2} +2.4	V	I_{OUT} = 133 mA,V_{VCC2} open
Active Shut Down Voltage *OFF* 1ED3491M	V_{ACTSD}[5]	–	–	V_{VEE2} +2.4	V	I_{OUT} = 200 mA,V_{VCC2} open

1) Integrated diode *ON* vs. *VCC2* clamping test
2) Parameter is not subject to production test - verified by design/characterization
3) *IN* = High, *ON* = High; *VCC2-ON* = 15 V; R_G = 0.1 Ω; *VCC2* = 15 V; *VEE2* = -8 V
4) *IN* = Low, *OFF* = Low; *OFF-VEE2* = 15 V; R_G = 0.1 Ω; *VCC2* = 15 V; *VEE2* = -8 V

[5] With reference to *VEE2*

5.4.5 Active Miller clamp

Table 15 Active Miller clamp

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High level clamp voltage	$V_{CLAMPH0}$	–	V_{VCC2} +1.5	V_{VCC2} +1.63	V	I_{CLAMP} = 500 mA[1] [2]
	$V_{CLAMPH1}$	–	V_{VCC2} +0.9	V_{VCC2} +1.1	V	I_{CLAMP} = 50 mA[1] [2]
Clamp-driver high level output voltage (1ED3461M, 1ED3491M)	$V_{CLAMPDH1}$	V_{VEE2}+7.5	V_{VEE2}+9.5	V_{VEE2}+11.5	V	I_{CLAMPH} = 5 mA[3]
	$V_{CLAMPDH2}$	V_{VEE2}+4.5	V_{VEE2}+6.7	–	V	I_{CLAMPH} = 50 mA[3]
Clamp-driver high level output peak current (1ED3461M, 1ED3491M)	I_{CLAMPH}	0.20	0.27	–	A	[4] *VCC2* = 15 V; *VEE2* = 0 V; C_{CLAMP} = 100 nF; R_{CLAMP} = 1 Ω
Clamp/Clamp-driver output low level current	$I_{CLAMPL,2}$	1.1	1.8	–	A	[4] *VCC2* = 15 V; *VEE2* = 0 V; V_{CLAMP} = 2 V; C_{CLAMP} = 100 nF; R_{CLAMP} = 0.1 Ω
Clamp/Clamp-driver output low level current	$I_{CLAMPL,5}$	2.2	3.5	–	A	[4] *VCC2* = 15 V; *VEE2* = 0 V; V_{CLAMP} = 5 V; C_{CLAMP} = 100 nF; R_{CLAMP} = 0.1 Ω
Clamp/Clamp-driver output low level ON resistance	$R_{DSON,CLP}$	0.50	0.85	1.35	Ω	I_{CLAMPL} = 200 mA
Clamp threshold voltage	V_{ON_CLAMP}	1.5	2.0	2.5	V	Related to *VEE2*
Clamp filter time	$t_{CLAMPfilter}$	195	235	275	ns	
CLAMP reaction time in CLAMP mode	t_{CLAMP_ON}	16 + $t_{CLAMPfilter}$	23 + $t_{CLAMPfilter}$	35 + $t_{CLAMPfilter}$	ns	[4] [5] C_{LOAD} = 100 pF
CLAMP reaction time in CLAMP driver mode	t_{CLAMPD_ON}	24 + $t_{CLAMPfilter}$	35 + $t_{CLAMPfilter}$	53 + $t_{CLAMPfilter}$	ns	[4] [6] C_{LOAD} = 100 pF
Switch-off time-out time	t_{CTT}	–	2.4	–	µs	[4]
Switch-off time-out soft-off offset time	t_{CTSOOS}	–	2.4	–	µs	[4] additional time-out delay during soft-off

[1] Integrated diode *CLAMP* vs. *VCC2* clamping test

[2] only valid for direct clamping: *IN* = High, *OUT* = High

[3] only valid for clamp pre-driver output: *IN* = Low, *OUT* = Low

[4] Parameter is not subject to production test - verified by design/characterization

[5] CLAMP mode reaction time specified with 3.3 kΩ pull-up from *CLAMP* to 3.3 V, from CLAMP threshold until reaching 0.8 V (falling) at *CLAMP* pin

[6] CLAMP driver mode reaction time specified from CLAMP threshold until reaching 0.8 V (rising) at *CLAMP(DRV)* pin

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5.4.6 Dynamic characteristics

Dynamic characteristics are measured with V_{VCC1} = 5 V, V_{VCC2} = 15 V and V_{VEE2} = -8 V unless specified otherwise.

Table 16 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input pulse suppression time *IN*	t_{INMIN}	98	103	108	ns	–
Input pulse suppression time *RDYC*/*FLT_N* for enable / fault off	$t_{RDYCMIN}$, t_{FLT_NMIN}	85	100	115	ns	–
Input pulse width *RDYC* for *FLT_N* reset (Fault clear time)	t_{CLRMIN}	–	1.0	1.2	µs	
Input *IN* to output propagation delay *ON*	t_{PDON}	226	244	270	ns	C_{LOAD} = 100 pF, V_{IN} = 70%, V_{OUT}=20%
Input *IN* to output propagation delay *OFF*	t_{PDOFF}	218	236	262	ns	C_{LOAD} = 100 pF, V_{IN} = 30%, V_{OUT}=80%
Input to output propagation delay distortion (t_{PDOFF} - t_{PDON})	t_{PDISTO}	-23	-8	7	ns	C_{LOAD} = 100 pF
Input *IN* to output propagation delay distortion between any devices (t_{PDON}-t_{PDON}) or (t_{PDOFF}-t_{PDOFF})	t_{PDD}	–	–	30	ns	[1] same conditions (V_{IN}, V_{VCC1}, V_{VCC2} and V_{VEE2}, C_{LOAD}, T_A)
State synchronization time between input and output	t_{SSIO}	–	–	13	µs	[1]
Input *RDYC* to output on propagation delay	t_{PDRDYC}	447	523	600	ns	C_{LOAD} = 100 pF; *IN* high; V_{RDYC} = 70%, V_{OUT}=20%
Input *RDYC* or *FLT_N* to Soft-off output propagation delay	$t_{PDRDYCS}$, t_{PDFLT_NS}	323	361	407	ns	C_{LOAD} = 100 pF, V_{Signal} = 30%, V_{OUT}=80%, Soft-off function $I_{CSOFF,15}$
Input RDYC or FLT_N to hard switch-off output propagation delay	$t_{PDRDYCH}$, t_{PDFLT_NH}	303	342	384	ns	C_{LOAD} = 100 pF, V_{Signal} = 30%, V_{OUT}=80%, OFF function
Rise time 1ED3431M	t_{RISE}	–	15	30	ns	C_{LOAD} = 1 nF, V_{OUT}: 20% to 80%

(table continues...)

Table 16 (continued) Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Fall time 1ED3431M	t_{FALL}	–	15	30	ns	C_{LOAD} = 1 nF, V_{OUT}: 80% to 20%
Rise time 1ED3461M	t_{RISE}	–	15	30	ns	C_{LOAD} = 2.2 nF, V_{OUT}: 20% to 80%
Fall Time 1ED3461M	t_{FALL}	–	15	30	ns	C_{LOAD} = 2.2 nF, V_{OUT}: 80% to 20%
Rise Time 1ED3491M	t_{RISE}	–	15	30	ns	C_{LOAD} = 3.3 nF, V_{OUT}: 20% to 80%
Fall Time 1ED3491M	t_{FALL}	–	15	30	ns	C_{LOAD} = 3.3 nF, V_{OUT}: 80% to 20%

1) Parameter is not subject to production test - verified by design/characterization

5.4.7 Desaturation protection

All parameters valid for *VCC1* = 5 V, *VCC2* = 15 V, and *VEE2* = 0 V unless specified otherwise.

Table 17 Desaturation protection

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
DESAT charge current	I_{DESATC}	470	500	525	µA	V_{DESAT} = 0 V
DESAT voltage divider resistance	R_{DVD}	259	312.5	366	kΩ	between *DESAT* and *GND2* pins
DESAT clamp and discharge ON resistance	$R_{DSON,D}$	–	7.7	25.0	Ω	I_{DESATD} = 200 mA
DESAT threshold level	V_{DESAT}	8.88	9.18	9.48	V	–
DESAT leading edge blanking time	$t_{DESATleb,d}$	356	400	444	ns	*ADJB* depending, V_{ON} 20% rising to V_{DESAT} = 1 V, C_{LOAD} = 100 pF, C_{DESAT} = 2 pF,
	$t_{DESATleb,s}$	597	650	703	ns	
	$t_{DESATleb,l}$	1077	1150	1223	ns	
DESAT filter time (default)	$t_{DESATfilter,def}$	190	*225*	263	ns	*ADJB* = *VCC1*
DESAT filter time (*ADJB* adjustable)	$t_{DESATfilter,A}$	1476	1575	1684	ns	*ADJB* depending
	$t_{DESATfilter,B}$	1667	1775	1895	ns	
	$t_{DESATfilter,C}$	1857	1975	2105	ns	
	$t_{DESATfilter,D}$	2238	2375	2526	ns	
	$t_{DESATfilter,E}$	2619	2775	2947	ns	
	$t_{DESATfilter,F}$	3000	3175	3368	ns	

(table continues...)

Table 17 (continued) Desaturation protection

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
	$t_{DESATfilter,G}$	3381	3575	3789	ns	
	$t_{DESATfilter,H}$	3762	3975	4211	ns	
DESAT sense to *FLT_N* low delay	$t_{DESATFLT}$	623	743	883	ns	V_{FLT_N} = 30%, I_{FLT_N} = 5 mA, $t_{DESATfilter,def}$, C_{FLT_N} = 100 pF
DESAT sense to *OFF* low delay, Soft-off	$t_{DESATOUTS}$	287 + $t_{DESATfilter}$	333 + $t_{DESATfilter}$	382 + $t_{DESATfilter}$	ns	V_{OUT} = 80%, C_{LOAD} = 100 pF, $I_{CSOFF,15}$

5.4.8 Soft-off current source

Soft-off current source values specified at *OFF* pin at V_{OFF} = 3 V with unipolar supply of V_{VCC2} = 15 V.

Table 18 **Current source turn-off**

Parameter	**Symbol**	**Values**			**Unit**	**Note or Test Condition**
		Min.	**Typ.**	**Max.**		
Soft-off current source current 1ED3431M	$I_{CSOFF,0}$	10	15	19	mA	depends on resistor value at *ADJA*
	$I_{CSOFF,1}$	24	29	36	mA	
	$I_{CSOFF,2}$	35	44	52	mA	
	$I_{CSOFF,3}$	47	58	70	mA	
	$I_{CSOFF,4}$	58	73	87	mA	
	I_{CSOFF5}	70	87	105	mA	
	$I_{CSOFF,6}$	82	102	122	mA	
	$I_{CSOFF,7}$	93	116	140	mA	
	$I_{CSOFF,8}$	105	131	157	mA	
	$I_{CSOFF,9}$	116	146	175	mA	
	$I_{CSOFF,10}$	128	160	192	mA	
	$I_{CSOFF,11}$	140	175	210	mA	
	$I_{CSOFF,12}$	151	189	227	mA	
	$I_{CSOFF,13}$	163	204	245	mA	
	$I_{CSOFF,14}$	175	218	262	mA	
	$I_{CSOFF,15}$	186	233	280	mA	
Soft-off current source current 1ED3461M	$I_{CSOFF,0}$	22	29	36	mA	depends on resistor value at *ADJA*
	$I_{CSOFF,1}$	45	58	72	mA	
	$I_{CSOFF,2}$	70	87	105	mA	
	$I_{CSOFF,3}$	93	116	140	mA	
	$I_{CSOFF,4}$	116	146	175	mA	
	$I_{CSOFF,5}$	140	175	210	mA	
	$I_{CSOFF,6}$	163	204	245	mA	
	$I_{CSOFF,7}$	186	233	280	mA	
	$I_{CSOFF,8}$	210	262	314	mA	
	$I_{CSOFF,9}$	233	291	349	mA	
	$I_{CSOFF,10}$	256	320	384	mA	
	$I_{CSOFF,11}$	280	349	419	mA	
	$I_{CSOFF,12}$	303	379	454	mA	
	$I_{CSOFF,13}$	326	408	489	mA	
	$I_{CSOFF,14}$	349	437	524	mA	

(table continues...)

Table 18 (continued) Current source turn-off

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
	$I_{CSOFF,15}$	373	466	559	mA	
Soft-off current source current 1ED3491M	$I_{CSOFF,0}$	34	44	54	mA	depends on resistor value at *ADJA*
	$I_{CSOFF,1}$	70	87	105	mA	
	$I_{CSOFF,2}$	105	131	157	mA	
	$I_{CSOFF,3}$	140	175	210	mA	
	$I_{CSOFF,4}$	175	218	262	mA	
	$I_{CSOFF,5}$	210	262	314	mA	
	$I_{CSOFF,6}$	245	306	367	mA	
	$I_{CSOFF,7}$	280	349	419	mA	
	$I_{CSOFF,8}$	314	393	472	mA	
	$I_{CSOFF,9}$	349	437	524	mA	
	$I_{CSOFF,10}$	384	480	577	mA	
	$I_{CSOFF,11}$	419	524	629	mA	
	$I_{CSOFF,12}$	454	568	681	mA	
	$I_{CSOFF,13}$	489	612	734	mA	
	$I_{CSOFF,14}$	524	655	786	mA	
	$I_{CSOFF,15}$	559	699	839	mA	

5.4.9 Over-temperature protection

Table 19 Over-temperature protection

Parameter[1]	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Over-temperature protection level	T_{OTPOFF}	150	160	170	°C	

[1] Parameter is not subject to production test - verified by design/characterization

6 Insulation characteristics

The following isolation classes are available for the 1ED34x1Mc12M family (X3 Analog).

Table 20 Product isolation classes

Product name	Marking	Insulation characteristics	Values specified in	UL values
1ED34x1MU12M	34x1MU12	UL 1577 certified insulation	-	Table 23
1ED34x1MC12M	34x1MC12	Reinforced insulation	Table 22	Table 23

Table 21 Safety limiting values

This coupler is suitable for rated insulation only within the given safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Description	Symbol	Characteristic	Unit
Maximum ambient safety temperature	T_S	150	°C
Maximum input-side power dissipation at $T_A = 25°C$	P_{SI}	100	mW
Maximum output-side power dissipation at $T_A = 25°C$ [1]	P_{SO}	1000	mW
Maximum driver output current (*ON*, *OFF*) [2] 1ED3431MC 1ED3461MC 1ED3491MC	I_{OUT}	 2.4 4.8 7.2	A

[1] IC output-side power dissipation is derated linearly at 8 mW/°C above 65 °C

[2] Maximum pulse length of $t = 5$ µs

6.1 Certified according to VDE 0884-11 reinforced insulation (Certificate no. 40053980)

Valid for parts with part name 1ED34x1MC12M, x indicate different variants.

This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 22 Reinforced insulation according to VDE 0884-11

Description	Symbol	Characteristic	Unit
Installation classification per EN 60664-1, Table 1 for rated mains voltage ≤ 150 V (rms) for rated mains voltage ≤ 300 V (rms) for rated mains voltage ≤ 600 V (rms) for rated mains voltage ≤1000 V (rms)		 I-IV I-IV I-III I-II	–
Climatic classification		40/125/21	–
Pollution degree (EN 60664-1)		2	–
Minimum external clearance	*CLR*	>8	mm
Minimum external creepage	*CPG*	>8	mm
Minimum comparative tracking index	*CTI*	400	–

(table continues...)

Table 22 (continued) Reinforced insulation according to VDE 0884-11

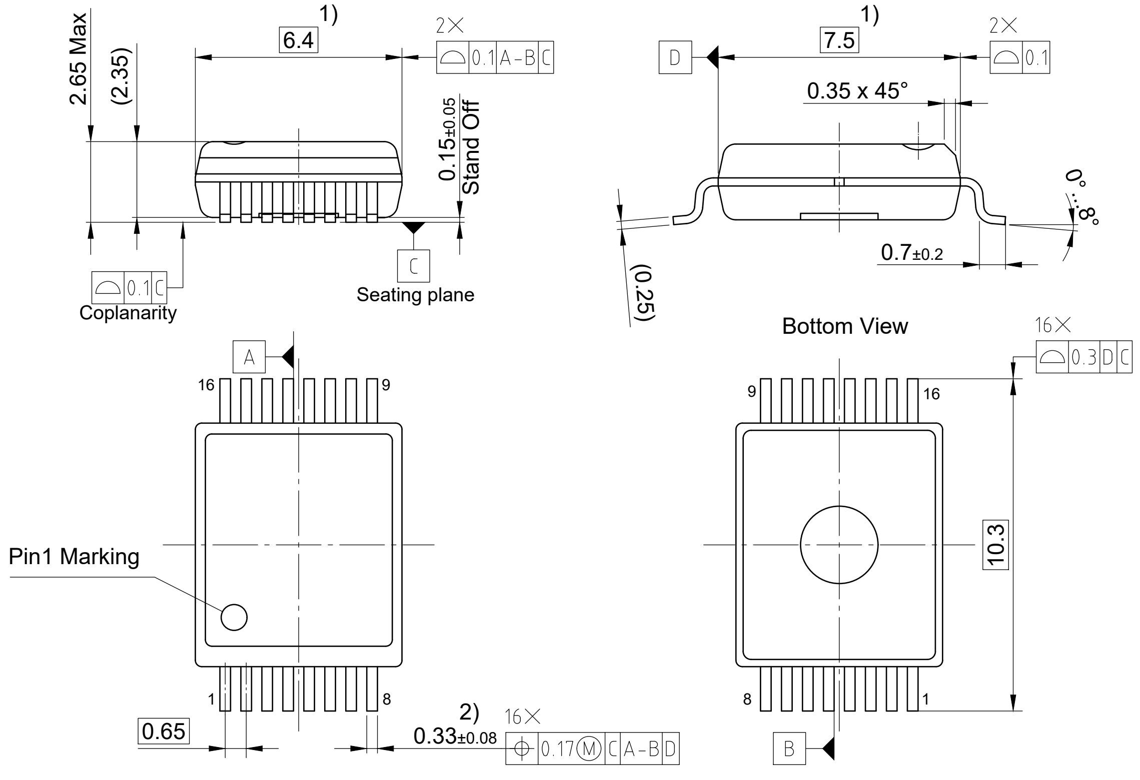
Description	Symbol	Characteristic	Unit
Apparent charge, method a $V_{pd(ini),a} = V_{IOTM}$, $V_{pd(m)} = 1.6 \times V_{IORM}$, $t_{ini} = 1$ min	q_C	<5	pC
Apparent charge, method b $V_{pd(ini),b} = V_{IOTM} \times 1.2$, $V_{pd(m)} = 1.875 \times V_{IORM}$, $t_{ini} = 1$ s	q_C	<5	pC
Isolation resistance at $T_{A,max}$	R_{IO}	$> 10^{11}$	Ω
Isolation resistance at T_S	R_{IO_S}	$> 10^{9}$	Ω
Maximum rated transient isolation voltage	V_{IOTM}	8000	V (peak)
Maximum repetitive insulation voltage	V_{IORM}	1767	V (peak)
Maximum surge isolation voltage for reinforced isolation $V_{TEST} = V_{IOSM} \times 1.6$	V_{IOSM}	6875	V (peak)
Insulation capacitance	C_{IO}	1.7	pF

6.2 Recognized under UL 1577 (File E311313)

Table 23 Recognized under UL 1577

Description	Symbol	Characteristic	Unit
Insulation withstand voltage/1 min	V_{ISO}	5700	V (rms)
Insulation test voltage/1 s	$V_{ISO, TEST}$	6840	V (rms)

7 Package information



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊏⊕]

Figure 24 PG-DSO-16-28/33 - 300 mil 16-pin fine pitch plastic green dual small outline package

8 Application notes

8.1 Reference layout for thermal data

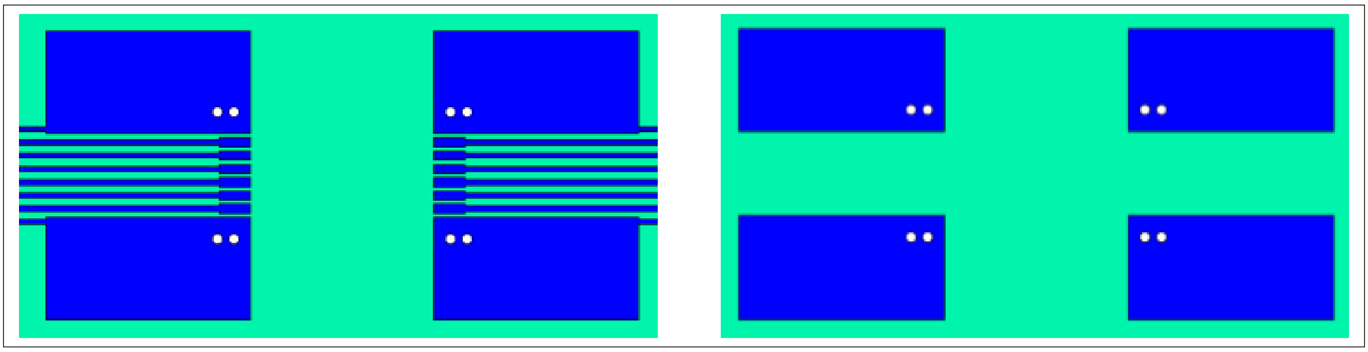


Figure 25 **Reference layout for thermal data (Two layer PCB; copper thickness 35 µm; left: top layer; right: bottom layer)**

The PCB layout represents the reference layout used for the thermal characterization. Pins 1 and 8 (*GND1*) and pins 9 and 16 (*VEE2*) require ground plane connections for achieving maximum power dissipation. The 1ED34x1Mc12M family (X3 Analog) is conceived to dissipate most of the heat generated through these pins.

8.2 Printed circuit board guidelines

Following factors should be taken into account for an optimum PCB layout.

- Sufficient spacing should be kept between high voltage isolated side and low voltage side circuits.
- The same minimum distance between two adjacent high-side isolated parts of the PCB should be maintained to increase the effective isolation and reduce parasitic coupling.
- In order to ensure low supply ripple and clean switching signals, bypass capacitor trace lengths should be kept as short as possible.

Revision history

Revision history

Reference	Description
v2.1 (2021-02-15)	• Change footnotes to table notes • added param V_{OFFSET} • update package drawing to latest revision • update certification status
(2021-09-01)	New version number schema: Target/Preliminary datasheet: 0.XY; Final datasheet: 1.XY
1.10 (2021-10-08)	• Certification information update (VDE certification) • Fix unit and conditions in certification table according to standards • Related product table update

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