Benefits and Features

- G3-PLC™ Compliant
- Prestandard Conformance: IEEE® P1901.2, ITU G.9903
- Frequency-Band Compliant with CENELEC, FCC, and ARIB
- Operating Frequency from 10kHz to 490kHz
- Single-Chip Solution Integrating Physical Layer (PHY) and Media Access Controller (MAC)
- Two UART and Two SPI™ Interfaces
- Supports IPV6-Compatible Networking Layer
  - 6LoWPAN IPV6 Header Compression Maximizes Payload Size
  - Dynamic Routing Mechanism Supports Mesh Networking
  - CSMA/CA (Carrier Sense Multiple Access with Collision Avoidance/Channel Access)
- High-Speed, Reliable Communication
  - Data Rate of up to 300kbps
  - Two Layers of Forward Error Correction (FEC) and Cyclic Redundancy Check (CRC16)
  - Enhanced FEC with Reed-Solomon and Viterbi
  - CCM* Authentication Coprocessor featuring AES-128 Encryption/Decryption
  - Automatic Repeat Request (ARQ) Enhances Error Detection and Data Reliability
  - Dynamic Link Adaptation to Select Optimum Data Rate Based on Channel Condition
  - Programmable Tone Notching
- AEC-Q100 Automotive Qualified

Applications

- Smart Grid Communications
- Advanced Metering Infrastructure (AMI)
- Smart Meters
- AMI Concentrators
- Electronic Vehicle Charging
- Street Lighting Automation
- Home Energy Monitoring
- Building Automation
- Solar and Renewable Energy Management

General Description

The MAX2992 powerline communication (PLC) baseband modem delivers half-duplex, asynchronous data communication over AC power lines at speeds up to 300kbps (full FCC band data rate). The MAX2992 is a system-on-chip (SoC) that combines the physical (PHY) and media access control (MAC) layers using Maxim's 32-bit MAXQ30 microcontroller core. The MAX2991 integrated analog front-end transceiver interfaces seamlessly with the MAX2992, and together with the MAX2992 G3-PLC firmware, forms a complete G3-PLC-compliant modem solution.

The MAX2992 utilizes OFDM techniques with DBPSK, DQPSK, D8PSK modulation and forward error correction (FEC) to enable robust data communication using the electrical power grid. The design provides inherent adaptability to frequency selective channels, robustness in the presence of group delay, and immunity to impulsive noise. To allow for regulatory compliance, the MAX2992 incorporates a programmable tone notching mechanism. This allows the notching of certain frequency bands in the transmit spectrum of the modem. This feature also provides an alternative method to address coexistence with other narrowband transmitters such as legacy FSK-based PLC systems.

The MAX2992 MAC incorporates a 6LoWPAN adaptation layer to support IPv6 packets. An enhanced CSMA/CA and ARQ, together with the mesh routing protocol, supports all common MAC layer services for various network topologies. Intelligent communication mechanisms adapt and enhance system performance over a range of channel conditions. These mechanisms include channel estimation, adaptive tone mapping, and routing protocols. An on-chip CCM (an extension of CCM specified in IEEE 802.15.4) authentication coprocessor with AES-128 encryption/decryption provides security and authentication.

Ordering Information

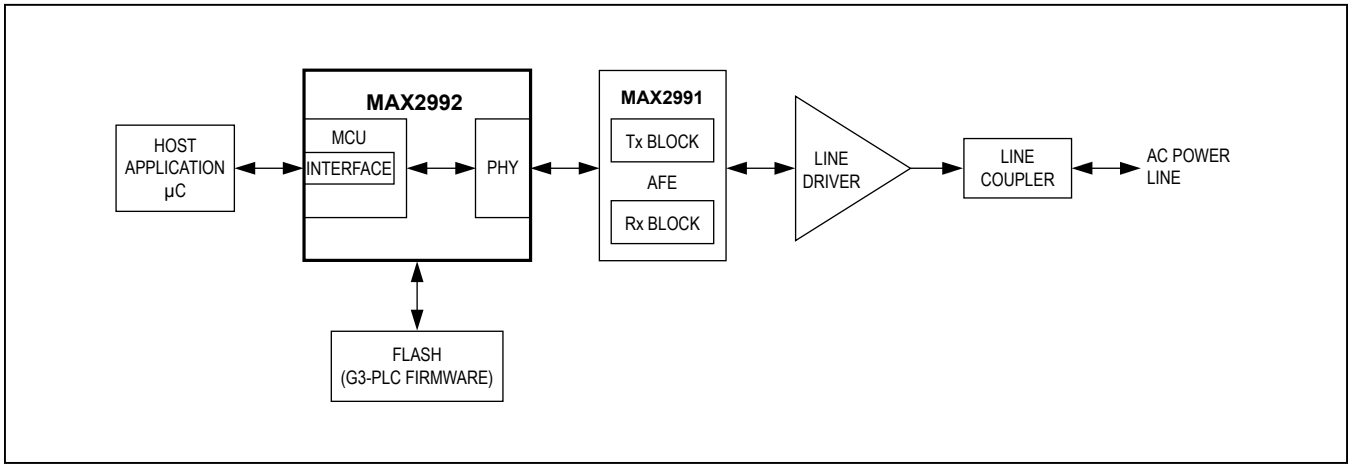
PART	TEMP RANGE	PIN-PACKAGE
MAX2992ECB+	-40°C to +85°C	64 LQFP

+Denotes lead(Pb)-free/RoHS-compliant package.

***Ordering Information* continued at end of data sheet.**

maxim integrated™

Typical Application Circuit



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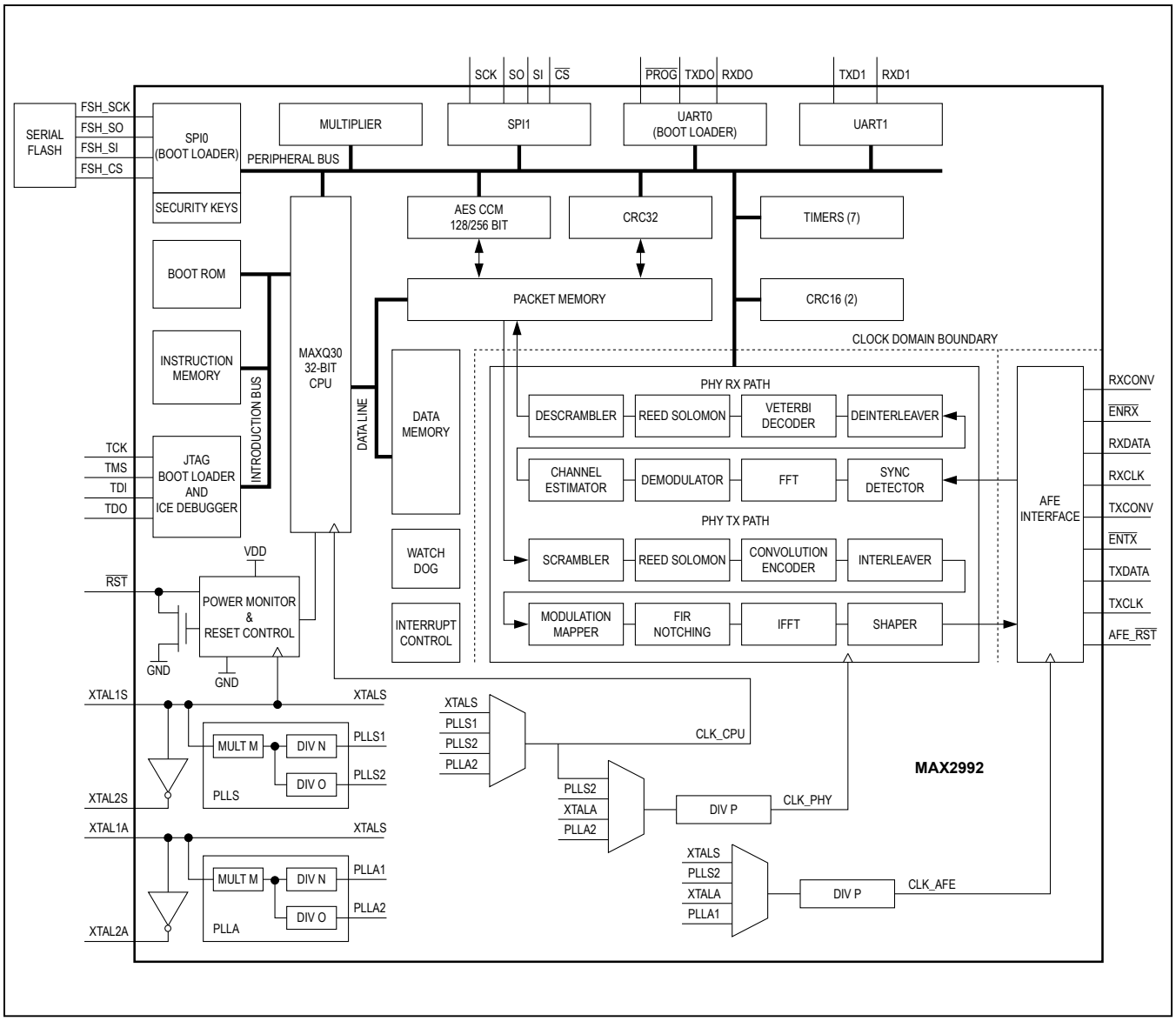
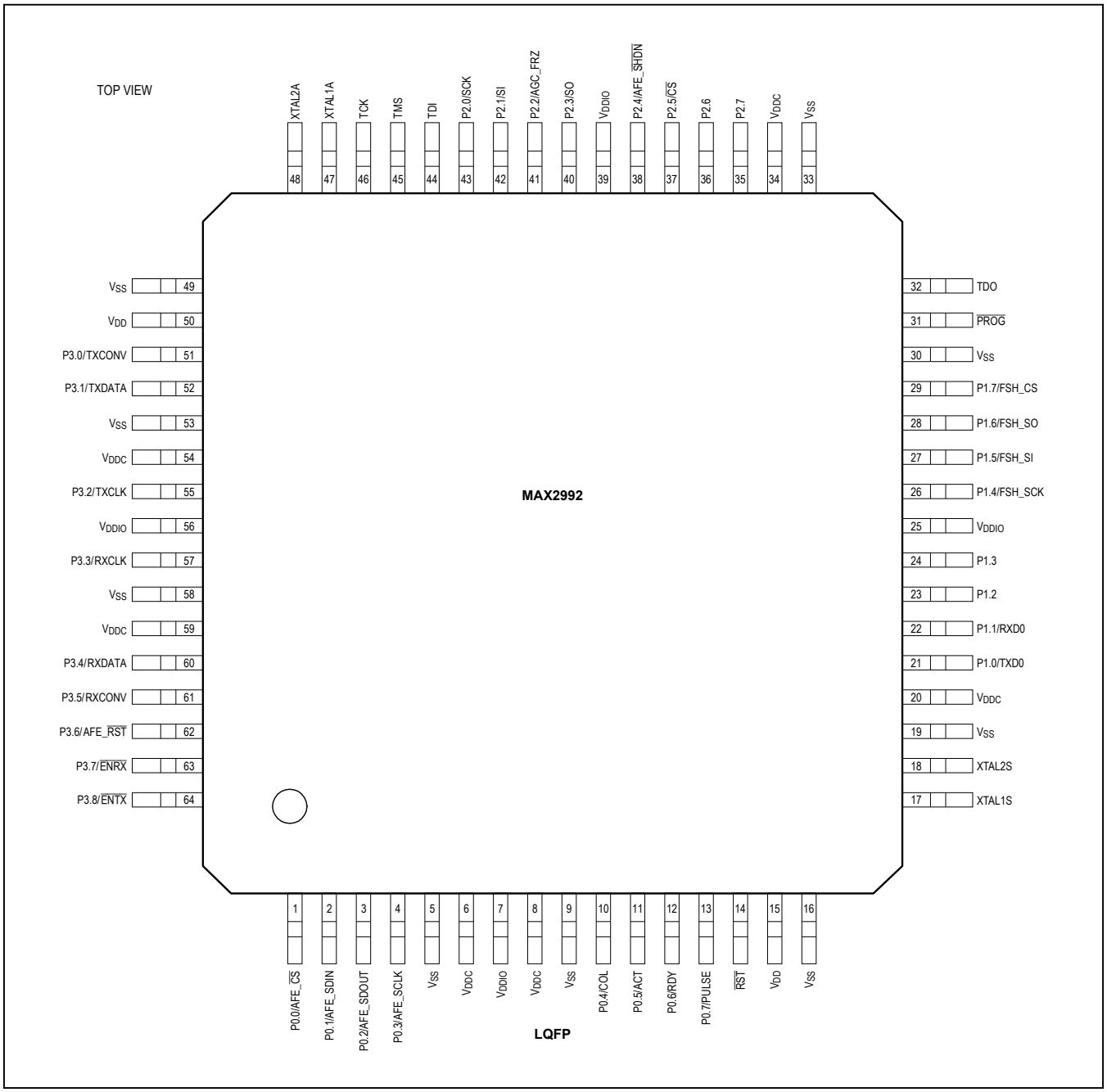
Functional Diagram



Pin Configuration



Pin Description

PIN	NAME	TYPE	FUNCTION
5, 9, 16, 19, 30, 33, 49, 53, 58	V_{SS}	P	Ground
6, 8, 20, 34, 54, 59,	V_{DDC}	P	+1.2V Digital Power Supply. Bypass V_{DDC} to V_{SS} with a 100nF capacitor as close as possible to the device.
7, 25, 39, 56	V_{DDIO}	P	+3.3V I/O Power Supply. Bypass V_{DDIO} to V_{SS} with a 100nF capacitor as close as possible to the device.
14	$\overline{RST}$	I/O	Reset. The $\overline{RST}$ input/output recognizes external active-low reset inputs and employs an internal pullup resistor to allow for a combination of wired-OR external reset sources. Bypass with a 220nF capacitor to V_{SS} and use a 10kΩ pullup resistor to V_{DDIO}.
15, 50	V_{DD}	P	+1.2V Analog Power Supply. Bypass V_{DD} to V_{SS} with a 100nF capacitor as close as possible to the device.
17	XTAL1S	I	Crystal Oscillator Input/Output. The crystal oscillator input/output provide support for parallel resonant, AT cut crystals. XTAL1S also acts as an input when there is an external clock source in place of a crystal. XTAL2S is the output of the crystal amplifier. Signal XTALS provides the clock base for the system clock.
18	XTAL2S	O	
31	$\overline{PROG}$	I	$\overline{PROG}$. $\overline{PROG}$ serves to initiate the UART boot loader. To activate the UART boot loader, $\overline{PROG}$ must be held low for at least 3 system clock cycles. The host must then send the autobaud character (0x0D) at a baud rate of 57,600 baud or less. The MAX2992 detects the serial baud rate and reply with the prompt character (0x3E). At this time, the bootloader protocol can be used to program the device.
32	TDO	O	JTAG Data Output
44	TDI	I	JTAG Data Input
45	TMS	I	JTAG Mode Select Input
46	TCK	I	JTAG Clock Input
47	XTAL1A	I	Crystal Oscillator Input/Output. The crystal oscillator input/output provides support for parallel resonant, AT cut crystals. XTAL1A also acts as an input when there is an external clock source in place of a crystal. XTAL2A is the output of the crystal amplifier. Signal XTALA provides the clock base for the AFE interface.
48	XTAL2A	O	
PORT 0			
1	P0.0/AFE_$\overline{CS}$	I/O O	P0.0/AFE_$\overline{CS}$. P0.0/AFE_$\overline{CS}$ is used by the MAX2992 G3-PLC firmware to implement an SPI command bus to the MAX2991 AFE. P0.0/AFE_$\overline{CS}$ is the chip-select line to the MAX2991. This is the general-purpose I/O hardware and part of the 8-bit I/O port P0. P0.0/AFE_$\overline{CS}$ provides hardware support that is available, but not utilized by the MAX2992 G3-PLC firmware. ● Interrupt input/stop mode wake-up. ● Timer I/O to Timer 0, In/Out A (Note 1).

Pin Description (continued)

PIN	NAME	TYPE	FUNCTION
2	P0.1/AFE_SDIN	I/O O	P0.1/AFE_SDIN. P0.1/AFE_SDIN is used by MAX2992 G3-PLC firmware to implement an SPI command bus to the MAX2991 AFE. P0.1/AFE_SDIN is the serial data to the MAX2991. This is general-purpose I/O hardware and part of the 8-bit I/O port P0. P0.1/AFE_SDIN provides hardware support that is available, but not utilized by the MAX2992 G3-PLC firmware. ● Interrupt input/stop mode wake-up. ● Timer I/O to Timer 0, In/Out B (Note 1).
3	P0.2/AFE_SDOUT	I/O O	P0.2/AFE_SDOUT. P0.2/AFE_SDOUT is used by the MAX2992 G3-PLC firmware to implement an SPI command bus to the MAX2991 AFE. P0.2/AFE_SDOUT is the serial data returned from the MAX2991. This is the general-purpose I/O hardware and part of the 8-bit I/O port P0. P0.2/AFE_SDOUT provides hardware support that is available, but not utilized by the MAX2992 G3-PLC firmware. ● Interrupt input/stop mode wake-up. ● Timer I/O to Timer 1, In/Out A (Note 1).
4	P0.3/AFE_SCLK	I/O O	P0.3/AFE_SCLK. P0.3/AFE_SCLK is used by MAX2992 G3-PLC firmware to implement an SPI command bus to the MAX2991 AFE. P0.3/AFE_SCLK is the serial clock to the MAX2991.This is the general-purpose I/O hardware and part of the 8-bit I/O port P0. P0.3/AFE_SCLK provides hardware support that is available, but not utilized by the MAX2992 G3-PLC firmware. ● Interrupt input/stop mode wake-up. ● Timer I/O to Timer 1, In/Out B (Note 1).
10	P0.4/COL	I/O O	P0.4/COL. P0.4/COL is used by the MAX2992 G3-PLC firmware to indicate modem status. P0.4/COL is the collision/packet error indicator, and can be used to drive a COL LED. This is the general-purpose I/O hardware and part of the 8-bit I/O port P0. P0.4/COL provides hardware support that is available, but not utilized by the MAX2992 G3-PLC firmware. ● Interrupt input/stop mode wake-up. ● Timer I/O to Timer 2, In/Out A (Note 1).
11	P0.5/ACT	I/O O	P0.5/ACT. P0.5/ACT is used by the MAX2992 G3-PLC firmware to indicate modem status. P0.5/ACT is the activity indicator and can be used to drive an ACT LED. This is general-purpose I/O hardware and part of the 8-bit I/O port P0. P0.5/ACT provides hardware support that is available, but not utilized by the MAX2992 G3-PLC firmware. ● Interrupt input/stop mode wake-up. ● Timer I/O to Timer 2, In/Out B (Note 1).

Pin Description (continued)

PIN	NAME	TYPE	FUNCTION
12	P0.6/RDY	I/O	P0.6/RDY. P0.6/RDY is used by the MAX2992 G3-PLC firmware to indicate modem status. PO.6/RDY is the modem-ready indicator and is used to drive a RDY LED. This is the general-purpose I/O hardware and part of the 8-bit I/O port P0. P0.6/RDY provides hardware support that is available, but not utilized by the MAX2992 G3-PLC firmware. ● Interrupt input/stop mode wake-up. ● Timer I/O to Timer 3, In/Out A (Note 1).
13	P0.7/PULSE	I/O	P0.7/PULSE. P0.7/PULSE is used by the MAX2992 G3-PLC firmware to input pulses from an external zero-crossing detector. This is general-purpose I/O hardware and part of the 8-bit I/O port P0. P0.7/PULSE provides hardware support that is available, but not utilized by the MAX2992 G3-PLC firmware. ● Interrupt input/stop mode wake-up. ● Timer I/O to Timer 3, In/Out B (Note 1).
PORT 1			
21	P1.0/TXD0	I/O O	P1.0/TXD0. P1.0/TXD0 provides connections to dedicated UART hardware. This is used by the MAX2992 G3-PLC firmware to implement the UART host interface. P1.0/TXD0 is the transmit data from the MAX2992 to the host. This is the general-purpose I/O hardware and part of the 8-bit I/O port P1. Connect P1.0/TXD0 with a 5kΩ resistor to V_{DDIO} (Note 1).
22	P1.1/RXD0	I/O I	P1.1/RXD0. P1.1/RXD0 provides connections to dedicated UART hardware. This is used by the MAX2992 G3-PLC firmware to implement the UART host interface. P1.1/RXD0 is the receive data from the host to the MAX2992. This is the general-purpose I/O hardware and part of the 8-bit I/O port P1 (Note 1).
23	P1.2	I/O O	P1.2. P1.2 provides connections to dedicated UART hardware used by the MAX2992 G3-PLC firmware for reserved function. Leave unconnected. This is the general-purpose I/O hardware and part of the 8-bit I/O port P1 (Note 1).
24	P1.3	I/O I	P1.3. P1.3 provides connections to dedicated UART hardware used by the MAX2992 G3-PLC firmware for reserved function. This is the general-purpose I/O hardware and part of the 8-bit I/O port P1 (Note 1).
26	P1.4/FSH_SCK	I/O O	P1.4/FSH_SCK. P1.4/FSH_SCK provides dedicated connections to the SPI hardware, and after power-on reset, the MAX2992 attempts to bootstrap code from an external flash if it is present. P1.4/FSH_SCK is the serial clock from the MAX2992 to the flash. This is the general-purpose I/O hardware and part of the 8-bit I/O port P1. After boot, the SPI hardware can be used by the MAX2992 G3-PLC firmware. This is not utilized by the MAX2992 G3-PLC firmware, but P1.4/FSH_SCK provides the capability of: ● SPI master clock output. ● SPI slave clock input (Note 1).

Pin Description (continued)

PIN	NAME	TYPE	FUNCTION
27	P1.5/FSH_SI	I/O O	P1.5/FSH_SI. P1.5/FSH_SI provides dedicated connections to the SPI hardware, and after power-on reset, the MAX2992 attempts to bootstrap code from an external flash if it is present. P1.5/FSH_SI is the serial data from the MAX2992 to the flash. This is the general-purpose I/O hardware and part of the 8-bit I/O port P1. After boot, the SPI hardware can be used by the MAX2992 G3-PLC firmware. This is not utilized by the MAX2992 G3-PLC firmware, but P1.4/FSH_SI provides the capability of: ● SPI master output data. ● SPI slave input data (Note 1).
28	P1.6/FSH_SO	I/O O	P1.6/FSH_SO. P1.6/FSH_SO provides dedicated connections to the SPI hardware, and after power-on reset, the MAX2992 attempts to bootstrap code from an external flash if it is present. P1.6/FSH_SO is the serial data return to the MAX2992 from the flash. This is the general-purpose I/O hardware and part of the 8-bit I/O port P1. After boot, the SPI hardware can be used by the MAX2992 G3-PLC firmware. This is not utilized by the MAX2992 G3-PLC firmware, but P1.6/FSH_SO provides the capability of: ● SPI master data input. ● SPI slave data output (Note 1).
29	P1.7/FSH_CS	I/O O	P1.7/FSH_CS. P1.7/FSH_CS provides dedicated connections to the SPI hardware, and after power-on reset, the MAX2992 attempts to bootstrap code from an external flash if it is present. P1.7/FSH_CS is the serial chip select from the MAX2992 to the flash. This is the general-purpose I/O hardware and part of the 8-bit I/O port P1. After boot, the SPI hardware can be used by the MAX2992 G3-PLC firmware. This is not utilized by the MAX2992 G3-PLC firmware, but P1.7/FSH_CS provides the capability of: ● SPI slave chip select (Note 1).
PORT 2			
35	P2.7	I/O	P2.7. P2.7 is not used by the MAX2992 G3-PLC firmware. It is configured as an unused input with the internal pullup enabled. It can be left unconnected. This is the general-purpose I/O hardware and part of the 8-bit I/O port P2. P2.7 provides hardware support that is available, but not utilized by the MAX2992 G3-PLC firmware: ● Hardware flow control line CTS for UART0. ● Timer I/O to Timer 4, In/Out A. ● Timer I/O to Timer 6, In/Out A (Note 1).

Pin Description (continued)

PIN	NAME	TYPE	FUNCTION
36	P2.6	I/O	P2.6. P2.6 is not used by the MAX2992 G3-PLC firmware. It is configured as an unused input with the internal pullup enabled. It can be left unconnected. This is the general-purpose I/O hardware and part of the 8-bit I/O port P2. P2.6 provides hardware support that is available, but not utilized by the MAX2992 G3-PLC firmware ● Hardware flow control line RTS for UART0. ● Timer I/O to Timer 4, In/Out A. ● Timer I/O to Timer 6, In/Out A (Note 1).
37	P2.5/$\overline{CS}$	I/O O	P2.5/$\overline{CS}$. P2.5/$\overline{CS}$ provides dedicated connections to SPI hardware. This is used by the MAX2992 G3-PLC firmware to implement the SPI host interface. P2.5/$\overline{CS}$ is the active-low, chip select from the host to the MAX2992. This is general-purpose I/O hardware and part of the 8-bit I/O port P2. P2.5/$\overline{CS}$ provides hardware support that is available, but not utilized by the MAX2992 G3-PLC firmware. ● Timer I/O to Timer 5, In/Out B (Note 1).
38	P2.4/AFE_$\overline{SHDN}$	I/O	P2.4/AFE_$\overline{SHDN}$. P2.4/AFE_$\overline{SHDN}$ is used by the MAX2992 G3-PLC firmware to place the MAX2991 AFE into shutdown mode for lowest power consumption. P2.4/AFE_$\overline{SHDN}$ provides hardware support that is available, but not utilized by the MAX2992 G3-PLC firmware. This is general-purpose I/O hardware and part of the 8-bit I/O port P2. ● Timer I/O to Timer 5, In/Out A (Note 1).
40	P2.3/SO	I/O O	P2.3/SO. P2.3/SO provides dedicated connections to SPI hardware. This is used by the MAX2992 G3-PLC firmware to implement the SPI host interface. P2.3/SO is the serial data to the host from the MAX2992. This is general-purpose I/O hardware and part of the 8-bit I/O port P2 (Note 1).
41	P2.2/AGC_FRZ	I/O O	P2.2/AGC_FRZ. P2.2/AGC_FRZ provides dedicated connections to the PHY hardware. This is used by the MAX2992 G3-PLC firmware to signal the MAX2991 AFE to freeze its automatic gain control (AGC) setting. This is general-purpose I/O hardware and part of the 8-bit I/O port P2 (Note 1).
42	P2.1/SI	I/O O	P2.1/SI. P2.1/SI provides dedicated connections to SPI hardware. This is used by the MAX2992 G3-PLC firmware to implement the SPI host interface. P2.1/SI is the serial data from the host to the MAX2992. This is general-purpose I/O hardware and part of the 8-bit I/O port P2 (Note 1).
43	P2.0/SCK	I/O I	P2.0/SCK. P2.0/SCK provides dedicated connections to SPI hardware. This is used by the MAX2992 G3-PLC firmware to implement the SPI host interface. P2.0/SCK is the serial clock from the host to the MAX2992. This is general-purpose I/O hardware and part of the 8-bit I/O port P2 (Note 1).

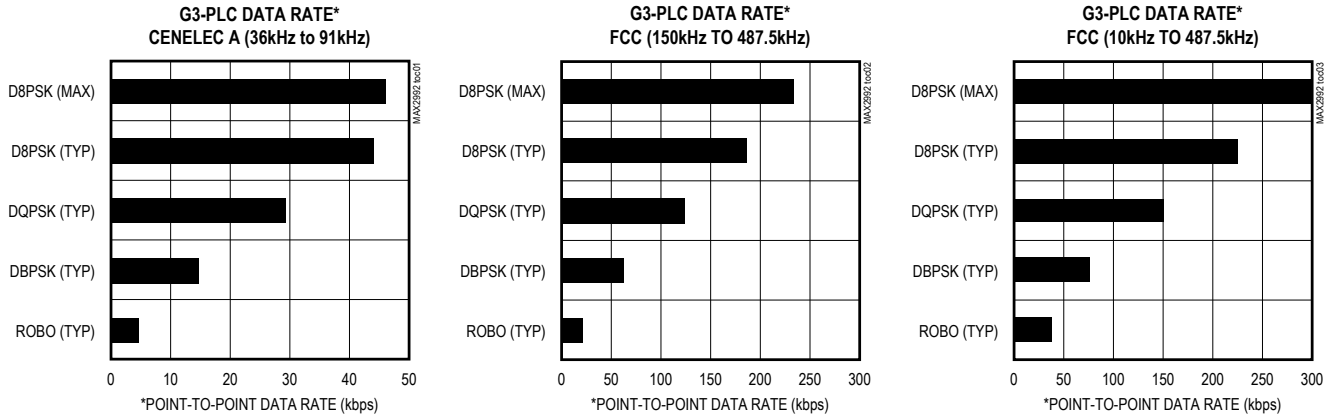
Pin Description (continued)

PIN	NAME	TYPE	FUNCTION
PORT 3			
51	P3.0/TXCONV	I/O O	P3.0/TXCONV. P3.0/TXCONV provides dedicated connections to AFE interface hardware. This is used by the MAX2992 G3-PLC firmware to implement the AFE interface to the MAX2991. P3.0/TXCONV is the TX enable line to the MAX2991. This is general-purpose I/O hardware and part of the 8-bit I/O port P3 (Note 1).
52	P3.1/TXDATA	I/O O	P3.1/TXDATA. P3.1/TXDATA provides dedicated connections to AFE interface hardware. This is used by the MAX2992 G3-PLC firmware to implement the AFE interface to the MAX2991. P3.1/TXDATA is the TX serial data output to the MAX2991. This is general-purpose I/O hardware and part of the 8-bit I/O port P3 (Note 1).
55	P3.2/TXCLK	I/O O	P3.2/TXCLK. P3.2/TXCLK provides dedicated connections to AFE interface hardware. This is used by the MAX2992 G3-PLC firmware to implement the AFE interface to the MAX2991. P3.2/TXCLK is the TX serial clock to the MAX2991. This is general-purpose I/O hardware and part of the 8-bit I/O port P3 (Note 1).
57	P3.3/RXCLK	I/O O	P3.3/RXCLK. P3.3/RXCLK provides dedicated connections to AFE interface hardware. This is used by the MAX2992 G3-PLC firmware to implement the AFE interface to the MAX2991. P3.3/RXCLK is the RX serial clock to the MAX2991. This is general-purpose I/O hardware and part of the 8-bit I/O port P3 (Note 1).
60	P3.4/RXDATA	I/O I	P3.4/RXDATA. P3.4/RXDATA provides dedicated connections to AFE interface hardware. This is used by the MAX2992 G3-PLC firmware to implement the AFE interface to the MAX2991. P3.4/AFE_SDI is the RX serial data from the MAX2991. This is general-purpose I/O hardware and part of the 8-bit I/O port P3 (Note 1).
61	P3.5/RXCONV	I/O O	P3.5/RXCONV. P3.5/RXCONV provides dedicated connections to AFE interface hardware. This is used by the MAX2992 G3-PLC firmware to implement the AFE interface to the MAX2991. P3.5/RXCONV is the RX Enable line to the MAX2991. This is general-purpose I/O hardware and part of the 8-bit I/O port P3 (Note 1).
62	P3.6/AFE_$\overline{RST}$	I/O O	P3.6/AFE_$\overline{RST}$. P3.6/AFE_$\overline{RST}$ is used by the MAX2992 G3-PLC firmware to reset the MAX2991. This is general-purpose I/O hardware and part of the 8-bit I/O port P3 (Note 1).
63	P3.7/$\overline{ENRX}$	I/O O	P3.7/$\overline{ENRX}$. P3.7/$\overline{ENRX}$ is used by the MAX2992 G3-PLC firmware to enable the RX channel in the MAX2991. This is general-purpose I/O hardware and part of the 8-bit I/O port P3 (Note 1).
64	P3.8/$\overline{ENTX}$	I/O O	P3.8/$\overline{ENTX}$. P3.8/$\overline{ENTX}$ is used by the MAX2992 G3-PLC firmware to enable the TX channel in the MAX2991. This is general-purpose I/O hardware and part of the 8-bit I/O port P3 (Note 1).

Note 1: Refer to the *MAX2992 G3-PLC Firmware Release* Note for updates to the function implemented.

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)



Detailed Description

The MAX2992 integrates a high-performance Maxim MAXQ30 32-bit RISC core with optimized OFDM PHY, 128/256-bit AES and CRC hardware and peripherals including UART serial communication, SPI interface, serial AFE interface, watchdog/countdown timers, GPIO, and external interrupts. The MAX2992 G3-PLC modem is based on Orthogonal Frequency Division Multiplexing (OFDM) that places multiple evenly spaced carriers within the available frequency band. Data is modulated onto these carriers and three modulation methods are supported: DBPSK, DQPSK, and D8PSK. Special data interleaving and forward error correction techniques enhance the robustness of communication that is immune to impulsive noise, adaptable to frequency selective channels, and robust in the presence of group delay. Additional performance is obtained by adaptive tone mapping, a process by which the MAX2992 automatically detects carriers with poor SNR, redistributing data onto better performing carriers. These features allow the MAX2992 to adapt to channel conditions to provide superior data rates for a given channel condition. External flash stores the complete G3-PLC application firmware supplied by Maxim, which executes from the on-chip SRAM memory. G3-PLC data and control is accomplished using the G3-PLC modem interface over the UART or SPI port. A full description of this interface is provided in the *MAX2992 G3-PLC Interface Guide*. The MAC, implemented on the MAXQ30, provides advanced CSMA/CA and ARQ functions and supports all common MAC layer services.

Power Management

The MAX2992 power-management features minimize power consumption by clock gating and by adjusting the operating frequency. Clock gating is used to eliminate active power of on-chip functional units when not in use. A clock divider of up to 256 is set by software to reduce the operating frequency to the required performance level per single application.

Normal Operating Mode

In normal operating mode, the MAX2992's power-management features minimize power consumption by adjusting the frequency of CPU and PHY operation to match the dynamic load on the device.

Idle Mode

In idle mode, the MAX2992 lowers power consumption by shutting down the MAXQ30 processor, but keeps the PHY's receive circuitry active so that it can detect a powerline packet. At least one clock must be running during idle mode. The processor awakes on the detection of a line SYNC at the beginning of a packet and returns to normal operating mode to receive the powerline packet.

Stop Mode

Stop mode disables all clocks and circuits within the MAX2992. All modem functions are disabled. This is

the lowest power state for the device where only leakage power is consumed. An external interrupt causes the MAX2992 to exit from the stop mode. Stop mode is controlled by the MAX2992 G3-PLC firmware. Refer to the MAX2992 G3-PLC Interface Guide and *MAX2992 G3-PLC Firmware Release Note* for details on the use of stop mode.

UART Interface

The MAX2992 features two hardware UARTs (UART0 and UART1). UART0 has a 16-byte deep receive and transmit FIFO with configurable interrupt thresholds and it supports hardware flow control. Additionally, UART0 provides a hardware function for booting the device. The MAX2992 G3-PLC firmware dedicates UART0 to the host interface with a baud rate of 115,200bps without flow control. See the *MAX2992 G3-PLC Firmware Release Note* for additional information on the UART0 host interface settings.

Data transfer for communication on the power line and status and control commands are passed between host and the MAX2992 G3-PLC modem over UART0. A simple frame format is used to define data and management primitives. A complete description of the frame format and command primitives is provided in the *MAX2992 G3-PLC Interface Guide*.

The MAX2992 G3-PLC firmware utilizes UART1 for a reserved function. Do not connect in user designs.

Serial Peripheral Interface (SPI)

The MAX2992 includes two serial peripheral interface modules (SPI0 and SPI1). The MAX2992 SPI hardware can operate in slave or master modes. This is a common, high-speed, synchronous peripheral interface that shifts a bit stream of variable length and data rate between the microcontroller and other peripheral devices. Programmable clock frequency, character lengths, polarity, and error handling enhance the usefulness of the peripheral. The maximum baud rate of the SPI interface is half the system clock for master mode operation and 1/8th the system clock for slave mode operation.

SPI0 features a boot loading function that is the primary method for initializing the MAXQ30 memory after reset. SPI0 boot loading is described in the *Boot Options* section.

SPI1 is assigned by the MAX2992 G3-PLC firmware to implement an alternative host interface to UART0. When used as a host interface, four MAX2992 signals, P2.0/SCK, P2.5/$\overline{CS}$, P2.1/SI, and P2.3/SO must be connected to the host processor.

Refer to the MAX2992 G3-PLC Interface Guide and *MAX2992 G3-PLC Firmware Release Note* for details on the use of the SPI1 port.

GPIO

The MAX2992 features 5V tolerant, 3.3V I/O. Each I/O can be either an input or output. The MAX2992 G3-PLC firmware configures each I/O as described in the *Pin Configuration* section. Refer to the *MAX2992 G3-PLC Firmware Release Note* for additional GPIO assignments.

When in input mode, a weak pullup resistance is enabled pulling the I/O high. A series NFET provides the I/O's high voltage tolerance (Figure 1). This degrades the VOH observed and an external resistive pullup is recommended when the I/O is not actively driven (such as $\overline{RST}$ or $\overline{PROG}$, see the *Pin Description*).

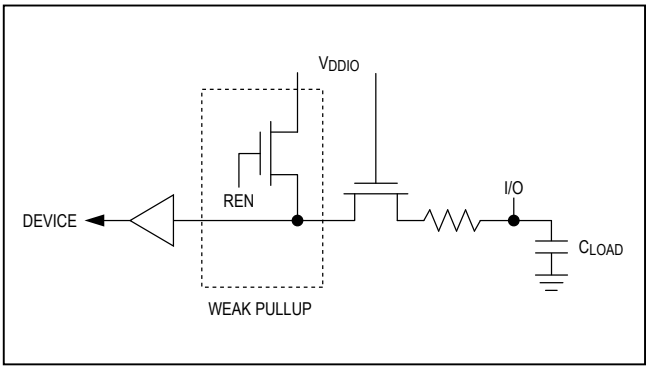


Figure 1. GPIO

Timers

The MAX2992 incorporates seven 16-bit programmable timers to allow precise control of internal and external events. Each timer can operate in two modes: count-stop or wrap-round. The timers can be configured so that the timers generate interrupts upon reaching the extreme value. The timers also feature output modes suitable for synthesizing PWM. The MAX2992 G3-PLC firmware uses these timers within its operating system, and to implement CSMA and AC phase detection. Refer to the *MAX2992 G3-PLC Interface Guide* and *MAX2992 G3-PLC Firmware Release Note* for information on timer use.

Clocks, PLL, and Power-on-Reset

The MAX2992 provides two built-in oscillators each with an associated PLL. The device can function in a one or a two crystal configuration, either reducing system components or maximizing flexibility of the operating frequencies in the system. The one crystal configuration requires a

crystal connected between XTAL1S and XTAL2S. Drive XTAL1A low, have XTAL2A unconnected, and connect V_{DD} (Pin 50) to V_{SS} in one crystal mode.

The MAX2992 G3-PLC firmware uses the one crystal configuration with a 19.2MHz crystal connected to XTAL1S and XTAL2S. This crystal is used to generate both CPU and AFE clocks. For this configuration, the CPU clock is set to 76.8MHz and AFE clock is 6.4MHz for the CENELEC frequency band with a 400kHz sample rate. For FCC and ARIB bands, the AFE clock is 19.2MHz with a 1.2MHz sample rate.

The two crystal configuration requires that a crystal be connected between XTAL1S and XTAL2S, and XTAL1A and XTAL2A. Refer to the *MAX2992 G3-PLC Firmware Release Note* for information on the crystal configuration used.

External Reset

During normal operation, the MAX2992 can be placed into external reset mode by holding $\overline{RST}$ low for a minimum of eight clock cycles. After $\overline{RST}$ returns high, the MAXQ30 processor exits the reset state within eight clock cycles and begins program execution.

Watchdog Timer

The watchdog timer is a programmable hardware timer that can be used to reset the processor in case of a software lockup or other unrecoverable error. The MAX2992 G3-PLC firmware uses the watchdog timer to enhance system reliability.

AFE Serial Interface

The MAX2992 AFE interface is designed to support the MAX2991. The interface includes separate receive and transmit serial interfaces. Connect the MAX2992 to the MAX2991 as shown in Figure 2. Refer to the MAX2991 data sheet for a description of the serial interface timing.

Boot Options

The MAX2992 executes program code from internal SRAM. This SRAM is volatile and must be loaded with application code after a power-cycle event. There are three options for loading the SRAM:

- Automatic bootstrap from external flash
- Bootstrap through the UART0 loader
- Bootstrap through the JTAG loader

Figure 3 shows the flow diagram for MAX2992 booting. The flowchart illustrates:

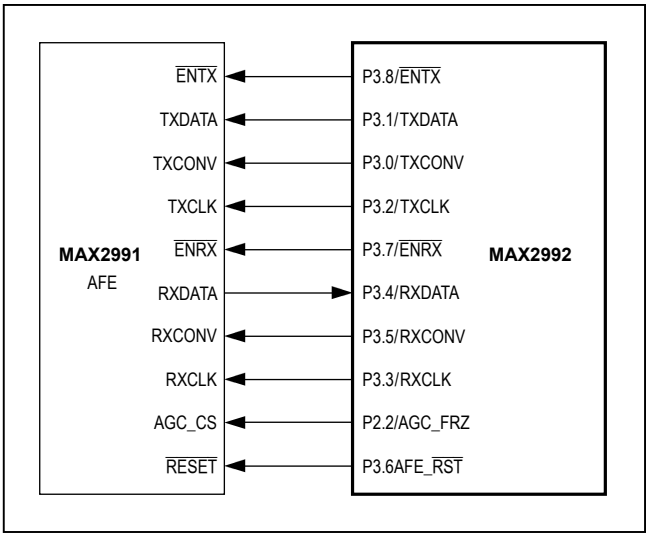


Figure 2. MAX2992 to MAX2991 Interface

- At any time, the $\overline{PROG}$ can be used to initiate a UART0 boot load cycle.
- From POR, if the JTAG interface and $\overline{PROG}$ are not active, the MAX2992 boots load from external flash using the SPI0 interface.
- Once a program is loaded (by any means) and the program valid bit is set, successive resets causes reexecution of the loaded code. An additional boot load cycle is not required.

Automatic Bootstrap from Flash

- When the JTAG and UART0 bootstrap are not selected, the MAX2992 boots from an external flash device over SPI0. The flash must be preprogrammed with the MAX2992 G3-PLC firmware. AES encryption of the flash image is supported to protect any deployed application. Refer to the MAX2992 Evaluation Kit for details on programming the flash.

Bootstrap Using the UART0 Loader

The MAX2992 can be booted over the UART0 host interface to avoid the need for a dedicated flash device. The UART0 boot load procedure is:

1. Pull $\overline{PROG}$ low for a minimum of 8 clock cycles. If automatic boot after power-up is desired, place an RC on $\overline{PROG}$ so that $\overline{PROG}$ rises at least 8 clock cycles after $\overline{RST}$.
2. Send the MAX2992 the character 0x0D (8-bit, no parity) at a rate of 57,600 baud or less.

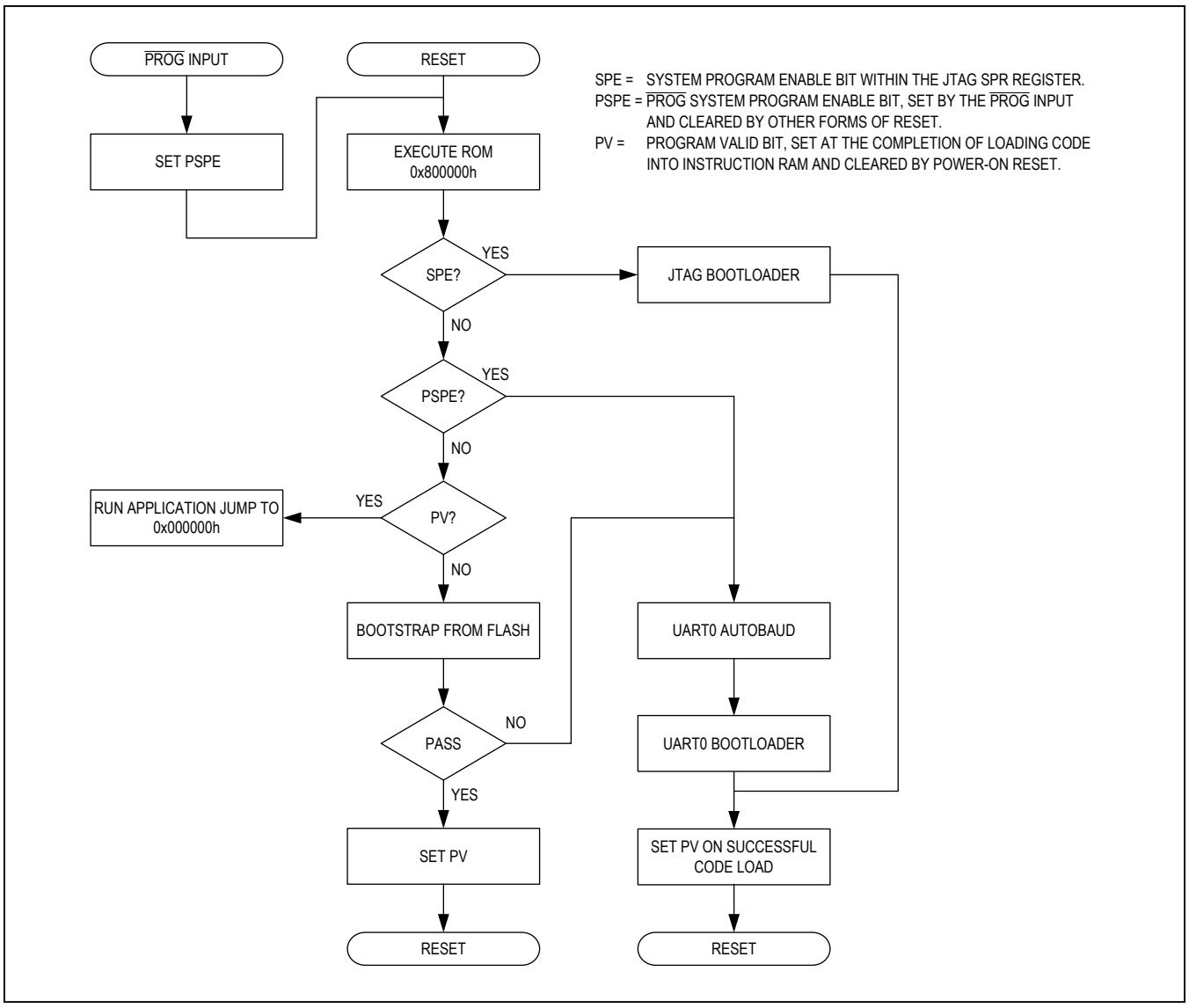


Figure 3. MAX2992 Boot Sequence Flow Chart

3. The MAX2992 measures the timing and autocalibrates to the baud rate.
4. The MAX2992 acknowledges entry to the serial loader by transmitting a prompt character (0x3E).

Details of using the serial boot-loader commands to implement a UART0 bootstrap are provided in the MAX2992 Evaluation Kit. The serial bootloader does not utilize the hardware flow control feature of UART0. The loader manages flow control using the communication protocol.

Toggling $\overline{RST}$ exits the serial boot loader whereby the MAX2992 follows the boot sequence described by Figure 3. Details of using the serial boot loader commands to implement a UART0 boot strap are provided in the MAX2992 Evaluation Kit.

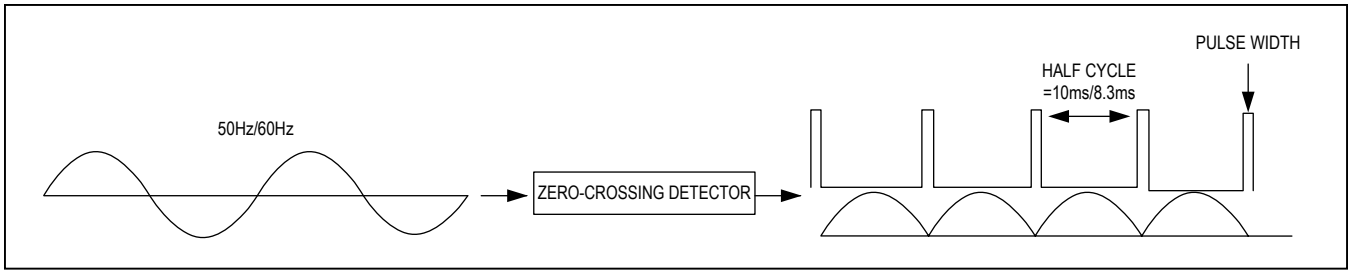


Figure 4. Zero-Crossing AC Detector

Bootstrap Using the JTAG Loader

The JTAG bootstrap loader mode initializes the nonvolatile memory of the internal MAXQ30 microcontroller. The JTAG loader is used by Maxim as a development interface and should not be utilized in user systems.

AC Phase Detector

To know the phases of each meter, the MAX2992 features internal timers to measure time intervals of pulses resulted from zero-crossing of AC 50Hz/60Hz as shown in Figure 4. P0.7/PULSE is used to input pulses received from an external zero-crossing detector to reset an 8-bit counter. The minimum required pulse width is 1% of the cycle.

CSMA/CA

Concurrent transmission by multiple nodes can result in frame collisions that occur when multiple transmissions interfere with each other, distorting the signal sufficiently to cause communication to fail. Carrier Sense Multiple Access/Collision Avoidance (CSMA/CA) is a mechanism to reduce the probability of collisions. When using CSMA as soon as a node is ready to transmit a packet, the device checks the channel for activity. If no other node is transmitting the node transmits its packet. If another transmitter is detected, the device waits for that transmission to end and then waits for a randomly selected period of time for another device to start transmitting on the channel. This wait time is called a random back-off time. If no other device has started transmitting at the end of the back-off time, the device starts its transmission. This process is repeated until the device gets access to the channel. All the devices in the system randomly choose their back-off time from one of a limited number of predefined time slots after the end of the prior transmission.

Automatic Repeat Request (ARQ)

To enhance error detection and improve data reliability, the MAX2992 utilizes an automatic repeat request protocol. Since PLC communication is a half-duplex connection, the transmitter waits for an acknowledgment (ACK) of each transmission before it proceeds with the next transmission. If the transmitter does not receive an ACK packet, the transmitter resends the packet.

PHY Overview

The MAX2992 powerline modem is designed to overcome the challenges associated with the harsh powerline environment for data communications. Some of the challenges are noted below:

- Channel variability with frequency, location, and time
- Narrowband, wideband, and impulsive noise commonly present on the power line
- Presence of narrowband interference and multipath signal propagation
- Low and time varying network impedance (3Ω to 30Ω)
- Propagation through transformers that subject the channel to severe group delay and attenuation

The MAX2992 modem solution is based on orthogonal frequency division multiplexing (OFDM) to overcome the powerline channel impairment, providing high reliability in data transmission. This method combines good bandwidth efficiency (high data rate) with the possibility of a very flexible bandwidth allocation. In combination with error correction coding, the MAX2992 is robust in the presence of frequency selective channels and resilient to jammer signals and impulsive noise.

The OFDM technique places evenly spaced carriers into the available frequency band. The MAX2992 can be configured to operate in a subset of frequencies in the range 10kHz to 490kHz, encompassing CENELEC, ARIB, and FCC frequency bands. Three modulation methods are supported; DBPSK, DQPSK, and D8PSK. This allows the MAX2992 to trade off channel condition and data rate to achieve the highest possible data through for a given channel condition. Additional performance is obtained by adaptive tone mapping, a process by which the MAX2992 automatically detects carriers with poor SNR, redistributing data onto better performing channels.

There are several advantages of the MAX2992 OFDM scheme as compared to traditional single carrier FSK or spread-spectrum systems:

- The MAX2992 OFDM allows an extremely flexible allocation and use of a given channel bandwidth. As an example, the lower and the upper limit of the used frequency band can easily be configured. It is also possible to use two or more noncontiguous sub-bands for the transmission of a single data stream.
- It is considerably more robust against intersymbol interference (ISI) or group delay distortion caused by the transmission channel than narrowband systems. This is mainly due to the fact that the parallel transmission on several carriers leads to longer symbol duration. Furthermore, ISI is simply removed by inserting guard intervals and cyclic prefixes between the symbols.

The MAX2992 is robust in presence of narrowband interference because such jammers typically destroy a single carrier only. Through the use of forward error correction coding—the erroneous data is detected and corrected using the received coded information.

On the transmitter side, the PLC modem layer receives input data from the UART and passes the data through the FEC, modulator, and IFFT. On the receiver side, the PLC modem layer receives inputs from the AFE and hands the data over to the application layer (Figure 5). Two separate signal paths are shown for the receiver. The first path is dedicated to the detection of narrow band interference, and the second path processes the preamble for symbol and frame synchronization followed by the FEC decoding block. After descrambling the output of the FEC decoder data are available for the MAC layer.

Table 1 shows the frequency bands with which the MAX2992 modem complies.

Table 1. Frequency Bands Supported by the MAX2992

COMPONENT	NUMBER OF CARRIERS	FIRST CARRIER (kHz)	LAST CARRIER (kHz)
CENELEC A	36	35.93	90.62
CENELEC B	16	98.43	121.87
CENELEC C	7	128.12	137.50
CENELEC BC	26	98.43	137.50
CENELEC D	4	142.18	146.87
FCC1	72	154.6875	487.5
FCC2	97	37.5	487.5
FCC3	24	154.6875	262.5
FCC4	40	304.6875	487.5
ARIB1	54	154.6875	403.125
ARIB2	79	37.5	403.125

The combined PHY and MAC in the MAX2992 meet the transmitter/receiver technical requirements for highly reliable data communication in powerline networks, as shown in Table 2 and Table 3.

Table 2. Frame Error Rate Requirements in AWGN Channels (100 Bytes)

SIGNAL-TO-NOISE RATIO (dB)	MODULATION AND CODING RATE	FRAME ERROR RATE (%)
-1.2	ROBO	0.01
2.6	DBPSK	0.01
6.1	DQPSK	0.01
9.9	D8PSK	0.01

Table 3. Receiver Specification with MAX2991

RECEIVER SPECIFICATION	REQUIREMENT
Sensitivity	1mV
Dynamic range	60dB
Clock frequency tolerance	±25ppm

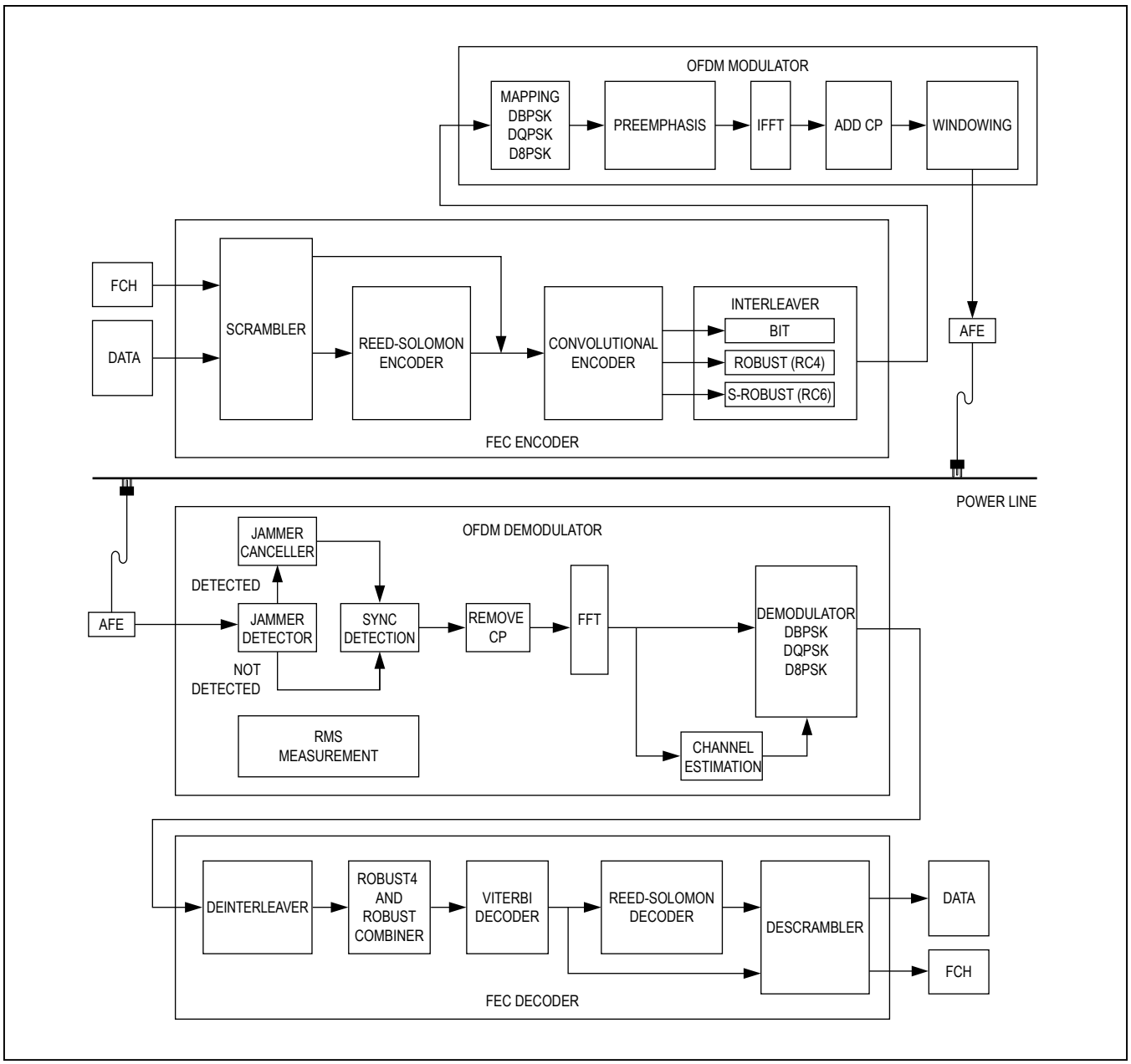


Figure 5. Transmitter/Receiver Block Diagram of the Baseband Processor

Absolute Maximum Ratings

V_{DDIO} to V_{SS} .....-0.5V to +4.0V
V_{DDC} to V_{SS} .....-0.5V to +1.5V
V_{DD} to V_{SS}.....-0.5V to +1.5V
XTAL1A, XTAL2A, XTAL1S, XTAL2S to V_{SS}.....-0.5V to +4.0V
All I/O Pins.....-0.5V to +5.5V
Continuous Power Dissipation (T_A = +70°C)
LQFP (derate 25mW/°C above +70°C).....2000mW

Operating Temperature Range..... -40°C to +105°C
Junction Temperature.....+125°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

LQFP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....40°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....8°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DDIO} = +3.3V, V_{DDC} = V_{DD} = +1.2V, V_{SS} = 0, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-SUPPLY CHARACTERISTICS						
Digital Supply Voltage Range	V_{DDIO}		3.0	3.3	3.6	V
Core Supply Voltage Range	V_{DDC}		1.14	1.2	1.32	V
PLL Supply Voltage Range	V_{DD}	Pins 15 and 50	1.14	1.2	1.32	V
Operating Supply Current	$I_{OPERATING}$	V_{DDIO} supply current		25		mA
		V_{DDC} supply current		40	70	
		V_{DD} supply current		1	3	
Idle Mode Current	I_{IDLE}	V_{DDIO} supply current		25		mA
		V_{DDC} supply current		12		
		V_{DD} supply current		1		
Stop Mode Current	I_{STOP}	V_{DDIO} supply current		2		mA
		V_{DDC} supply current		1.8		
		V_{DD} supply current		0.2		
Output Voltage High	V_{OH}	I_{OH} = -5mA	2.4			V
		I_{OH} = -8mA (pins 55 and 57)	2.4			
Output Voltage Low	V_{OL}	I_{OI} = 5mA			0.4	V
		I_{OI} = 8mA (pins 55 and 57)			0.4	
LOGIC INPUT CHARACTERISTICS						
Input High Voltage	V_{IH}		2		5.5	V
		XTAL1S, XTAL1A	2		3.6	
Input Low Voltage	V_{IL}		-0.3		+0.8	V
Input Capacitance	C_{IN}	XTAL1S and XTAL1A		3		pF
Input Leakage current	I_{IN}	Internal pullup disabled	-10		+10	µA
GPIO Pullup Resistance	R_{PU}	Internal pullup enabled	25	45	60	kΩ

AC Electrical Characteristics

(V_{DDIO} = +3.3V, V_{DDC} = V_{DD} = +1.2V, V_{SS} = 0, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
External Crystal/Input Frequency	$1/t_{XTAL}$	ESR < 90Ω for 19.2MHz (Note 4)	2	19.2	30	MHz
External Crystal/Clock Tolerance		(Note 4)		25		ppm
CPU Clock Frequency	$1/t_{CPU}$	As configured by G3-PLC firmware (Note 4)			76.8	MHz
AFE Clock Frequency	$1/t_{AFE}$	As configured by G3-PLC firmware (Note 4)			48	MHz
UART Baud Rate		As configured by G3-PLC firmware (Notes 3 and 4)		115,200	1/16 x t_{CPU}	bps
SPI MASTER (Flash Bootloader, See Figure 6)						
SPI Master Operating Frequency	$1/t_{MCK}$	Flash boot after POR (Note 4)			1/2 x t_{XTAL}	MHz
		User programmable after bootstrap (Note 4)			1/ 2 x t_{CPU}	
I/O Rise/Fall Time	t_{MRF}	C_L = 100pF, pullup = 560Ω			5	ns
SCLK Output Pulse Width High/ Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$ - t_{RF}			ns
MOSI Output Valid to SCLK Sample Edge	t_{MOH}	MOSI setup	$t_{MCK}/2$ - t_{RF}			ns
MOSI Output Hold after SCLK Last Sample Edge	t_{MOV}		$t_{MCK}/2$ - t_{RF}			ns
SCLK Last Sample Edge to MOSI Output Change	t_{MLH}	MOSI last hold			t_{MCK} + t_{RF}	ns
MISO Input Valid to SCLK Sample Edge	t_{MIS}	MISO setup	10			ns
MISO Input Hold After SCLK Sample Edge	t_{MIH}		0			ns
SPI SLAVE (See Figure 7)						
SPI Slave Operating Frequency	$1/t_{SCK}$	(Note 4)			1/8 x t_{CPU}	MHz
I/O Rise/Fall Time	t_{SRF}	C_L = 100pF, pullup = 560Ω			5	ns
SCLK Input Pulse Width High/ Low	t_{SCH}, t_{SCL}		t_{CPU}			ns
SSEL Active to First Shift Edge	t_{SSE}		0			ns
MOSI Input to SCLK Sample Edge Rise/Fall Setup	t_{SIS}		t_{CPU}			ns

AC Electrical Characteristics (continued)

(V_{DDIO} = +3.3V, V_{DDC} = V_{DD} = +1.2V, V_{SS} = 0, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MOSI Input from SCLK Sample Edge Transition Hold	t_{SIH}		t_{CPU}			ns
MISO Output Valid after SCLK Shift Edge Transition	t_{SOV}				4 x t_{CPU}	ns
SSEL Inactive to Next SSEL Asserted	t_{SSH}		2 x t_{CPU}			ns
SCLK Inactive to SSEL Deasserted	t_{SD}		3 x t_{CPU}			ns
MISO Output Disabled After SSEL Edge Deasserted	t_{SLH}		4 x t_{CPU}			ns
AFE INTERFACE SERIAL MODE (See Figure 8)						
AFE Interface Operating Frequency	$1/t_{TRCK}$	(Note 5)			48	MHz
Clock Rise/Fall Time	t_{CRF}	C_L = 100pF			5	ns
RXCLK/TXCLK Output Pulse Width High/Low	t_{RCH}, t_{RCL}		0.4 x t_{TRCK}		0.6 x t_{TRCK}	ns
SDI Input Setup to RXCLK Active Edge	t_{RIS}		6			ns
SDI Input Hold After RXCLK Active Edge	t_{RIH}		1			ns
RXEN/TXEN Inactive Level Output Pulse Width	t_{TREW}		0.8 x t_{TRCK}	t_{TRCK}	1.2 x t_{TRCK}	ns
RXCLK/TXCLK to RXEN/TXEN Active	t_{TREDF}		0		10	ns
RXCLK/TXCLK to RXEN/TXEN Inactive	t_{TREDR}		0		10	ns
TXCLK to SDO Output	t_{TOD}		0		10	ns

Note 3: Typical values are measured at T_A = +25°C, V_{DDC} = 1.2V.
Note 4: Guaranteed by design.
Note 5: The maximum operating frequency is 20MHz when paired with the MAX2991.

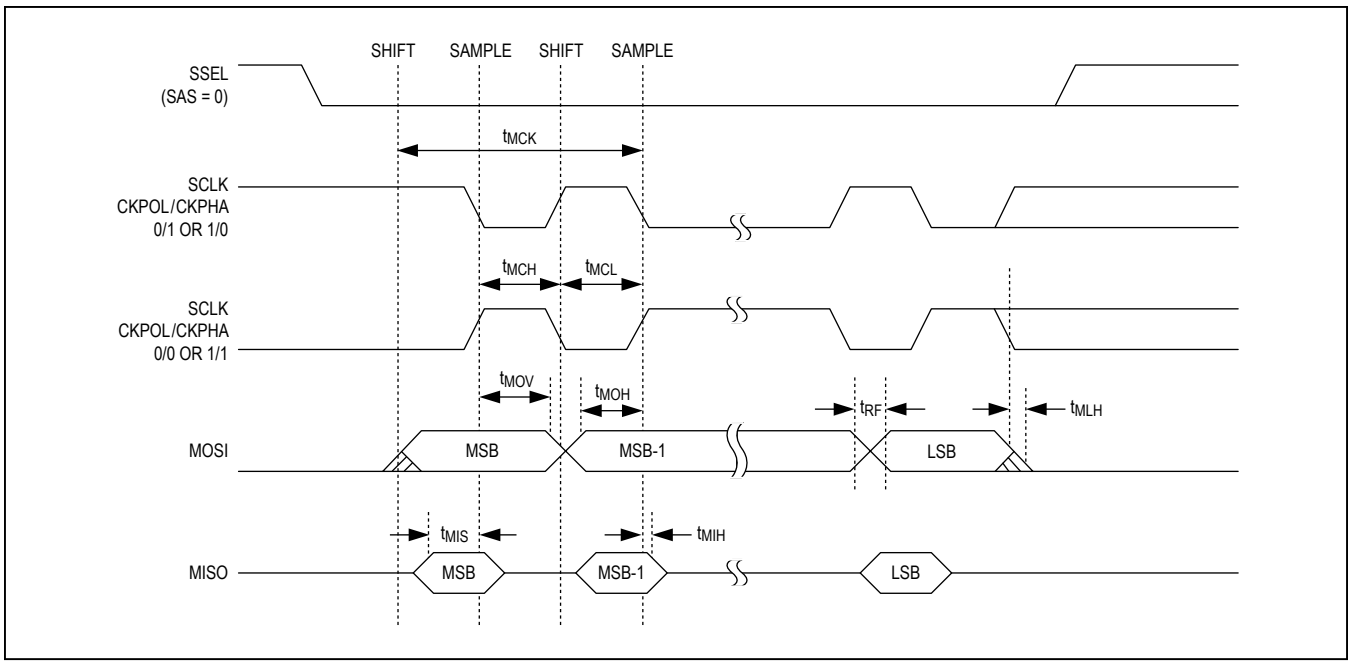


Figure 6. SPI Master Timing Diagram

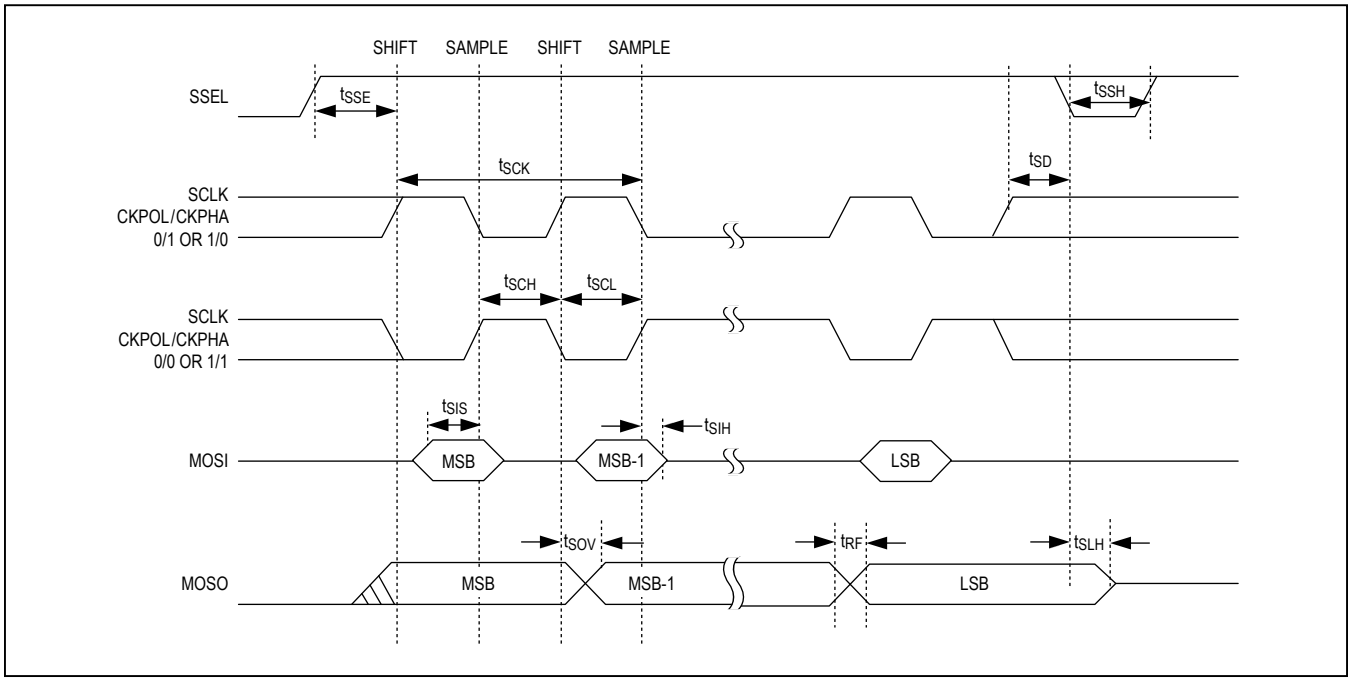


Figure 7. SPI Slave Timing Diagram

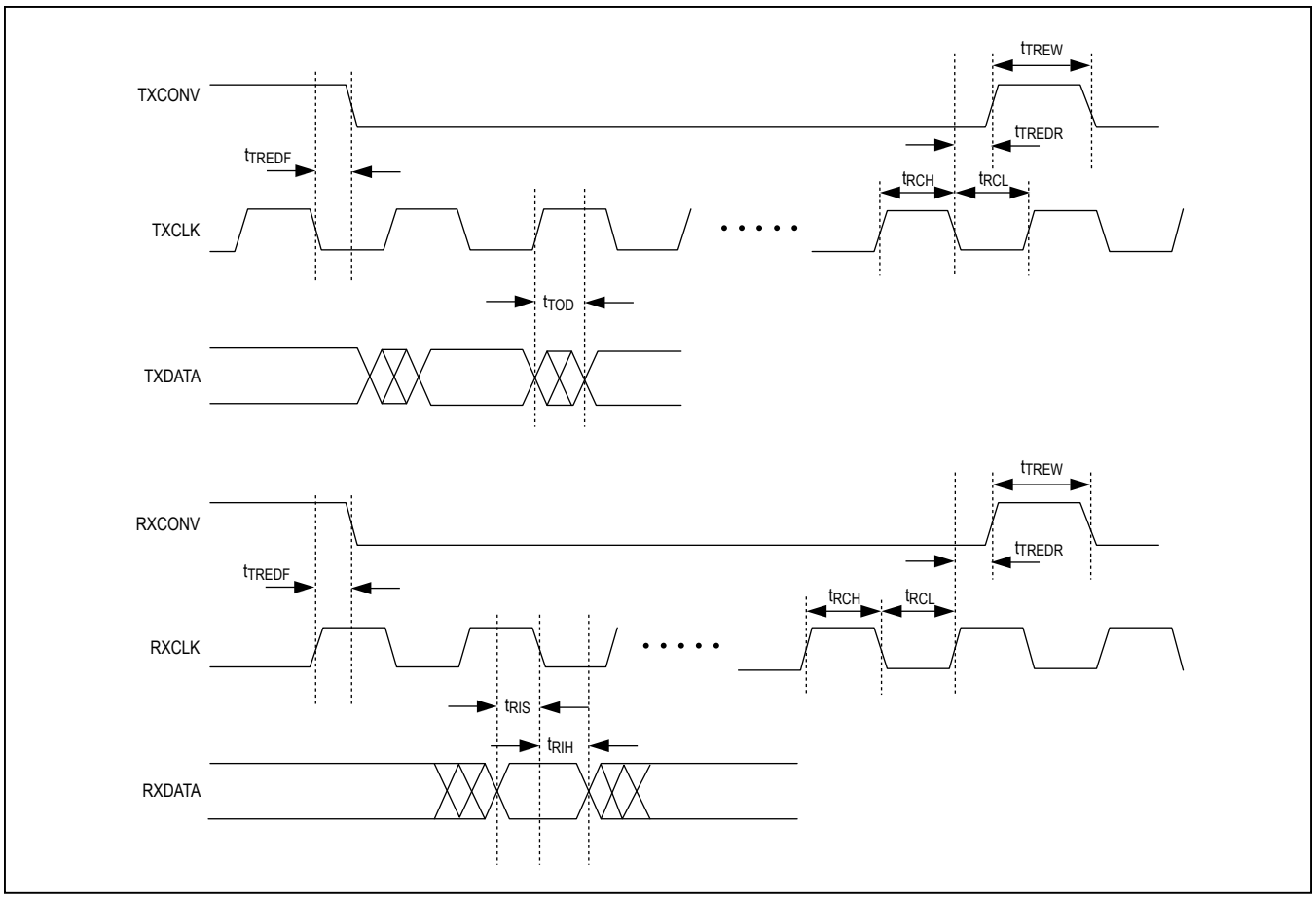


Figure 8. AFE Timing Diagram

Applications Information

The MAX2992 is a powerline communications device that transports information from the application layer across a powerline network. In a typical application, the MAX2992 is used with an external host processor that handles application layers and an IPV6 stack. For instance, in a metering application, an external host processor that is connected to the MAX2992 using the UART or SPI interface processes metering data and encapsulates the processed data into IPV6 packets to be transported over the AC line. Additionally, the host implements interface primitives to communicate to the MAX2992. These primitives direct data transfer as well as status and control commands between the host and the MAX2992. Refer to the *MAX2992 G3-PLC Interface Guide* for a description of the interface primitives.

External Crystal Requirements

The MAX2992 accepts crystals of various designs to set the clock frequency. For example, use a crystal with a maximum ESR of 1kΩ and C_L of 20pF between 2MHz and 6MHz. Use a crystal with a maximum ESR of 160Ω and C_L of 16pF between 6MHz and 10MHz. Use a crystal with a maximum ESR of 90Ω and C_L of 12pF between 10MHz and 20MHz. Use a crystal with a maximum ESR of 40Ω and C_L of 8pF between 20MHz and 30MHz.

External Flash Requirements

An external flash device is required for the automatic bootstrap from the external flash option (see the *Boot Options* section). The external flash supported by the MAX2992 for booting is the AT45DB021D.

Network Support

Depending on the application requirements, the MAX2992 can use various network topologies. In a star topology, communication is established between devices and a single central controller. Applications such as industrial control and monitoring, sensor networks, asset and inventory tracking, and security benefit from the star topology.

The MAX2992 can also operate in a tree network topology where a controller communicates with devices in the network either directly or by having messages forwarded by other devices in the network. Applications such as metering and lighting automation benefits from the tree network topology.

The MAX2992 supports peer-to-peer mesh network topologies. In peer-to-peer mesh networks, two devices communicate with each other using other devices as forwarders without either of the devices in the network being a controller.

MAX2992 Routing

The MAX2992 network of devices discovers routes among the devices in the network. A route is discovered by a device sending a route request message. The route request message is sent by a device when the device does not know how to route its message to the desired device. Every device in the network except the target device forwards the route request message at least once.

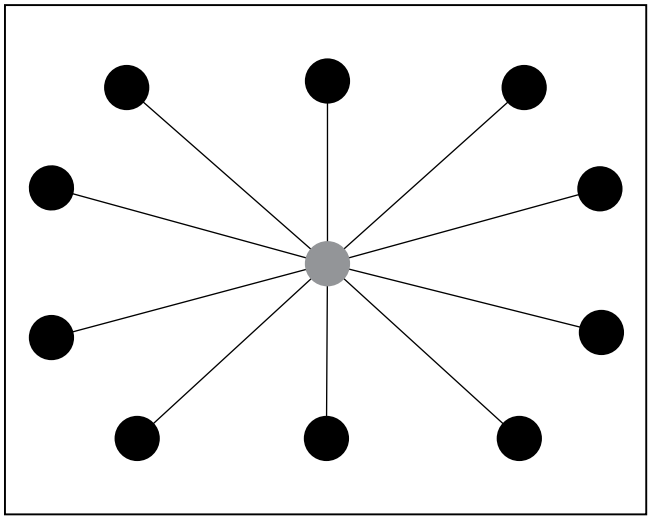


Figure 9. Star Network Topology

When a device receives a route request message, it calculates the route cost required for the message to get to it. It stores that route cost and sends on the route request message with the route cost it calculated. Since there are many devices forwarding the route request message, devices are likely to receive more than one route request messages to support the creation of the same route. The redundant copies of the message have the same or higher calculated route cost. All the redundant copies are dropped. When the message forwarding is complete, the devices along the best path have the lowest route cost back to the route request originator in their memory. Figure 12 shows the route generated in bold by the route request that makes up the best path from the requester to the target. The lighter lines show messages that are not on the optimal path.

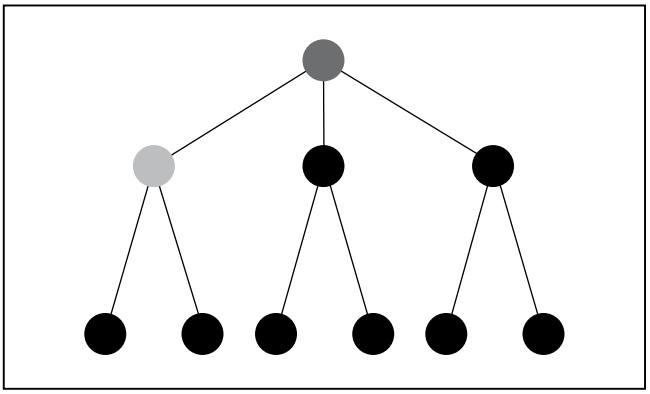


Figure 10. Tree Network Topology

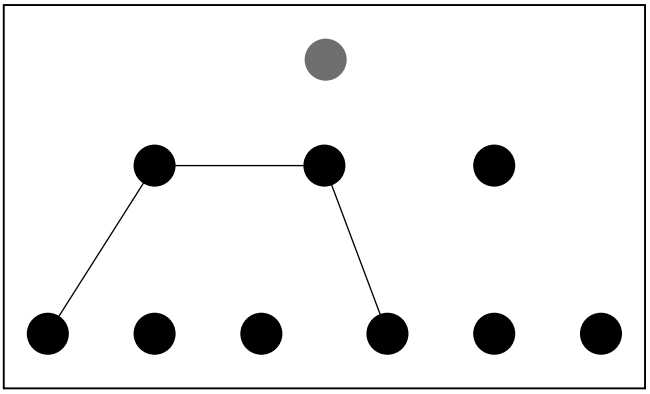


Figure 11. Peer-to-Peer Network Topology

When the route request message reaches the target device, it broadcasts a route reply message. This message includes the lowest route cost from the requestor it received. Other devices update the message and rebroadcast it if the route reply message contains a route cost from the requester that is more than the route cost back to the requester in their memory. Each device updates its routing table with the path that is the lowest route cost from the target. Figure 13 shows the route reply messages generated in this example. The MAX2992 builds an optimal route from device A to device B.

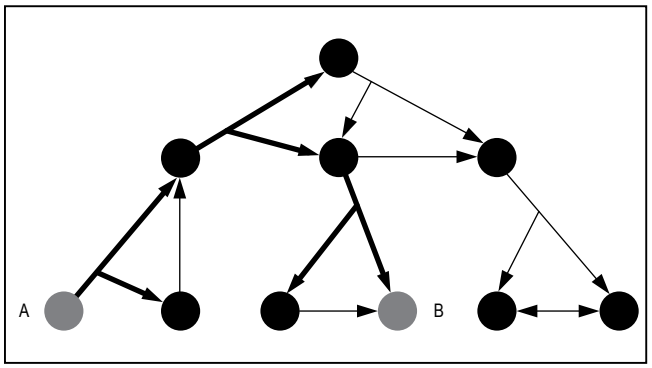


Figure 12. Route Request Message Flow

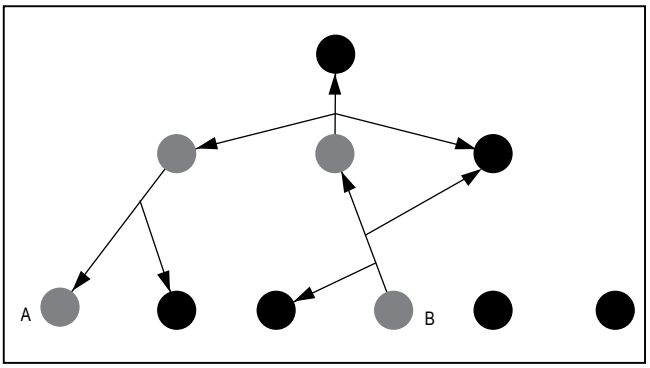


Figure 13. Route Reply Message Flow

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX2992ECB+T	-40°C to +85°C	64 LQFP
MAX2992GCB+	-40°C to +85°C	64 LQFP
MAX2992GCB+T	-40°C to +85°C	64 LQFP

+Denotes lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
64 LQPF	C64-8	21-0083	90-0141

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/11	Initial release	—
1	4/14	Updated *General Description*, *Benefits and Features*, *Ordering Information*, *Pin Description*, *Electrical Characteristics* table, *AC Electrical Characteristics* table sections and Table 1	1, 11, 18, 20, 21

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