

### FEATURES

- Yaw rate gyroscope with range scaling
  - ±80°/sec, ±160°/sec, and ±320°/sec settings
- No external configuration required to start data collection
  - Start-up time: 165 ms
  - Sleep mode recovery time: 2.5 ms
- Factory-calibrated sensitivity and bias
  - ADIS16265 calibration temperature range: -40°C to +85°C
  - ADIS16260 calibration temperature: +25°C
- SPI-compatible serial interface
- Relative angle displacement output
- Embedded temperature sensor
- Programmable operation and control
  - Automatic and manual bias correction controls
  - Sensor bandwidth selection: 50 Hz/330 Hz
  - Sample rate: 256 SPS/2048 SPS settings
  - Bartlett window FIR filter length, number of taps
  - Digital I/O: data ready, alarm indicator, general-purpose
  - Alarms for condition monitoring
  - Sleep mode for power management
  - DAC output voltage
  - Single-command self-test
- Single-supply operation: 4.75 V to 5.25 V
  - 3.3 V compatible digital lines
- 2000 g shock survivability
- Operating temperature range: -40°C to +105°C

### APPLICATIONS

- Platform control and stabilization
- Navigation
- Medical instrumentation
- Robotics

### GENERAL DESCRIPTION

The ADIS16260 and the ADIS16265 are programmable digital gyroscopes that combine industry-leading MEMS and signal processing technology in a single compact package. They provide accuracy performance that would require full motion calibration with any other MEMS gyroscope in their class. When power is applied, the ADIS16260 and the ADIS16265 automatically start up and begin sampling sensor data, without requiring configuration commands from a system processor. An addressable register structure and a common serial peripheral interface (SPI) provide simple access to sensor data and configuration settings. Many digital processor platforms support the SPI with simple firmware-level instructions.

The ADIS16260 and the ADIS16265 provide several programmable features for in-system optimization. The sensor bandwidth switch (50 Hz and 330 Hz), Bartlett window FIR filter length, and sample rate settings provide users with controls that enable noise vs. bandwidth optimization. The digital input/output lines offer options for a data ready signal that helps the master processor efficiently manage data coherency, an alarm indicator signal for triggering master processor interrupts, and a general-purpose function for setting and monitoring system-level digital controls/conditions.

The ADIS16260 and the ADIS16265 come in a LGA package (11.2 mm × 11.2mm × 5.5 mm), which supports Pb-free solder reflow assembly, in accordance with JEDEC J-STD-020. They have an extended operating temperature range of -40°C to +105°C.

### FUNCTIONAL BLOCK DIAGRAM

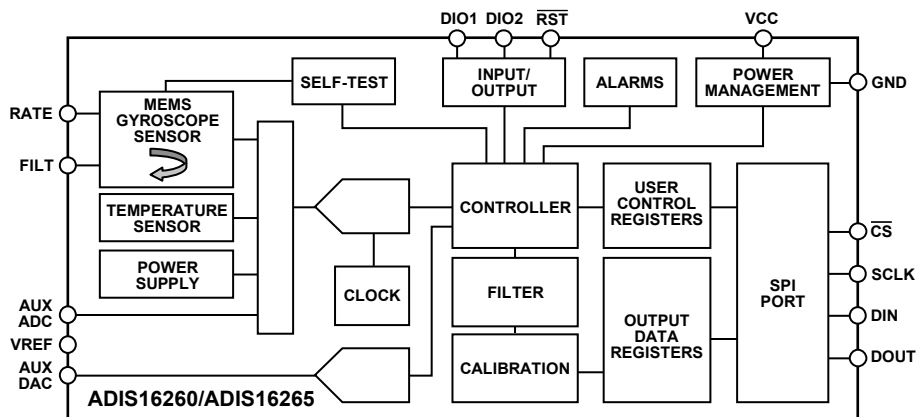


Figure 1.

Rev. F

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## REVISION HISTORY

### 9/2018—Rev. E to Rev. F

|   |    |
|---|----|
| Changes to General Description Section .....  | 1  |
| Changes to Assembly Section, Interface Printed Circuit Board Section, and Figure 19 ..... | 18 |
| Changes to Ordering Guide .....   | 20 |

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|   |    |
|---|----|
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| Change to Bias Optimization Section ..... | 18 |

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|   |    |
|---|----|
| Change to Step 9, Bias Optimization Section ..... | 18 |
|---|----|

### 5/2011—Rev. B to Rev. C

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|--|----|
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|--|----|

### 12/2010—Rev. A to Rev. B

|   |    |
|---|----|
| Changes to Equation in Internal Sample Rate Section ..... | 13 |
| Changes to Figure 15 .....                                | 14 |
| Changes to Bias Optimization Section .....                | 18 |

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|  |           |
|--|-----------|
| Added ADIS16260 .....  | Universal |
| Changes to Features List and General Description Section ..... | 1         |
| Changes to Table 1 .....                                       | 4         |
| Change to Absolute Maximum Ratings Table Section .....         | 6         |
| Changes to Interface Printed Circuit Board Section .....       | 18        |
| Changes to Ordering Guide .....                                | 20        |

### 9/2009—Revision 0: Initial Version

## SPECIFICATIONS

$T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V}$ , angular rate =  $0^{\circ}/\text{sec}$ ,  $\pm 1\text{ g}$ ,  $\pm 320^{\circ}/\text{sec}$  range setting, unless otherwise noted.

Table 1.

| Parameter                         | Test Conditions/Comments  | Min  | Typ       | Max     | Unit                                       |
|-----------------------------------|---|------|-----------|---------|--|
| SENSITIVITY <sup>1</sup>          | Clockwise rotation is positive output                                       |      |           |         |  |
|                                   | 25°C, dynamic range = $\pm 320^{\circ}/\text{sec}^2$                        |      | 0.07326   |         | $^{\circ}/\text{sec}/\text{LSB}$           |
|                                   | 25°C, dynamic range = $\pm 160^{\circ}/\text{sec}$                          |      | 0.03663   |         | $^{\circ}/\text{sec}/\text{LSB}$           |
|                                   | 25°C, dynamic range = $\pm 80^{\circ}/\text{sec}$                           |      | 0.01832   |         | $^{\circ}/\text{sec}/\text{LSB}$           |
| Initial Tolerance                 | 25°C, dynamic range = $\pm 320^{\circ}/\text{sec}$                          |      | $\pm 0.2$ | $\pm 1$ | %  |
| Temperature Coefficient           | ADIS16260   |      | 125       |         | ppm/ $^{\circ}\text{C}$                    |
|                                   | ADIS16265   |      | 25        |         | ppm/ $^{\circ}\text{C}$                    |
| Nonlinearity                      | Best fit straight line  |      | 0.1       |         | % of FS                                    |
| BIAS                              |   |      |           |         |  |
| In-Run Bias Stability             | 25°C, $1\sigma$   |      | 0.007     |         | $^{\circ}/\text{sec}$                      |
| Turn-On-to-Turn-On Bias Stability | 25°C, $1\sigma$   |      | 0.025     |         | $^{\circ}/\text{sec}$                      |
| Angular Random Walk               | 25°C, $1\sigma$   |      | 2         |         | $^{\circ}/\sqrt{\text{hour}}$              |
| Temperature Coefficient           | ADIS16260   |      | 0.03      |         | $^{\circ}/\text{sec}/^{\circ}\text{C}$     |
|                                   | ADIS16265   |      | 0.005     |         | $^{\circ}/\text{sec}/^{\circ}\text{C}$     |
| Linear Acceleration Effect        | Any axis  |      | 0.2       |         | $^{\circ}/\text{sec}/\text{g}$             |
| Voltage Sensitivity               | $V_{CC} = 4.75\text{ V}$ to $5.25\text{ V}$                                 |      | 0.5       |         | $^{\circ}/\text{sec}/\text{V}$             |
| NOISE PERFORMANCE                 |   |      |           |         |  |
| Output Noise                      | 25°C, $\pm 320^{\circ}/\text{sec}$ range, no filtering, 50 Hz, 256 SPS      |      | 0.4       |         | $^{\circ}/\text{sec rms}$                  |
|                                   | 25°C, $\pm 320^{\circ}/\text{sec}$ range, no filtering, 330 Hz, 2048 SPS    |      | 0.9       |         | $^{\circ}/\text{sec rms}$                  |
|                                   | 25°C, $\pm 160^{\circ}/\text{sec}$ range, 4-tap filter setting, 50 Hz       |      | 0.2       |         | $^{\circ}/\text{sec rms}$                  |
|                                   | 25°C, $\pm 80^{\circ}/\text{sec}$ range, 16-tap filter setting, 50 Hz       |      | 0.1       |         | $^{\circ}/\text{sec rms}$                  |
| Rate Noise Density                | 25°C, $f = 25\text{ Hz}$ , $\pm 320^{\circ}/\text{sec}$ range, no filtering |      | 0.044     |         | $^{\circ}/\text{sec}/\sqrt{\text{Hz rms}}$ |
| FREQUENCY RESPONSE                |   |      |           |         |  |
| 3 dB Bandwidth                    | SENS_AVG[7] = 0   |      | 50        |         | Hz   |
|                                   | SENS_AVG[7] = 1   |      | 330       |         | Hz   |
| Sensor Resonant Frequency         |   |      | 14        |         | kHz  |
| SELF-TEST STATE                   |   |      |           |         |  |
| Change for Positive Stimulus      | $320^{\circ}/\text{sec}$ dynamic range setting                              | +575 | +1100     | +1500   | LSB  |
| Change for Negative Stimulus      | $320^{\circ}/\text{sec}$ dynamic range setting                              | -575 | -1100     | -1500   | LSB  |
| Internal Self-Test Cycle Time     |   |      | 25        |         | ms   |
| ADC INPUT                         |   |      |           |         |  |
| Resolution                        |   |      | 12        |         | Bits                                       |
| Integral Nonlinearity             |   |      | $\pm 2$   |         | LSB  |
| Differential Nonlinearity         |   |      | $\pm 1$   |         | LSB  |
| Offset Error                      |   |      | $\pm 4$   |         | LSB  |
| Gain Error                        |   |      | $\pm 2$   |         | LSB  |
| Input Range                       |   | 0    |           | 2.5     | V  |
| Input Capacitance                 | During acquisition  |      | 20        |         | pF   |
| ON-CHIP VOLTAGE REFERENCE         |   |      |           |         |  |
| Accuracy                          | 25°C  | -10  | 2.5       | +10     | V  |
| Temperature Coefficient           |   |      | $\pm 40$  |         | ppm/ $^{\circ}\text{C}$                    |
| Output Impedance                  |   |      | 70        |         | $\Omega$                                   |

| Parameter                         | Test Conditions/Comments  | Min    | Typ       | Max      | Unit     |
|-----------------------------------|---|--------|-----------|----------|----------|
| DAC OUTPUT                        | 5 k $\Omega$ /100 pF to GND   |        |           |          |          |
| Resolution                        |   |        | 12        |          | Bits     |
| Relative Accuracy                 | For Code 101 to Code 4095   |        | 4         |          | LSB      |
| Differential Nonlinearity         |   |        | 1         |          | LSB      |
| Offset Error                      |   |        | $\pm 5$   |          | mV       |
| Gain Error                        |   |        | $\pm 0.5$ |          | %        |
| Output Range                      |   | 0      |           | 2.5      | V        |
| Output Impedance                  |   |        | 2         |          | $\Omega$ |
| Output Settling Time              |   |        | 10        |          | $\mu$ s  |
| LOGIC INPUTS                      | Internal 3.3 V interface  |        |           |          |          |
| Input High Voltage, $V_{INH}$     |   | 2.0    |           |          | V        |
| Input Low Voltage, $V_{INL}$      |   |        |           | 0.8      | V        |
| Logic 1 Input Current, $I_{INH}$  | $V_{IH} = 3.3$ V  |        | $\pm 0.2$ | $\pm 10$ | $\mu$ A  |
| Logic 0 Input Current, $I_{INL}$  | $V_{IL} = 0$ V  |        |           |          | $\mu$ A  |
| All Except $\overline{RST}$       |   |        | -40       | -60      | $\mu$ A  |
| $\overline{RST}$                  | The $\overline{RST}$ pin has an internal pull-up.   |        | -1        |          | mA       |
| Input Capacitance, $C_{IN}$       |   |        | 10        |          | pF       |
| DIGITAL OUTPUTS                   | Internal 3.3 V interface  |        |           |          |          |
| Output High Voltage, $V_{OH}$     | $I_{SOURCE} = 1.6$ mA   | 2.4    |           |          | V        |
| Output Low Voltage, $V_{OL}$      | $I_{SINK} = 1.6$ mA   |        |           | 0.4      | V        |
| SLEEP TIMER                       |   |        |           |          |          |
| Timeout Period <sup>3</sup>       |   | 0.5    |           | 128      | sec      |
| START-UP TIME                     |   |        |           |          |          |
| Initial Start-Up Time             |   |        | 165       |          | ms       |
| Sleep Mode Recovery               |   |        | 2.5       |          | ms       |
| Flash Update Time                 |   |        | 50        |          | ms       |
| Flash Test Process Time           | Normal mode, $SMPL\_PRD[7:0] \leq 0x07$<br>Low power mode, $SMPL\_PRD[7:0] \geq 0x08$               |        | 18        |          | ms       |
|                                   |   |        | 70        |          | ms       |
| FLASH MEMORY                      |   |        |           |          |          |
| Endurance <sup>4</sup>            |   | 20,000 |           |          | Cycles   |
| Data Retention <sup>5</sup>       | $T_J = 55^\circ$ C  | 10     |           |          | Years    |
| CONVERSION RATE                   |   |        |           |          |          |
| Minimum Conversion Time           | $SMPL\_PRD[7:0] = 0x00$   |        | 0.488     |          | ms       |
| Maximum Conversion Time           | $SMPL\_PRD[7:0] = 0xFF$   |        | 7.75      |          | sec      |
| Maximum Throughput Rate           | $SMPL\_PRD[7:0] = 0x00$   |        | 2048      |          | SPS      |
| Minimum Throughput Rate           | $SMPL\_PRD[7:0] = 0xFF$   |        | 0.129     |          | SPS      |
| POWER SUPPLY                      |   |        |           |          |          |
| Operating Voltage Range, $V_{CC}$ |   | 4.75   | 5.0       | 5.25     | V        |
| Power Supply Current              | Low power mode, $SMPL\_PRD[7:0] \geq 0x08$<br>Normal mode, $SMPL\_PRD[7:0] \leq 0x07$<br>Sleep mode |        | 17        |          | mA       |
|                                   |   |        | 41        |          | mA       |
|                                   |   |        | 350       |          | $\mu$ A  |

<sup>1</sup> ADIS16260/ADIS16265 characterization data represents  $\pm 4\sigma$  to fall within the  $\pm 1\%$  limit.

<sup>2</sup> The maximum guaranteed measurement range is  $\pm 320^\circ$ /sec. The sensor outputs will measure beyond this range, but performance is not assured.

<sup>3</sup> Guaranteed by design.

<sup>4</sup> Endurance is qualified as per JEDEC Standard 22, Method A117, and measured at  $-40^\circ$ C,  $+25^\circ$ C,  $+85^\circ$ C, and  $+125^\circ$ C.

<sup>5</sup> Retention lifetime equivalent at a junction temperature ( $T_J$ ) of  $55^\circ$ C, as per JEDEC Standard 22, Method A117. Retention lifetime decreases with junction temperature.

**TIMING SPECIFICATIONS**

T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = 5.0 V, unless otherwise noted.

**Table 2.**

| Parameter             | Description  | Normal Mode<br>(SMPL_PRD[7:0] ≤ 0x07, f <sub>s</sub> ≥ 64 Hz) |     |                  | Low Power Mode<br>(SMPL_PRD[7:0] ≥ 0x08, f <sub>s</sub> ≤ 56.9 Hz) |     |                  | Unit |
|-----------------------|--|---|-----|------------------|--|-----|------------------|------|
|                       |  | Min <sup>1</sup>  | Typ | Max <sup>1</sup> | Min <sup>1</sup>   | Typ | Max <sup>1</sup> |      |
| f <sub>SCLK</sub>     | Serial clock   | 0.01  |     | 2.5              | 0.01   |     | 1.0              | MHz  |
| t <sub>DATARATE</sub> | Data rate period                                       | 32  |     |                  | 42   |     |                  | μs   |
| t <sub>STALL</sub>    | Stall period between data                              | 9   |     |                  | 12   |     |                  | μs   |
| t <sub>CS</sub>       | Chip select to clock edge                              | 48.8  |     |                  | 48.8   |     |                  | ns   |
| t <sub>DAV</sub>      | Data output valid after SCLK falling edge <sup>2</sup> |   |     | 100              |  |     | 100              | ns   |
| t <sub>DSU</sub>      | Data input setup time before SCLK rising edge          | 24.4  |     |                  | 24.4   |     |                  | ns   |
| t <sub>DHD</sub>      | Data input hold time after SCLK rising edge            | 48.8  |     |                  | 48.8   |     |                  | ns   |
| t <sub>DF</sub>       | Data output fall time                                  |   | 5   | 12.5             |  | 5   | 12.5             | ns   |
| t <sub>DR</sub>       | Data output rise time                                  |   | 5   | 12.5             |  | 5   | 12.5             | ns   |
| t <sub>SFS</sub>      | CS high after SCLK edge <sup>3</sup>                   | 5   |     |                  | 5  |     |                  | ns   |

<sup>1</sup> Guaranteed by design; not production tested.

<sup>2</sup> The MSB presents an exception to this parameter. The MSB clocks out on the falling edge of CS. The rest of the DOUT bits are clocked after the falling edge of SCLK and are governed by this specification.

<sup>3</sup> This parameter may need to be expanded to allow for proper capture of the LSB. After CS goes high, the DOUT line goes into a high impedance state.

**Timing Diagrams**

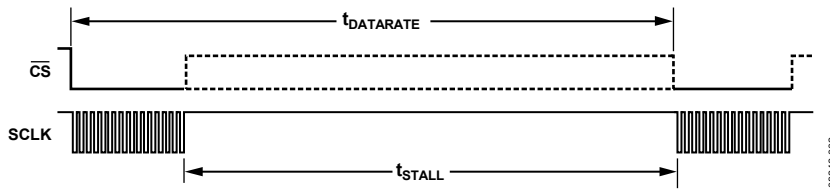


Figure 2. SPI Chip Select Timing

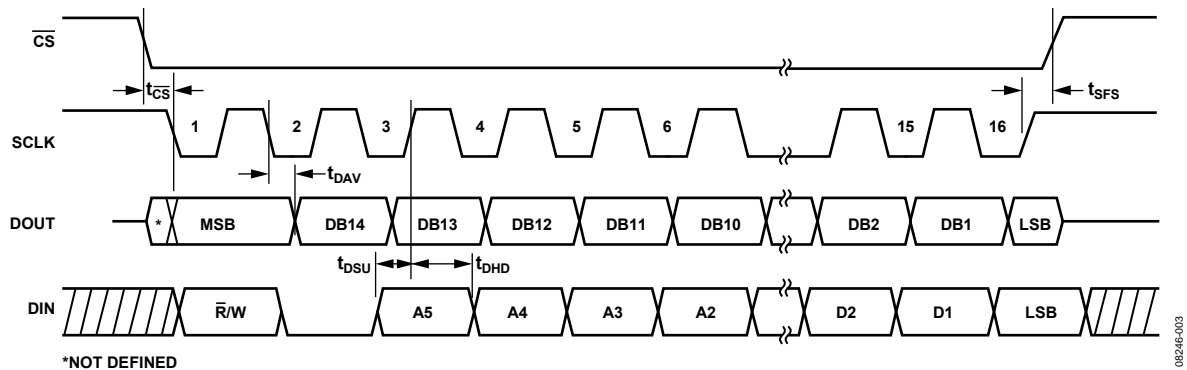


Figure 3. SPI Timing (Using SPI Settings Typically Identified as CPOL = 1, CPHA = 1)

## ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter                                | Rating           |
|--|------------------|
| Acceleration                             |                  |
| Any Axis, Unpowered, 0.5 ms              | 2000 <i>g</i>    |
| Any Axis, Powered, 0.5 ms                | 2000 <i>g</i>    |
| VCC to GND                               | −0.3 V to +6.0 V |
| Digital Input/Output Voltage to GND      | −0.3 V to +5.3 V |
| Analog Inputs to GND                     | −0.3 V to +3.5 V |
| Operating Temperature Range <sup>1</sup> | −40°C to +125°C  |
| Storage Temperature Range <sup>1</sup>   | −65°C to +150°C  |

<sup>1</sup> Extended exposure to temperatures outside the temperature range of −40°C to +85°C can adversely affect the accuracy of the factory calibration. For best accuracy, store the part within the temperature range of −40°C to +85°C.

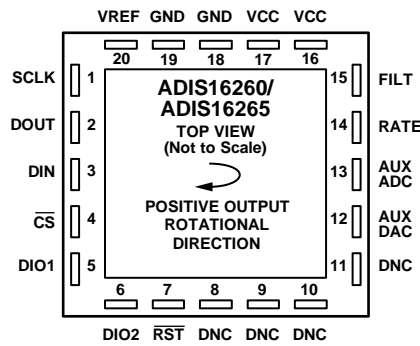
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



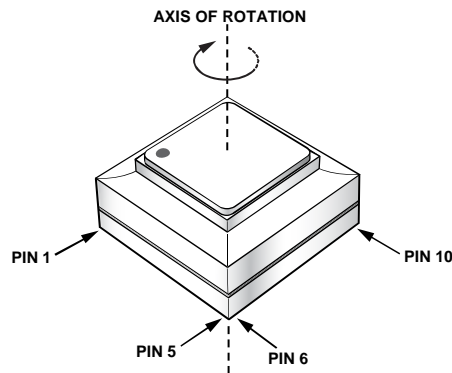
**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



**NOTES**  
 1. DNC = DO NOT CONNECT.  
 2. THE PINS CANNOT BE SEEN FROM THE TOP. THIS LOOK-THROUGH VIEW OF THEIR LOCATION IS OFFERED FOR REFERENCE IN DEVELOPING PCB PATTERNS.

Figure 4. Pin Configuration



**NOTES**  
 1. ARROW INDICATES THE DIRECTION OF ROTATION THAT PRODUCES A POSITIVE RESPONSE IN THE GYRO\_OUT REGISTER.

Figure 5. Axial Orientation

Table 4. Pin Function Descriptions

| Pin No.      | Mnemonic         | Type <sup>1</sup> | Description   |
|--------------|------------------|-------------------|---|
| 1            | SCLK             | I                 | SPI Serial Clock.   |
| 2            | DOUT             | O                 | SPI Data Output. Clocks output on SCLK falling edge.                |
| 3            | DIN              | I                 | SPI Data Input. Clocks input on SCLK rising edge.                   |
| 4            | $\overline{CS}$  | I                 | SPI Chip Select. Active low.  |
| 5, 6         | DIO1, DIO2       | I/O               | Configurable Digital Input/Output.                                  |
| 7            | $\overline{RST}$ | I                 | Reset. Active low.  |
| 8, 9, 10, 11 | DNC              |                   | Do Not Connect.   |
| 12           | AUX DAC          | O                 | Auxiliary DAC Output.   |
| 13           | AUX ADC          | I                 | Auxiliary ADC Input.  |
| 14           | RATE             | O                 | Rate Output. For bandwidth reduction only; output is not specified. |
| 15           | FILT             | I                 | Filter Terminal.  |
| 16, 17       | VCC              | S                 | 5.0 V Power Supply.   |
| 18, 19       | GND              | S                 | Ground.   |
| 20           | VREF             | O                 | Precision Reference Output.   |

<sup>1</sup> I = input, I/O = input/output, O = output, S = supply.

### TYPICAL PERFORMANCE CHARACTERISTICS

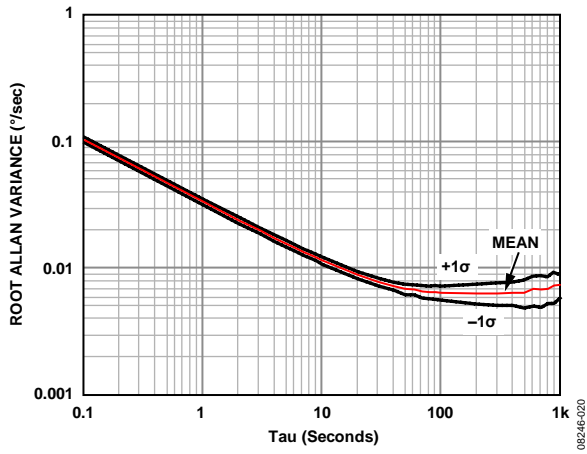


Figure 6. Gyroscope Allan Variance



## THEORY OF OPERATION

The ADIS16260 and the ADIS16265 integrate a MEMS gyroscope with data sampling, signal processing, and calibration functions, along with a simple user interface. This sensing system collects data autonomously and makes it available to any processor system that supports a 4-wire serial peripheral interface (SPI).

### SENSING ELEMENT

The sensing element operates on the principle of a resonator gyro. Two polysilicon sensing structures each contain a dither frame that is electrostatically driven to resonance, producing the necessary velocity element to produce a Coriolis force during angular rate. At two of the outer extremes of each frame, orthogonal to the dither motion, movable fingers are placed between fixed pickoff fingers to form a capacitive pickoff structure that senses Coriolis motion. The resulting signal is fed into a series of gain and demodulation stages that produce the electrical rate signal output. The differential structure minimizes the response to linear acceleration (gravity, vibration, and so on) and to EMI.

### DATA SAMPLING AND PROCESSING

The ADIS16260 and the ADIS16265 run autonomously, based on the configuration in the user control registers. The analog gyroscope signal feeds into an analog-to-digital converter (ADC) stage, which passes digitized data into the controller for data processing and register loading. Data processing in the embedded controller includes correction formulas, filtering, and checking for preset alarm conditions. The correction formulas are unique for each individual ADIS16260/ADIS16265 and come from the factory characterization of each device over a temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

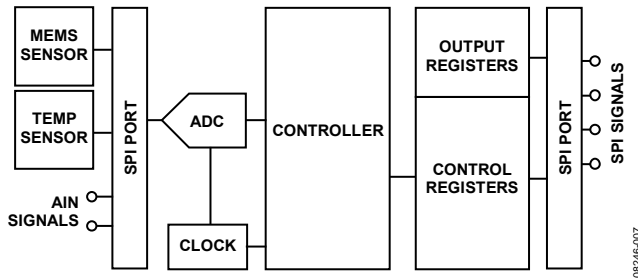


Figure 7. Simplified Sensor Signal Processing Diagram

## USER INTERFACE

### SPI Interface

Data collection and configuration commands both use the SPI, which consists of four wires. The chip select ( $\overline{\text{CS}}$ ) signal activates the SPI interface, and the serial clock (SCLK) signal synchronizes the serial data lines. The serial input data clocks into DIN on the SCLK rising edge, and the serial output data clocks out of DOUT on the SCLK falling edge. Many digital processor platforms support this interface with dedicated serial ports and simple instruction sets.

### User Registers

The user registers provide addressing for all input/output operations on the SPI interface. Each 16-bit register has its own unique bit assignment and has two 7-bit addresses: one for its upper byte and one for its lower byte. Table 7 provides a memory map of the user registers, along with the function of each register.

The control registers use a dual memory structure. The SRAM controls operation while the part is on and facilitates all user configuration inputs. The flash memory provides nonvolatile storage for control registers that have flash backup (see Table 7). Storing configuration data in the flash memory requires a separate command ( $\text{GLOB\_CMD}[3] = 1, \text{DIN} = 0\text{xBE08}$ ). When the device powers on or resets, the flash memory contents are loaded into the SRAM, and the device then starts producing data according to the configuration in the control registers.

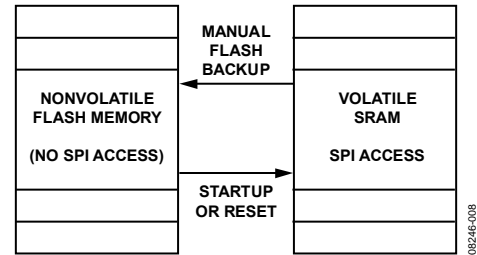


Figure 8. SRAM and Flash Memory Diagram

## BASIC OPERATION

The ADIS16260 and the ADIS16265 require only power, ground, and the four SPI signals to produce data and make it available to an embedded processor. Figure 9 provides a schematic for connecting the ADIS16260 and the ADIS16265 to a SPI-compatible processor and includes one of the configurable digital I/O lines. The MSC\_CTRL[2:0] bits are used to configure this line as a data ready indicator (see the Data Ready I/O Indicator section).

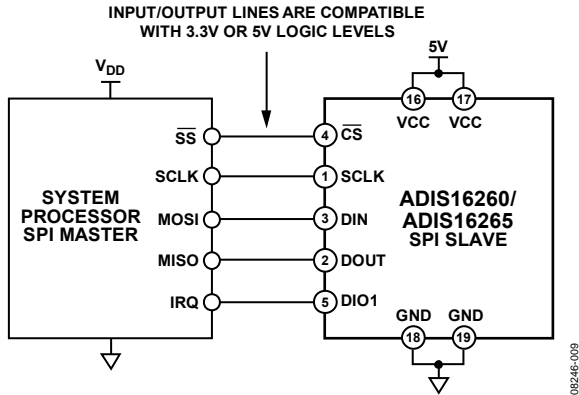


Figure 9. Electrical Connection Diagram

Table 5. Generic Master Processor Pin Names and Functions

| Pin Name | Function                   |
|----------|----------------------------|
| SS       | Slave select               |
| IRQ      | Interrupt request input    |
| MOSI     | Master output, slave input |
| MISO     | Master input, slave output |
| SCLK     | Serial clock               |

The ADIS16260 and the ADIS16265 SPI interface supports full-duplex serial communication (simultaneous transmit and receive) and uses the bit sequence shown in Figure 11. Processor platforms typically support SPI communication with general-purpose serial ports that require some configuration in their control registers. Table 6 provides a list of the most common settings that require attention to initialize the serial port of a processor for communication with the ADIS16260 and the ADIS16265.

Table 6. Generic Master Processor SPI Settings

| Processor Setting        | Description                                       |
|--------------------------|---|
| Master                   | The ADIS16260 and the ADIS16265 operate as slaves |
| SCLK Rate $\leq$ 2.5 MHz | Bit rate setting (SMPL_PRD[7:0] $\leq$ 0x07)      |
| SPI Mode 3               | Clock polarity, phase (CPOL = 1, CPHA = 1)        |
| MSB First Mode           | Bit sequence                                      |
| 16-Bit Mode              | Shift register/data length                        |

User registers govern all data collection and configuration. Table 7 provides a memory map that includes all user registers, along with references to the bit assignment tables that follow the generic bit assignments in Figure 10.

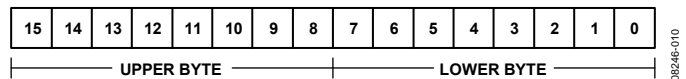
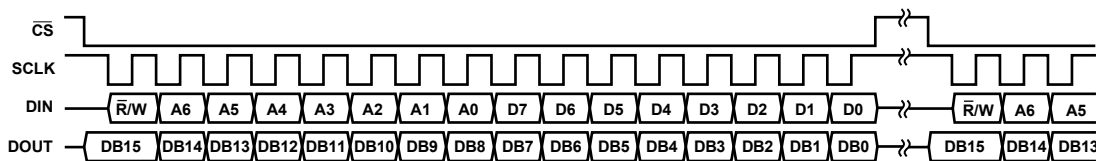


Figure 10. Generic Register Bit Definitions



NOTES

1. DOUT BITS ARE BASED ON THE PREVIOUS 16-BIT SEQUENCE ( $\bar{R}/W = 0$ ).

Figure 11. SPI Communication Bit Sequence

**SPI WRITE COMMANDS**

Master processors write to the control registers, one byte at a time, using the bit sequence shown in Figure 11. Some configurations require writing both bytes to a register, which takes two separate 16-bit sequences, whereas others require only one byte. The programmable registers in Table 7 provide controls for optimizing sensor operation and for starting various automated functions. For example, to start an automatic bias null sequence, set GLOB\_CMD[0] = 1 by writing 0xBE01 to the SPI transmit register of the master processor, which feeds the DIN line. The process starts immediately after the last bit clocks into DIN (16<sup>th</sup> SCLK rising edge).

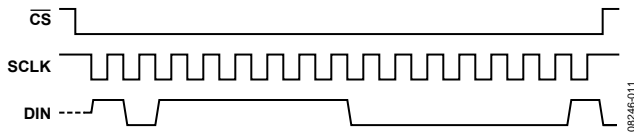


Figure 12. SPI Sequence for Autonull (DIN = 0xBE01)

**SPI READ COMMANDS**

Reading data through the SPI requires two consecutive 16-bit sequences, separated by an appropriate stall time (see Figure 2). The first sequence transmits the read command and address on DIN, and the second receives the resulting data from DOUT. The 7-bit register address can represent either the upper or lower byte address for the target register. For example, when reading the GYRO\_OUT register, the address can be either 0x04 or 0x05. Figure 13 provides a full-duplex mode example of reading the GYRO\_OUT register. In addition, the second SPI segment sets the device up to read TEMP\_OUT on the following SPI segment (not shown in Figure 13).

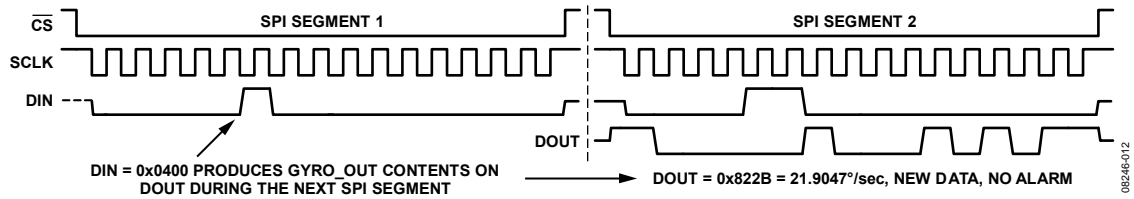


Figure 13. Example SPI Read Sequence ( $\pm 320^\circ/\text{sec}$  Range Setting)

**MEMORY MAP**

All unused memory locations are reserved for future use.

**Table 7. User Register Memory Map**

| Name       | Access     | Flash Backup | Address <sup>1</sup> | Default       | Register Description                                   | Bit Assignments |
|------------|------------|--------------|----------------------|---------------|--|-----------------|
| FLASH_CNT  | Read only  | Yes          | 0x00                 | N/A           | Flash memory write count                               |                 |
| SUPPLY_OUT | Read only  | No           | 0x02                 | N/A           | Output, power supply measurement                       | See Table 9     |
| GYRO_OUT   | Read only  | No           | 0x04                 | N/A           | Output, rate of rotation measurement                   | See Table 10    |
|            |            |              | 0x06 to 0x09         | N/A           | Reserved   |                 |
| AUX_ADC    | Read only  | No           | 0x0A                 | N/A           | Output, analog input channel measurement               | See Table 13    |
| TEMP_OUT   | Read only  | No           | 0x0C                 | N/A           | Output, internal temperature measurement               | See Table 12    |
| ANGL_OUT   | Read/write | No           | 0x0E                 | N/A           | Output, angle displacement                             | See Table 11    |
|            |            |              | 0x10 to 0x13         | N/A           | Reserved   |                 |
| GYRO_OFF   | Read/write | Yes          | 0x14                 | 0x0000        | Calibration, offset/bias adjustment                    | See Table 16    |
| GYRO_SCALE | Read/write | Yes          | 0x16                 | 0x0800        | Calibration, scale adjustment                          | See Table 17    |
|            |            |              | 0x18 to 0x1F         | N/A           | Reserved   |                 |
| ALM_MAG1   | Read/write | Yes          | 0x20                 | 0x0000        | Alarm 1 magnitude/polarity setting                     | See Table 26    |
| ALM_MAG2   | Read/write | Yes          | 0x22                 | 0x0000        | Alarm 2 magnitude/polarity setting                     | See Table 26    |
| ALM_SMPL1  | Read/write | Yes          | 0x24                 | 0x0000        | Alarm 1 dynamic rate of change setting                 | See Table 27    |
| ALM_SMPL2  | Read/write | Yes          | 0x26                 | 0x0000        | Alarm 2 dynamic rate of change setting                 | See Table 27    |
| ALM_CTRL   | Read/write | Yes          | 0x28                 | 0x0000        | Alarm control register                                 | See Table 28    |
|            |            |              | 0x2A to 0x2F         | N/A           | Reserved   |                 |
| AUX_DAC    | Read/write | No           | 0x30                 | 0x0000        | Control, DAC output voltage setting                    | See Table 22    |
| GPIO_CTRL  | Read/write | No           | 0x32                 | N/A           | Control, digital I/O line                              | See Table 20    |
| MSC_CTRL   | Read/write | Yes          | 0x34                 | 0x0000        | Control, data ready, self-test settings                | See Table 21    |
| SMPL_PRD   | Read/write | Yes          | 0x36                 | 0x0001        | Control, internal sample rate                          | See Table 14    |
| SENS_AVG   | Read/write | Yes          | 0x38                 | 0x0402        | Control, dynamic range, filtering                      | See Table 15    |
| SLP_CNT    | Read/write | Yes          | 0x3A                 | 0x0000        | Control, sleep mode initiation                         | See Table 19    |
| DIAG_STAT  | Read only  | No           | 0x3C                 | N/A           | Diagnostic, error flags                                | See Table 25    |
| GLOB_CMD   | Write only | No           | 0x3E                 | N/A           | Control, global commands                               | See Table 18    |
|            |            |              | 0x40 to 0x51         | N/A           | Reserved   |                 |
| LOT_ID1    | Read only  | Yes          | 0x52                 | N/A           | Lot Identification Code 1                              | See Table 31    |
| LOT_ID2    | Read only  | Yes          | 0x54                 | N/A           | Lot Identification Code 2                              | See Table 31    |
| PROD_ID    | Read only  | Yes          | 0x56                 | 0x3F89/0x3F84 | Product identifier; convert to decimal = 16,265/16,260 | See Table 31    |
| SERIAL_NUM | Read only  | Yes          | 0x58                 | N/A           | Serial number  | See Table 31    |

<sup>1</sup> Each register contains two bytes. The address of the lower byte is displayed. The address of the upper byte is equal to the address of the lower byte plus 1.

**PROCESSING SENSOR DATA**

Table 8 provides a summary of the output data registers, which use the bit pattern shown in Figure 14. The ND bit is equal to 1 when the register contains unread data. The EA bit is high when any error/alarm flag in the DIAG\_STAT register is equal to 1.

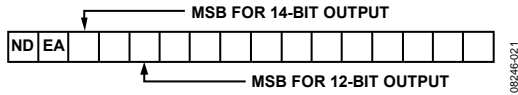


Figure 14. Output Register Bit Assignments

**Table 8. Output Data Register Formats**

| Register              | Bits | Scale        | Reference    |
|-----------------------|------|--------------|--------------|
| SUPPLY_OUT            | 12   | 1.8315 mV    | See Table 9  |
| GYRO_OUT <sup>1</sup> | 14   | 0.07326°/sec | See Table 10 |
| ANGL_OUT              | 14   | 0.03663°     | See Table 11 |
| TEMP_OUT <sup>2</sup> | 12   | 0.1453°C     | See Table 12 |
| AUX_ADC               | 12   | 610.5 μV     | See Table 13 |

<sup>1</sup> Assumes that the scaling is set to ±320°/sec. This factor scales with the range.  
<sup>2</sup> 0x0000 = 25°C (±5°C).

**Table 9. SUPPLY\_OUT Data Format Examples**

| Supply Voltage (V) | Decimal  | Hex   | Binary Output  |
|--------------------|----------|-------|----------------|
| 5.25               | 2867 LSB | 0xB33 | 1011 0011 0011 |
| 5.0 + 0.00183      | 2731 LSB | 0xAAB | 1010 1010 1011 |
| 5.0                | 2730 LSB | 0xAAA | 1010 1010 1010 |
| 5.0 – 0.00183      | 2729 LSB | 0xAA9 | 1010 1010 1001 |
| 4.75               | 2594 LSB | 0xA22 | 1010 0010 0010 |

**Table 10. GYRO\_OUT Data Format Examples**

| Rotation Rate (°/sec) <sup>1</sup> | Decimal   | Hex    | Binary Output     |
|------------------------------------|-----------|--------|-------------------|
| +320                               | +4368 LSB | 0x1110 | 01 0001 0001 0000 |
| +0.07326                           | +1 LSB    | 0x0001 | 00 0000 0000 0001 |
| 0                                  | 0 LSB     | 0x0000 | 00 0000 0000 0000 |
| –0.07326                           | –1 LSB    | 0x3FFF | 11 1111 1111 1111 |
| –320                               | –4368 LSB | 0x2EF0 | 10 1110 1111 0000 |

<sup>1</sup> For the ±320°/sec setting, rate values scale with the range setting.

**Table 11. ANGL\_OUT Data Format Examples**

| Angle <sup>1</sup> | Decimal  | Hex    | Binary Output     |
|--------------------|----------|--------|-------------------|
| 359.9630°          | 9827 LSB | 0x2663 | 10 0110 0110 0011 |
| 359.9264°          | 9826 LSB | 0x2662 | 10 0110 0110 0010 |
| 0.36630°           | 10 LSB   | 0x000A | 00 0000 0000 1010 |
| 0.03663°           | 1 LSB    | 0x0001 | 00 0000 0000 0001 |
| 0°                 | 0 LSB    | 0x0000 | 00 0000 0000 0000 |

<sup>1</sup> 359.963° + 1 LSB is equal to 0x0000.

**Table 12. TEMP\_OUT Data Format Examples**

| Temperature | Decimal  | Hex   | Binary Output  |
|-------------|----------|-------|----------------|
| +105°C      | +551 LSB | 0x227 | 0010 0010 0111 |
| +25.1453°C  | +1 LSB   | 0x001 | 0000 0000 0001 |
| +25°C       | 0 LSB    | 0x000 | 0000 0000 0000 |
| +24.8547°C  | –1 LSB   | 0xFFF | 1111 1111 1111 |
| –40°C       | –447 LSB | 0xE41 | 1110 0100 0001 |

**Table 13. AUX\_ADC Data Format Examples**

| Input (mV) | Decimal  | Hex   | Binary Output  |
|------------|----------|-------|----------------|
| 2500       | 4095 LSB | 0xFFF | 1111 1111 1111 |
| 1200       | 1966 LSB | 0x7AE | 0111 1010 1110 |
| 0.6105     | 1 LSB    | 0x001 | 0000 0000 0001 |
| 0          | 0 LSB    | 0x000 | 0000 0000 0000 |

**OPERATIONAL CONTROLS**

**Internal Sample Rate**

The SMPL\_PRD register controls the internal sample rate using the bit assignments in Table 14. When SMPL\_PRD[7:0] = 0x00, the internal sample rate is 2048 SPS. When SMPL\_PRD[7:0] ≥ 0x01, use the bit definitions in Table 14 and the following equation to calculate the sample rate.

$$f_s = \frac{1}{t_s} = \frac{1}{t_B \times (N_s + 1)}$$

**Table 14. SMPL\_PRD Bit Descriptions**

| Bits   | Description (Default = 0x0001)                          |
|--------|---|
| [15:8] | Not used  |
| 7      | Time base (t <sub>B</sub> ): 0 = 1.953 ms, 1 = 60.54 ms |
| [6:0]  | Increment setting (N <sub>s</sub> )                     |

**Sensor Bandwidth**

The gyroscope signal chain has several filter stages that shape its frequency response. Figure 15 provides a block diagram of each filter stage and Table 15 lists the SENS\_AVG register controls for bandwidth.

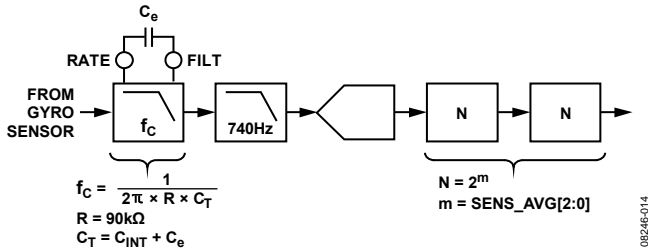


Figure 15. Signal Processing Diagram

**Table 15. SENS\_AVG Bit Descriptions**

| Bits    | Description (Default = 0x0402)   |
|---------|--|
| [15:11] | Not used.  |
| [10:8]  | Measurement range (sensitivity) selection.<br>100 = ±320°/sec (default condition).<br>010 = ±160°/sec, filter taps ≥ 4 (Bits[2:0] ≥ 0x02).<br>001 = ±80°/sec, filter taps ≥ 16 (Bits[2:0] ≥ 0x04). |
| 7       | Primary pole setting (k).<br>1: C <sub>INT</sub> = 0.0047 μF (bandwidth = 330 Hz).<br>0: C <sub>INT</sub> = 0.0377 μF (bandwidth = 50 Hz).   |
| [6:3]   | Not used.  |
| [2:0]   | Number of taps in each stage; value of m in N = 2 <sup>m</sup> .   |

**Digital Filtering**

A programmable low-pass filter provides additional opportunity for noise reduction on the inertial sensor outputs. This filter contains two cascaded averaging filters that provide a Bartlett window, FIR filter response (see Figure 16). For example, set SENS\_AVG[2:0] = 100 (DIN = 0xB804) to set each stage to 16 taps. When used with the default sample rate of 256 SPS, this reduces the bandwidth of the digital filter to approximately 5.2 Hz.

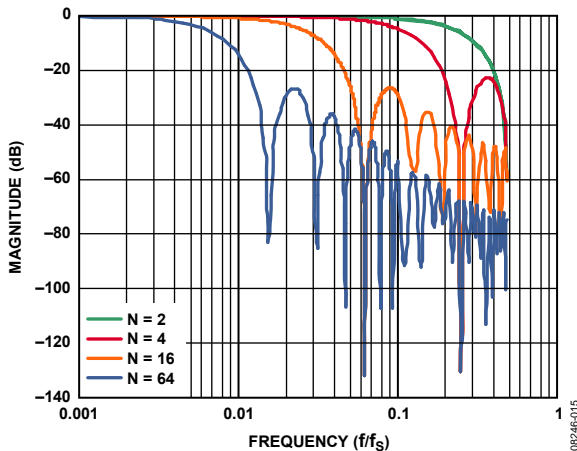


Figure 16. Digital Filter Frequency, Bartlett Window FIR Filter (Phase = N Samples)

**Dynamic Range**

The SENS\_AVG[10:8] bits provide three dynamic range settings for this gyroscope. The lower dynamic range settings (±80°/sec and ±160°/sec) limit the minimum filter tap sizes to maintain resolution. For example, set SENS\_AVG[10:8] = 010 (DIN = 0xB902) for a measurement range of ±160°/sec. Because this setting can influence the filter settings, program SENS\_AVG[10:8] and then SENS\_AVG[2:0] if more filtering is required.

**Calibration**

The GYRO\_OFF and GYRO\_SCALE registers provide user controls for making in-system adjustments to offset and scale factor.

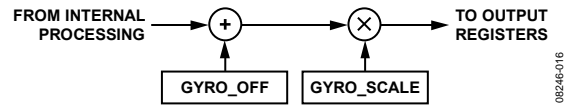


Figure 17. User Calibration Registers

**Table 16. GYRO\_OFF Bit Descriptions**

| Bits    | Description (Default = 0x0000)   |
|---------|--|
| [15:12] | Not used.  |
| [11:0]  | Offset adjustment factor, twos complement format, 0.018315°/sec per LSB.<br>Examples follow:<br>0x000: Add 0°/sec to gyroscope data.<br>0x001: Add 0.018315°/sec to gyroscope data.<br>0x0AA: Add 3.11355°/sec to gyroscope data.<br>0xF0F: Subtract 4.41392°/sec from gyroscope data.<br>0xFFF: Subtract 0.018315°/sec from gyroscope data. |

**Table 17. GYRO\_SCALE Bit Descriptions**

| Bits    | Description (Default = 0x0800)   |
|---------|--|
| [15:12] | Not used.  |
| [11:0]  | Scale adjustment factor, offset binary format, 0.00048828/LSB.<br>Examples follow:<br>0x000: Multiply output by 0.<br>0x7F0: Multiply gyroscope data by 0.99218.<br>0x800: Multiply output by 1.<br>0x8A0: Multiply output by 1.077812.<br>0xFFF: Multiply output by 1.9995. |

### Global Commands

The GLOB\_CMD register provides trigger bits for several functions. Setting the assigned bit to 1 starts each operation, which returns the bit to 0 after completion. For example, set GLOB\_CMD[7] = 1 (DIN = 0xBE80) to execute a software reset, which stops the sensor operation and runs the device through its start-up sequence. This sequence includes loading the control registers with the contents of their respective flash memory locations prior to producing new data.

**Table 18. GLOB\_CMD Bit Descriptions**

| Bits   | Description                          |
|--------|--------------------------------------|
| [15:8] | Not used.                            |
| 7      | Software reset command.              |
| [6:4]  | Not used.                            |
| 3      | Flash update command.                |
| 2      | Auxiliary DAC data latch.            |
| 1      | Factory calibration restore command. |
| 0      | Autonull command.                    |

### Power Management

Setting SMPL\_PRD[7:0]  $\geq$  0x08 also sets the sensor to low power mode. For systems that require lower power dissipation, in-system characterization helps users to quantify the associated performance trade-offs. In addition to sensor performance, low power mode affects SPI data rates (see Table 2). Use SLP\_CNT[7:0] to put the device into sleep mode for a specified period. For example, SLP\_CNT[7:0] = 0x64 (DIN = 0xBA64) puts the ADIS16260 and ADIS16265 to sleep for 50 seconds.

**Table 19. SLP\_CNT Bit Descriptions**

| Bits   | Description (Default = 0x0000)             |
|--------|--|
| [15:8] | Not used.                                  |
| [7:0]  | Programmable sleep time bits, 0.5 sec/LSB. |

## INPUT/OUTPUT FUNCTIONS

### General-Purpose I/O

DIO1 and DIO2 are configurable, general-purpose I/O lines that serve multiple purposes according to the following control register priority: MSC\_CTRL, ALM\_CTRL, and GPIO\_CTRL. For example, set GPIO\_CTRL = 0x0202 (DIN = 0xB302, and then 0xB202) to configure DIO1 as an input and DIO2 as an output set high.

**Table 20. GPIO\_CTRL Bit Descriptions**

| Bits    | Description  |
|---------|--|
| [15:10] | Not used.  |
| 9       | General-Purpose I/O Line 2 (DIO2) data level.                                  |
| 8       | General-Purpose I/O Line 1 (DIO1) data level.                                  |
| [7:2]   | Not used.  |
| 1       | General-Purpose I/O Line 2 (DIO2) direction control.<br>1 = output, 0 = input. |
| 0       | General-Purpose I/O Line 1 (DIO1) direction control.<br>1 = output, 0 = input. |

### Data Ready I/O Indicator

The MSC\_CTRL[2:0] bits configure one of the digital I/O lines as a data ready signal for driving an interrupt. For example, set MSC\_CTRL[2:0] = 100 (DIN = 0xB404) to configure DIO1 as a negative-pulse data ready signal. The pulse width is between 100  $\mu$ s and 200  $\mu$ s over all conditions.

**Table 21. MSC\_CTRL Bit Descriptions**

| Bits    | Description (Default = 0x0000)   |
|---------|--|
| [15:12] | Not used.  |
| 11      | Memory test (cleared upon completion).<br>1 = enabled, 0 = disabled.               |
| 10      | Internal self-test enable (cleared upon completion).<br>1 = enabled, 0 = disabled. |
| 9       | Manual self-test, negative stimulus.<br>1 = enabled, 0 = disabled.                 |
| 8       | Manual self-test, positive stimulus.<br>1 = enabled, 0 = disabled.                 |
| [7:3]   | Not used.  |
| 2       | Data ready enable.<br>1 = enabled, 0 = disabled.                                   |
| 1       | Data ready polarity.<br>1 = active high, 0 = active low.                           |
| 0       | Data ready line select.<br>1 = DIO2, 0 = DIO1.                                     |

### Auxiliary DAC

The 12-bit AUX\_DAC line can drive its output to within 5 mV of the ground reference when it is not sinking current. As the output approaches 0 V, the linearity begins to degrade (~100 LSB starting point). As the sink current increases, the nonlinear range increases. The DAC latch command moves the values of the AUX\_DAC register into the DAC input register, enabling both bytes to take effect at the same time.

**Table 22. AUX\_DAC Bit Descriptions**

| Bits    | Description (Default = 0x0000)   |
|---------|--|
| [15:12] | Not used.  |
| [11:0]  | Data bits, scale factor = 0.6105 mV/code.<br>Offset binary format, 0V = 0 codes. |

**Table 23. Setting AUX\_DAC = 2 V**

| DIN    | Description  |
|--------|--|
| 0xB0CC | AUX_DAC[7:0] = 0xCC (204 LSB).   |
| 0xB10C | AUX_DAC[15:8] = 0x0C (3072 LSB).   |
| 0xBE04 | GLOB_CMD[2] = 1.<br>Move values into the DAC input register, resulting in a 2V output level. |

**DIAGNOSTICS**

**Self-Test**

The self-test function allows the user to verify the mechanical integrity of each MEMS sensor. It applies an electrostatic force to each sensor element, which results in mechanical displacement that simulates a response to actual motion. Table 1 lists the expected response for each sensor, which provides pass/fail criteria.

Set MSC\_CTRL[10] = 1 (DIN = 0xB504) to run the internal self-test routine, which exercises the inertial sensor, measures the response, makes a pass/fail decision, reports the decision to error flags in the DIAG\_STAT register, and then restores normal operation. MSC\_CTRL[10] resets itself to 0 after completing the routine. The MSC\_CTRL[9:8] bits provide manual control of the self-test function for investigation of potential failures. Table 24 outlines an example test flow for using this option to verify the gyroscope function.

**Table 24. Manual Self-Test Example Sequence**

| DIN    | Description  |
|--------|--|
| 0xB601 | SMPL_PRD[7:0] = 0x01, sample rate = 256 SPS.   |
| 0xB904 | SENS_AVG[15:8] = 0x04, gyroscope range = ±320°/sec.  |
| 0xB802 | SENS_AVG[7:0] = 0x02, four-tap averaging filter. Delay = 50 ms.  |
| 0x0400 | Read GYRO_OUT.   |
| 0xB502 | MSC_CTRL[9:8] = 10, gyroscope negative self-test. Delay = 50 ms.   |
| 0x0400 | Read GYRO_OUT.<br>Determine whether the bias in the gyroscope output changed according to the self-test response specified in Table 1. |
| 0xB501 | MSC_CTRL[9:8] = 01, gyroscope/accelerometer positive self-test. Delay = 50 ms.   |
| 0x0400 | Read GYRO_OUT.<br>Determine whether the bias in the gyroscope output changed according to the self-test response specified in Table 1. |
| 0xB500 | MSC_CTRL[15:8] = 0x00.   |

Zero motion provides results that are more reliable. The settings in Table 24 are flexible and allow for optimization around speed and noise influence. For example, using fewer filtering taps decreases delay times but increases the potential for noise influence.

**Memory Test**

Setting MSC\_CTRL[11] = 1 (DIN = 0xB508) performs a checksum comparison between the flash memory and SRAM to help verify memory integrity. The pass/fail result is loaded into the DIAG\_STAT[6] register.

**Status**

The error flags provide indicator functions for common system level issues. All of the flags are cleared (set to 0) after each DIAG\_STAT register read cycle. If an error condition remains, the error flag returns to 1 during the next sample cycle. DIAG\_STAT[1:0] does not require a read of this register to return to 0. If the power supply voltage goes back into range, these two flags are cleared automatically.

**Table 25. DIAG\_STAT Bit Descriptions**

| Bits    | Description   |
|---------|---|
| [15:10] | Not used.   |
| 9       | Alarm 2 status (1 = active, 0 = inactive).                                      |
| 8       | Alarm 1 status (1 = active, 0 = inactive).                                      |
| 7       | Not used.   |
| 6       | Flash test, checksum flag (1 = fail, 0 = pass).                                 |
| 5       | Self-test diagnostic error flag (1 = fail, 0 = pass).                           |
| 4       | Sensor overrange (1 = fail, 0 = pass).  |
| 3       | SPI communication failure (1 = fail, 0 = pass).                                 |
| 2       | Flash update failure (1 = fail, 0 = pass).                                      |
| 1       | Power supply > 5.25 V.<br>1 = power supply > 5.25 V, 0 = power supply ≤ 5.25 V. |
| 0       | Power supply < 4.75 V.<br>1 = power supply < 4.75 V, 0 = power supply ≥ 4.75 V. |

**Alarm Registers**

The alarm function provides monitoring for two independent conditions. The ALM\_CTRL register provides control inputs for data source, data filtering (prior to comparison), static comparison, dynamic rate-of-change comparison, and output indicator configurations. The ALM\_MAGx registers establish the trigger threshold and polarity configurations. Table 29 gives an example of how to configure a static alarm. The ALM\_SMPLx registers provide the numbers of samples to use in the dynamic rate-of-change configuration. The period equals the number in the ALM\_SMPLx register multiplied by the sample period time, which is established by the SMPL\_PRD register. See Table 30 for an example of how to configure the sensor for this type of function.

**Table 26. ALM\_MAG1, ALM\_MAG2 Bit Descriptions**

| Bits   | Description (Default = 0x0000)                                   |
|--------|--|
| 15     | Comparison polarity (1 = greater than, 0 = less than).           |
| 14     | Not used.  |
| [13:0] | Data bits that match the format of the trigger source selection. |

**Table 27. ALM\_SMPL1, ALM\_SMPL2 Bit Descriptions**

| Bits   | Description (Default = 0x0000)                         |
|--------|--|
| [15:8] | Not used.  |
| [7:0]  | Data bits: number of samples (both 0x00 and 0x01 = 1). |



Table 28. ALM\_CTRL Bit Descriptions

| Bits    | Description (Default = 0x0000)   |
|---------|--|
| 15      | Rate-of-change enable for Alarm 2 (1 = rate of change, 0 = static level).  |
| [14:12] | Alarm 2 source selection.<br>000 = disable.<br>001 = power supply output.<br>010 = gyroscope output.<br>011 = not used.<br>100 = not used.<br>101 = auxiliary ADC input.<br>110 = temperature output.<br>111 = not used. |
| 11      | Rate-of-change enable for Alarm 1 (1 = rate of change, 0 = static level).  |
| [10:8]  | Alarm 1 source selection (same as for Alarm 2).  |
| [7:5]   | Not used.  |
| 4       | Comparison data filter setting (1 = filtered data, 0 = unfiltered data).   |
| 3       | Not used.  |
| 2       | Alarm output enable (1 = enabled, 0 = disabled).   |
| 1       | Alarm output polarity (1 = active high, 0 = active low).   |
| 0       | Alarm output line select (1 = DIO2, 0 = DIO1).   |

Table 29. Alarm Configuration Example 1

| DIN            | Description  |
|----------------|--|
| 0xA922, 0xA817 | ALM_CTRL = 0x2217.<br>Alarm 1 input = GYRO_OUT.<br>Alarm 2 input = GYRO_OUT.<br>Static level comparison, filtered data.<br>DIO2 output indicator, positive polarity. |
| 0xA181, 0xA000 | ALM_MAG1 = 0x8100.<br>Alarm 1 is true if GYRO_OUT > +18.755°/sec.  |
| 0xA33F, 0xA200 | ALM_MAG2 = 0x3F00.<br>Alarm 2 is true if GYRO_OUT < -18.755°/sec.  |

Table 30. Alarm Configuration Example 2

| DIN            | Description  |
|----------------|--|
| 0xA9AA, 0xA804 | ALM_CTRL = 0xAA04.<br>Alarm 1 input = GYRO_OUT.<br>Alarm 2 input = GYRO_OUT.<br>Rate-of-change comparison, unfiltered data.<br>DIO1 output indicator, negative polarity. |
| 0xB601         | SMPL_PRD = 0x0001.<br>Sample rate = 256 SPS.   |
| 0xA40A         | ALM_SMPL1[7:0] = 0x000A.<br>Alarm 1 rate of change period = 3.906 ms.  |
| 0xA60A         | ALM_SMPL2[7:0] = 0x000A.<br>Alarm 2 rate of change period = 3.906 ms.  |
| 0xA181, 0xA000 | ALM_MAG1 = 0x8100.<br>Alarm 1 is true if GYRO_OUT changes more than 18.755°/sec over a period of 3.906 ms.   |
| 0xA30F, 0xA200 | ALM_MAG2 = 0x0F00.<br>Alarm 2 is true if GYRO_OUT changes less than 18.755°/sec over a period of 3.906 ms.   |

## PRODUCT IDENTIFICATION

Table 31 provides a summary of the registers that identify the product: PROD\_ID, which identifies the product type; LOT\_ID1 and LOT\_ID2, the 32-bit lot identification code; and SERIAL\_NUM, which displays the 16-bit serial number. All four registers are two bytes in length.

Table 31. Identification Registers

| Register Name | Address | Description   |
|---------------|---------|---|
| LOT_ID1       | 0x52    | Lot Identification Code 1   |
| LOT_ID2       | 0x54    | Lot Identification Code 2   |
| PROD_ID       | 0x56    | Product identification = 0x3F89 or 0x3F84<br>(0x3F89 = 16,265 decimal; 0x3F84 = 16,260 decimal) |
| SERIAL_NUM    | 0x58    | Serial number   |

## APPLICATIONS INFORMATION

### ASSEMBLY

When developing a process flow for installing [ADIS16260/ADIS16265](#) devices on printed circuit boards (PCBs), see the JEDEC J-STD-020C standard document for the reflow temperature profile and processing information. The [ADIS16260/ADIS16265](#) can use the Sn-Pb eutectic process and the Pb-free eutectic process from this standard, with one exception, the peak temperature exposure is 240°C. For a more complete list of assembly process suggestions, see the [ADIS162xx LGA Assembly Guidelines](#) page on Engineer Zone. Figure 18 provides an example pattern for the location of the [ADIS16260/ADIS16265](#) on a printed circuit board.

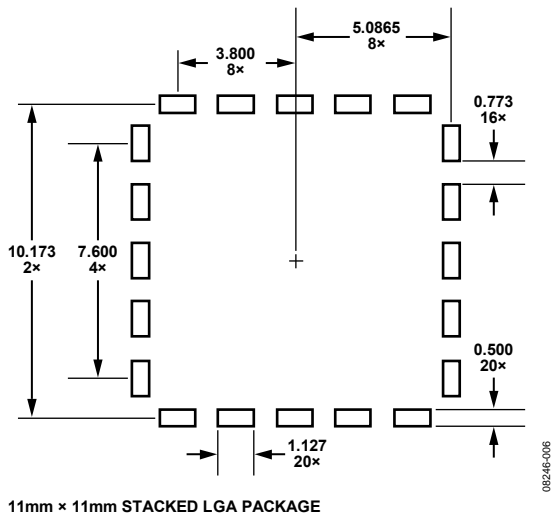


Figure 18. Recommended Pad Layout (Units in Millimeters)

### BIAS OPTIMIZATION

Use the following steps to fine-tune the bias to an accuracy that approaches the in-run bias stability, 0.007°/sec (1  $\sigma$ ).

1. Apply 5 V and wait 10 sec.
2. Set SENS\_AVG[10:8] = 001 (DIN = 0xB901).
3. Set GYRO\_OFF = 0x0000 (DIN = 0x9400, DIN = 0x9500).
4. Collect GYRO\_OUT data for 150 sec at a sample rate of 256 SPS.
5. Average data record.
6. Round to the nearest integer.

7. Multiply by -1.
8. Write to GYRO\_OFF.
9. Update flash, set GLOB\_CMD[3] = 1 (DIN = 0xBE08), and wait for >50 ms and resume operation.

The Allan Variance curve in Figure 6 provides a trade-off relationship between accuracy and averaging time. For example, an average time of 1 second produce an accuracy of ~0.035 °/sec (1  $\sigma$ ).

### INTERFACE PRINTED CIRCUIT BOARD

The [ADIS16265/PCBZ](#) includes one [ADIS16265BCCZ](#) IC on a 1.2 inch x 1.3 inch PCB. The interface PCB simplifies the IC connection of these devices to an existing processor system. The four mounting holes accommodate either M2 (2 mm) or 2-56 machine screws. These boards are made of IS410 material and are 0.063 inches thick. The second-level assembly uses a SAC305-compatible solder composition, which has a presolder reflow thickness of approximately 0.005 inches.

The pad pattern on these PCBs matches that shown in Figure 20. J1 and J2 are dual-row, 2 mm (pitch) connectors that work with a number of ribbon cable systems, including 3M Part Number 152212-0100-GB (ribbon crimp connector) and 3M Part Number 3625/12 (ribbon cable). The schematic and connector pin assignments for the [ADIS16265/PCBZ](#) are shown in Figure 19.

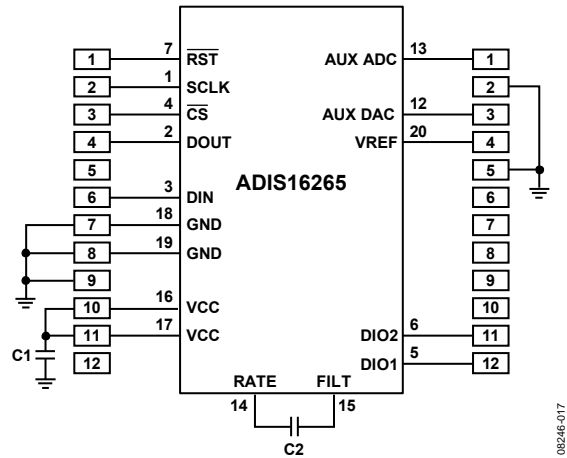


Figure 19. Electrical Schematic

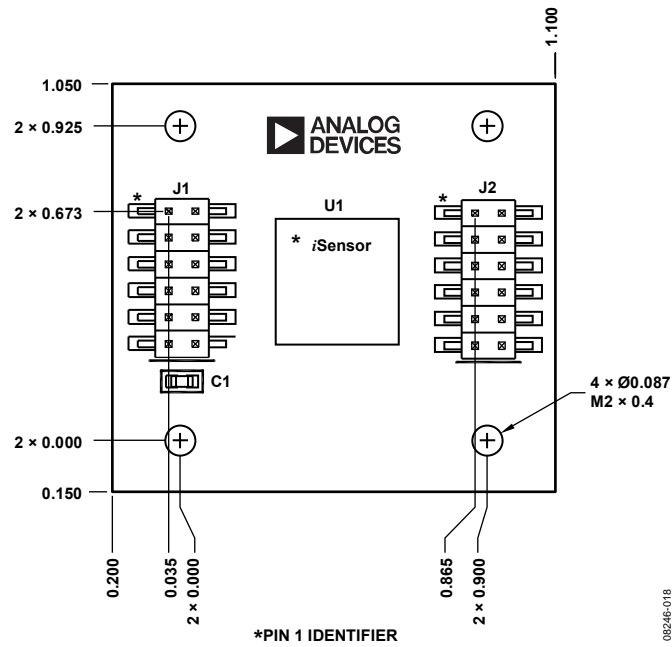


Figure 20. PCB Assembly View and Dimensions

OUTLINE DIMENSIONS

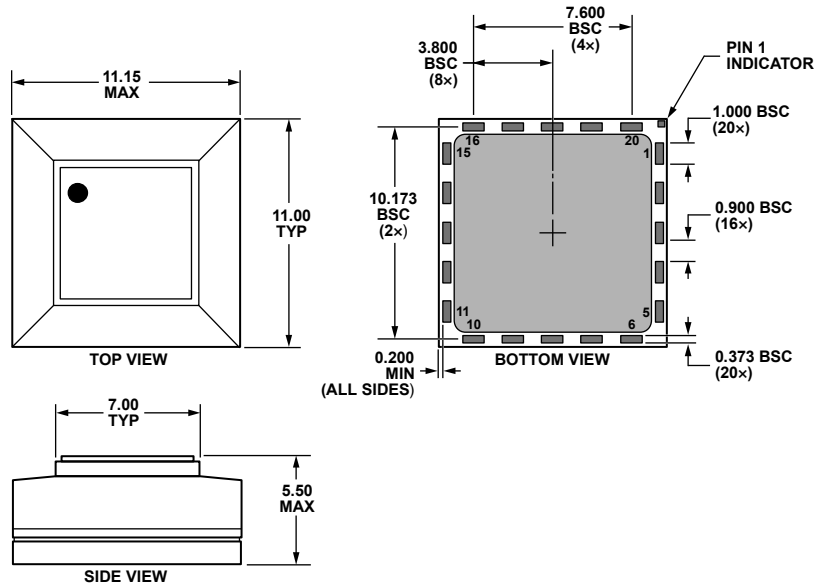


Figure 21. 20-Terminal Stacked Land Grid Array [LGA]  
(CC-20-1)  
Dimensions shown in millimeters

ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                       | Package Option |
|--------------------|-------------------|---|----------------|
| ADIS16260BCCZ      | -40°C to +105°C   | 20-Terminal Stacked Land Grid Array [LGA] | CC-20-1        |
| ADIS16265BCCZ      | -40°C to +105°C   | 20-Terminal Stacked Land Grid Array [LGA] | CC-20-1        |
| ADIS16265/PCBZ     |                   | Evaluation Board                          |                |

<sup>1</sup> Z = RoHS Compliant Part.

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