Interleaved Inverting Charge Pump with Negative LDO Regulator

Data Sheet **ADP5600**

FEATURES

- Input voltage: 2.7 V to 16 V
- Maximum output current: −100 mA
- Integrated power MOSFETs
- Four LDO selectable output voltage options
  - −0.505 V, −1.5 V, −2.5 V, −5 V
- Adjustable output voltage range: −0.505 V to $-V_{IN}$ + 0.5 V
- Programmable charge pump switching frequency range
  - 100 kHz to 1 MHz
- Frequency synchronization via SYNC pin
- Precision enable and power good
- Internal soft start
- Output short-circuit and overload protection
- Shorted charge pump fly capacitor protection
- Integrated LDO output discharge resistor
- 16-lead, 4 mm × 4 mm LFCSP

APPLICATIONS

- Powering the negative rail on bipolar/split supply
  - ADC/DAC/AMP/mux applications

TYPICAL APPLICATIONS CIRCUITS

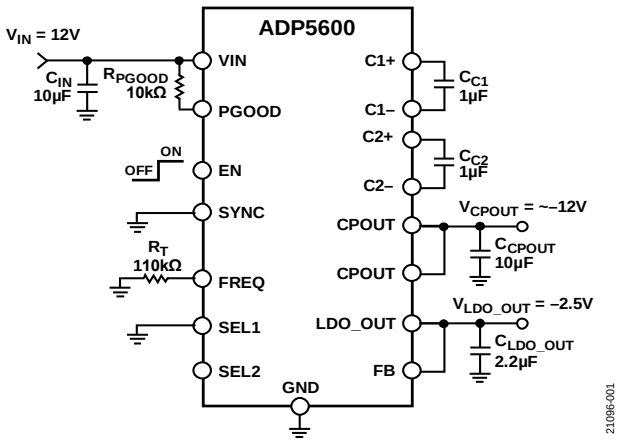

Figure 1. Fixed Output Voltage, V_{LDO_OUT} = −2.5 V

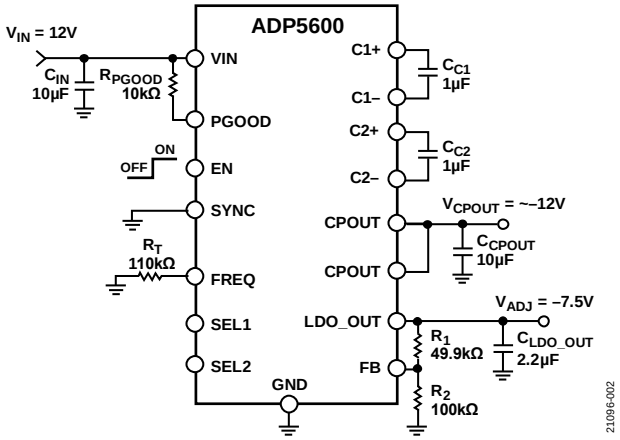

Figure 2. Adjustable Output Voltage, V_{ADJ} = −7.5 V

GENERAL DESCRIPTION

The ADP5600 is an interleaved charge pump inverter with an integrated, negative, low dropout (LDO) linear regulator. The interleaved charge pump inverter exhibits reduced output voltage ripple and reflected input current noise over conventional inductive or conventional capacitive based solutions. The integrated LDO provides a rail with good regulation at sufficient power supply rejection ratio (PSRR).

The ADP5600 charge pump operates via resistor programming or external clock synchronization at switching frequency range of 100 kHz to 1 MHz. Operating at a higher switching frequency allows the use of small input, output, and fly capacitors. To combine the high switching frequency with internal field effect transistors (FETs), compensation, and soft start gives a best-in-class total solution size for negative rail generation.

The ADP5600 also features comprehensive fault protection for robust applications. These protections include overload protection, shorted fly capacitor protection, undervoltage lockout (UVLO), and thermal shutdown. For easy sequencing, the ADP5600 has a power-good pin.

The integrated LDO of the ADP5600 uses an advanced proprietary architecture to provide high power supply rejection. It also achieves decent line and load transient response with only a small 2.2 µF ceramic output capacitor. The output can be configured via the SEL1 and SEL2 pins to one of four fixed output voltages and is adjustable from −0.505 V to $-V_{IN}$ + 0.5 V via an external feedback divider.

Rev. A Document Feedback

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REVISION HISTORY

4/2021—Rev. 0 to Rev. A

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7/2020—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = V_{EN} = 2.7 V or |V_{LDO_OUT} − 0.5 V| whichever is higher to 16 V, V_{LDO_OUT} = −2.5 V, C_{IN} = C_{CPOUT} = 10 µF, C1 = C2 = 1 µF, C_{LDO_OUT} = 2.2 µF , I_{LDO_OUT} = −10 mA, f_{OSC} = 500 kHz, T_J = −40°C to +125°C for minimum/maximum specifications unless otherwise noted.
V_{IN} = V_{EN} = 12 V, T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameters	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY REQUIREMENTS						
Input Voltage	V_{IN}	2.7		16	V	
Active Switching Current	I_{SW}		3.75	4	mA	V_{IN} = 5 V, f_{OSC} = 100 kHz
			5	5.6	mA	V_{IN} = 5 V, f_{OSC} = 500 kHz
			7.7	8.5	mA	V_{IN} = 5 V, f_{OSC} = 1 MHz
			6.5		mA	V_{IN} = 16 V, f_{OSC} = 500 kHz
Shutdown Current	I_{SHDN}			26.1	µA	EN = GND, V_{IN} =16 V
VIN Undervoltage Lockout Threshold	$UVLO_{RISING}$		2.58	2.63	V	V_{IN} rising
	$UVLO_{FALLING}$	2.46	2.5		V	V_{IN} falling
	$UVLO_{HYS}$		90		mV	V_{IN} falling
SEL1, SEL2 PULL-UP CURRENT	I_{SEL}	4.5	5	5.7	µA	V_{SELx} = 0.5 V
THERMAL SHUTDOWN						
Threshold	TSD_{RISING}		150		°C	
Hysteresis	TSD_{HYS}		20		°C	
EN						
EN Shutdown Threshold (High to Low)	EN_{SD2}	0.5	0.71		V	Threshold to enter shutdown
EN Rising Threshold, Precision	EN_{TH}	1.17		1.26	V	Precision threshold
EN Input Hysteresis, Precision	EN_{HYS}		70		mV	
EN Noise Filter Time	EN_{FILT_LO-HI}		5.4		µs	EN low to high noise filter
EN Leakage Current			3.5	5.2	µA	V_{IN} = V_{EN} = 16 V
OSCILLATOR (FREQ)						
Oscillator Frequency Range	f_{OSC}	0.1		1.1	MHz	Frequency range of the resistor programmable internal oscillator
FREQ Resistor Range	R_T	0		530	kΩ	
FREQ = GND Frequency Range	f_{OSC_GND}	0.85		1.1	MHz	R_T = 0 Ω
FREQ Voltage	V_{FREQ}		1		V	Buffered output
SYNC						
Synchronization Range	f_{SYNC}	0.2		2.2	MHz	f_{OSC} = f_{SYNC}/2
SYNC Minimum Pulse Width	$t_{SYNC\_MIN\_ON}$	100			ns	
SYNC Minimum Off Time	$t_{SYNC\_MIN\_OFF}$	150			ns	
SYNC Input High Voltage	V_{IH_SYNC}	1.3			V	
SYNC Input Low Voltage	V_{IL_SYNC}			0.5	V	
SYNC Leakage Current	I_{SYNC_LKG}		4.5	100	nA	V_{SYNC} = 5.5 V
POWER-GOOD OUTPUT						
Rising Threshold	PG_{TH}	91	93	95	%	Nominal V_{LDO_OUT}
Hysteresis	PG_{HYS}		3		%	
Power-Good Rising Deglitch Time	t_{PG}		16		$1/f_{OSC}$	
Power-Good Leakage Current	I_{PG_LKG}		5	100	nA	V_{PG} =16 V
Power-Good Output Low Voltage	V_{OL}		130	209	mV	I_{PG} = 1 mA

CHARGE PUMP REGULATOR SPECIFICATIONS

Table 2.

Parameters	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHARGE PUMP OUTPUT IMPEDANCE	R_{OUT}		9.5		Ω	I_{CPOUT} = −50 mA
ON RESISTANCES						
VIN to Cx+ PFET Switch	R_{CPHx}		2.9	4.55	Ω	x = inverting Charge Pump 1 or Charge Pump 2
Cx− to GND PFET Switch	R_{CPGx}		1.95	3.69	Ω	
Cx+ to GND NFET Switch	R_{FNGx}		1.81	3.41	Ω	
Cx− to CPOUT NFET Switch	R_{FNOx}		1.83	2.9	Ω	
CURRENT LIMIT						
Charge Pump Input Current Limit	$I_{PMOSLIMIT}$		235	280	mA	
Charge Pump Output Current Limit	$I_{NMOSLIMIT}$		270	330	mA	
OFF STATE ISOLATION LEAKAGE	I_{CPOUT_LKG}		4	6	µA	V_{IN} = 16 V, V_{EN} = 0 V
POWER EFFICIENCY			88		%	V_{IN} = 16 V, I_{CPOUT} = −100 mA

LDO REGULATOR SPECIFICATIONS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER-GOOD THRESHOLD						
Rising Threshold	PG_{TH_CP}	−1.87	−2	−2.1	V	
Hysteresis	PG_{HYS_CP}		130		mV	
LDO OUTPUT VOLTAGE						LDO_OUT shorted to FB, V_{IN} = +12 V, I_{LDO_OUT} = −10 mA
SEL1 = GND||SEL2 = GND	V_{LDO_OUT1}	−0.487	−0.505	−0.523	V	
SEL1 =NC||SEL2 = GND	V_{LDO_OUT2}	−1.47	−1.5	−1.53	V	
SEL1 = GND||SEL2 = NC	V_{LDO_OUT3}	−2.465	−2.5	−2.535	V	
SEL1 =NC||SEL2 = NC	V_{LDO_OUT4}	−4.925	−5.0	−5.075	V	
LDO LINE REGULATION	$\Delta V_{LDO\_OUT}/\Delta V_{IN}$					
			−0.59		mV/V	V_{LDO_OUT1} = −0.505 V
			−1.04		mV/V	V_{LDO_OUT2} = −1.5 V
			−1.42		mV/V	V_{LDO_OUT3} = −2.5 V
			−2.33		mV/V	V_{LDO_OUT4} = −5 V
LDO LOAD REGULATION	$\Delta V_{LDO\_OUT}/\Delta I_{LDO\_OUT}$					I_{LDO_OUT} = −1 mA to −100 mA
			−0.10		mV/mA	V_{LDO_OUT1} = −0.505 V
			−0.12		mV/mA	V_{LDO_OUT2} = −1.5 V
			−0.13		mV/mA	V_{LDO_OUT3} = −2.5 V
			−0.16		mV/mA	V_{LDO_OUT4} = −5 V
FB BIAS CURRENT	I_{FB}		5	100	nA	
LDO CURRENT LIMIT	I_{LIM_LDO}	110	160		mA	
DROPOUT VOLTAGE[1]	$V_{DROPOUT}$		−21	−58	mV	I_{LDO_OUT} = −10 mA
			−111	−190	mV	I_{LDO_OUT} = −100 mA
LDO_OUT DISCHARGE RESISTOR			400	430	Ω	V_{EN} = 0 V, I_{LDO_OUT} = −1 mA
SOFT START TIME[2]	t_{ss}		160		µs	V_{LDO_OUT3} = −2.5 V
TOTAL START-UP TIME[3]	$t_{START\text{-}UP}$		900		µs	V_{LDO_OUT3} = −2.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT NOISE	LDO_OUT_{NOISE}		59		μV rms	10 Hz to 100 kHz, V_{LDO_OUT3} = −2.5 V
			57		μV rms	100 Hz to 100 kHz, V_{LDO_OUT3} = −2.5 V
			163		μV rms	10 Hz to 100 kHz, V_{ADJ} = −7.5 V, C_{NR} = open, R_{NR} = open, R_1 = 150 kΩ, R_2 = 75 kΩ
			158		μV rms	100 Hz to 100 kHz, V_{ADJ} = −7.5 V, C_{NR} = open, R_{NR} = open, R_1 = 150 kΩ, R_2 = 75 kΩ
			99		μV rms	10 Hz to 100 kHz, V_{ADJ}= −7.5 V, C_{NR} = 100 nF, R_{NR} = 75 kΩ, R_1 = 150 kΩ, R_2 = 75 kΩ
			96		μV rms	100 Hz to 100 kHz, V_{ADJ} = −7.5 V, C_{NR} = 100 nF, R_{NR} = 75 kΩ, R_1 = 150 kΩ, R_2 = 75 kΩ
POWER SUPPLY REJECTION RATIO	PSRR					
			45		dB	10 kHz, V_{LDO_OUT3} = −2.5 V, V_{IN} = +4.5 V
			41		dB	100 kHz, V_{LDO_OUT3} = −2.5 V, V_{IN} = +4.5 V
			69		dB	1 MHz, V_{LDO_OUT} = −2.5 V, V_{IN} = +4.5 V
			45		dB	10 kHz, V_{LDO_OUT4} = −5 V, V_{IN} = +6 V
			39		dB	100 kHz, V_{LDO_OUT4} = −5 V, V_{IN} = +6 V
			70		dB	1 MHz, V_{LDO_OUT4} = −5 V, V_{IN} = +6 V
			40		dB	10 kHz, V_{ADJ} = −7.5 V, V_{IN} = +16 V, adjustable mode, R_1 = 150 kΩ, R_2 = 75 kΩ
			43		dB	100 kHz, V_{ADJ} = −7.5 V, V_{IN} = +16 V, adjustable mode, R_1 = 150 kΩ, R_2 = 75 kΩ
			68		dB	1 MHz, V_{ADJ} = −7.5 V, V_{IN} = +16 V, adjustable mode, R_1 = 150 kΩ, R_2 = 75 kΩ

[1] Dropout voltage is measured by forcing the input voltage at CPOUT to be equal to the nominal output voltage of LDO_OUT. Dropout applies only for output voltages below −2.7 V.
[2] Soft start time is defined as the time between 0% to 98% of V_{LDO_OUT}.
[3] Total start-up time is defined as the time between EN going high to PG_{TH} going high.

RECOMMENDED INPUT AND OUTPUT CAPACITOR SPECIFICATIONS

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CAPACITANCE[1]		T_A = −40°C to +125°C				
VIN	C_{IN}		4.7	10		μF
C1	C_{C1}		0.47	1		μF
C2	C_{C2}		0.47	1		μF
CPOUT	C_{CPOUT}		4.7	10		μF
LDO_OUT	C_{LDO_OUT}		1.0	2.2		μF
CAPACITOR EQUIVALENT SERIES RESISTANCE (ESR)	R_{ESR}	T_A = −40°C to +125°C				
C_{IN}, C_{CPOUT}			0.001		0.1	Ω
C_{LDO_OUT}			0.001		0.1	Ω

[1] The minimum capacitance over the full range of the operating conditions must be greater than the minimum specifications. Consider the full range of the operating conditions in the application during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended. Y5V and Z5U capacitors are not recommended.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
VIN, C1+, C2+, EN to GND	−0.3 V to +20 V
PGOOD to GND	−0.3V to +20 V
SYNC to GND	−0.3V to +5.5 V
FREQ to GND	−0.3V to +2.5 V
SEL1, SEL2 to GND	−0.3V to +2.5 V
C1−, C2−, CPOUT, LDO_OUT to GND	−20 V to +0.3 V
FB to GND	−5.5 V to +0.3 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in the circuit board (4-layer, JEDEC standard board) for surface mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Ψ_{JT}	Unit
CP-16-17[1]	45.42	2.22	0.52	°C/W

[1] θ_{JA}, θ_{JC}, and Ψ_{JT} are based on a 4-layer PCB (two signal and two power planes) with four thermal vias connecting the exposed pad to the CPOUT plane.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

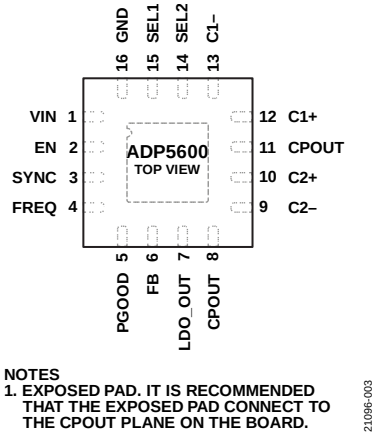


Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN	Power Input. Connect Pin 1 to the input power source and connect a 10 µF bypass capacitor between Pin 1 and GND.
2	EN	Precision Enable Pin. Pull EN high to enable the ADP5600 and pull EN low to disable ADP5600. The EN pin has an internal pull-down resistor to GND to prevent operation if EN is left floating.
3	SYNC	Synchronization Input (SYNC). Connect this pin to an external clock with a range of 180 kHz to 2.2 MHz, to synchronize the charge pump oscillator to $f_{SYNC}/2$. If this pin is shorted to GND or does not change for some period of time, then the internal clock frequency determined by the FREQ pin is used instead of the external clock connected to the SYNC pin. See the Oscillator and Synchronization sections for more information. Do not leave the SYNC pin floating. If Pin 3 is not used, short SYNC to GND.
4	FREQ	Frequency Setting. Connect a resistor between FREQ and GND to program the oscillator frequency between 100 kHz and 1.0 MHz. If FREQ is shorted to GND, the charge pump switching frequency is programmed to 1 MHz (typical). Do not leave this pin floating.
5	PGOOD	Power-Good Output (Open Drain). A pull-up resistor of 10 kΩ to 100 kΩ is recommended. When not used, this pin can be left floating or connected to GND.
6	FB	Feedback Voltage Sense Input. For fixed output voltages, short FB to LDO_OUT. For adjustable mode, connect an external resistor divider between LDO_OUT and GND through the FB pin to set the output voltage.
7	LDO_OUT	Output of the LDO. Connect a 2.2 µF or greater capacitor from LDO_OUT to GND.
9	C2–	C2 Flying Capacitor Negative Terminal.
10	C2+	C2 Flying Capacitor Positive Terminal.
8, 11	CPOUT	Inverting Charge Pump Output. Connect CPOUT to the exposed pad. Connect a 10 µF or greater capacitor from CPOUT to GND.
12	C1+	C1 Flying Capacitor Positive Terminal.
13	C1–	C1 Flying Capacitor Negative Terminal.
14	SEL2	Output Voltage Selector 2. Short SEL2 to GND or leave floating to select one of four LDO_OUT voltage options.
15	SEL1	Output Voltage Selector 1. Short SEL1 to GND or leave floating to select one of four LDO_OUT voltage options.
16	GND	Ground.
	EP	Exposed Pad. It is recommended that the exposed pad connect to the CPOUT plane on the board.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12 V, V_{LDO_OUT} = −2.5 V, I_{LDO_OUT} = −10 mA, C_{IN} = C_{CPOUT} = 10 µF, C_{LDO_OUT} = 2.2 µF, C1 = C2 = 1 µF, f_{OSC} = 500 kHz, unless otherwise noted.

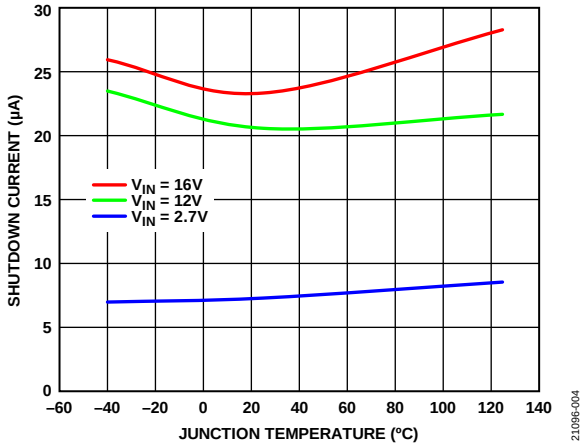


Figure 4. Shutdown Current (I_{SHDN}) vs. Junction Temperature (T_J) at Various Input Voltages (V_{IN})

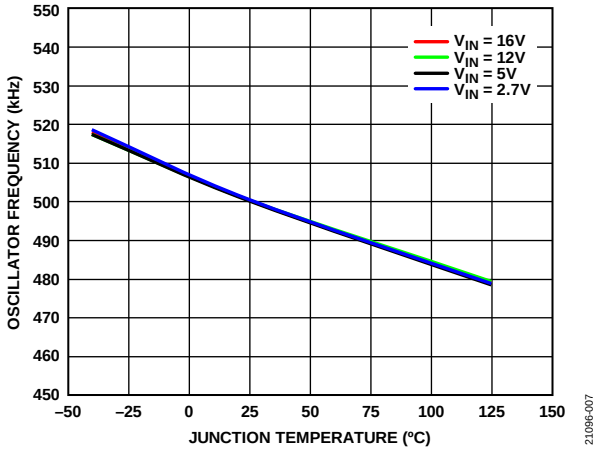


Figure 7. Oscillator Frequency (f_{OSC}) vs. Junction Temperature (T_J) at Various Input Voltages (V_{IN})

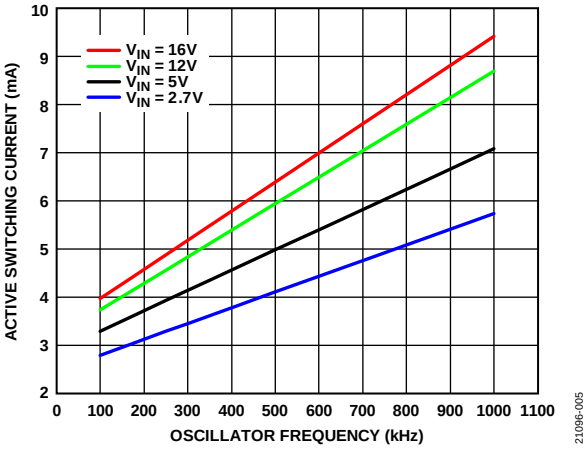


Figure 5. Active Switching Current (I_{SW}) vs. Oscillator Frequency (f_{OSC}) at Various Input Voltages (V_{IN})

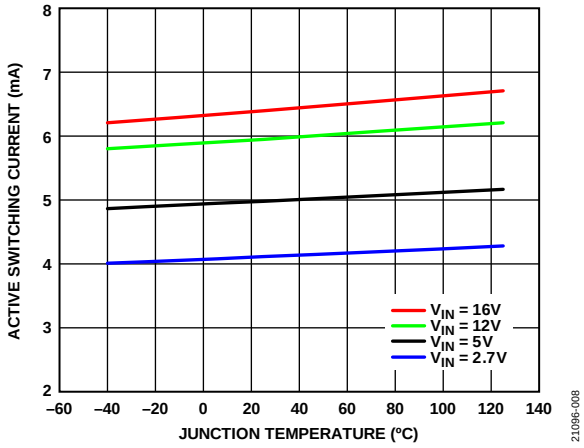


Figure 8. Active Switching Current (I_{SW}) vs. Junction Temperature (T_J) at Various Input Voltages (V_{IN})

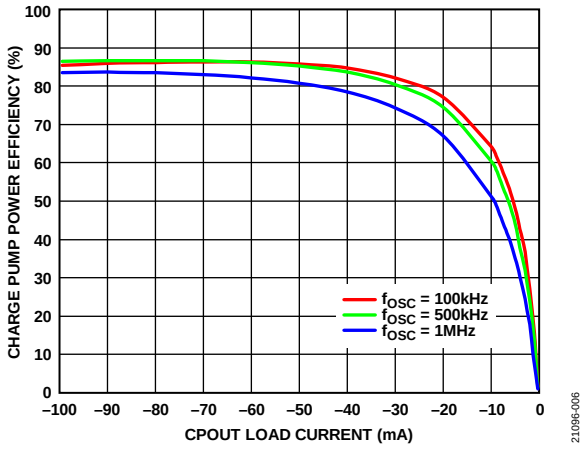


Figure 6. Charge Pump Power Efficiency vs. CPOUT Load Current (I_{CPOUT}) at Various Oscillator Frequencies (f_{OSC}), V_{IN} = 12 V

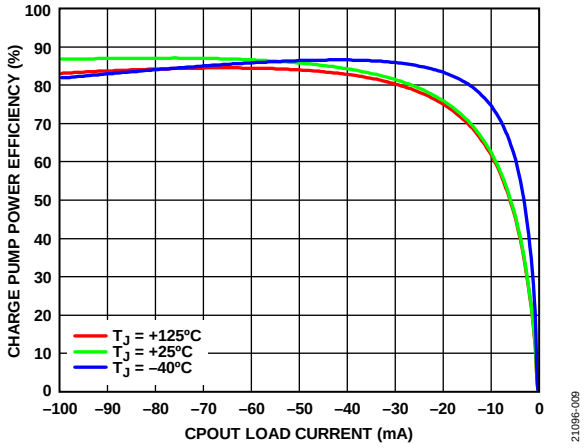


Figure 9. Charge Pump Power Efficiency vs. CPOUT Load Current (I_{CPOUT}) at Various Junction Temperatures (T_J), V_{IN} = 12 V

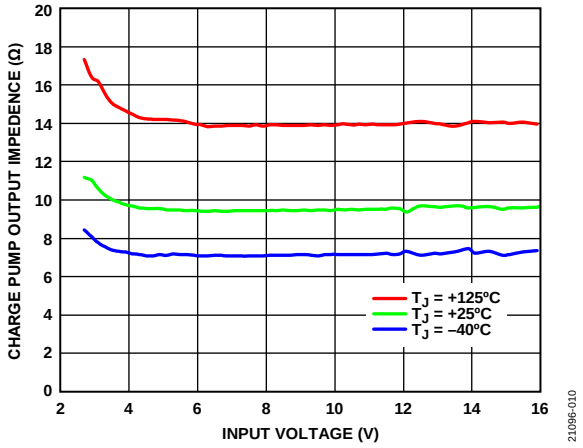


Figure 10. Charge Pump Output Impedance (R_{OUT}) vs. Input Voltage (V_{IN}) at Various Junction Temperatures (T_J)

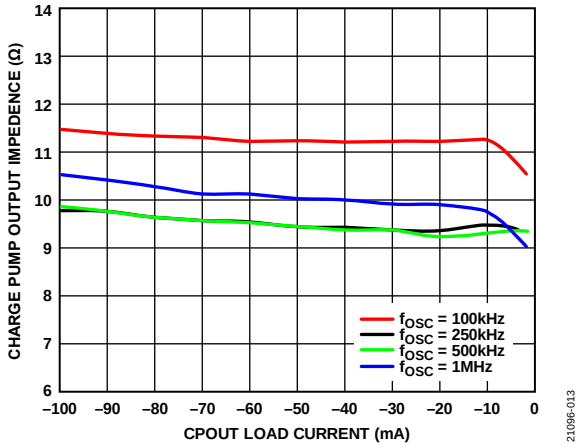


Figure 13. Charge Pump Output Impedance (R_{OUT}) vs. CPOUT Load Current (I_{CPOUT}) at Various Oscillator Frequencies (f_{OSC})

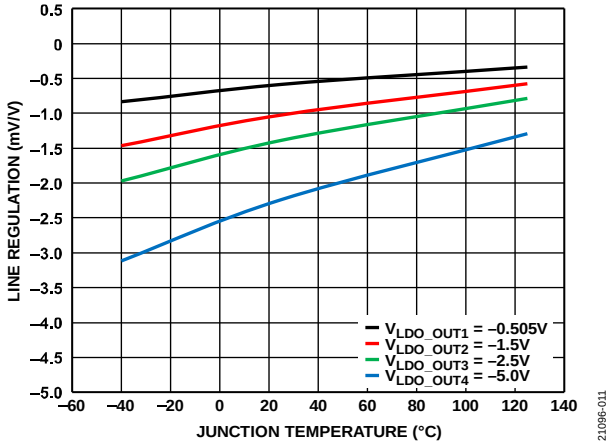


Figure 11. LDO Line Regulation vs. Junction Temperature (T_J)

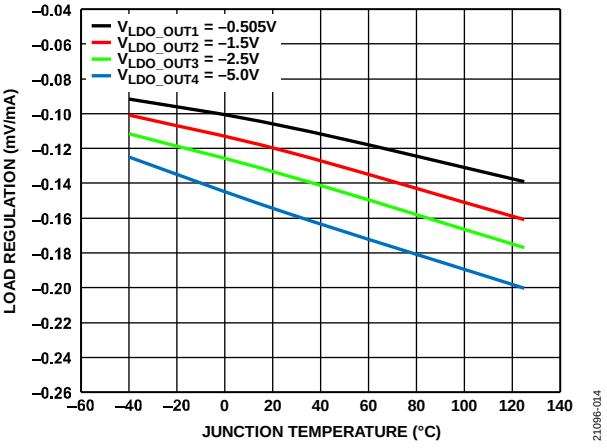


Figure 14. LDO Load Regulation vs. Junction Temperature (T_J)

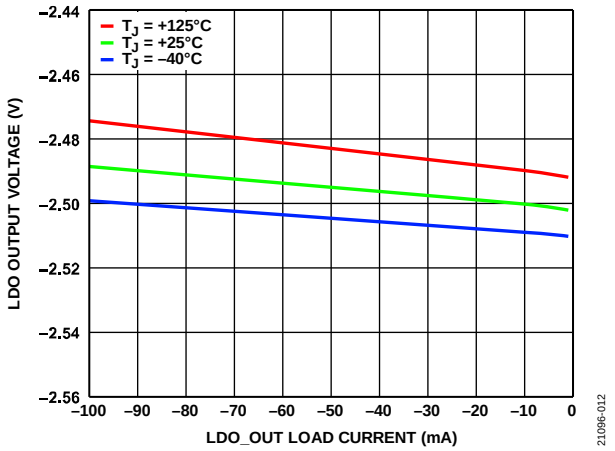


Figure 12. LDO Output Voltage (V_{LDO_OUT2}) vs. LDO_OUT Load Current (I_{LDO_OUT}) at Various Junction Temperatures (T_J)

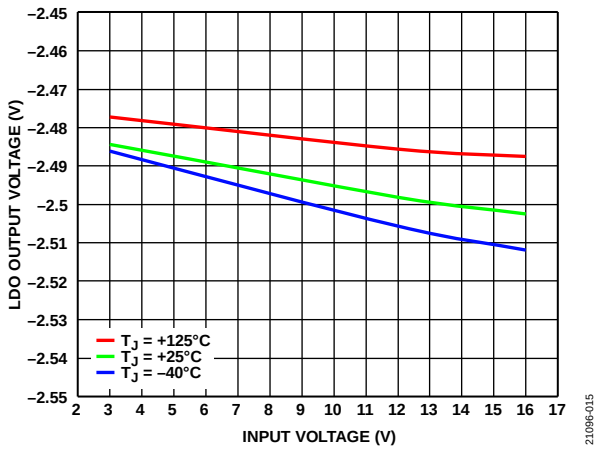


Figure 15. LDO Output Voltage (V_{LDO_OUT2}) vs. Input Voltage (V_{IN}) at Various Junction Temperatures (T_J)

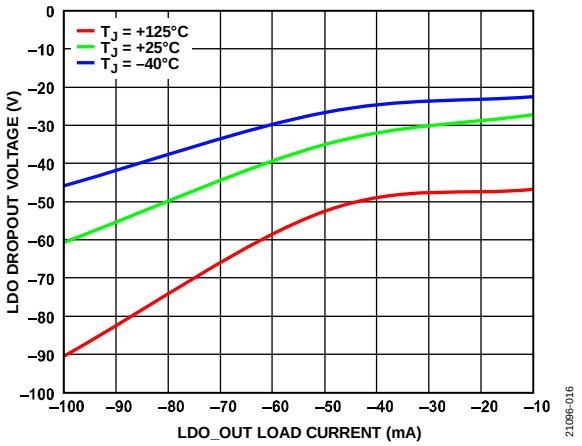


Figure 16. LDO Dropout Voltage vs. LDO_OUT Load Current (I_{LDO_OUT}) at Various Junction Temperatures (T_J), V_{LDO_OUT4} = −5 V

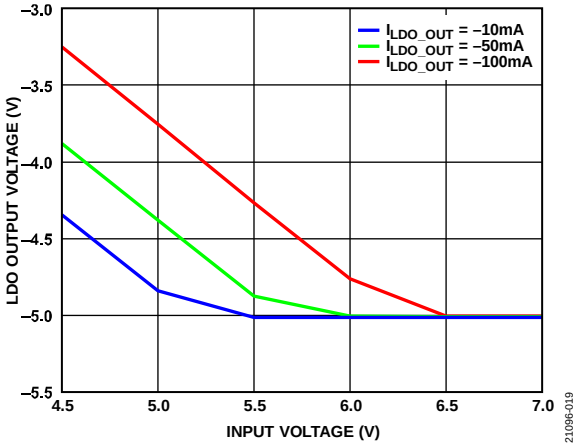


Figure 19. LDO Output Voltage (V_{LDO_OUT}) vs. Input Voltage (V_{IN}) in Dropout at Various LDO Load Currents (I_{LDO_OUT}), V_{DLO_OUT4} = −5 V

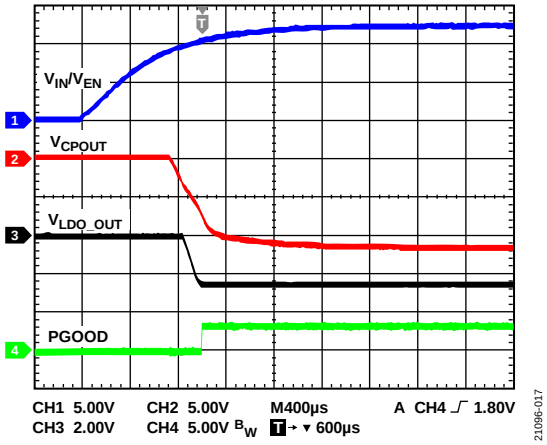


Figure 17. Start-Up Response

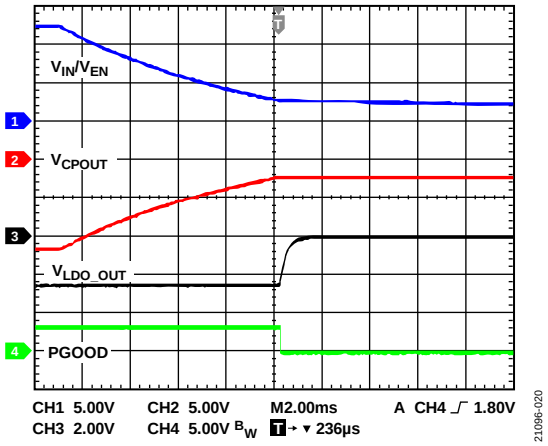


Figure 20. Power-Down Response

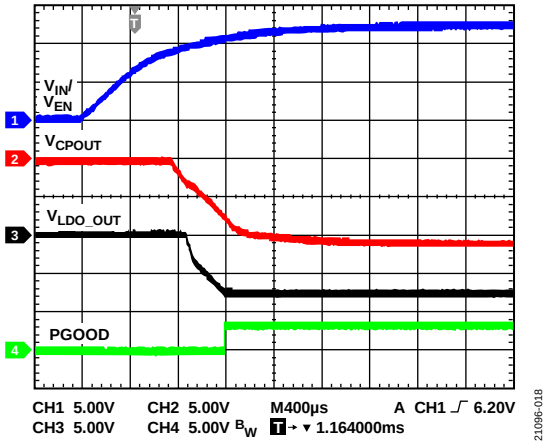


Figure 18. Start-Up Response, Adjustable Output Option, V_{ADJ} = −7.5 V, I_{LDO_OUT} = −100 mA

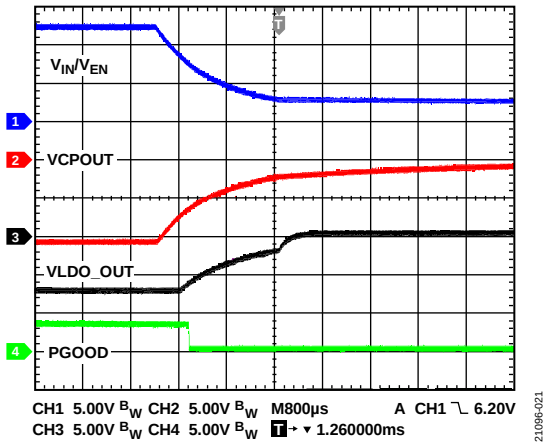


Figure 21. Power-Down Response, Adjustable Output Option, V_{ADJ} = −7.5 V, I_{LDO_OUT} = −100 mA

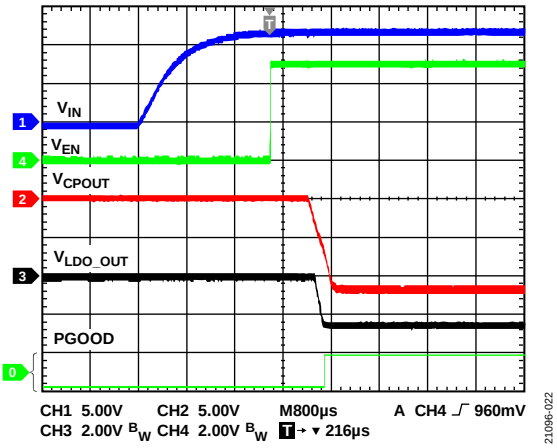


Figure 22. Start-Up Response, V_{IN} First

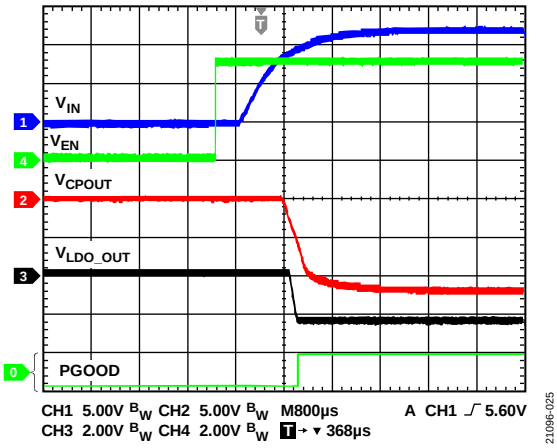


Figure 25. Start-Up Response, V_{EN} First

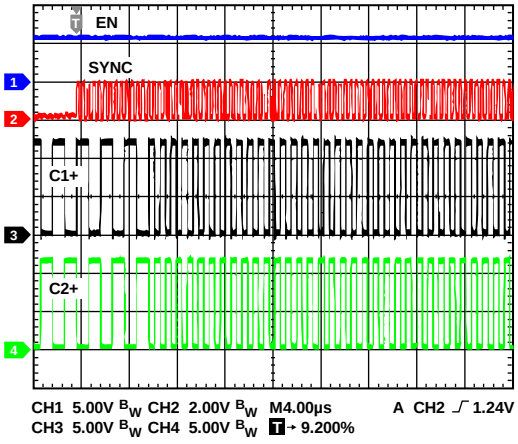


Figure 23. Oscillator Frequency (f_{OSC}) Transition, R_T = 110 kΩ to f_{SYNC} = 2.2 MHz

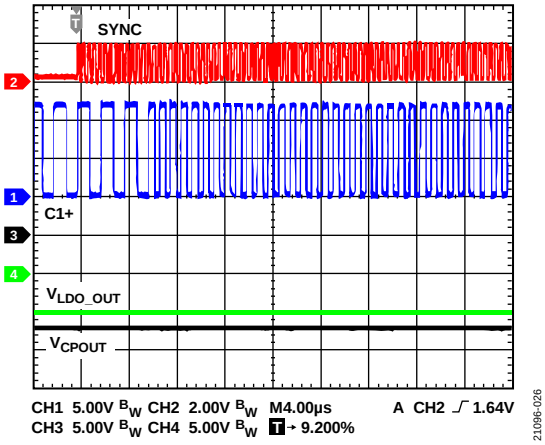


Figure 26. Oscillator Frequency (f_{OSC}) Transition, R_T = 110 kΩ to f_{SYNC} = 2.2 MHz, I_{CPOUT} = −100 mA

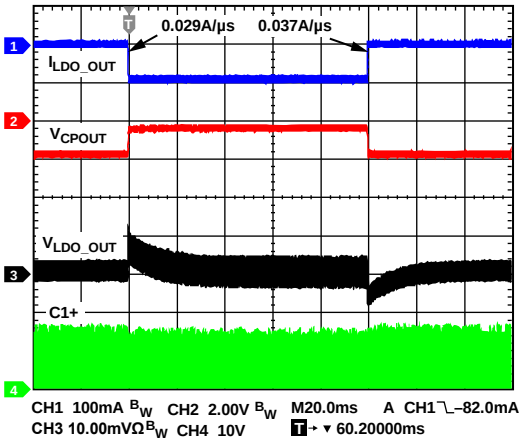


Figure 24. Load Transient Response, I_{LDO_OUT} = −1 mA to −100 mA

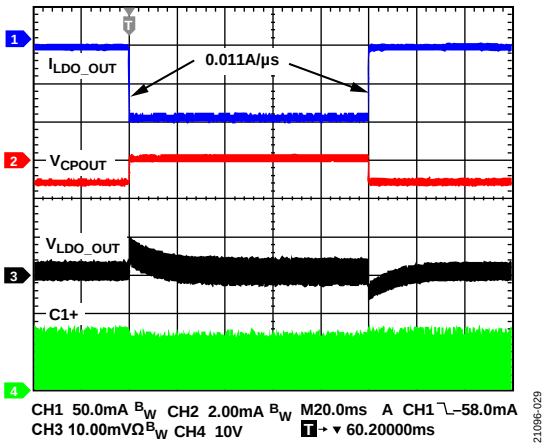


Figure 27. Load Transient Response, I_{LDO_OUT} = −10 mA to −100 mA

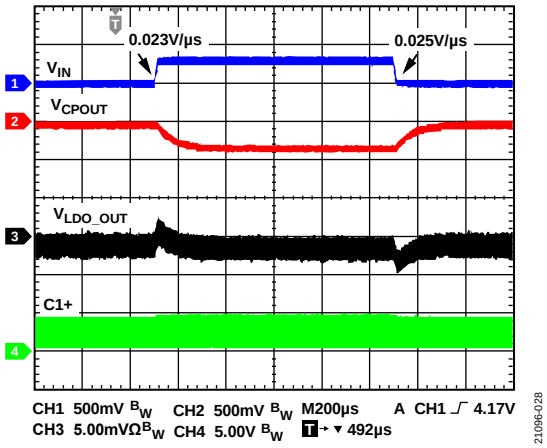


Figure 28. Line Transient Response, V_{IN} = 4 V to 4.2 V, I_{LDO_OUT} = −100 mA

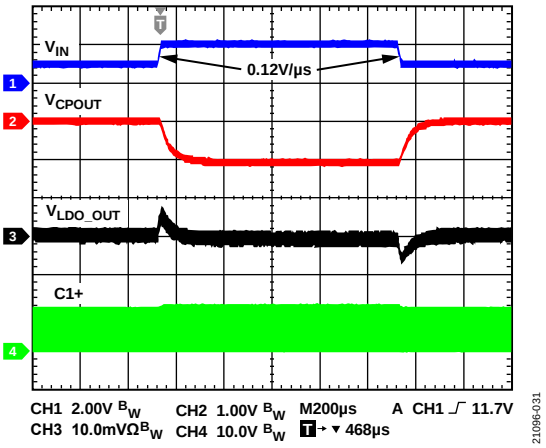


Figure 31. Line Transient Response, V_{IN} = 11 V to 12 V, I_{LDO_OUT} = −100 mA

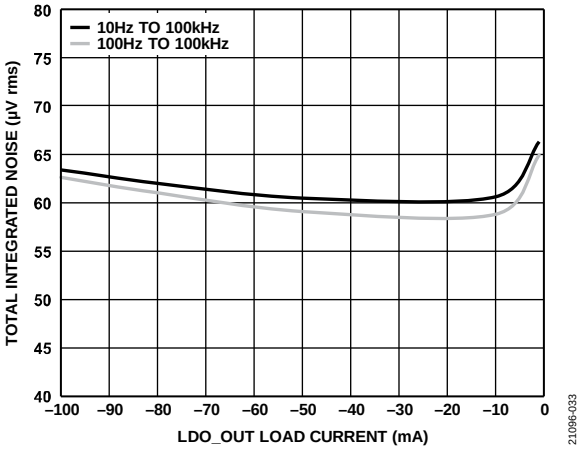


Figure 29. Total Integrated Noise vs. LDO_OUT Load Current (I_{LDO_OUT})

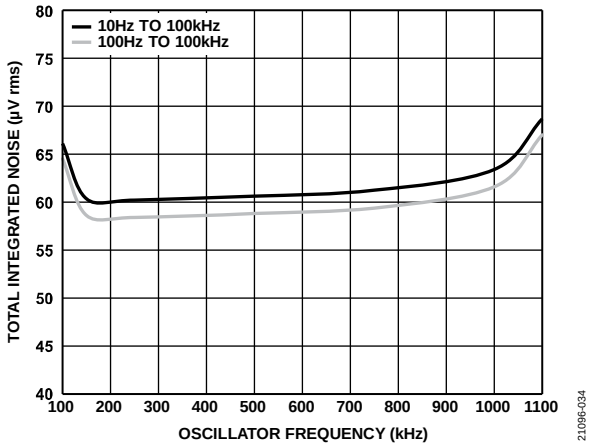


Figure 32. Total Integrated Noise vs. Oscillator Frequency (f_{OSC})

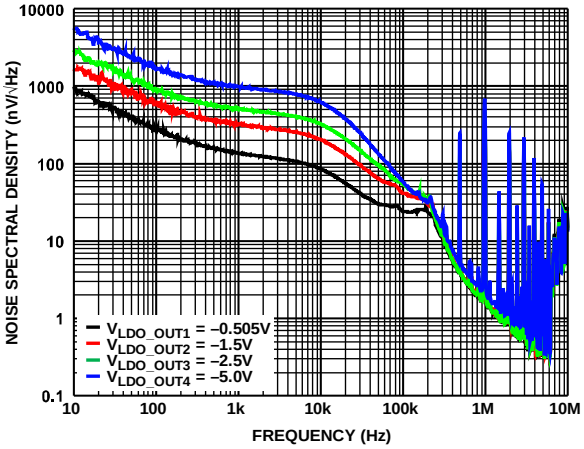


Figure 30. Noise Spectral Density vs. Frequency at Various LDO Output Voltages

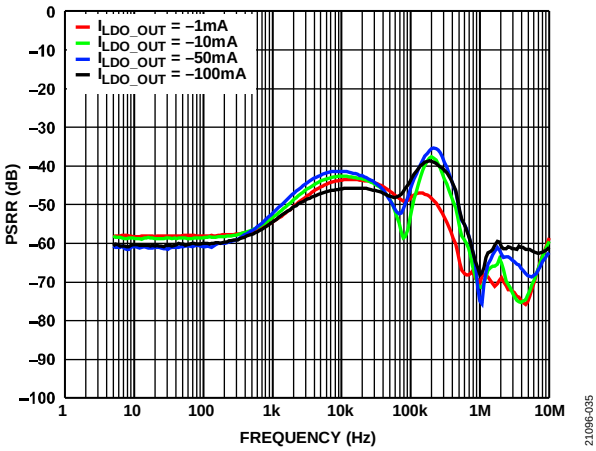


Figure 33. VIN to LDO_OUT PSRR vs. Frequency at Various I_{LDO_OUT}

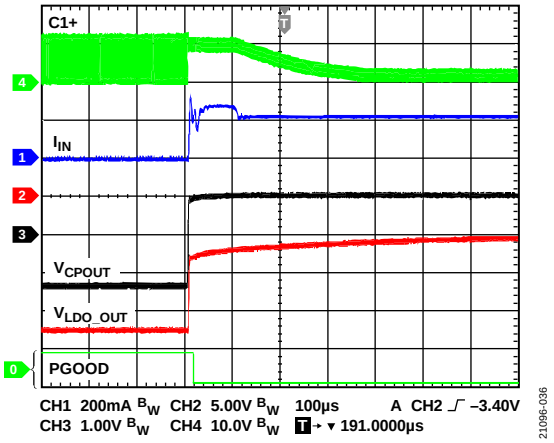


Figure 34. CPOUT Entry to Short Circuit

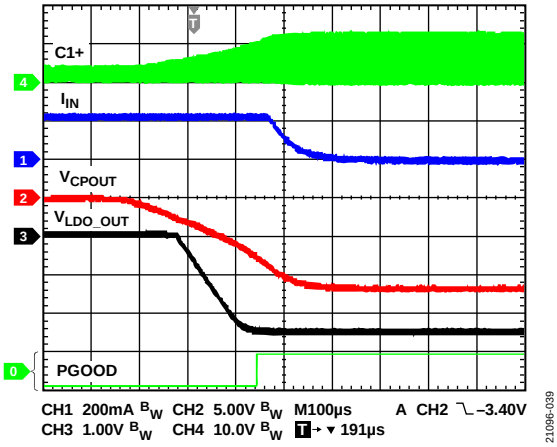


Figure 37. CPOUT Recovery from Short Circuit

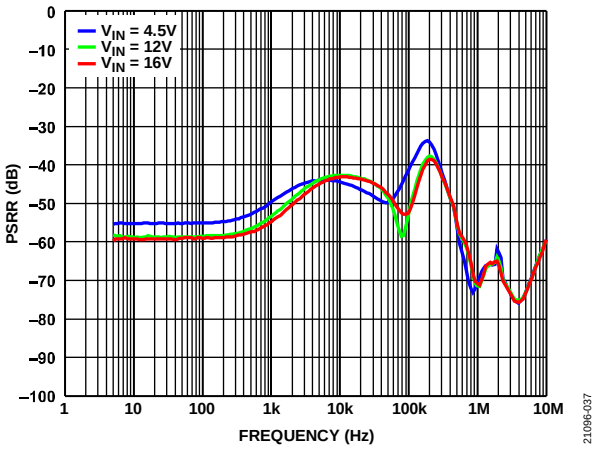


Figure 35. VIN to LDO_OUT PSRR vs. Frequency at Various Input Voltages (V_{IN})

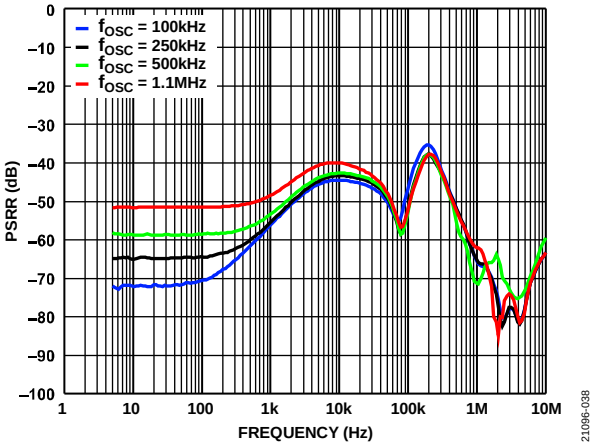


Figure 38. VIN to LDO_OUT PSRR vs. Frequency at Various Oscillator Frequencies (f_{OSC})

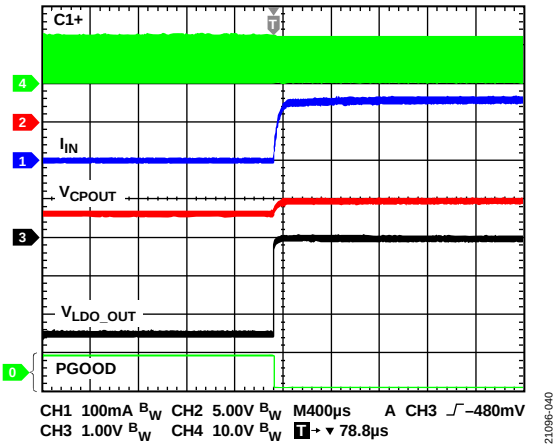


Figure 36. LDO_OUT Entry to Short Circuit

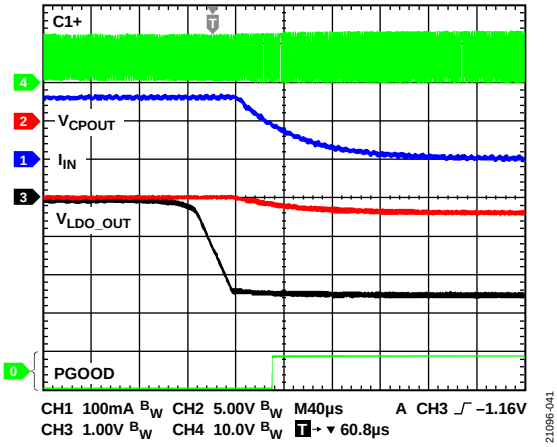


Figure 39. LDO_OUT Recovery From Short Circuit

THEORY OF OPERATION

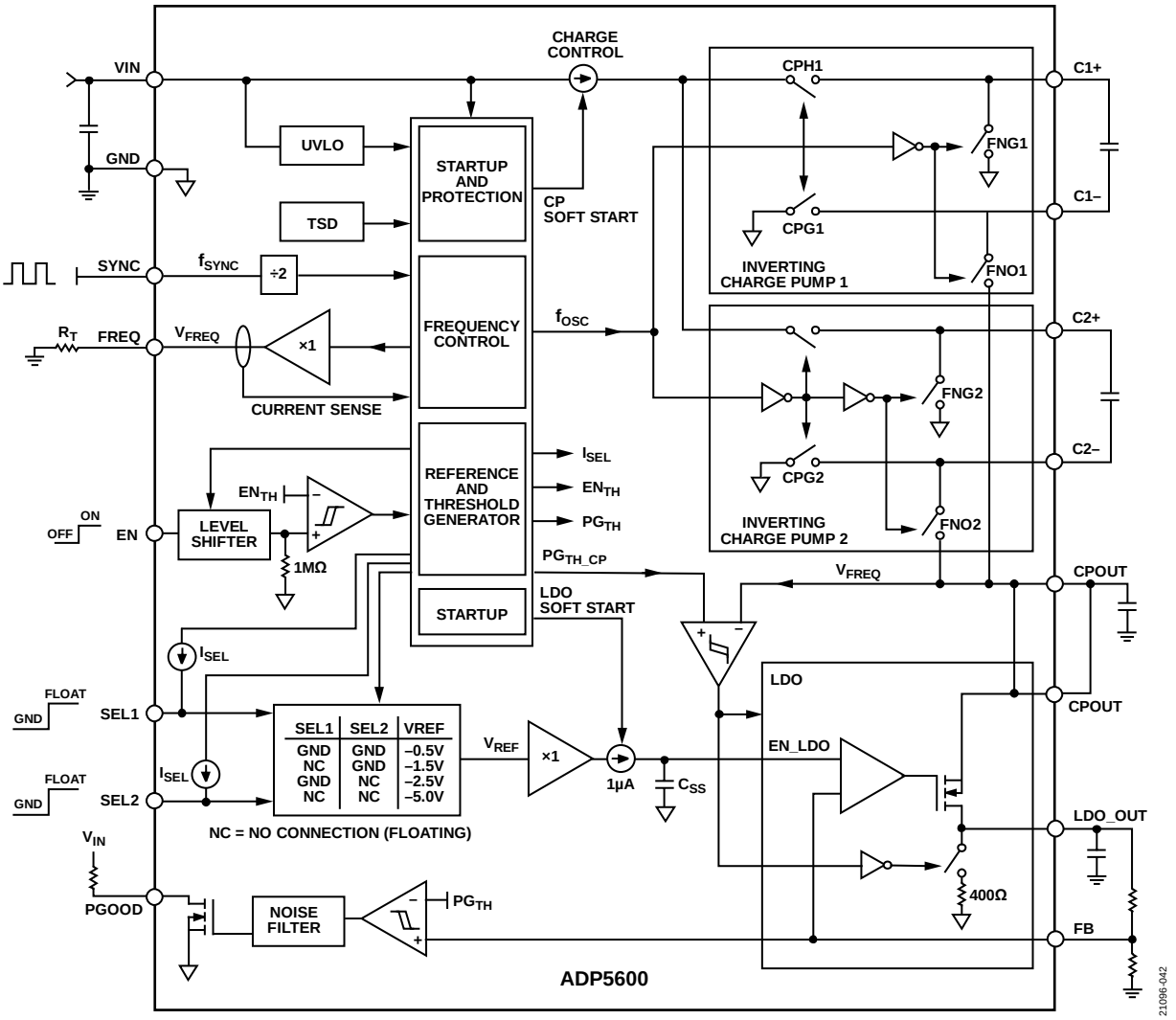


Figure 40. Functional Block Diagram

The ADP5600 is unique among inverting regulators in that it has two charge pump blocks that operate in an interleaving manner. Interleaved operation gives greatly reduced input and output voltage ripple without sacrificing efficiency, output resistance, or ease of use compared to inductor-based solutions. An LDO regulates the output voltage and filters out low frequency spurious signals.

INVERTING CHARGE PUMP OPERATION

The basic voltage conversion task is achieved using a switched capacitor technique with two external charge storage capacitors. An internal oscillator and switching network transfer charge between the two charge storage capacitors. The basic principle of the voltage inversion scheme is illustrated in Figure 41.

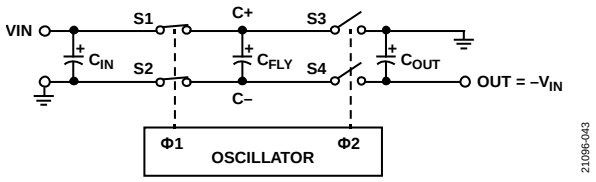


Figure 41. Basic Inverting Charge Pump

In Figure 41, an oscillator generating antiphase signals (φ1 and φ2) controls the S1, S2, and S3, S4 switches. During the charging phase, φ1, the S1 and S2 switches are closed, charging C_{FLY} up to the voltage at VIN. During output phase, φ2, S1 and S2 open and S3 and S4 close. The positive terminal of C_{FLY} is connected to GND via S3 and the negative terminal of C_{FLY} connects to OUT via S4. The charge on C_{FLY} is transferred to C_{OUT} during φ2.

The net result at steady state is voltage inversion at OUT with respect to GND. Ideally, capacitor C_{OUT} maintains its voltage during φ1. However, due to limited storage capacity, this voltage drops due to the load (I_{OUT}) until φ2 arrives. This discharging and charging action of C_{OUT} is the output ripple. The charge transfer efficiency depends on the on-resistance of the switches, the frequency at which they are being switched, and on the equivalent series resistance (ESR) of the external capacitors. For minimum losses and maximum efficiency, capacitors with low ESR are, therefore, recommended.

The charging and discharging current are always discontinuous and the output voltage ripple for the charge pumps is always

$$\Delta V_{OUT} = \frac{I_{OUT}}{2 \times f_{OSC} \times C_{OUT}}$$

Similarly, the input voltage ripple is always

$$\Delta V_{IN} = \frac{I_{OUT}}{2 \times f_{OSC} \times C_{IN}}$$

where:
ΔV_{OUT} is the output voltage ripple.
ΔV_{IN} is the input voltage ripple.
I_{OUT} is the charge pump load current.
f_{OSC} is the charge pump switching frequency.
C_{IN} is the charge pump input capacitor.
C_{OUT} is the charge pump output capacitor.

Therefore, the voltage ripple (noise) can only be improved by decreasing I_{OUT} (impractical), increasing the switching frequency (less efficient), or increasing the capacitance (costly).

By adding another charge pump of the opposite phase, the ADP5600 offers a solution with an almost continuous current flowing at the input and output nodes, greatly reducing the voltage ripple.

INTERLEAVED INVERTING CHARGE PUMP OPERATION

The ADP5600 has two inverting charge pumps that operate in an interleaving manner, requiring the use of two small flying capacitors (C_{C1} and C_{C2}), which are typically of the same value. Each fly capacitor operates on a separate charge pump inverter that runs out of phase with each other. The output is then combined at CPOUT as shown in Figure 42. The interleaving operation results in a periodic ripple that is twice the frequency of the oscillator.

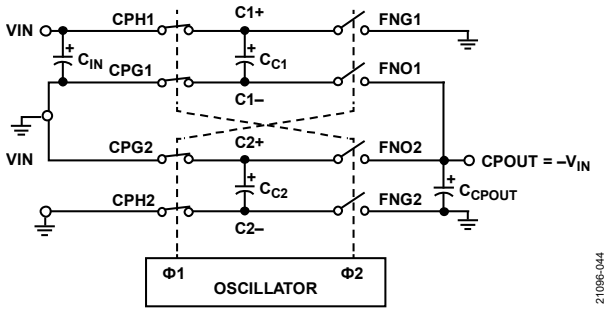


Figure 42. Interleaved Operation

This approach provides a roughly constant input and output current that dramatically reduces the voltage ripple. For an interleaved inverting charge pump, the output voltage ripple is given by

$$\Delta V_{CPOUT} = \frac{I_{CPOUT}}{4 \times f_{OSC} \times C_{CPOUT}} - I_{CPOUT} \times (R_{OUT} - 2 \times R_{ON}) \times \frac{C_{C1}}{C_{CPOUT}} \times \frac{\beta - 1}{\sqrt{\beta}}$$

where:
ΔV_{CPOUT} is the ripple voltage in CPOUT.
I_{CPOUT} is the load current in CPOUT.
f_{OSC} is the charge pump switching frequency.
C_{CPOUT} is the output capacitor in CPOUT.
C_{C1} is the fly capacitor.
R_{OUT} is the effective output resistance of the charge pump.
R_{ON} is the average on resistance of the four switches.

$$\beta = e^{\left(\frac{1}{8 \times f_{OSC} \times R_{ON} \times C_{C1}}\right)}$$

A comparison of the conventional charge pump topology and the interleaving approach is shown in Figure 43 and Figure 44.

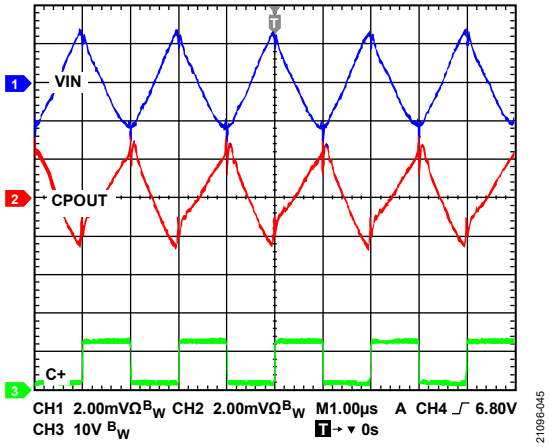


Figure 43. Noninterleaved Charge Pump Operation (f_{OSC} = 500 kHz, C_{IN} = 10 µF, C_1 = 1 µF, C_2 = Float, C_{CPOUT} = 10 µF)

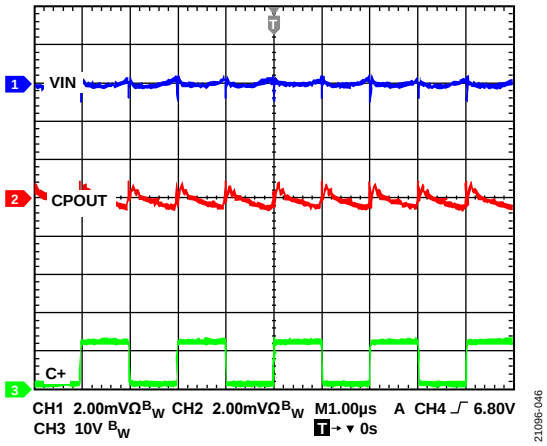


Figure 44. Interleaved Charge Pump Operation (f_{OSC} = 500 kHz, C_{IN} = 10 µF, $C_1 = C_2$ = 1 µF, C_{CPOUT} = 10 µF)

CHARGE PUMP OUTPUT RESISTANCE

The output resistance is the main loss contributor in a charge pump switching converter. A simplified model is shown in Figure 45 where the output resistance is just before the output capacitor. The model shows that when a load current, I_{CPOUT}, is pulled from V_{CPOUT}, a resulting voltage drop is generated.

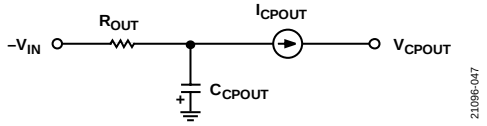


Figure 45. Simplified Output Resistance Model

Always consider the output resistance when designing for a desired output voltage because the voltage drop across the charge pump scales with the load current.

To estimate ADP5600 output resistance, R_{OUT}, use the following equation:

$$R_{OUT} = 1/(2 \times C1 \times f_{OSC}) + 4 \times R_{ON} + 2 \times R_{C1\_ESR}$$

where:
R_{ON} is the average on resistance of the four switches, the typical value is ~2.1 Ω.
R_{C1_ESR} is the ESR of C1.

NEGATIVE LDO REGULATOR

Internally, the ADP5600 has a negative LDO regulator that consists of a reference, an error amplifier, a feedback voltage divider, and an N-channel metal-oxide-semiconductor (NMOS) pass transistor. Current flows from CPOUT to LDO_OUT via the NMOS pass transistor, which is controlled by the error amplifier.

The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is more positive than the reference voltage, the gate of the NMOS transistor is pulled toward GND, allowing more current to pass and increasing the output voltage magnitude. If the feedback voltage is more negative than the reference voltage, the gate of the NMOS transistor is pulled toward V_{CPOUT}, allowing less current to pass and decreasing the output voltage.

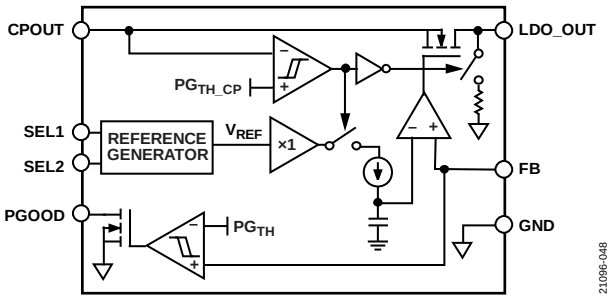


Figure 46. Simplified LDO Model

STARTUP AND SOFT START

Charge Pump Startup

The ADP5600 starts switching when $V_{IN} \geq UVLO_{RISING}$ and $V_{EN} \geq EN_{TH}$. If left unprotected, large inrush currents can flow from C_{IN} to C1 and C2 until the capacitors reach their steady state values. Therefore, the ADP5600 implements a controlled soft start profile where the maximum input current is limited to 200 mA over a time period.

If $V_{IN} \geq UVLO_{RISING}$ and $V_{EN} < EN_{TH}$, the output pull-down resistor is enabled, discharging the output. If $V_{IN} < UVLO_{RISING}$, the output pull-down resistor is disabled.

LDO Soft Start

If the voltage magnitude at CPOUT exceeds PG_{TH_CP}, the LDO is enabled and starts to ramp up the reference voltage at the input of the error amplifier, causing a soft start response at LDO_OUT. Estimate the LDO soft start time, t_{SS}, using the following formula:

$$t_{SS} = (C_{SS} \times V_{LDO\_OUT})/I_{SS}$$

where:
V_{LDO_OUT}, output voltage according to SEL1 and SEL2.
C_{SS}, internal soft start capacitor, is 98.4 pF.
I_{SS}, internal source current to C_{SS}, is 1 µA.

If V_{CPOUT} is less negative than PG_{TH_CP}, the LDO is disabled and the output pull-down resistor is enabled.

Figure 47 shows the start-up response of ADP5600 at different LDO output voltages.

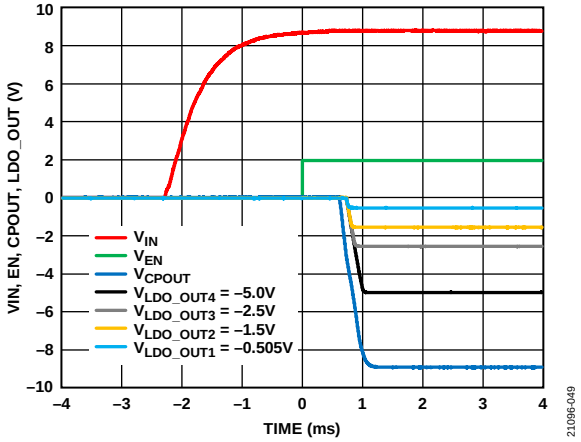


Figure 47. Start-Up Response at Various LDO Output Voltages

PRECISION ENABLE/SHUTDOWN

The EN input pin has a precision analog threshold of 1.2 V (typical) with 70 mV of hysteresis. When the enable voltage exceeds 1.2 V, the regulator turns on; when it falls below 1.13 V (typical), the regulator turns off. To force the regulator to automatically start when input power is applied, connect EN to VIN.

Through an internal switch, the precision EN pin has an internal pull-down resistor of approximately 1 MΩ, providing a default turn-off if the EN pin is open. However, it is not recommended to leave EN open. EN should be pulled high or low to enable or disable the device, respectively.

When the EN pin voltage exceeds 0.8 V (typical), the ADP5600 starts up and enables its housekeeping block. Below this voltage, the device operates in a deep shutdown mode for minimum current consumption. As EN voltage rises to 1.2 V, the precision enable is triggered, turning on the oscillator, charge pump, and LDO blocks.

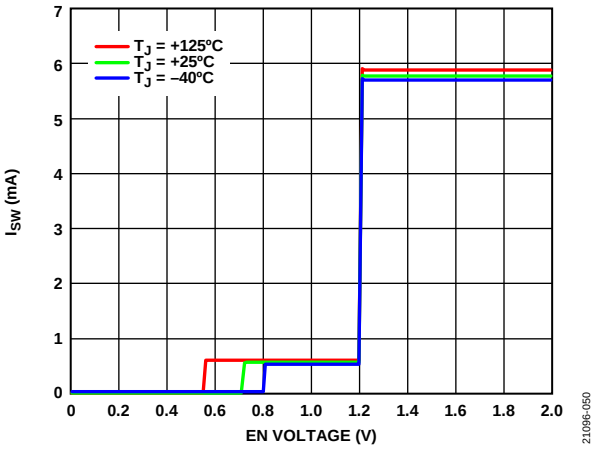


Figure 48. I_{SW} vs. EN Voltage

ADP5600 also includes an output discharge resistor to force the CPOUT and LDO output voltages to zero when the ADP5600 is disabled. This procedure ensures that the outputs of CPOUT and the LDO are always in a well-defined state, whether enabled or not.

OSCILLATOR

The oscillator frequency, f_{OSC}, of the ADP5600 can be set to a value from 100 kHz to 1 MHz by connecting a resistor, R_T, from the FREQ pin to ground. The oscillator frequency can be estimated using the following equation:

$$f_{OSC}\ [\text{kHz}] = 64{,}700/R_T\ [\text{k}\Omega]$$

If R_T is approximately 50 kΩ or less, the oscillator frequency clamps at near 1 MHz.

Figure 49 shows the typical relationship between f_{OSC} and R_T. The adjustable frequency allows the user to make decisions based on the trade-off between efficiency and solution size.

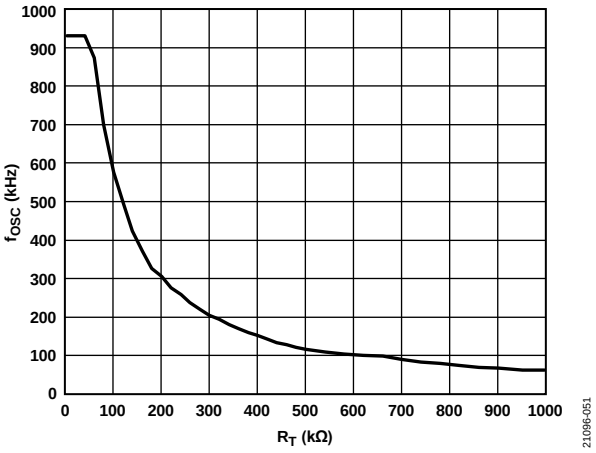


Figure 49. f_{OSC} vs. R_T

SYNCHRONIZATION

To synchronize the ADP5600, connect an external clock to the SYNC pin. The frequency of the external clock can be in the range of 180 kHz to 2.2 MHz. The ADP5600 uses the rising edge of this signal to create the 50% duty cycle charge pump oscillator. Therefore, each of the two charge pumps operates at one half of the SYNC frequency, and the input and output voltage ripple frequency is exactly at the original SYNC input frequency.

If this external clock is applied to the SYNC pin prior to EN, then the ADP5600 starts up with the SYNC signal running the oscillator. If the external clock is applied after the ADP5600 starts up, then the ADP5600 uses the oscillator set by the condition of the FREQ pin until the SYNC signal becomes available. In this way, the charge pump starts up normally even if there is some delay between the enable of the ADP5600 and the application of the synchronization clock.

CURRENT-LIMIT AND OUTPUT SHORT-CIRCUIT PROTECTION (SCP)

The ADP5600 includes a current-limit protection circuitry to limit the input and output current. The current-limit circuitry clamps the current flow to 200 mA on both the charging phase and output phase. Because C1 and C2 are out of phase, there is a continuous 200 mA flowing at VIN and CPOUT, as shown in Figure 50 and Figure 51.

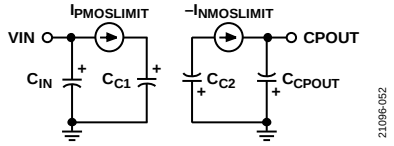


Figure 50. Current Limit, C1 Charging Phase and C2 Output Phase

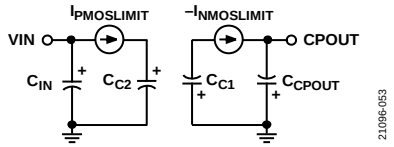


Figure 51. Current Limit, C2 Charging Phase and C1 Output Phase

Figure 52 shows the response of ADP5600 when a hard short from CPOUT to ground occurs.

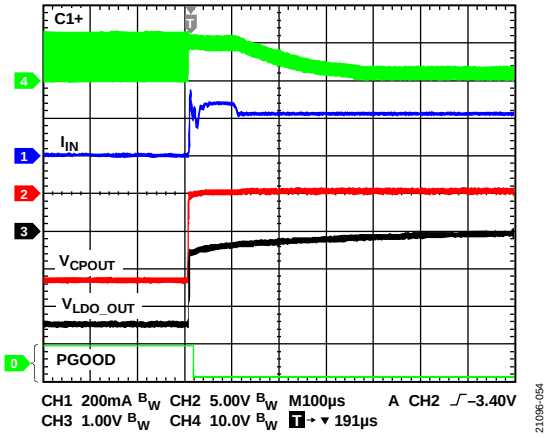


Figure 52. CPOUT Entry to Short Circuit

If the hard short occurs from LDO_OUT to GND, the ADP5600 LDO current limit is hit first, so that only −160 mA is conducted into the short.

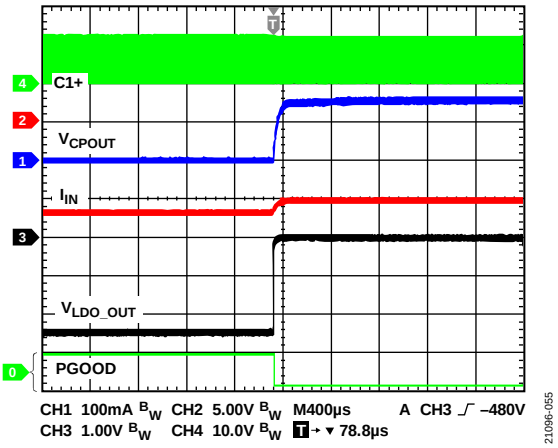


Figure 53. LDO_OUT Entry to Short Circuit

POWER GOOD

Power good (PGOOD) is an active high, open-drain output and requires a resistor to pull it up to a voltage. When PGOOD is high, it indicates that the voltage on the FB pin, and therefore the LDO output voltage, is near the desired value. A low on the PGOOD pin indicates that the voltage on the FB pin is not within the desired value. There is an eight-switching cycle waiting period after FB goes below PG_{TH} and PGOOD asserts low. If V_{FB} goes above PG_{TH} within the eight switching cycles, the event is ignored by the PGOOD circuitry.

UNDERVOLTAGE LOCKOUT (UVLO)

Undervoltage lockout circuitry is integrated in the ADP5600 to prevent the occurrence of power-on glitches. If the VIN voltage drops below $UVLO_{FALLING}$, then the ADP5600 partially shuts down with the oscillator, charge pump, and LDO regulator turned off. When the VIN voltage rises again above $UVLO_{RISING}$, the soft start period is initiated and the ADP5600 is fully enabled.

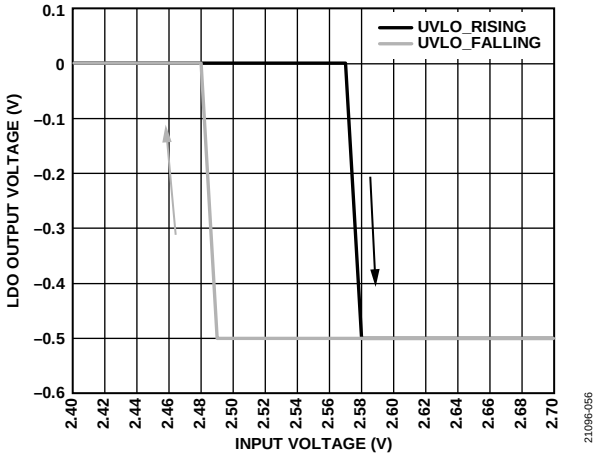


Figure 54. UVLO Threshold

THERMAL CONSIDERATIONS

If the ADP5600 junction temperature rises above 150°C, the internal thermal shutdown circuit turns off the oscillator, charge pump, and LDO for self protection. Extreme junction temperatures can be the result of high current operation, poor circuit board thermal design, and/or high ambient temperature. TSD_{HYS} is included in the thermal shutdown circuit so that if an overtemperature event occurs, the ADP5600 does not return to normal operation until the on-chip temperature drops below 135°C. Upon recovery, both the charge pump and LDO soft starts are initiated before normal operation begins.

The junction temperature of the ADP5600 can be calculated by

$$T_J = T_A + (P_D \times \theta_{JA})$$

where:
T_A is the ambient temperature.
θ_{JA} is the JEDEC thermal resistance.
P_D is the power dissipation in the die, given by

$$P_D = ((V_{IN} - V_{LDO\_OUT}) \times I_{LDO\_OUT}) + (V_{IN} \times I_{SW})$$

where:
V_{IN} and V_{LDO_OUT} are the input and output voltages, respectively.
I_{LDO_OUT} is the LDO load current.
I_{SW} is the active switching current.

Figure 55 shows junction temperature calculations for different ambient temperatures and power dissipation.

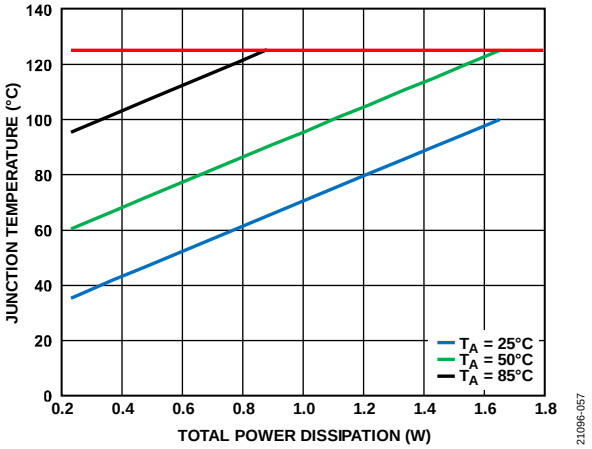


Figure 55. Junction Temperature vs. Total Power Dissipation at Various Ambient Temperatures

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Charge Pump Input and Output Capacitor Selection

The input and output capacitors dictate the amount of ripple voltage present in their respective nodes. The minimum effective capacitance that is required to keep the input and output ripple at a reasonable level is 4.7 µF. A 10 µF 10% X7R ceramic capacitor with twice the voltage rating compared to the intended input voltage is recommended for C_{IN} and C_{CPOUT}.

Charge Pump Flying Capacitor Selection

The flying capacitance affects the output resistance of the charge pump, as seen in Figure 56. A low flying capacitance causes a voltage drop from the input to output transfer due to the small charge storage capacity and higher reactance. In general, higher flying capacitance improves both the load transient response and the steady state ripple.

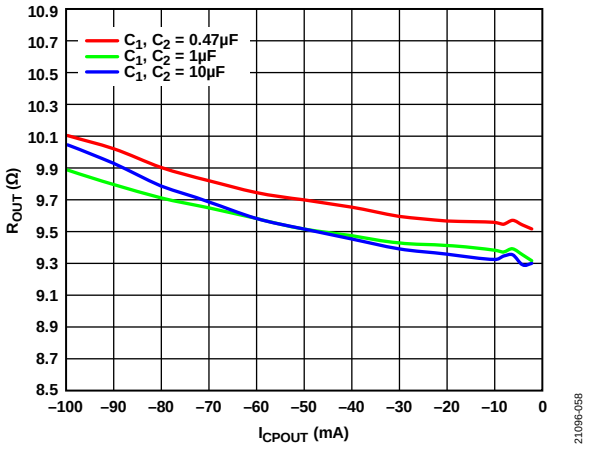


Figure 56. R_{OUT} vs. I_{CPOUT} at Different C_{FLY} Values, f_{OSC} = 500 kHz

LDO Capacitor Selection

ADP5600 is designed to operate with small space-saving ceramic capacitors, as long as its ESR value is taken into consideration. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 2.2 µF capacitance with an ESR of 0.1 Ω or less is recommended to ensure the stability of the ADP5600. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP5600 to large changes in load current. Figure 57 shows the transient response at C_{LDO_OUT} = 10 µF.

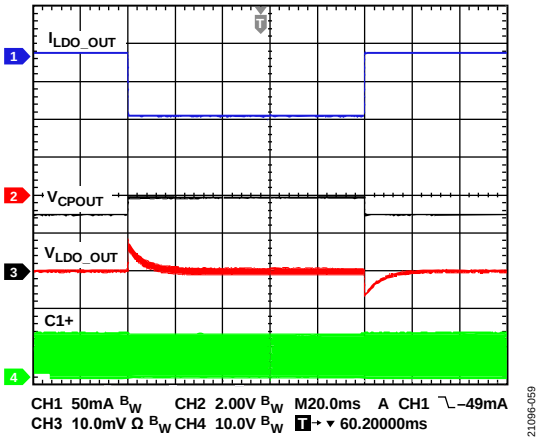


Figure 57. Output Transient Response, C_{LDO_OUT} = 10 µF

OUTPUT VOLTAGE SETTINGS

The inverting charge pump provides a voltage on CPOUT that is approximately equal to the negative of its input voltage and some loss, depending on the output current, I_{CPOUT}, and output resistance, R_{OUT}. More specifically, the CPOUT voltage is given by the equation

$$V_{CPOUT} = -(V_{IN} + I_{CPOUT} \times R_{OUT})$$

where:
V_{CPOUT} is the voltage at CPOUT.
V_{IN} is the voltage at VIN.
I_{CPOUT} is the load current at CPOUT.
R_{OUT} is the charge pump output resistance.

The LDO output voltage of the ADP5600 can be configured for preprogrammed, fixed, output voltages, or adjusted using feedback resistors. Setting the SEL1 and SEL2 pins changes the LDO fixed output voltage, according to Table 8.

Table 8. LDO Fixed Output Voltage Configurations

SEL1	SEL2	V_{LDO_OUT}
GND	GND	−0.505 V
Floating	GND	−1.5 V
GND	Floating	−2.5 V
Floating	Floating	−5.0 V

If the desired output voltage of the LDO is −0.505 V, −1.5 V, −2.5 V, or −5.0 V, set the SEL1 and SEL2 pins as shown in Table 8 and connect the FB pin directly to LDO_OUT. To obtain any other voltage between −0.505 V and $-V_{IN}$, use a resistor divider on the FB pin, as shown in Figure 58.

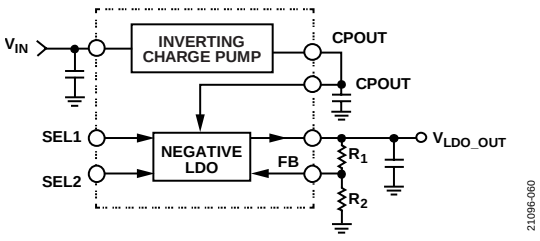


Figure 58. LDO Output Voltage Setup

For the best noise performance, choose the LDO output voltage nearest to the desired adjustable LDO output voltage without exceeding it. For example, if the desired adjustable LDO output voltage is −3.3 V, then choose the −2.5 V LDO output voltage (SEL1 = GND, SEL2 = floating), and place a resistor divider between LDO_OUT, FB, and ground. The programmed adjustable output voltage, V_{ADJ}, can be calculated as

$$V_{ADJ} = V_{LDO\_OUT} \times \left(1 + \frac{R1}{R2}\right)$$

where:
V_{ADJ} is the programmed adjustable LDO output voltage.
V_{LDO_OUT} is the LDO output voltage when the LDO_OUT pin is shorted to the FB pin.
$R1$ is the feedback resistor between LDO_OUT and FB.
$R2$ is the feedback resistor between FB and GND (R2 is recommended to be 40 kΩ or higher).

NOISE REDUCTION

The low output noise of the ADP5600 is achieved by keeping the LDO error amplifier in unity gain and setting the reference voltage equal to the output voltage. The ADP5600 uses two feedback resistors to adjust the output of the LDO. The disadvantage of this LDO scheme is that the output voltage noise is proportional to the error amplifier gain and total feedback resistance.

The LDO circuit can be modified slightly to reduce the output voltage noise to levels close to that of the fixed output of the ADP5600. The circuit shown in Figure 59 adds two additional components to the output voltage setting resistor divider. C_{NR} and R_{NR} are added in parallel with R_1 to reduce the ac gain of the error amplifier. R_{NR} is chosen to be nearly equal to R_2, limiting the ac gain of the error amplifier to approximately 6 dB. The actual gain is the parallel combination of R_{NR} and R_1 divided by R_2. This resistance ensures that the error amplifier always operates at greater than unity gain.

C_{NR} is chosen by setting the reactance of C_{NR} equal to $R_1 - R_{NR}$ at a frequency between 10 Hz and 100 Hz. This capacitance sets the frequency where the ac gain of the error amplifier is 3 dB down from its dc gain.

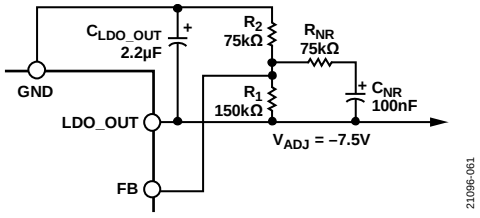


Figure 59. Noise Reduction Modification

The noise of the adjustable LDO is found by using the following formula, assuming the noise of a fixed output LDO is approximately 59 µV:

$$Noise = 59\ \mu V \times (R_{PAR} + R_2) \div R_2$$

where R_{PAR} is a parallel combination of R_1 and R_{NR}.

Based on the component values shown in Figure 59, the ADP5600 has the following characteristics:

- DC gain of 3 (9.54 dB)
- High frequency ac gain of 1.67 (4.44 dB)
- Measured rms noise of the adjustable LDO at −100 mA without noise reduction of ~163 µV rms
- Measured rms noise of the adjustable LDO at −100 mA with noise reduction circuit of ~99 µV rms

Figure 60 shows the difference in noise spectral density for the adjustable ADP5600 set to −7.5 V with and without the noise reduction network. In the 20 Hz to 20 kHz frequency range, the reduction in noise is observable.

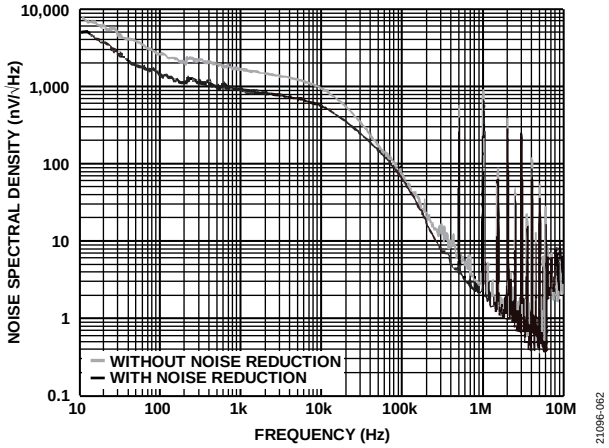


Figure 60. V_{ADJ} = −7.5 V Adjustable ADP5600 With and Without the Noise Reduction Network (C_{NR} and R_{NR})

CHANGING THE OSCILLATOR SOURCE ON-THE-FLY

The Synchronization section describes how the charge pumps react on application and removal of an external clock on the SYNC pin. The charge pump frequency transitions smoothly upon syncing to the external clock. However, upon removal of the external clock, the charge pump stops switching, which causes a drop at CPOUT, leaving the C_{CPOUT} supplying the charge requirement of the output (see Figure 61).

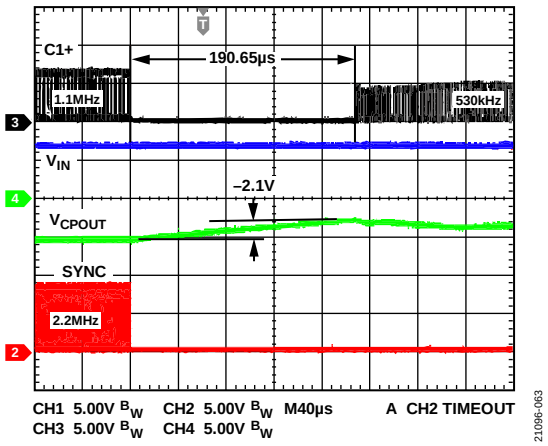


Figure 61. Response of CPOUT upon Removal of the External Clock on SYNC

If LDO is the only load of CPOUT and it has not reached its dropout region then the LDO can be represented by a constant current source and the effective circuit at the charge pump output is shown in Figure 62.

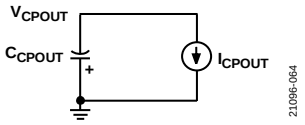


Figure 62. Simplified Circuit of the Output upon Removal of External Clock on SYNC

The effective circuit is similar to a simple discharging of a capacitor using a current source, I_{CPOUT}. This drop can be estimated using the following equation:

$$V_{SYNCOFF} = (I_{CPOUT} \times t_{SYNCOFF})/C_{CPOUT}$$

where:

$V_{SYNCOFF}$ is the drop from the initial CPOUT voltage.

$t_{SYNCOFF}$ is 189.63 µs (typical).

I_{CPOUT} is the total current being pulled out of the C_{CPOUT} capacitor.

C_{CPOUT} is the effective capacitance at CPOUT, this includes tolerance, dc bias effect, and temperature coefficient.

DESIGN EXAMPLE

This section provides an example of the step by step design procedures and the external components required for ADP5600. Table 9 lists the design requirements for this example.

Table 9. Example Design Requirements for ADP5600

Parameter	Specification
LDO Output Voltage	V_{LDO_OUT} = −3.3 V
LDO Output Current	I_{LDO_OUT} = −100 mA

SETTING THE SWITCHING FREQUENCY OF THE CHARGE PUMP

The first step is to determine the switching frequency for the ADP5600 design. In general, higher switching frequencies produce a smaller solution size due to the lower component values required, whereas lower switching frequencies result in higher conversion efficiency due to lower switching losses.

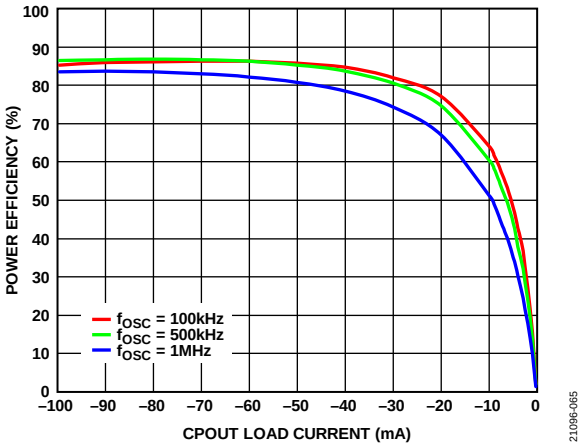


Figure 63. Power Efficiency vs. I_{CPOUT} at Various Oscillator Frequencies

The oscillator frequency of the ADP5600 can be set from 0.1 MHz to 1 MHz by connecting a resistor from the FREQ pin to ground. The selected resistor allows the user to make decisions based on the trade-off between efficiency and solution size.

In this design example, a switching frequency of 500 kHz achieves an ideal combination of small solution size and high conversion efficiency. To set the switching frequency to 500 kHz, use the following equation to calculate the R_T value:

$$R_T\ [\text{k}\Omega] = 64{,}700/f_{OSC}\ [\text{kHz}]$$

Therefore, select a standard resistor, R_T = 130 kΩ.

SELECTING THE CHARGE PUMP FLYING CAPACITOR

The flying capacitor dictates the amount of voltage drop across the charge pump due to the output resistance ,which depends on the charge pump switching frequency.

Operation at high switching frequencies allows the use of smaller flying capacitances, however, the minimum value is limited due to its inverse effect on the charge pump impedance.

Refer to Table 10 for the recommended flying capacitor value for each switching frequency.

Table 10. Recommended Minimum C1 and C2

f_{OSC}	C1 and C2 Capacitances
100 kHz	1 µF
250 kHz	1 µF
500 kHz	1 µF
750 kHz	0.47 µF
1 MHz	0.47 µF

SETTING THE OUTPUT VOLTAGE OF THE LDO REGULATOR

Select a value for R_2 and then calculate R_1 by using the following equation:

$$R_1 = ((V_{ADJ}/V_{LDO\_OUT}) - 1) \times R_2$$

where:
V_{LDO_OUT} is −2.5 V.
R_1 is the feedback resistor between LDO_OUT and FB.
R_2 is the feedback resistor between FB and GND (R_2 is recommended to be 40 kΩ or higher).

To set the output voltage to −3.3 V, R_2 is set to 40 kΩ, giving a calculated R_1 value of 12.8 kΩ.

DETERMINING THE MINIMUM V_{IN} VOLTAGE

To achieve the desired performance of the ADP5600, a minimum input voltage, V_{IN}, is required per application. This both considers the PSRR performance that requires a headroom voltage across the LDO and the drop on the charge pump due to the output resistance. To calculate the minimum V_{IN}, use the following formula:

$$V_{IN} = V_{LDO\_OUT} + V_{HR} + (R_{OUT} \times I_{CPOUT})$$

where:
R_{OUT} is the output resistance of the charge pump.
V_{HR} is the LDO headroom required to achieve a certain PSRR performance. The recommended minimum headroom voltage is 500 mV.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Because the internal switches of the ADP5600 turn on and off very fast, good printed circuit board (PCB) layout practices are critical to ensure optimum operation of the device. Improper layouts result in poor load regulation, especially under heavy loads. Output performance can be improved by following these simple layout guidelines:

- Place the input capacitor (C_{IN}) as close as possible to the VIN and GND pins.
- Place the output capacitors (C_{CPOUT}) and C_{LDO_OUT} as close as possible to the CPOUT/LDO_OUT and GND pins.
- Place fly capacitors (C_{C1} and C_{C2}) close to the respective fly capacitor pins (C1+/C2+ and C1−/C2−).
- Use of 0603 and 0402 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.
- Connect the exposed pad to CPOUT.
- Use adequate ground and power traces or planes.
- Use a single-point ground for device ground and input and output capacitor grounds.
- Keep external components as close to the device as possible.
- Use short and wide traces/planes from the input and output capacitors to the input and output pins, respectively.

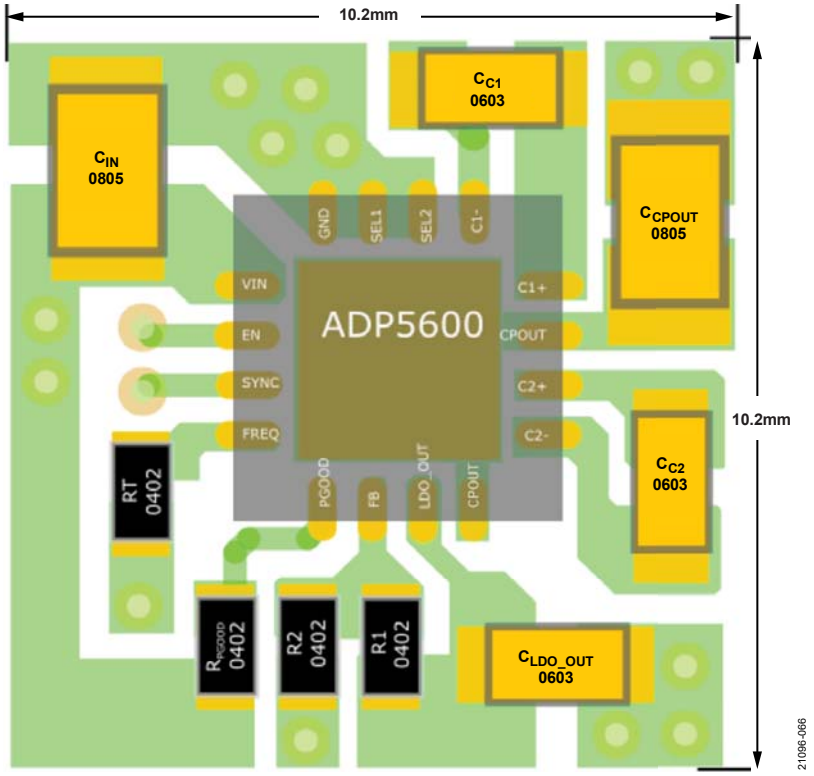
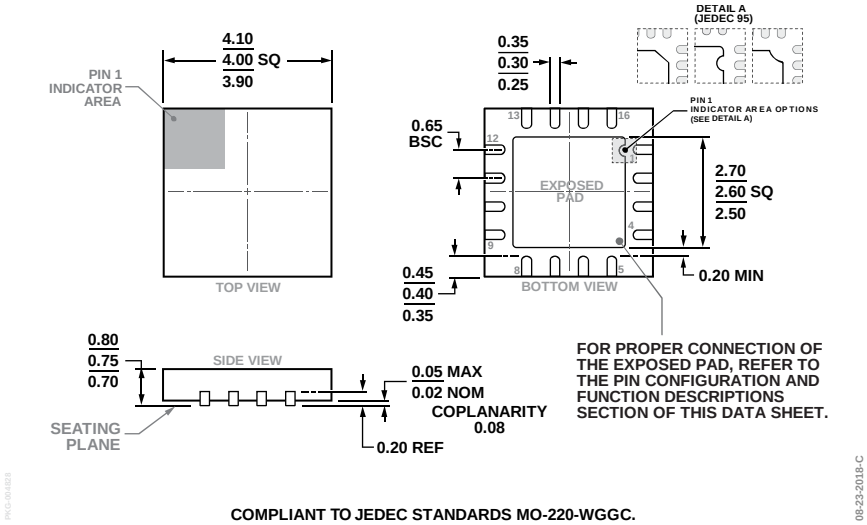


Figure 64. Example PCB Layout

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 65. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP5600ACPZ-R7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-17
ADP5600CP-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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