Quad 3-State Noninverting Buffers

High-Performance Silicon-Gate CMOS

The MC74HC125A and MC74HC126A are identical in pinout to the LS125 and LS126. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

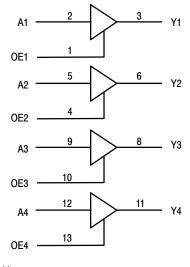
The HC125A and HC126A noninverting buffers are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The devices have four separate output enables that are active-low (HC125A) or active-high (HC126A).

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

LOGIC DIAGRAM

HC125A



HC126A

Active-High Output Enables

PIN 14 = V_{CC} PIN 7 = GND



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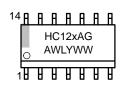


SOIC-14 NB D SUFFIX CASE 751A TSSOP-14 DT SUFFIX CASE 948G

PIN ASSIGNMENT

OE1	1●	14	v _{cc}
A1 [2	13	OE4
Y1 [3	12	A4
OE2 [4	11	Y4
A2 [5	10	ОЕЗ
Y2 [6	9	_ A3
GND [7	8	Y3
			•

MARKING DIAGRAMS





SOIC-14 NB

TSSOP-14

x = 5, 6

A = Assembly Location

L, WL = Wafer Lot Y, YY = Year

W, WW = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

	HC1	25A	
Inp	outs	Output	
Α	OE	Y	
Н	L	Н	
L	L	L	
lχ	Н	Z	

HC126A				
Inputs Output				
Α	OE	Y		
Н	Н	Н		
L	Н	L		
Х	L	Z		

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

1

13

OE4

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I _{in}	DC Input Current, per Pin	±20	mA
l _{out}	DC Output Current, per Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air SOIC Package† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or TSSOP Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: –7 mW/°C from 65° to 125°C TSSOP Package: –6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time $V_{CC} = 2.0$ (Figure 1) $V_{CC} = 4.5$ $V_{CC} = 6.0$	0	1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Guaranteed Limit			
Symbol	Parameter	Test Conditions	v _{cc} v	–55 to 25°C	≤ 85°C	≤ 125°C	Unit
V _{IH}	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$	2.0	1.5	1.5	1.5	V
		$ I_{out} \le 20 \mu\text{A}$	3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V	2.0	0.5	0.5	0.5	V
		$ I_{out} \le 20 \mu\text{A}$	3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output	$V_{in} = V_{IH}$	2.0	1.9	1.9	1.9	V
	Voltage	$ I_{out} \le 20 \mu\text{A}$	4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH}$ $ I_{out} \le 3.6 \text{ mA}$	3.0	2.48	2.34	2.2	
		$ I_{out} \le 6.0 \text{ mA}$	4.5	3.98	3.84	3.7	
		$ I_{out} \le 7.8 \text{ mA}$	6.0	5.48	5.34	5.2	
V _{OL}	Maximum Low-Level Output	$V_{in} = V_{IL}$	2.0	0.1	0.1	0.1	V
	Voltage	$ I_{out} \le 20 \mu\text{A}$	4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IL}$ $ I_{out} \le 3.6 \text{ mA}$	3.0	0.26	0.33	0.4	
		$ I_{out} \le 6.0 \text{ mA}$	4.5	0.26	0.33	0.4	
		$ I_{out} \le 7.8 \text{ mA}$	6.0	0.26	0.33	0.4	
l _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μΑ
l _{OZ}	Maximum Three–State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	±0.5	±5.0	±10	μΑ
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4.0	40	160	μΑ

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \ pF$, Input $t_r = t_f = 6.0 \ ns$)

			Guaranteed Limit			
Symbol	Parameter	V _{CC}	–55 to 25°C	≤ 85°C	≤ 125°C	Unit
t _{PLH} ,	Maximum Propagation Delay, Input A to Output Y	2.0	90	115	135	ns
t_{PHL}	(Figures 1 and 3)	3.0	36	45	60	
		4.5	18	23	27	
		6.0	15	20	23	
t _{PLZ} ,	Maximum Propagation Delay, Output Enable to Y	2.0	120	150	180	ns
t_{PHZ}	(Figures 2 and 4)	3.0	45	60	80	
		4.5	24	30	36	
		6.0	20	26	31	
t _{PZL} ,	Maximum Propagation Delay, Output Enable to Y	2.0	90	115	135	ns
t_{PZH}	(Figures 2 and 4)	3.0	36	45	60	
		4.5	18	23	27	
		6.0	15	20	23	
t _{TLH} ,	Maximum Output Transition Time, Any Output	2.0	60	75	90	ns
t_{THL}	(Figures 1 and 3)	3.0	22	28	34	
		4.5	12	15	18	
		6.0	10	13	15	
C _{in}	Maximum Input Capacitance	-	10	10	10	pF
C _{out}	Maximum 3-State Output Capacitance (Output in High-Impedance State)	-	15	15	15	pF
			Typical	@ 25°C, V _C	_C = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)*			30		pF

^{*} Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

SWITCHING WAVEFORMS

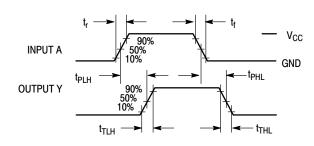


Figure 1.

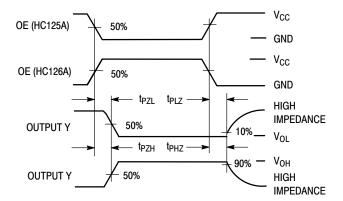
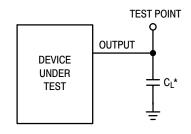


Figure 2.



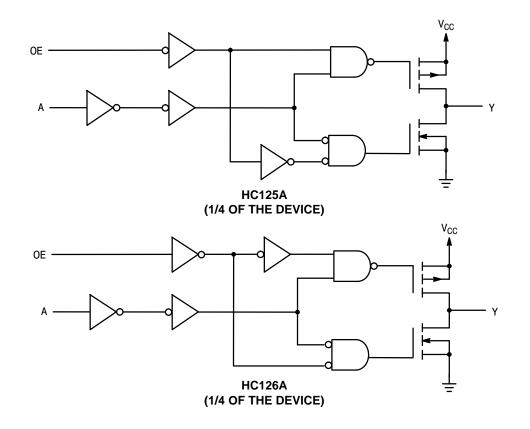
*Includes all probe and jig capacitance

DEVICE UNDER TEST C_L^* CONNECT TO V_{CC} WHEN TESTING t_{PLZ} AND t_{PZL} . CONNECT TO GND WHEN TESTING t_{PHZ} and t_{PZH} .

*Includes all probe and jig capacitance

Figure 3. Test Circuit

Figure 4. Test Circuit



ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HC125ADG	SOIC-14 NB (Pb-Free)	55 Units / Rail
MC74HC125ADR2G	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel
MC74HC125ADTG	TSSOP-14 (Pb-Free)	96 Units / Rail
MC74HC125ADTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
MC74HC126ADG	SOIC-14 NB (Pb-Free)	55 Units / Rail
MC74HC126ADR2G	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel
MC74HC126ADTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NLV74HC125ADG*	SOIC-14 NB (Pb-Free)	55 Units / Rail
NLV74HC125ADR2G*	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel
NLV74HC125ADTG*	TSSOP-14 (Pb-Free)	55 Units / Rail
NLV74HC125ADTR2G*	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NLV74HC126ADR2G*	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel
NLV74HC126ADTR2G*	TSSOP-14 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

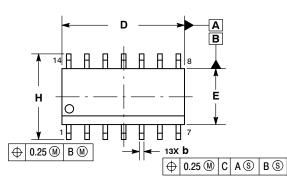
^{*}NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

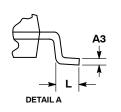


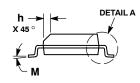
△ 0.10

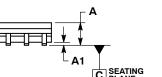
SOIC-14 NB CASE 751A-03 ISSUE L

DATE 03 FEB 2016









- NOTES:
 1. DIMENSIONING AND TOLERANCING PER
 - ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
 - DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT
 - MAXIMUM MATERIAL CONDITION.
 DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
- 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
АЗ	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
Е	3.80	4.00	0.150	0.157
œ	1.27	BSC	0.050 BSC	
Н	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
М	0 °	7°	0 °	7 °

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code Α = Assembly Location

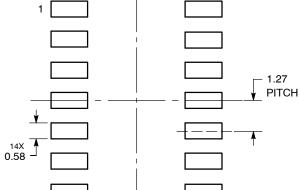
WL = Wafer Lot Υ = Year WW = Work Week G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator. "G" or microdot " ■". may or may not be present.

1 [1.18

SOLDERING FOOTPRINT*

- 6.50 —



DIMENSIONS: MILLIMETERS

STYLES ON PAGE 2

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^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

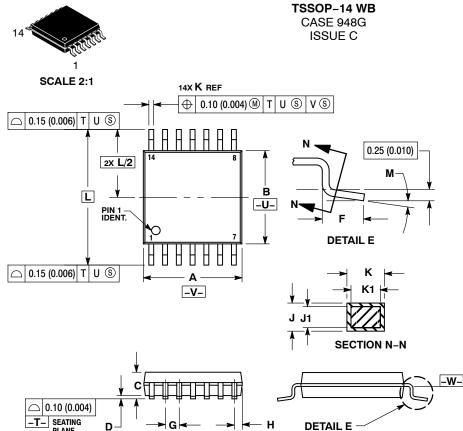
SOIC-14 CASE 751A-03 ISSUE L

DATE 03 FEB 2016

STYLE 1: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. NO CONNECTION 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. NO CONNECTION 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 2: CANCELLED	STYLE 3: PIN 1. NO CONNECTION 2. ANODE 3. ANODE 4. NO CONNECTION 5. ANODE 6. NO CONNECTION 7. ANODE 8. ANODE 9. ANODE 10. NO CONNECTION 11. ANODE 12. ANODE 13. NO CONNECTION 14. COMMON CATHODE	STYLE 4: PIN 1. NO CONNECTION 2. CATHODE 3. CATHODE 4. NO CONNECTION 5. CATHODE 6. NO CONNECTION 7. CATHODE 8. CATHODE 9. CATHODE 10. NO CONNECTION 11. CATHODE 12. CATHODE 13. NO CONNECTION 14. COMMON ANODE
STYLE 5: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. NO CONNECTION 7. COMMON ANODE 8. COMMON CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. ANODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE	STYLE 7: PIN 1. ANODE/CATHODE 2. COMMON ANODE 3. COMMON CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. ANODE/CATHODE 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. COMMON CATHODE 12. COMMON ANODE 13. ANODE/CATHODE 14. ANODE/CATHODE	STYLE 8: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. ANODE/CATHODE 7. COMMON ANODE 8. COMMON ANODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. NO CONNECTION 12. ANODE/CATHODE 13. ANODE/CATHODE 14. COMMON CATHODE

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DATE 17 FEB 2016

- NOTES.

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

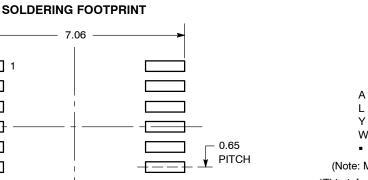
 3. DIMENSION A DOES NOT INCLUDE MOLD
- FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 DIMENSION B DOES NOT INCLUDE
- INTERLEAD FLASH OR PROTRUSION.
 INTERLEAD FLASH OR PROTRUSION SHALL
- INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.

 6. TERMINAL NUMBERS ARE SHOWN FOR DEFERENCE ONLY
- REFERENCE ONLY.
 DIMENSION A AND B ARE TO BE
- DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
Н	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
М	o °	8 °	o °	a °

GENERIC MARKING DIAGRAM*



DIMENSIONS: MILLIMETERS



= Assembly Location

= Wafer Lot = Year

= Work Week

= Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

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