

## LMP8646 Precision Current Limiter

### 1 Features

- Provides Circuit Protection and Current Limiting
- Single Supply Operation
- –2-V to 76-V Common-Mode Voltage Range
- Variable Gain Set by External Resistor
- Adjustable Bandwidth Set by External Capacitor
- Buffered Output
- 3% Output Accuracy Achievable at  $V_{SENSE} = 100$  mV
- Key Specifications:
  - Supply Voltage Range 2.7 V to 12 V
  - Output Current (Source) 0 to 5 mA
  - Gain Accuracy 2.0% (max)
  - Transconductance 200  $\mu\text{A/V}$
  - Offset  $\pm 1$  mV (Maximum)
  - Quiescent Current 380  $\mu\text{A}$
  - Input Bias 12  $\mu\text{A}$  (Typical)
  - PSRR 85 dB
  - CMRR 95 dB
  - Temperature Range  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
  - 6-Pin SOT Package

### 2 Applications

- High-Side and Low-Side Current Limit
- Circuit Fault Protection
- Battery and Supercap Charging
- LED Constant Current Drive
- Power Management

### 3 Description

The LMP8646 is a precision current limiter used to improve the current limit accuracy of any switching or linear regulator with an available feedback node.

The LMP8646 accepts input signals with a common-mode voltage ranging from  $-2$  V to 76 V. It has a variable gain which is used to adjust the sense current. The gain is configured with a single external resistor,  $R_G$ , providing a high level of flexibility and accuracy up to 2%. The adjustable bandwidth, which allows the device to be used with a variety of applications, is configurable with a single external capacitor in parallel with  $R_G$ . In addition, the output is buffered in order to provide a low output impedance.

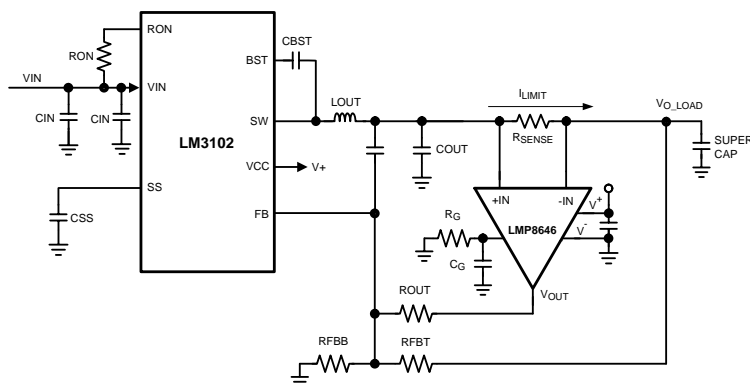
The LMP8646 is an ideal choice for industrial, automotive, telecommunications, and consumer applications where circuit protection and improved precision systems are required. The LMP8646 is available in a 6-pin SOT package and can operate at temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMP8646	SOT (6)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Typical Application



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	7.2 Functional Block Diagram .....	<b>13</b>
<b>2 Applications</b> .....	<b>1</b>	7.3 Feature Description .....	<b>13</b>
<b>3 Description</b> .....	<b>1</b>	7.4 Device Functional Modes .....	<b>15</b>
<b>4 Revision History</b> .....	<b>2</b>	<b>8 Application and Implementation</b> .....	<b>17</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	8.1 Application Information .....	<b>17</b>
<b>6 Specifications</b> .....	<b>4</b>	8.2 Typical Applications .....	<b>17</b>
6.1 Absolute Maximum Ratings .....	<b>4</b>	<b>9 Power Supply Recommendations</b> .....	<b>23</b>
6.2 ESD Ratings .....	<b>4</b>	<b>10 Layout</b> .....	<b>23</b>
6.3 Recommended Operating Conditions .....	<b>4</b>	10.1 Layout Guidelines .....	<b>23</b>
6.4 Thermal Information .....	<b>4</b>	10.2 Layout Example .....	<b>23</b>
6.5 Electrical Characteristics: 2.7 V .....	<b>5</b>	<b>11 Device and Documentation Support</b> .....	<b>24</b>
6.6 Electrical Characteristics: 5 V .....	<b>6</b>	11.1 Trademarks .....	<b>24</b>
6.7 Electrical Characteristics: 12 V .....	<b>7</b>	11.2 Electrostatic Discharge Caution .....	<b>24</b>
6.8 Typical Characteristics .....	<b>8</b>	11.3 Glossary .....	<b>24</b>
<b>7 Detailed Description</b> .....	<b>13</b>	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>24</b>
7.1 Overview .....	<b>13</b>		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision A (March 2013) to Revision B

Page

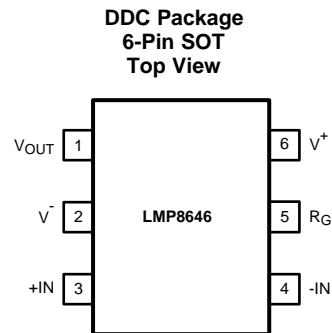
- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ..... **1**

### Changes from Original (March 2013) to Revision A

Page

- Changed layout of National Semiconductor Data Sheet to TI format ..... **22**

## 5 Pin Configuration and Functions



### Pin Functions

PIN		DESCRIPTION
NAME	NO.	
$V_{OUT}$	1	Single-Ended Output Voltage
$V^-$	2	Negative Supply Voltage. This pin should be connected to ground.
+IN	3	Positive Input
-IN	4	Negative Input
$R_G$	5	External Gain Resistor. An external capacitance ( $C_G$ ) may be added in parallel with $R_G$ to limit the bandwidth.
$V^+$	6	Positive Supply Voltage

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(1)</sup>

	MIN	MAX	UNIT
Supply Voltage ( $V_S = V^+ - V^-$ )		13.2	V
Differential voltage +IN- (-IN)		6	V
Voltage at pins +IN, -IN	-6	80	V
Voltage at $R_G$ pin		13.2	V
Voltage at OUT pin	$V^-$	$V^+$	V
Junction Temperature <sup>(2)</sup>		150	°C
Storage temperature range	-65	150	°C
For soldering specifications see <a href="#">SNOA549</a>			

- (1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the *Electrical Characteristics: 2.7 V* tables.
- (2) The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{J(MAX)}$ ,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable power dissipation  $P_{DMAX} = (T_{J(MAX)} - T_A) / \theta_{JA}$  or the number given in Absolute Maximum Ratings, whichever is lower.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	Pins +IN and -IN	±4000	V
		All pins except +IN and -IN	±2000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>		±1250	
	Machine model		±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply Voltage ( $V_S = V^+ - V^-$ )	2.7	12	V
Temperature Range <sup>(1)</sup>	-40	125	V

- (1) The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{J(MAX)}$ ,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable power dissipation  $P_{DMAX} = (T_{J(MAX)} - T_A) / \theta_{JA}$  or the number given in Absolute Maximum Ratings, whichever is lower.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LMP8646	UNIT
		DDC	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics: 2.7 V

Unless otherwise specified, all limits ensured for at  $T_A = 25^\circ\text{C}$ ,  $V_S = (V^+ - V^-) = (2.7\text{ V} - 0\text{ V}) = 2.7\text{ V}$ ,  $-2\text{ V} < V_{\text{CM}} < 76\text{ V}$ ,  $R_G = 25\text{ k}\Omega$ ,  $R_L = 10\text{ k}\Omega$ .<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
V <sub>OFFSET</sub>	Input Offset Voltage	V <sub>CM</sub> = 2.1 V	-1		1	mV
		V <sub>CM</sub> = 2.1 V, -40°C ≤ T <sub>J</sub> ≤ 125°C	-1.7		1.7	
TCV <sub>OS</sub>	Input Offset Voltage Drift <sup>(4)(5)</sup>	V <sub>CM</sub> = 2.1 V			7	μV/°C
I <sub>B</sub>	Input Bias Current <sup>(6)</sup>	V <sub>CM</sub> = 2.1 V		12	20	μA
e <sub>ni</sub>	Input Voltage Noise <sup>(5)</sup>	f > 10 kHz, R <sub>G</sub> = 5 kΩ		120		nV/√Hz
V <sub>SENSE</sub>	Max Input Sense Voltage <sup>(5)</sup>	V <sub>CM</sub> = 12 V, R <sub>G</sub> = 5 kΩ			600	mV
Gain A <sub>V</sub>	Adjustable Gain Setting <sup>(5)</sup>	V <sub>CM</sub> = 12 V	1		100	V/V
G <sub>m</sub>	Transconductance = 1/R <sub>IN</sub>	V <sub>CM</sub> = 2.1 V		200		μA/V
	Accuracy	V <sub>CM</sub> = 2.1 V	-2%		2%	
		V <sub>CM</sub> = 2.1 V, -40°C ≤ T <sub>J</sub> ≤ 125°C	-3.4%		3.4%	
G <sub>m</sub> drift <sup>(5)</sup>	-40°C to 125°C, V <sub>CM</sub> = 2.1 V			140	ppm /°C	
PSRR	Power Supply Rejection Ratio	V <sub>CM</sub> = 2.1 V, 2.7 V < V <sup>+</sup> < 12 V	85			dB
CMRR	Common-Mode Rejection Ratio	2.1 V < V <sub>CM</sub> < 76 V	95			dB
		-2 V < V <sub>CM</sub> < 2.1 V	55			
SR	Slew Rate <sup>(7)(5)</sup>	V <sub>CM</sub> = 5 V, C <sub>G</sub> = 4 pF, V <sub>SENSE</sub> from 25 mV to 175 mV, C <sub>L</sub> = 30 pF, R <sub>L</sub> = 1MΩ		0.5		V/μs
I <sub>S</sub>	Supply Current	V <sub>CM</sub> = 2.1 V		380	610	μA
		V <sub>CM</sub> = 2.1 V, -40°C ≤ T <sub>J</sub> ≤ 125°C			807	
		V <sub>CM</sub> = -2 V		2000	2500	
		V <sub>CM</sub> = -2 V, -40°C ≤ T <sub>J</sub> ≤ 125°C			2700	
V <sub>OUT</sub>	Maximum Output Voltage	V <sub>CM</sub> = 2.1 V, R <sub>G</sub> = 500 kΩ	1.1			V
	Minimum Output Voltage	V <sub>CM</sub> = 2.1 V			20	mV
	Maximum Output Voltage	V <sub>S</sub> = V <sub>CM</sub> = 3.3 V, R <sub>G</sub> = 500 kΩ	1.6			V
	Minimum Output Voltage	V <sub>S</sub> = V <sub>CM</sub> = 3.3 V, R <sub>G</sub> = 500 kΩ			22	mV
I <sub>OUT</sub>	Output current <sup>(5)</sup>	Sourcing, V <sub>OUT</sub> = 600 mV, R <sub>G</sub> = 150 kΩ		5		mA
C <sub>LOAD</sub>	Max Output Capacitance Load <sup>(5)</sup>			30		pF

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T<sub>J</sub> = T<sub>A</sub>. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T<sub>J</sub> > T<sub>A</sub>.
- (2) All limits are specified by testing, design, or statistical analysis.
- (3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
- (4) Offset voltage temperature drift is determined by dividing the change in V<sub>OS</sub> at the temperature extremes by the total temperature change.
- (5) This parameter is specified by design and/or characterization and is not tested in production.
- (6) Positive Bias Current corresponds to current flowing into the device.
- (7) The number specified is the average of rising and falling slew rates and measured at 90% to 10%.

## 6.6 Electrical Characteristics: 5 V

Unless otherwise specified, all limits ensured for at  $T_A = 25^\circ\text{C}$ ,  $V_S = V^+ - V^-$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $-2\text{ V} < V_{CM} < 76\text{ V}$ ,  $R_G = 25\text{ k}\Omega$ ,  $R_L = 10\text{ k}\Omega$ .<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
V <sub>OFFSET</sub>	Input Offset Voltage	V <sub>CM</sub> = 2.1 V	-1		1	mV
		V <sub>CM</sub> = 2.1 V, -40°C ≤ T <sub>J</sub> ≤ 125°C	-1.7		1.7	
TCV <sub>OS</sub>	Input Offset Voltage Drift <sup>(4)(5)</sup>	V <sub>CM</sub> = 2.1 V			7	μV/°C
I <sub>B</sub>	Input Bias Current <sup>(6)</sup>	V <sub>CM</sub> = 2.1 V		12.5	22	μA
e <sub>ni</sub>	Input Voltage Noise <sup>(5)</sup>	f > 10 kHz, R <sub>G</sub> = 5 kΩ		120		nV/√Hz
V <sub>SENSE(MAX)</sub>	Max Input Sense Voltage <sup>(5)</sup>	V <sub>CM</sub> = 12 V, R <sub>G</sub> = 5 kΩ		600		mV
Gain A <sub>V</sub>	Adjustable Gain Setting <sup>(5)</sup>	V <sub>CM</sub> = 12 V	1		100	V/V
G <sub>m</sub>	Transconductance = 1/R <sub>IN</sub>	V <sub>CM</sub> = 2.1 V		200		μA/V
	Accuracy	V <sub>CM</sub> = 2.1 V	-2%		2%	
		V <sub>CM</sub> = 2.1 V, -40°C ≤ T <sub>J</sub> ≤ 125°C	-3.4%		3.4%	
G <sub>m</sub> drift <sup>(5)</sup>	-40°C to 125°C, V <sub>CM</sub> = 2.1 V				140	ppm /°C
PSRR	Power Supply Rejection Ratio	V <sub>CM</sub> = 2.1 V, 2.7 V < V <sup>+</sup> < 12 V,	85			dB
CMRR	Common-Mode Rejection Ratio	2.1 V < V <sub>CM</sub> < 76 V	95			dB
		-2 V < V <sub>CM</sub> < 2.1 V	55			
SR	Slew Rate <sup>(7)(5)</sup>	V <sub>CM</sub> = 5 V, C <sub>G</sub> = 4 pF, V <sub>SENSE</sub> from 100 mV to 500 mV, C <sub>L</sub> = 30 pF, R <sub>L</sub> = 1MΩ		0.5		V/μs
I <sub>S</sub>	Supply Current	V <sub>CM</sub> = 2.1 V		450	660	μA
		V <sub>CM</sub> = 2.1 V, -40°C ≤ T <sub>J</sub> ≤ 125°C			939	
		V <sub>CM</sub> = -2 V		2100	2800	
		V <sub>CM</sub> = -2 V, -40°C ≤ T <sub>J</sub> ≤ 125°C			3030	
V <sub>OUT</sub>	Maximum Output Voltage	V <sub>CM</sub> = 5 V, R <sub>G</sub> = 500 kΩ	3.3			V
	Minimum Output Voltage	V <sub>CM</sub> = 2.1 V			22	mV
I <sub>OUT</sub>	Output current <sup>(5)</sup>	Sourcing, V <sub>OUT</sub> = 1.65 V, R <sub>G</sub> = 150 kΩ		5		mA
C <sub>LOAD</sub>	Max Output Capacitance Load <sup>(5)</sup>			30		pF

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T<sub>J</sub> = T<sub>A</sub>. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T<sub>J</sub> > T<sub>A</sub>.
- (2) All limits are specified by testing, design, or statistical analysis.
- (3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
- (4) Offset voltage temperature drift is determined by dividing the change in V<sub>OS</sub> at the temperature extremes by the total temperature change.
- (5) This parameter is specified by design and/or characterization and is not tested in production.
- (6) Positive Bias Current corresponds to current flowing into the device.
- (7) The number specified is the average of rising and falling slew rates and measured at 90% to 10%.

## 6.7 Electrical Characteristics: 12 V

Unless otherwise specified, all limits ensured for at  $T_A = 25^\circ\text{C}$ ,  $V_S = V^+ - V^-$ ,  $V^+ = 12\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $-2\text{ V} < V_{\text{CM}} < 76\text{ V}$ ,  $R_g = 25\text{ k}\Omega$ ,  $R_L = 10\text{ k}\Omega$ .<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
V <sub>OFFSET</sub>	Input Offset Voltage	V <sub>CM</sub> = 2.1 V	-1		1	mV
		V <sub>CM</sub> = 2.1 V, -40°C ≤ T <sub>J</sub> ≤ 125°C	-1.7		1.7	
TCV <sub>OS</sub>	Input Offset Voltage Drift <sup>(4)(5)</sup>	V <sub>CM</sub> = 2.1 V			7	μV/°C
I <sub>B</sub>	Input Bias Current <sup>(6)</sup>	V <sub>CM</sub> = 2.1 V		13	23	μA
e <sub>ni</sub>	Input Voltage Noise <sup>(5)</sup>	f > 10 kHz, R <sub>G</sub> = 5 kΩ		120		nV/√Hz
V <sub>SENSE(MAX)</sub>	Max Input Sense Voltage <sup>(5)</sup>	V <sub>CM</sub> = 12 V, R <sub>G</sub> = 5 kΩ		600		mV
Gain A <sub>V</sub>	Adjustable Gain Setting <sup>(5)</sup>	V <sub>CM</sub> = 12 V	1		100	V/V
G <sub>m</sub>	Transconductance = 1/R <sub>IN</sub>	V <sub>CM</sub> = 2.1 V		200		μA/V
	Accuracy	V <sub>CM</sub> = 2.1 V	-2%		2%	
		V <sub>CM</sub> = 2.1 V, -40°C ≤ T <sub>J</sub> ≤ 125°C	-3.4%		3.4%	
G <sub>m</sub> drift <sup>(5)</sup>	-40°C to 125°C, V <sub>CM</sub> = 2.1 V			140	ppm /°C	
PSRR	Power Supply Rejection Ratio	V <sub>CM</sub> = 2.1 V, 2.7 V < V <sup>+</sup> < 12 V	85			dB
CMRR	Common-Mode Rejection Ratio	2.1 V < V <sub>CM</sub> < 76 V	95			dB
		-2 V < V <sub>CM</sub> < 2.1 V	55			
SR	Slew Rate <sup>(7)(5)</sup>	V <sub>CM</sub> = 5 V, C <sub>G</sub> = 4 pF, V <sub>SENSE</sub> from 100 mV to 500 mV, C <sub>L</sub> = 30 pF, R <sub>L</sub> = 1 MΩ		0.6		V/μs
I <sub>S</sub>	Supply Current	V <sub>CM</sub> = 2.1 V		555	845	μA
		V <sub>CM</sub> = 2.1 V, -40°C ≤ T <sub>J</sub> ≤ 125°C			1123	
		V <sub>CM</sub> = -2 V		2200	2900	
		V <sub>CM</sub> = -2 V, -40°C ≤ T <sub>J</sub> ≤ 125°C			3110	
V <sub>OUT</sub>	Maximum Output Voltage	V <sub>CM</sub> = 12 V, R <sub>G</sub> = 500 kΩ,	10			V
	Minimum Output Voltage	V <sub>CM</sub> = 2.1 V			24	mV
I <sub>OUT</sub>	Output current <sup>(5)</sup>	Sourcing, V <sub>OUT</sub> = 5.25 V, R <sub>G</sub> = 150 kΩ		5		mA
C <sub>LOAD</sub>	Max Output Capacitance Load <sup>(5)</sup>			30		pF

- Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T<sub>J</sub> = T<sub>A</sub>. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T<sub>J</sub> > T<sub>A</sub>.
- All limits are specified by testing, design, or statistical analysis.
- Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
- Offset voltage temperature drift is determined by dividing the change in V<sub>OS</sub> at the temperature extremes by the total temperature change.
- This parameter is specified by design and/or characterization and is not tested in production.
- Positive Bias Current corresponds to current flowing into the device.
- The number specified is the average of rising and falling slew rates and measured at 90% to 10%.

## 6.8 Typical Characteristics

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $V_S = V^+ - V^-$ ,  $V_{\text{SENSE}} = +\text{IN} - (-\text{IN})$ ,  $R_L = 10\text{ k}\Omega$ .

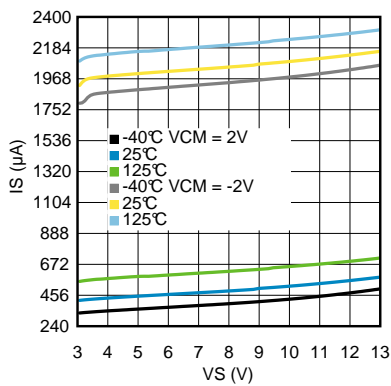


Figure 1. Supply Current vs. Supply Voltage for  $V_{\text{CM}} = 2\text{ V}$

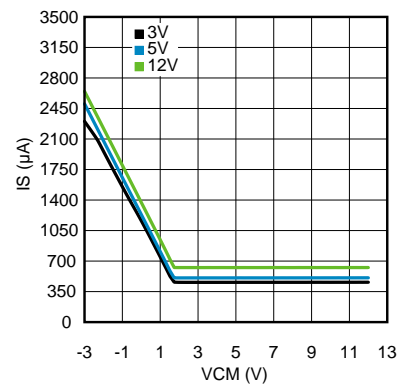


Figure 2. Supply Current vs.  $V_{\text{CM}}$

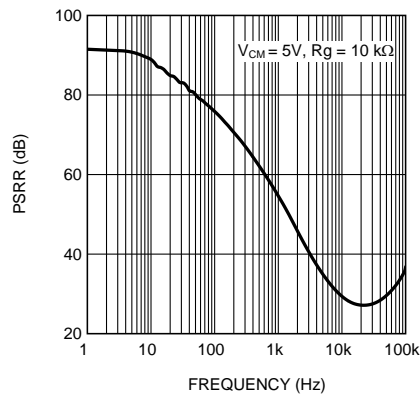


Figure 3. AC PSRR vs. Frequency

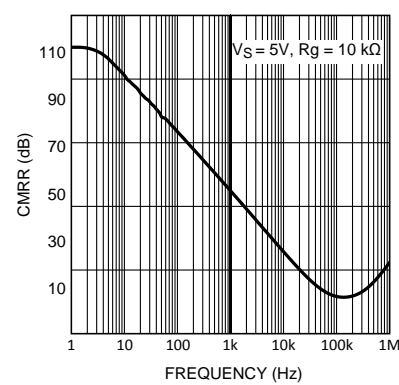


Figure 4. AC CMRR vs. Frequency

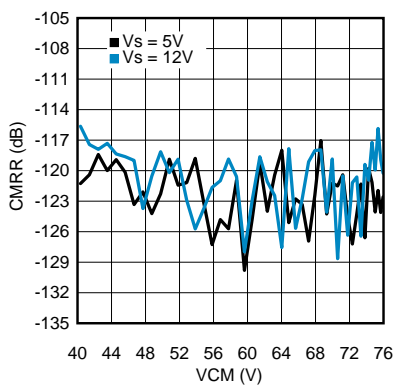


Figure 5. CMRR vs. High  $V_{\text{CM}}$

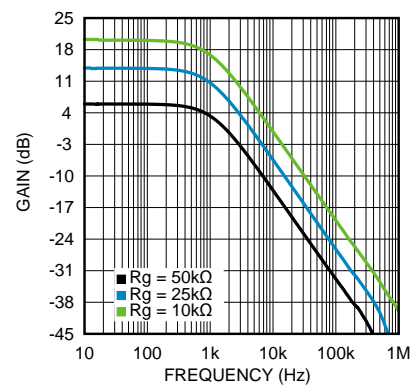


Figure 6. Gain vs. Frequency (BW = 1kHz)



Typical Characteristics (continued)

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $V_S = V^+ - V^-$ ,  $V_{\text{SENSE}} = +\text{IN} - (-\text{IN})$ ,  $R_L = 10\text{ k}\Omega$ .

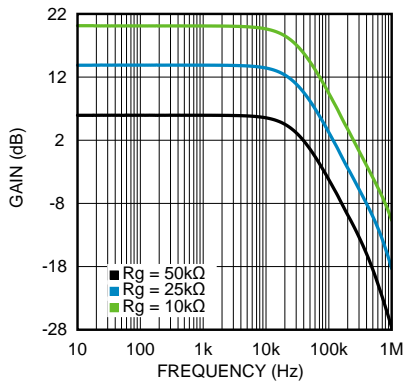


Figure 7. Gain vs. Frequency (BW = 35 kHz)

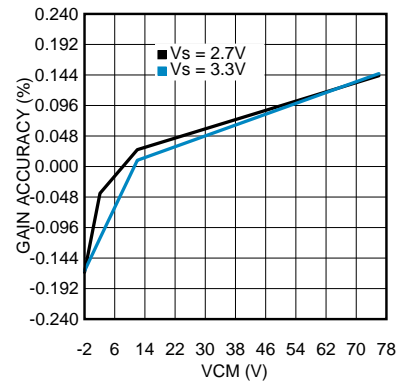


Figure 8. Gain Accuracy vs.  $V_{\text{CM}}$

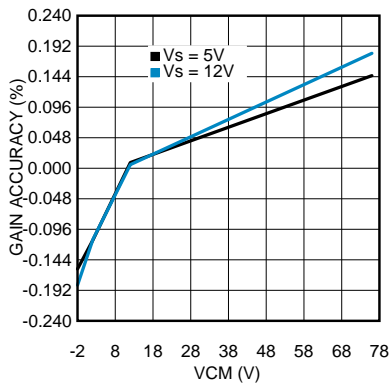


Figure 9. Gain Accuracy vs.  $V_{\text{CM}}$

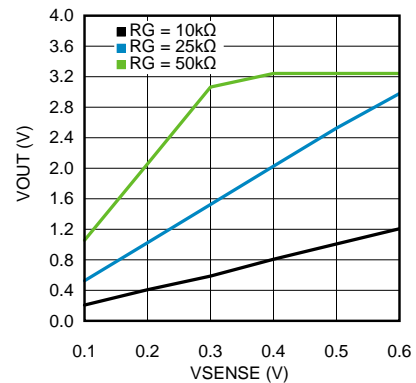


Figure 10.  $V_{\text{OUT}}$  vs.  $V_{\text{SENSE}}$

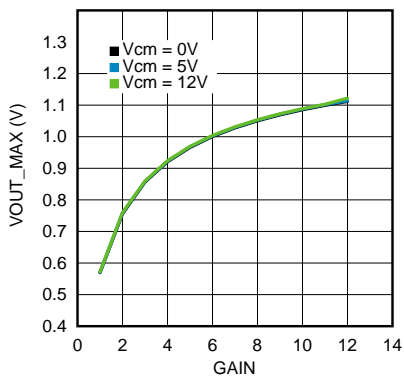


Figure 11.  $V_{\text{OUT\_MAX}}$  vs. Gain at  $V_S = 2.7\text{ V}$

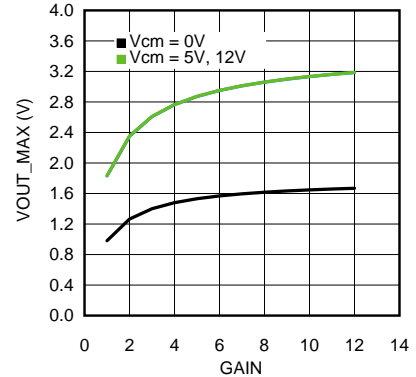


Figure 12.  $V_{\text{OUT\_MAX}}$  vs. Gain at  $V_S = 5.0\text{ V}$

### Typical Characteristics (continued)

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $V_S = V^+ - V^-$ ,  $V_{\text{SENSE}} = +\text{IN} - (-\text{IN})$ ,  $R_L = 10\text{ k}\Omega$ .

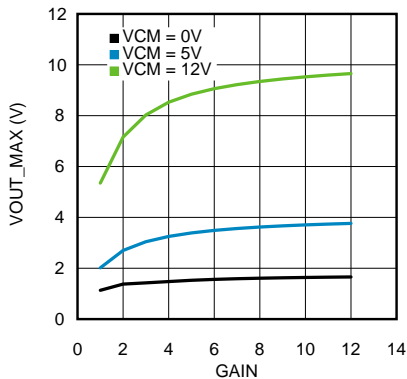


Figure 13.  $V_{\text{OUT\_MAX}}$  vs. Gain at  $V_S = 12\text{ V}$

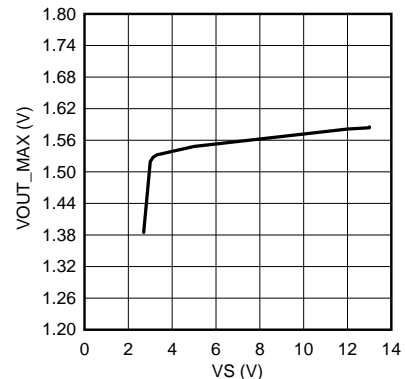


Figure 14.  $V_{\text{OUT\_MAX}}$  vs.  $V_S$  at  $V_{\text{CM}} = -2\text{ V}$

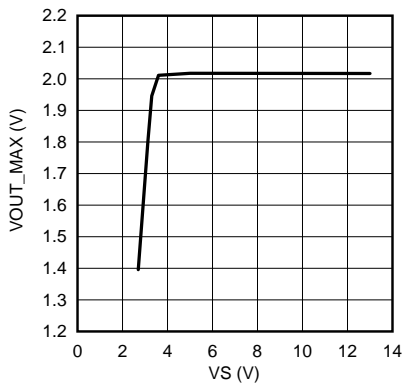


Figure 15.  $V_{\text{OUT\_MAX}}$  vs.  $V_S$  at  $V_{\text{CM}} = 2.1\text{ V}$

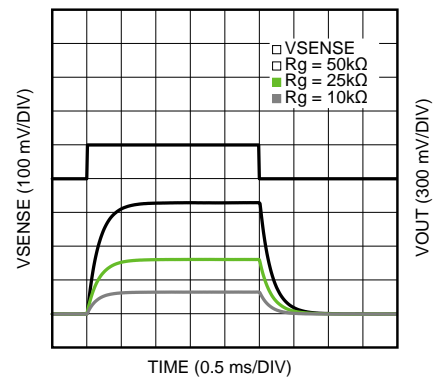


Figure 16. Large Step Response at  $\text{BW} = 1\text{ kHz}$

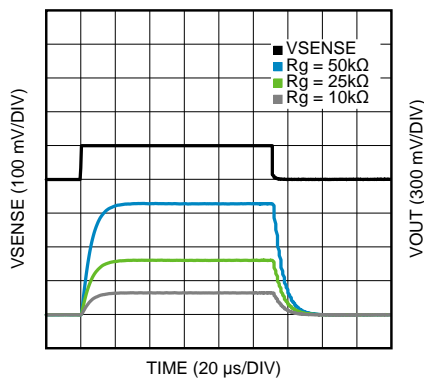


Figure 17. Large Step Response at  $\text{BW} = 35\text{ kHz}$

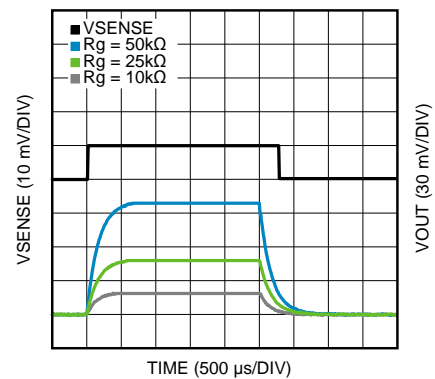


Figure 18. Small Step Response at  $\text{BW} = 1\text{ kHz}$

### Typical Characteristics (continued)

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $V_S = V^+ - V^-$ ,  $V_{\text{SENSE}} = +\text{IN} - (-\text{IN})$ ,  $R_L = 10\text{ k}\Omega$ .

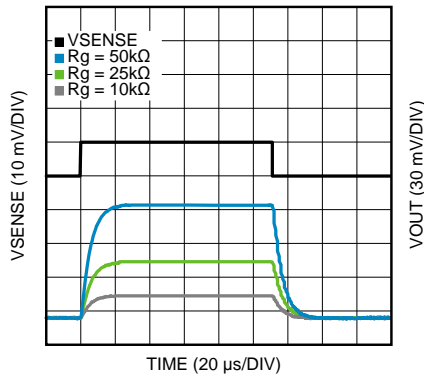


Figure 19. Small Step Response at BW = 35 kHz

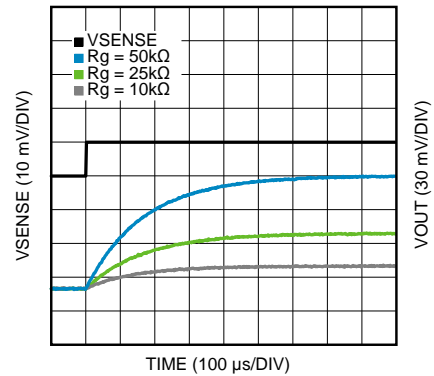


Figure 20. Settling Time (Rise) at 1 kHz

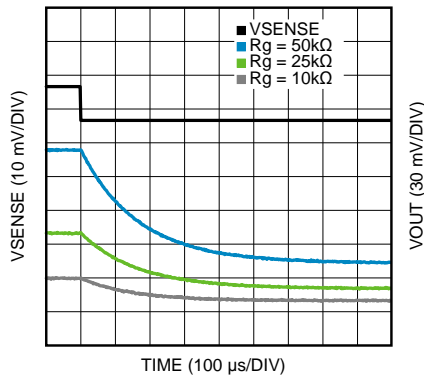


Figure 21. Settling Time (Fall) at 1 kHz

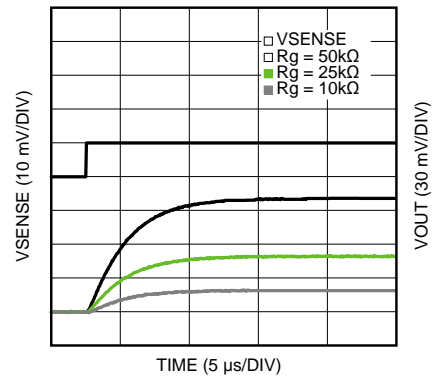


Figure 22. Settling Time (Rise) at 35 kHz

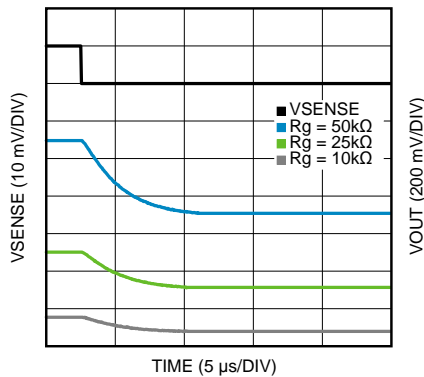


Figure 23. Settling Time (Fall) at 35 kHz

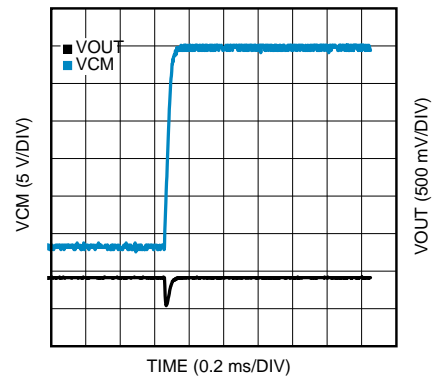
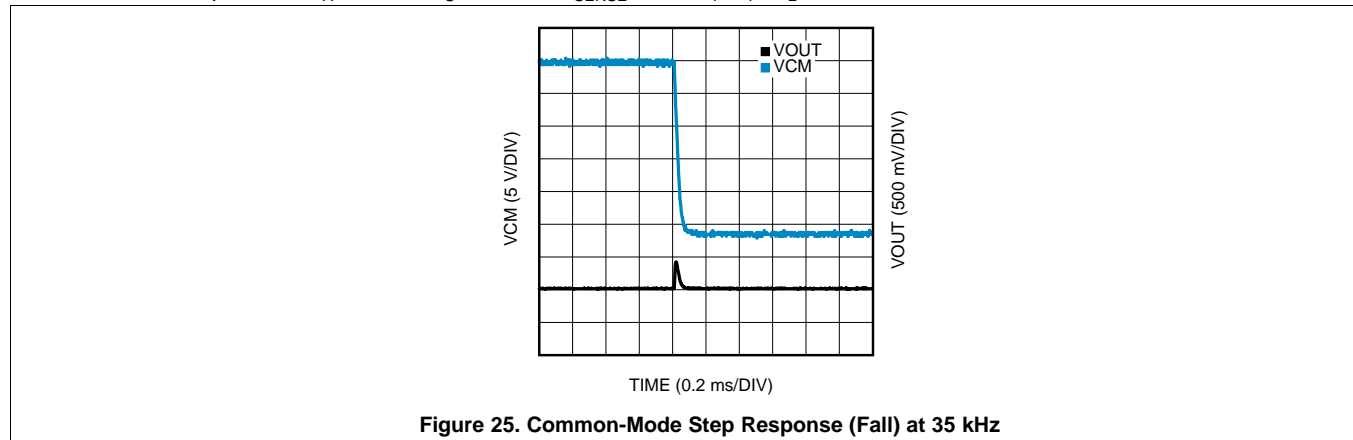


Figure 24. Common-Mode Step Response (Rise) at 35 kHz

**Typical Characteristics (continued)**

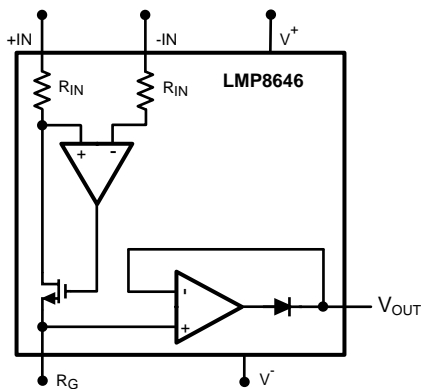
 Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $V_S = V^+ - V^-$ ,  $V_{\text{SENSE}} = +\text{IN} - (-\text{IN})$ ,  $R_L = 10\text{ k}\Omega$ .


## 7 Detailed Description

### 7.1 Overview

The LMP8646 is a single-supply precision current limiter with variable gain selected through an external resistor ( $R_G$ ) and a variable bandwidth selected through an external capacitor ( $C_G$ ) in parallel with  $R_G$ . Its common-mode of operation is  $-2\text{ V}$  to  $76\text{ V}$ , and the LMP8646 has a buffered output to provide a low-output impedance. More details of the LMP8646's functional description can be seen in the following subsections.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Theory of Operation

As seen from [Figure 26](#), the sense current flowing through  $R_{SENSE}$  develops a voltage drop equal to  $V_{SENSE}$ . The high impedance inputs of the amplifier does not conduct this current and the high open-loop gain of the sense amplifier forces its noninverting input to the same voltage as the inverting input. In this way the voltage drop across  $R_{IN}$  matches  $V_{SENSE}$ . The current  $I_{IN}$  flowing through  $R_{IN}$  has the following equation:

$$I_{IN} = V_{SENSE} / R_{IN} = R_{SENSE} * I_{SENSE} / R_{IN}$$

where

- $R_{IN} = 1/G_m = 1/(200\ \mu\text{A/V}) = 5\ \text{k}\Omega$  (1)

$I_{IN}$  flows entirely across the external gain resistor  $R_G$  to develop a voltage drop equal to:

$$V_{RG} = I_{IN} * R_G = (V_{SENSE} / R_{IN}) * R_G = [(R_{SENSE} * I_{SENSE}) / R_{IN}] * R_G$$
 (2)

This voltage is buffered and showed at the output with a very low impedance allowing a very easy interface of the LMP8646 with the feedback of many voltage regulators. This output voltage has the following equation:

$$V_{OUT} = V_{RG} = [(R_{SENSE} * I_{SENSE}) / R_{IN}] * R_G$$
 (3)

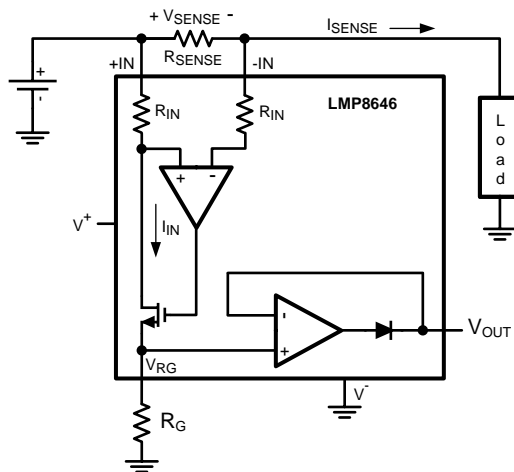
$$V_{OUT} = V_{SENSE} * R_G / R_{IN}$$
 (4)

$$V_{OUT} = V_{SENSE} * R_G / (5\ \text{k}\Omega)$$
 (5)

$$V_{OUT} = V_{SENSE} * \text{Gain}$$

where

- $\text{Gain} = R_G / R_{IN}$  (6)

**Feature Description (continued)**

**Figure 26. Current Monitor**
**7.3.1.1 Maximum Output Voltage,  $V_{OUT\_MAX}$** 

The maximum output voltage,  $V_{OUT\_MAX}$ , depends on the supply voltage,  $V_S = V^+ - V^-$ , and on the common-mode voltage,  $V_{CM} = (+IN + -IN) / 2$ .

The following subsections show three cases to calculate for  $V_{OUT\_MAX}$ .

**7.3.1.1.1 Case 1:  $-2\text{ V} < V_{CM} < 1.8\text{ V}$ , and  $V_S > 2.7\text{ V}$** 

If  $V_S \geq 5\text{ V}$ ,

then  $V_{OUT\_MAX} = 1.3\text{ V}$ .

Else if  $V_S = 2.7\text{ V}$ ,

then  $V_{OUT\_MAX} = 1.1\text{ V}$ .

**7.3.1.1.2 Case 2:  $1.8\text{ V} < V_{CM} < V_S$ , and  $V_S > 3.3\text{ V}$** 

In this case,  $V_X$  is a fixed value that depends on the supply voltage.  $V_X$  has the following values:

If  $V_S = 12\text{ V}$ , then  $V_X = 10\text{ V}$ .

Else if  $V_S = 5\text{ V}$ , then  $V_X = 3.3\text{ V}$ .

Else if  $V_S = 2.7\text{ V}$ , then  $V_X = 1.1\text{ V}$ .

If  $V_X \leq (V_{CM} - V_{SENSE} - 0.25)$ ,

then  $V_{OUT\_MAX} = V_X$ .

Else,

$V_{OUT\_MAX} = (V_{CM} - V_{SENSE} - 0.25)$ .

For example, if  $V_{CM} = 4\text{ V}$ ,  $V_S = 5\text{ V}$  (and thus  $V_X = 3.3\text{ V}$ ),  $V_{SENSE} = 0.1\text{ V}$ , then  $V_{OUT\_MAX} = 3.3\text{ V}$  because  $3.3\text{ V} \leq (4 - 0.1 - 0.25)$ .

**7.3.1.1.3 Case 3:  $V_{CM} > V_S$ , and  $V_S > 2.7\text{ V}$** 

If  $V_S = 12\text{ V}$ , then  $V_{OUT\_MAX} = 10\text{ V}$ .

Else if  $V_S = 5\text{ V}$ , then  $V_{OUT\_MAX} = 3.3\text{ V}$ .

Else if  $V_S = 2.7\text{ V}$ , then  $V_{OUT\_MAX} = 1.1\text{ V}$ .

## 7.4 Device Functional Modes

### 7.4.1 Output Accuracy

The output accuracy is the device error contributed by the LMP8646 based on its offset and gain errors. The LMP8646 output accuracy has the following equations:

$$\text{Output Accuracy} = \left| \frac{V_{\text{OUT\_THEO}} - V_{\text{OUT\_CAL}}}{V_{\text{OUT\_THEO}}} \right| \times 100(\%)$$

$$\text{where } V_{\text{OUT\_THEO}} = (V_{\text{SENSE}}) \times \frac{R_G}{1/G_m}$$

$$\text{and } V_{\text{OUT\_CALC}} = \frac{(V_{\text{SENSE}} + V_{\text{OFFSET}}) \times R_G}{1/[G_m (1 + G_m\text{-Accuracy})]}$$

Output Accuracy Equations (7)

For example, assume  $V_{\text{SENSE}} = 100 \text{ mV}$ ,  $R_G = 10 \text{ k}\Omega$ , and it is known that  $V_{\text{OFFSET}} = 1 \text{ mV}$  and  $G_m\text{-Accuracy} = 2\%$  (Electrical Characteristics Table), then the output accuracy can be calculated as:

$$V_{\text{OUT\_THEO}} = (100 \text{ mV}) \times \frac{10 \text{ k}\Omega}{1/(200\mu)} = 0.2\text{V}$$

$$V_{\text{OUT\_CALC}} = \frac{(100 \text{ mV} + 1 \text{ mV}) \times 10 \text{ k}\Omega}{1/[200\mu (1 + 2/100)]} = 0.20604\text{V}$$

$$\text{Output Accuracy} = \left| \frac{0.2\text{V} - 0.20604\text{V}}{0.2\text{V}} \right| \times 100 = 3.02\%$$

Output Accuracy Example (8)

In fact, as  $V_{\text{SENSE}}$  decreases, the output accuracy worsens as seen in [Figure 27](#). These equations provide a valuable tool to estimate how the LMP8646 affects the overall system performance. Knowing this information allows the system designer to pick the appropriate external resistances ( $R_{\text{SENSE}}$  and  $R_G$ ) to adjust for the tolerable system error. Examples of this tolerable system error can be seen in the next sections.

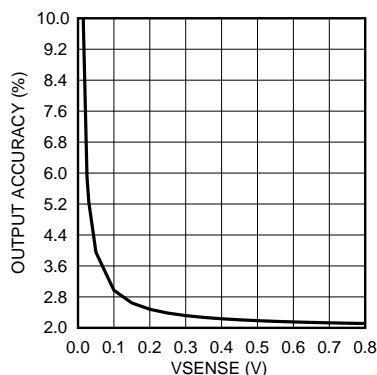


Figure 27. Output Accuracy vs.  $V_{\text{SENSE}}$

### 7.4.2 Selection of the Sense Resistor, $R_{\text{SENSE}}$

The accuracy of the current measurement also depends on the value of the shunt resistor  $R_{\text{SENSE}}$ . Its value depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the load line.

$R_{\text{SENSE}}$  is directly proportional to  $V_{\text{SENSE}}$  through the equation  $R_{\text{SENSE}} = (V_{\text{SENSE}}) / (I_{\text{SENSE}})$ . If  $V_{\text{SENSE}}$  is small, then there is a smaller voltage loss in the load line, but the output accuracy is worse because the LMP8646 offset error will contribute more. Therefore, high values of  $R_{\text{SENSE}}$  provide better output accuracy by minimizing the effects of offset, while low values of  $R_{\text{SENSE}}$  minimize the voltage loss in the load line. For most applications, best performance is obtained with an  $R_{\text{SENSE}}$  value that provides a  $V_{\text{SENSE}}$  of 100 mV to 200 mV.

## Device Functional Modes (continued)

### 7.4.2.1 $R_{SENSE}$ Consideration for System Error

The output accuracy described in the previous section talks about the error contributed just by the LMP8646. The system error, however, consists of the errors contributed by the LMP8646 as well as other external resistors such as  $R_{SENSE}$  and  $R_G$ . Let's rewrite the output accuracy equation for the system error assuming that  $R_{SENSE}$  is non-ideal and  $R_G$  is ideal. This equation can be seen as:

$$\text{System Error} = \left| \frac{V_{OUT\_THEO} - V_{OUT\_CAL}}{V_{OUT\_THEO}} \right| \times 100(\%)$$

$$\text{where } V_{OUT\_THEO} = (R_{SENSE} \times I_{SENSE}) \times \frac{R_G}{1/G_m}$$

$$\text{and } V_{OUT\_CALC} = \frac{[R_{SENSE} (1 + \text{Tolerance}) \times I_{SENSE} + V_{OFFSET}] \times R_G}{1/[G_m (1 + G_m\_Accuracy)]}$$

$$\text{System Error Example Assuming } R_{SENSE} \text{ is Non-ideal and } R_G \text{ is Ideal} \tag{9}$$

Continuing from the previous output accuracy example, we can calculate for the system error assuming that  $R_{SENSE} = 100 \text{ m}\Omega$  (with 1% tolerance),  $I_{SENSE} = 1\text{A}$ , and  $R_G = 10 \text{ k}\Omega$ . From the Electrical Characteristics Table, it is also known that  $V_{OFFSET} = 1 \text{ mV}$  and  $G_m\_Accuracy = 2\%$ .

$$V_{OUT\_THEO} = (100 \text{ m}\Omega \times 1\text{A}) \times \frac{10 \text{ k}\Omega}{1/(200\mu)} = 0.2\text{V}$$

$$V_{OUT\_CALC} = \frac{[100 \text{ m}\Omega (1 + 1/100) \times 1\text{A} + 1\text{mV}] \times 10 \text{ k}\Omega}{1/[200\mu (1 + 2/100)]} = 0.20808\text{V}$$

$$\text{System Error} = \left| \frac{0.2\text{V} - 0.20808\text{V}}{0.2\text{V}} \right| \times 100 = 4.04\%$$

$$\text{System Error Example Assuming } R_{SENSE} \text{ is Non-ideal and } R_G \text{ is Ideal} \tag{10}$$

Because an  $R_{SENSE}$  tolerance will increase the system error, we recommend selecting an  $R_{SENSE}$  resistor with low tolerance.



## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The LMP8646 can be driven by many different regulators with a feedback pin and connected to many different types of loads such as capacitive and resistive. The following sections gives three typical applications of the LMP8646.

### 8.2 Typical Applications

#### 8.2.1 Application #1: Current Limiter With a Capacitive Load

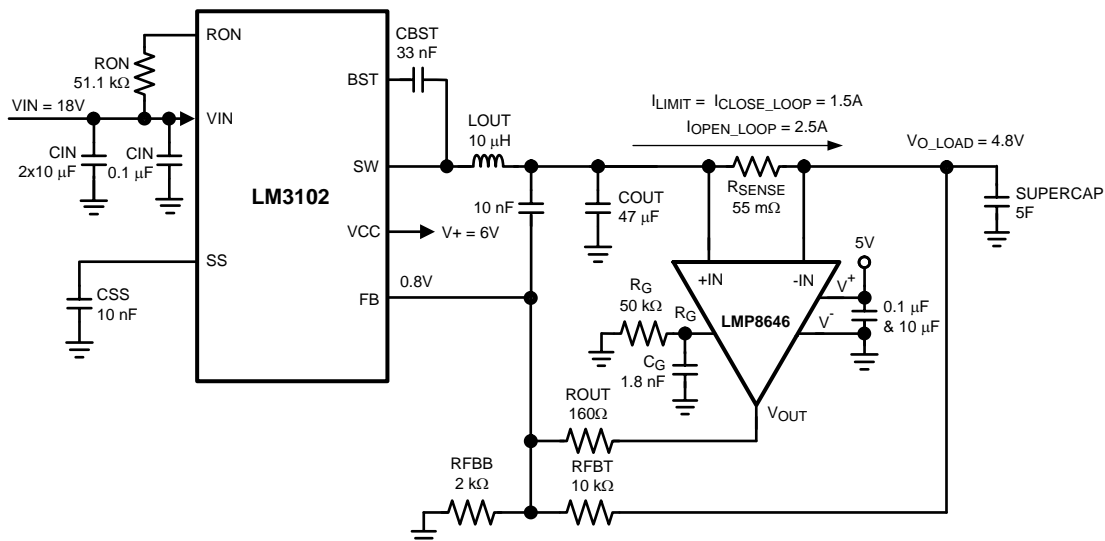


Figure 28. SuperCap Application With LM3102 Regulator

##### 8.2.1.1 Design Requirements

A supercap application requires a very high capacitive load to be charged. This example assumes the output capacitor is 5F with a limited sense current at 1.5A. The LM3102 will provide the current to charge the supercap, and the LMP8646 will monitor this current to make sure it does not exceed the desired 1.5A value.

##### 8.2.1.2 Detailed Design Procedure

To limit the capacitor current, first connect the LMP8646 output to the feedback pin of the LM3102, as shown in Figure 28. This feedback voltage at the FB pin is compared to a 0.8V internal reference. Any voltage above this 0.8V means the output current is above the desired value of 1.5A, and the LM3102 will reduce its output current to maintain the desired 0.8V at the FB pin.

The following steps show the design procedures for this supercap application. In summary, the steps consist of selecting the components for the voltage regulator, integrating the LMP8646 and selecting the proper values for its gain, bandwidth, and output resistor, and adjusting these components to yield the desired performance.

#### Step 1: Choose the components for the Regulator.

Refer to the LM3102 evaluation board application note (AN-1646) to select the appropriate components for the LM3102 voltage regulator.

## Typical Applications (continued)

### Step 2: Choose the sense resistor, $R_{SENSE}$

$R_{SENSE}$  sets the voltage  $V_{SENSE}$  between +IN and -IN and has the following equation:

$$R_{SENSE} = V_{OUT} / [(I_{LIMIT}) * (R_G / 5k\Omega)] \quad (11)$$

In general,  $R_{SENSE}$  depends on the output voltage, limit current, and gain. Refer to section [Selection of the Sense Resistor,  \$R\_{SENSE}\$](#)  to choose the appropriate  $R_{SENSE}$  value; this example uses 55 m $\Omega$ .

### Step 3: Choose the gain resistor, $R_G$ , for LMP8646

$R_G$  is chosen from the limited sense current. As stated,  $V_{OUT} = (R_{SENSE} * I_{LIMIT}) * (R_G / 5k\Omega)$ . Since  $V_{OUT} = V_{FB} = 0.8V$ , the limited sense current is 1.5A, and  $R_{SENSE}$  is 55 m $\Omega$ ,  $R_G$  can be calculated as:

$$R_G = (V_{OUT} * 5 k\Omega) / (R_{SENSE} * I_{LIMIT}) \quad (12)$$

$$R_G = (0.8 * 5 k\Omega) / (55 m\Omega * 1.5A) = 50 k\Omega \text{ (approximate)} \quad (13)$$

### Step 4: Choose the Bandwidth Capacitance, $C_G$ .

The product of  $C_G$  and  $R_G$  determines the bandwidth for the LMP8646. Refer to the Typical Performance Characteristics plots to see the range for the LMP8646 bandwidth and gain. Since each application is very unique, the LMP8646 bandwidth capacitance,  $C_G$ , needs to be adjusted to fit the appropriate application.

Bench data has been collected for the supercap application with the LM3102 regulator, and we found that this application works best for a bandwidth of 500 Hz to 3 kHz. Operating outside of this recommended bandwidth range might create an undesirable load current ringing. We recommend choosing a bandwidth that is in the middle of this range and using the equation  $C_G = 1/(2*\pi*R_G*Bandwidth)$  to find  $C_G$ . For example, if the bandwidth is 1.75 kHz and  $R_G$  is 50 k $\Omega$ , then  $C_G$  is approximately 1.8 nF. After this selection, capture the plot for  $I_{LIMIT}$  and adjust  $C_G$  until a desired load current plot is obtained.

### Step 5: Calculate the Output Accuracy and Tolerable System Error

Since the LMP8646 is a precision current limiter, the output current accuracy is extremely important. This accuracy is affected by the system error contributed by the LMP8646 device error and other errors contributed by external resistances, such as  $R_{SENSE}$  and  $R_G$ .

In this application,  $V_{SENSE} = I_{LIMIT} * R_{SENSE} = 1.5A * 55 m\Omega = 0.0825V$ , and  $R_G = 50 k\Omega$ . From the Electrical Characteristics Table, it is known that  $V_{OFFSET} = 1 mV$  and  $Gm\_Accuracy = 2\%$ . Using the equations shown in [Equation 8](#), the output accuracy can be calculated as 3.24%.

After figuring out the LMP8646 output accuracy, choose a tolerable system error or the output current accuracy that is bigger than the LMP8646 output accuracy. This tolerable system error will be labeled as  $I_{ERROR}$ , and it has the equation  $I_{ERROR} = (I_{MAX} - I_{LIMIT})/I_{MAX}$  (%). In this example, we will choose an  $I_{ERROR}$  of 5%, which will be used to calculate for  $R_{OUT}$  shown in the next step.

### Step 6: Choose the output resistor, $R_{OUT}$

At start-up, the capacitor is not charged yet and thus the output voltage of the LM3102 is very small. Therefore, at start-up, the output current is at its maximum ( $I_{MAX}$ ). When the output voltage is at its nominal, then the output current will settle to the desired limited value. Because a large current error is not desired,  $R_{OUT}$  needs to be chosen to stabilize the loop with minimal initial start-up current error. Follow the equations and example below to choose the appropriate value for  $R_{OUT}$  to minimize this initial error.

As discussed in step 4, the allowable  $I_{ERROR}$  is 5%, where  $I_{ERROR} = (I_{MAX} - I_{LIMIT})/I_{MAX}$  (%). Therefore, the maximum allowable current is calculated as:  $I_{MAX} = I_{LIMIT} (1 + I_{ERROR}) = 1.5A * (1 + 5/100) = 1.575 A$ .

Next, use [Equation 14](#) below to calculate for  $R_{OUT}$ :

$$R_{OUT} = \frac{(I_{MAX} * R_{SENSE} * Gain - V_{FB})}{\frac{V_{FB}}{RFBB} - \frac{(V_{O\_REG\_MIN} - V_{FB})}{RFBT}} \quad (14)$$

For example, assume the minimum LM3102 output voltage,  $V_{O\_REG\_MIN}$ , is 0.6V, then  $R_{OUT}$  can be calculated as  $R_{OUT} = [1.575A * 55 m\Omega * (49.9k / 5k) - 0.8] / [(0.8 / 2k) - (0.6 - 0.8) / 10k] = 153.6 \Omega$ .

### Typical Applications (continued)

Populate ROUT with a resistor that is as close as possible to 153.6 Ohm (this application uses 160 Ohm). If the limited sense current has a gain error and is not 1.5A at any point in time, then adjust this ROUT value to obtain the desired limit current.

We recommend that the value for ROUT is at least 50 Ohm.

#### Step 7: Adjusting Components

Capture the output current and output voltage plots and adjust the components as necessary. The most common components to adjust are CG to decrease the current ripple and ROUT to get a low current error. An example output current and voltage plot can be seen in Figure 29.

#### 8.2.1.3 Application Curve

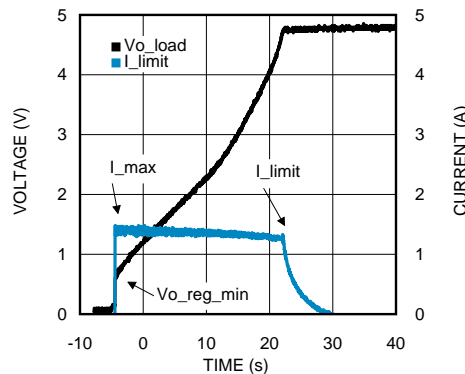


Figure 29. SuperCap Application With LM3102 Regulator Plot

#### 8.2.2 Application #2: Current Limiter With a Resistive Load

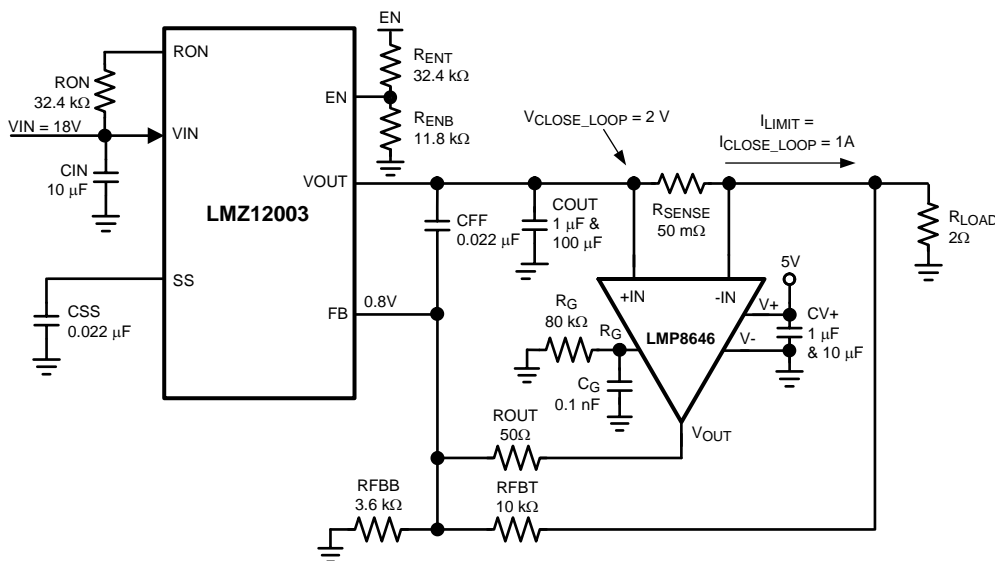


Figure 30. Resistive Load Application With LMZ12003 Regulator

## Typical Applications (continued)

### 8.2.2.1 Design Requirements

This subsection describes the design process for a resistive load application with the LMZ12003 voltage regulator as seen in [Figure 30](#). To see the current limiting capability of the LMP8646, the open-loop current must be greater than the close-loop current. An open-loop occurs when the LMP8646 output is not connected the LMZ12003's feedback pin. For this example, we will let the open-loop current to be 1.5A and the close-loop current,  $I_{LIMIT}$ , to be 1A.

### 8.2.2.2 Detailed Design Procedure

#### Step 1: Choose the components for the Regulator.

Refer to the LMZ12003 application note ([AN-2031](#)) to select the appropriate components for the LMZ12003.

#### Step 2: Choose the sense resistor, $R_{SENSE}$

$R_{SENSE}$  sets the voltage  $V_{SENSE}$  between +IN and -IN and has the following equation:

$$R_{SENSE} = V_{OUT} / [(I_{LIMIT}) * (R_G / 5k\Omega)] \quad (15)$$

In general,  $R_{SENSE}$  depends on the output voltage, limit current, and gain. Refer to section [Selection of the Sense Resistor,  \$R\_{SENSE}\$](#)  to choose the appropriate  $R_{SENSE}$  value; this example uses 50 mOhm.

#### Step 3: Choose the gain resistor, $R_G$ , for LMP8646

$R_G$  is chosen from  $I_{LIMIT}$ . As stated,  $V_{OUT} = (R_{SENSE} * I_{LIMIT}) * (R_G / 5k\Omega)$ . Since  $V_{OUT} = V_{FB} = 0.8V$ ,  $I_{LIMIT} = 1A$ , and  $R_{SENSE} = 50$  mOhm,  $R_G$  can be calculated as:

$$R_G = (V_{OUT} * 5 k\Omega) / (R_{SENSE} * I_{LIMIT}) \quad (16)$$

$$R_G = (0.8 * 5 k\Omega) / (50 m\Omega * 1A) = 80 k\Omega \quad (17)$$

#### Step 4: Choose the Bandwidth Capacitance, $C_G$ .

The product of  $C_G$  and  $R_G$  determines the bandwidth for the LMP8646. Refer to the Typical Performance Characteristics plots to see the range for the LMP8646 bandwidth and gain. Since each application is very unique, the LMP8646 bandwidth capacitance,  $C_G$ , needs to be adjusted to fit the appropriate application.

Bench data has been collected for this resistive load application with the LMZ12003 regulator, and we found that this application works best for a bandwidth of 2 kHz to 30 kHz. Operating anything less than this recommended bandwidth might prevent the LMP8646 from quickly limiting the current. We recommend choosing a bandwidth that is in the middle of this range and using the equation:  $C_G = 1/(2*\pi*R_G*Bandwidth)$  to find  $C_G$  (this example uses a  $C_G$  value of 0.1nF). After this selection, capture the load current plot and adjust  $C_G$  until a desired output current plot is obtained.

#### Step 5: Choose the output resistor, $R_{OUT}$ , for the LMP8646

$R_{OUT}$  plays a very small role in the overall system performance for the resistive load application.  $R_{OUT}$  was important in the supercap application because it affects the initial current error. Because current is directly proportional to voltage for a resistive load, the output current is not large at start-up. The bigger the  $R_{OUT}$ , the longer it takes for the output voltage to reach its final value. We recommend that the value for  $R_{OUT}$  is at least 50 Ohm, which is the chosen value for this example.

#### Step 6: Adjusting Components

Capture the output current and output voltage plots and adjust the components as necessary. The most common component to adjust is  $C_G$  for the bandwidth. An example of the output current and voltage plot can be seen in [Figure 31](#).

## Typical Applications (continued)

### 8.2.2.3 Application Curve

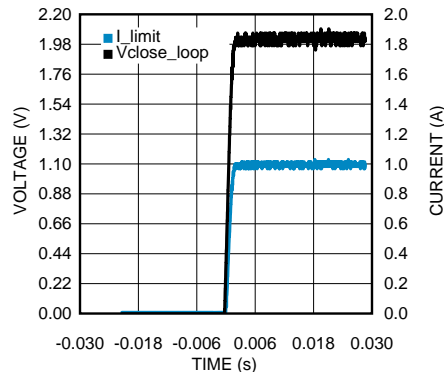


Figure 31. Plot for the Resistive Load Application With LMZ12003 Regulator Plot

### 8.2.3 Application #3: Current Limiter With a Low-Dropout Regulator and Resistive Load

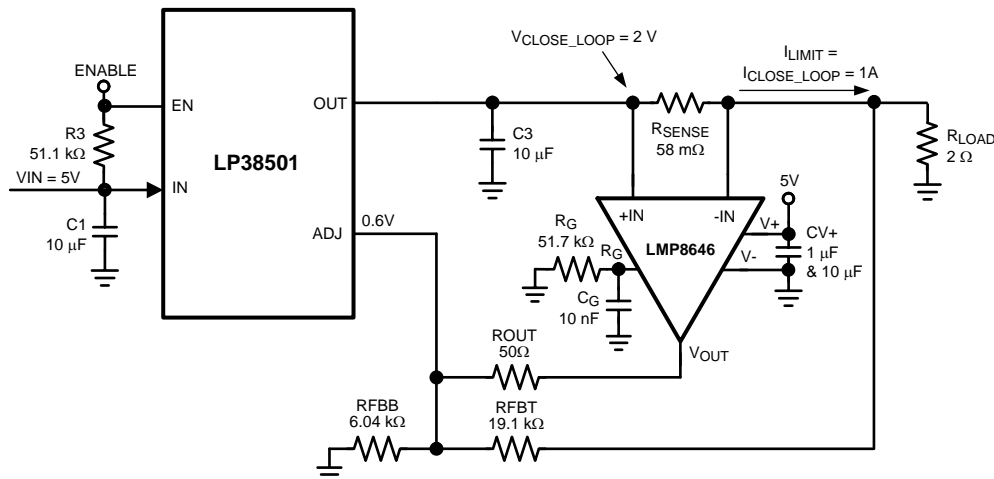


Figure 32. Resistive Load Application With LP38501 Regulator

#### 8.2.3.1 Design Requirements

This next example is the same as the last example, except that the regulator is now a low-dropout regulator, the LP38501, as seen in Figure 32. For this example, we will let the open-loop current to be 1.25A and the close-loop current,  $I_{LIMIT}$ , to be 1A.

#### 8.2.3.2 Detailed Design Procedure

##### Step 1: Choose the components for the Regulator.

Refer to the LP38501 application note (AN-1830) to select the appropriate components for the LP38501.

##### Step 2: Choose the sense resistor, $R_{SENSE}$

$R_{SENSE}$  sets the voltage  $V_{SENSE}$  between +IN and -IN and has the following equation:

$$R_{SENSE} = V_{OUT} / [(I_{LIMIT}) * (R_G / 5k\Omega)] \quad (18)$$

In general,  $R_{SENSE}$  depends on the output voltage, limit current, and gain. Refer to section [Selection of the Sense Resistor,  \$R\_{SENSE}\$](#)  to choose the appropriate  $R_{SENSE}$  value; this example uses 58 mOhm.

##### Step 3: Choose the gain resistor, $R_G$ , for LMP8646

**Typical Applications (continued)**

$R_G$  is chosen from  $I_{LIMIT}$ . As stated,  $V_{OUT} = (R_{SENSE} * I_{LIMIT}) * (R_G / 5kOhm)$ . Since  $V_{OUT} = ADJ = 0.6V$ ,  $I_{LIMIT} = 1A$ , and  $R_{SENSE} = 58\text{ mOhm}$ ,  $R_G$  can be calculated as:

$$R_G = (V_{OUT} * 5\text{ kOhm}) / (R_{SENSE} * I_{LIMIT}) \tag{19}$$

$$R_G = (0.6 * 5\text{ kOhm}) / (58\text{ mOhm} * 1A) = 51.7\text{ kOhm} \tag{20}$$

**Step 4: Choose the Bandwidth Capacitance,  $C_G$ .**

The product of  $C_G$  and  $R_G$  determines the bandwidth for the LMP8646. Refer to the Typical Performance Characteristics plots to see the range for the LMP8646 bandwidth and gain. Since each application is very unique, the LMP8646 bandwidth capacitance,  $C_G$ , needs to be adjusted to fit the appropriate application.

Bench data has been collected for this resistive load application with the LP38501 regulator, and we found that this application works best for a bandwidth of 50 Hz to 300 Hz. Operating anything larger than this recommended bandwidth might prevent the LMP8646 from quickly limiting the current. We recommend choosing a bandwidth that is in the middle of this range and using the equation:  $C_G = 1/(2*\pi*R_G*Bandwidth)$  to find  $C_G$  (this example uses a  $C_G$  value of 10 nF). After this selection, capture the plot for  $I_{SENSE}$  and adjust  $C_G$  until a desired sense current plot is obtained.

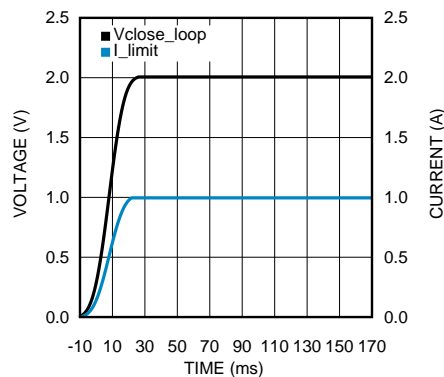
**Step 5: Choose the output resistor,  $R_{OUT}$ , for the LMP8646**

$R_{OUT}$  plays a very small role in the overall system performance for the resistive load application.  $R_{OUT}$  was important in the supercap application because it affects the initial current error. Because current is directly proportional to voltage for a resistive load, the output current is not large at start-up. The bigger the  $R_{OUT}$ , the longer it takes for the output voltage to reach its final value. We recommend that the value for  $R_{OUT}$  is at least 50 Ohm, which is the value we used for this example.

**Step 6: Adjusting Components**

Capture the output current and output voltage plots and adjust the components as necessary. The most common component to adjust is  $C_G$  for the bandwidth. An example plot of the output current and voltage can be seen in [Figure 33](#).

**8.2.3.3 Application Curve**



**Figure 33. Plot for the Resistive Load Application With the LP38501 LDO Regulator**



## 9 Power Supply Recommendations

Source V+ with an external voltage as recommended in the electrical characteristics table. It is recommended to place a 100nF ceramic bypass capacitor to ground as close to possible to the V+ pin. In addition, an electrolytic or tantalum capacitor of 10μF is recommended. The bulk capacitor does not need to be in close vicinity with the LMP8646 and could be close to the voltage source terminals or at the output of the voltage regulator powering the LMP8646.

## 10 Layout

### 10.1 Layout Guidelines

- In a 4-layer board design, the recommended layer stack order from top to bottom is: signal, power, ground, and signal
- Bypass capacitors should be placed in close proximity to the V+ pin
- The trace for pins +IN and -IN should be big enough to handle the current running through it.

### 10.2 Layout Example

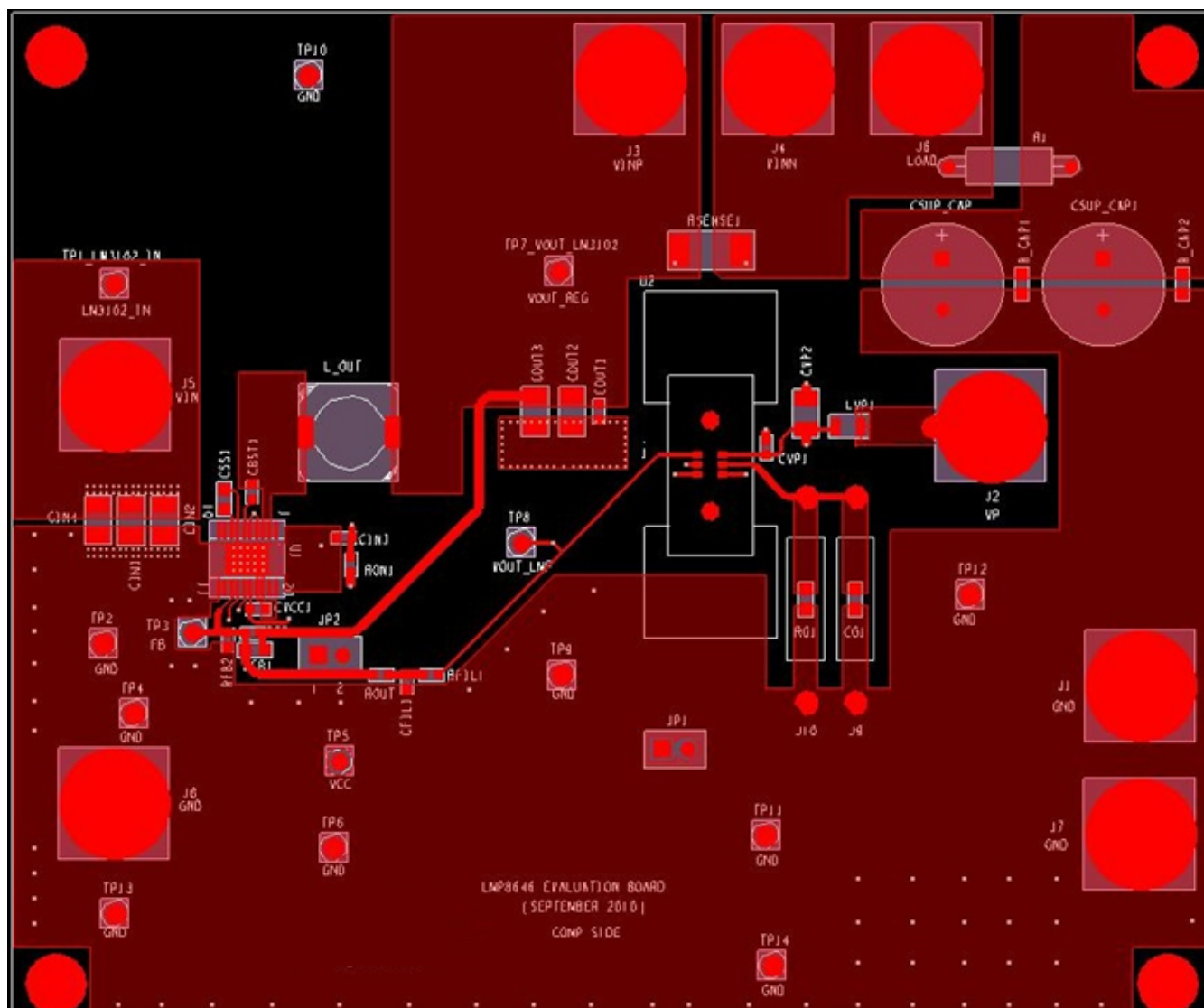


Figure 34. LMP8646 Evaluation Board Layout

## 11 Device and Documentation Support

### 11.1 Trademarks

All trademarks are the property of their respective owners.

### 11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP8646MK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AK7A	<a href="#">Samples</a>
LMP8646MKE/NOPB	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AK7A	<a href="#">Samples</a>
LMP8646MKX/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AK7A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

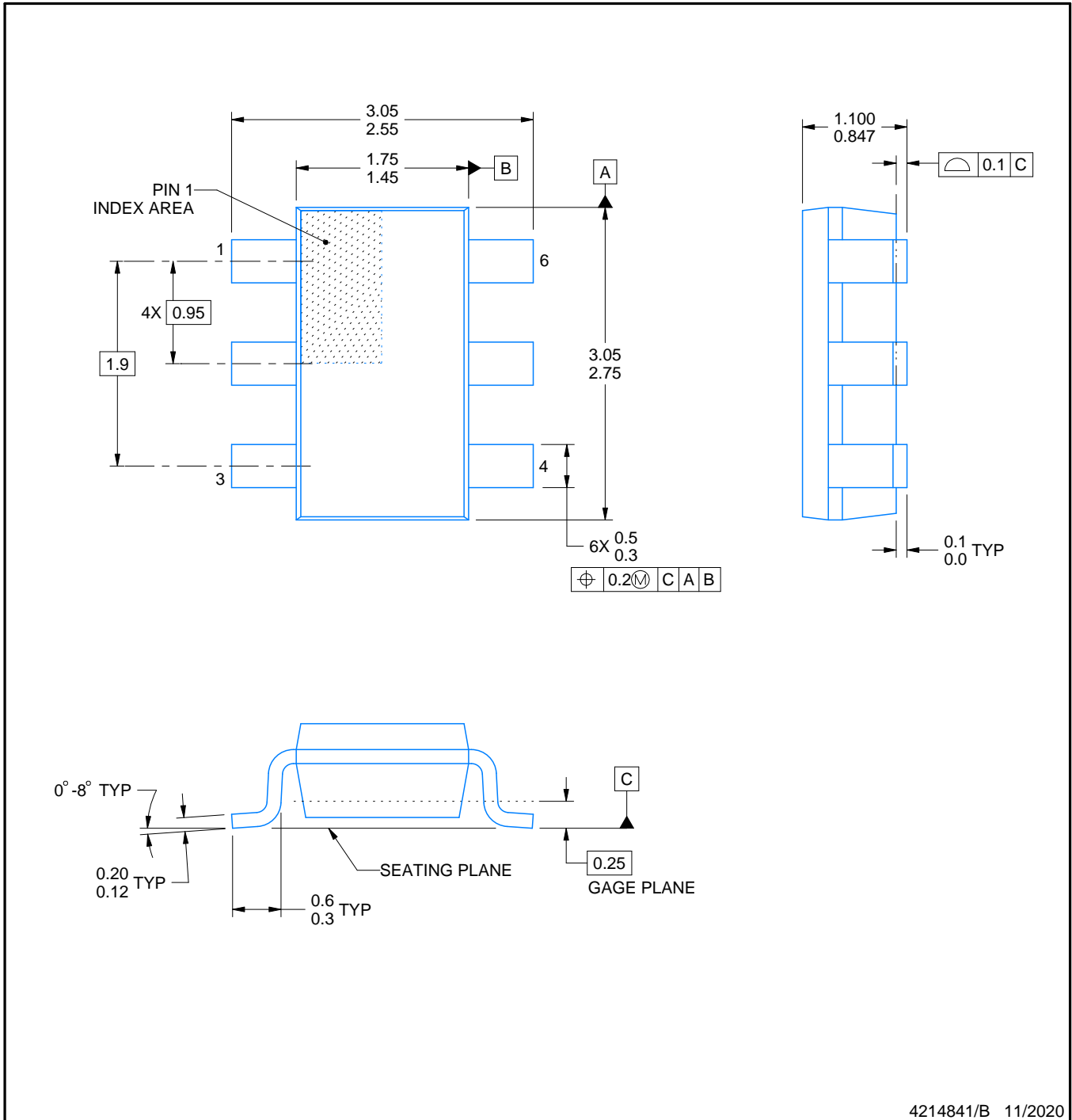

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8646MK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8646MKE/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8646MKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

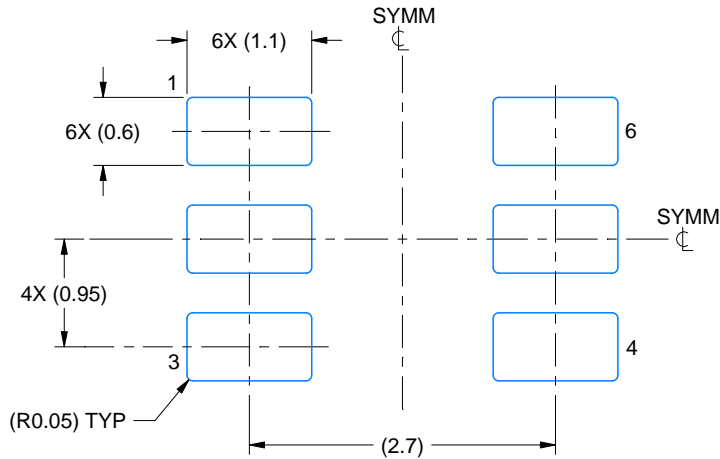
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8646MK/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LMP8646MKE/NOPB	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
LMP8646MKX/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0



4214841/B 11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE  
EXPLODED METAL SHOWN  
SCALE:15X

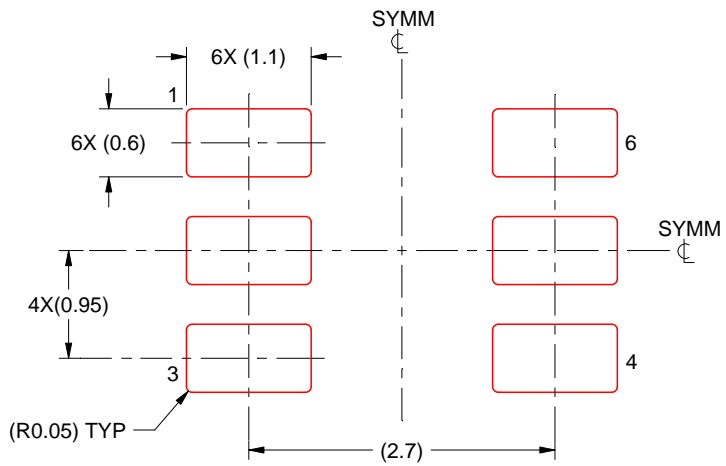


SOLDEMASK DETAILS

4214841/B 11/2020

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

4214841/B 11/2020

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 7. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated