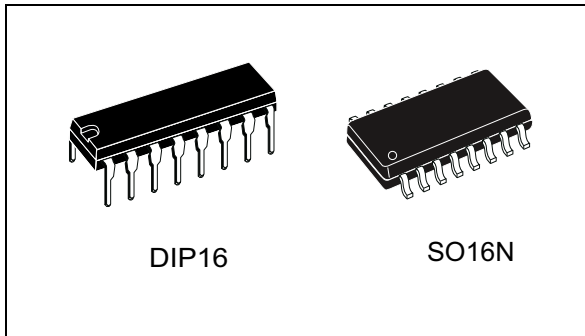


High voltage resonant controller

Datasheet - production data



- Sense op amp for closed loop control or protection features
- High accuracy current controlled oscillator
- Integrated bootstrap diode
- Clamping on V_s
- Available in DIP16 and SO16 packages

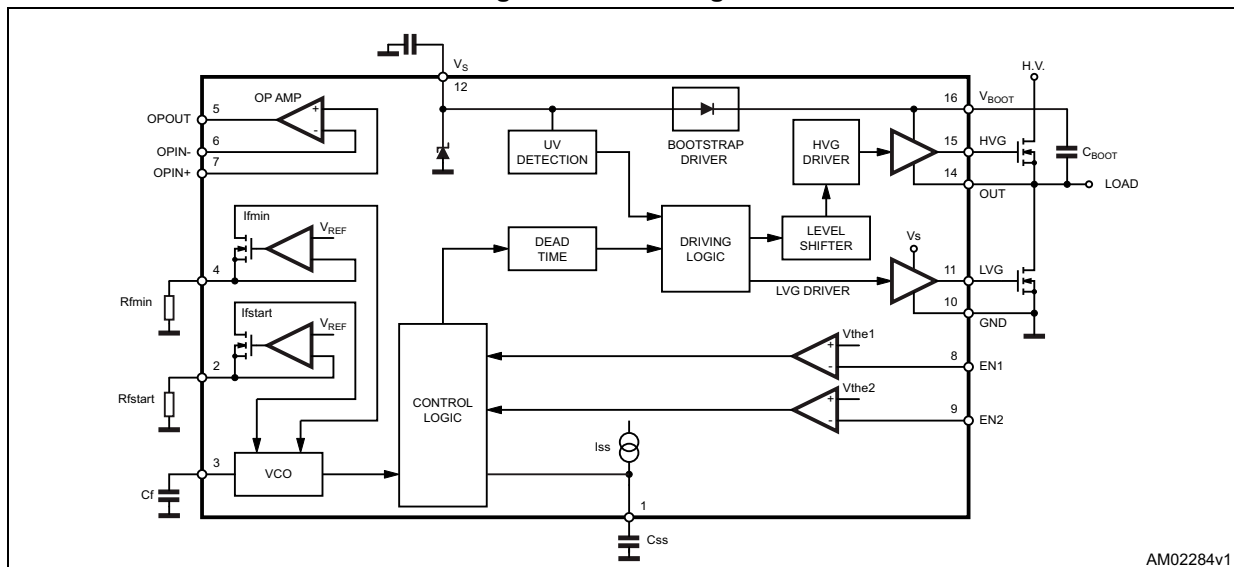
Description

The L6598 device is manufactured with the BCD™ offline technology, able to ensure voltage ratings up to 600 V, making it perfectly suited for AC/DC adapters and wherever a resonant topology can be beneficial. The device is intended to drive two power MOSFETs, in the classical half bridge topology. A dedicated timing section allows the designer to set soft-start time, soft-start and minimum frequency. An error amplifier, together with the two enable inputs, are made available. In addition, the integrated bootstrap diode and the Zener clamping on low voltage supply, reduces to a minimum the external parts needed in the applications.

Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/ns in full temperature range
- Driver current capability: 250 mA source 450 mA sink
- Switching times 80/40 ns rise/fall with 1 nF load
- CMOS shutdown input
- Undervoltage lockout
- Soft-start frequency shifting timing

Figure 1. Block diagram



Contents

| | | |
|----------|---|-----------|
| 1 | Maximum ratings | 3 |
| 2 | Electrical characteristics | 4 |
| 3 | Pin connections | 6 |
| 4 | Timing diagrams | 7 |
| 5 | Block diagram description | 9 |
| 5.1 | High/low side driving section | 9 |
| 5.2 | Timing and oscillator section | 9 |
| 5.3 | Bootstrap section | 13 |
| 5.4 | Op amp section | 14 |
| 5.5 | Comparators | 15 |
| 6 | Package information | 19 |
| 7 | Ordering codes | 22 |
| 8 | Revision history | 23 |

1 Maximum ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|------------|--|-----------------|------|
| IS | Supply current at $V_{cl}^{(1)}$ | 25 | mA |
| VLVG | Low side output | 14.6 | V |
| VOUT | High side reference | -1 to VBOOT -18 | V |
| VHVG | High side output | -1 to VBOOT | V |
| VBOOT | Floating supply voltage | 618 | V |
| dVBOOT/dt | VBOOT pin slew rate (repetitive) | ± 50 | V/ns |
| dVOUT/dt | OUT pin slew rate (repetitive) | ± 50 | V/ns |
| Vir | Forced input voltage (pins Rfmin, Rfstart) | -0.3 to 5 | V |
| Vic | Forced input voltage (pins C _{ss} , Cf) | -0.3 to 5 | V |
| VEN1, VEN2 | Enable input voltage | -0.3 to 5 | V |
| IEN1, IEN2 | Enable input current | ± 3 | mA |
| Vopc | Sense op amp common mode range | -0.3 to 5 | V |
| Vopd | Sense op amp differential mode range | -5 to 5 | V |
| Vopo | Sense op amp output voltage (forced) | 4.6 | V |
| Tstg | Storage temperature | -40 to +150 | °C |
| Tj | Junction temperature | -40 to +150 | °C |
| Tamb | Ambient temperature | -40 to +125 | °C |

1. The device is provided of an internal clamping Zener between GND and the Vs pin, It must not be supplied by a low impedance voltage source.

Note: ESD immunity for pins 14, 15 and 16 is guaranteed up to 900 (human body model).

Table 2. Thermal data

| Symbol | Parameter | SO16N | DIP16 | Unit |
|-------------------|--|-------|-------|------|
| R _{thJA} | Thermal resistance junction to ambient | 120 | 80 | °C/W |

Table 3. Recommended operating conditions

| Symbol | Parameter | Value | Unit |
|----------------------------------|-----------------------------|-------------------------------|------|
| V _S | Supply voltage | 10 to V _{cl} | V |
| V _{out} ⁽¹⁾ | High side reference | -1 to Vboot - V _{cl} | V |
| V _{boot} ⁽¹⁾ | Floating supply rail | 500 | V |
| f _{max} | Maximum switching frequency | 400 | kHz |

1. If the condition $V_{boot} - V_{out} < 18$ is guaranteed, V_{out} can range from -3 to 580 V.

2 Electrical characteristics

$$V_S = 12 \text{ V}; V_{\text{BOOT}} - V_{\text{OUT}} = 12 \text{ V}; T_A = 25 \text{ }^\circ\text{C}$$

Table 4. Electrical characteristics

| Symbol | Pin | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|------------------------------|-------|--|--|------|------|------|---------------|
| Supply voltage | | | | | | | |
| V_{suVP} | 12 | V_S turn on threshold | | 10 | 10.7 | 11.4 | V |
| V_{suVn} | | V_S turn off threshold | | 7.3 | 8 | 8.7 | V |
| V_{suVh} | | Supply voltage under voltage hysteresis | | | 2.7 | | V |
| V_{cl} | | Supply voltage clamping | | 14.6 | 15.6 | 16.6 | V |
| I_{su} | | Start up current | $V_S < V_{\text{suVn}}$ | | | 250 | μA |
| I_{q} | | Quiescent current, $f_{\text{out}} = 60 \text{ kHz}$, no load | $V_S > V_{\text{suVP}}$ | | 2 | 3 | mA |
| High voltage section | | | | | | | |
| I_{bootleak} | 16 | BOOT pin leakage current | $V_{\text{BOOT}} = 580 \text{ V}$ | | | 5 | μA |
| I_{outleak} | 14 | OUT pin leakage current | $V_{\text{OUT}} = 562 \text{ V}$ | | | 5 | μA |
| R_{DSon} | 16 | Bootstrap driver on-resistance | | 100 | 150 | 300 | Ω |
| High/low side drivers | | | | | | | |
| I_{hVgso} | 15 | High side driver source current | $V_{\text{HVG}} - V_{\text{OUT}} = 0$ | 170 | 250 | | mA |
| I_{hVgsi} | | High side driver sink current | $V_{\text{HVG}} - V_{\text{BOOT}} = 0$ | 300 | 450 | | mA |
| I_{lVgso} | 11 | Low side driver source current | $V_{\text{LVG}} - \text{GND} = 0$ | 170 | 250 | | mA |
| I_{lVgsi} | | Low side driver sink current | $V_{\text{LVG}} - V_S = 0$ | 300 | 450 | | mA |
| t_{rise} | 15,11 | Low/high side output rise time | $C_{\text{load}} = 1 \text{ nF}$ | | 80 | 120 | ns |
| t_{fall} | | | $C_{\text{load}} = 1 \text{ nF}$ | | 40 | 80 | ns |
| Oscillator | | | | | | | |
| DC | 14 | Output duty cycle | | 48 | 50 | 52 | % |
| f_{min} | | Minimum output oscillation frequency | $C_f = 470 \text{ pF};$ $R_{\text{fmin}} = 50 \text{ k}\Omega$ | 58.2 | 60 | 61.8 | kHz |
| f_{start} | | Soft-start output oscillation frequency | $C_f = 470 \text{ pF};$ $R_{\text{fmin}} = 50 \text{ k}\Omega;$ $R_{\text{fstart}} = 47 \text{ k}\Omega$ | 114 | 120 | 126 | kHz |

Table 4. Electrical characteristics (continued)

| Symbol | Pin | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-----------------------|------|---|-------------------|-------|------|-------|------------|
| V_{ref} | 2, 4 | Voltage to current converters threshold | | 1.9 | 2 | 2.1 | V |
| t_d | 14 | Deadtime between low and high side conduction | | 0.2 | 0.27 | 0.35 | μ s |
| IVref | 2, 4 | Reference current | | 120 | | | μ A |
| Timing section | | | | | | | |
| k_{ss} | 1 | Soft-start timing constant | $C_{ss} = 330$ nF | 0.115 | 0.15 | 0.185 | s/ μ F |
| Sense op amp | | | | | | | |
| I_{IB} | 6, 7 | Input bias current | | | | 0.1 | μ A |
| V_{io} | | Input offset voltage | | -10 | | 10 | mV |
| R_{out} | 5 | Output resistance | | 200 | | 300 | ? |
| I_{out-} | | Source output current | $V_{out} = 4.5$ V | 1 | | | mA |
| I_{out+} | | Sink output current | $V_{out} = 0.2$ V | 1 | | | mA |
| V_{ic} | 6,7 | Op amp input common mode range | | -0.2 | | 3 | V |
| GBW | | Sense op amp gain band width product ⁽¹⁾ | | 0.5 | 1 | | MHz |
| Gdc | | DC open loop gain | | 60 | 80 | | dB |
| Comparators | | | | | | | |
| V_{the1} | 8 | Enabling comparator threshold | | 0.56 | 0.6 | 0.64 | V |
| V_{the2} | 9 | Enabling comparator threshold | | 1.05 | 1.2 | 1.35 | V |
| t_{pulse} | 8,9 | Minimum pulse length | | | | 200 | ns |

1. Guaranteed by design.

3 Pin connections

Figure 2. Pin connections

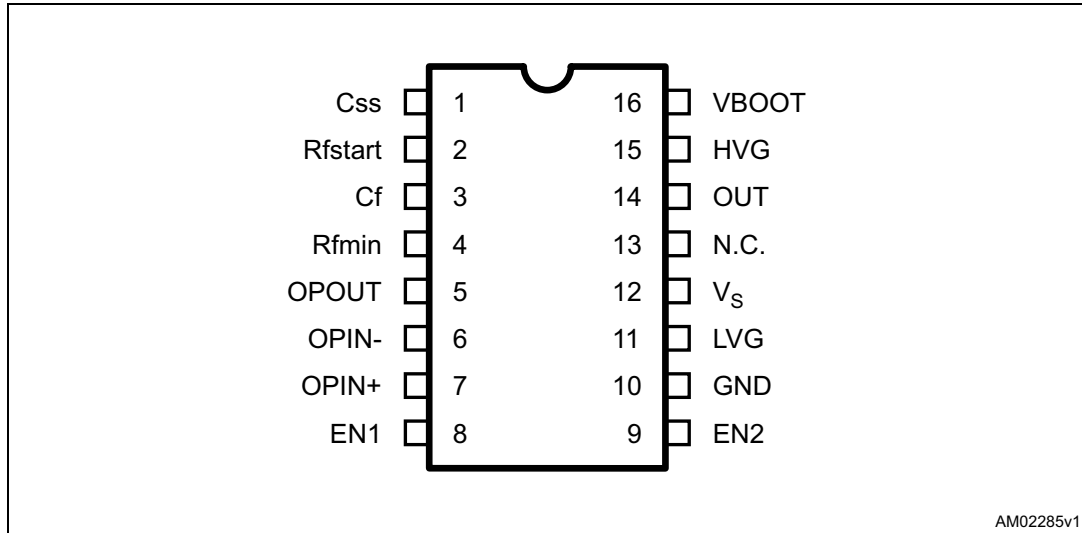
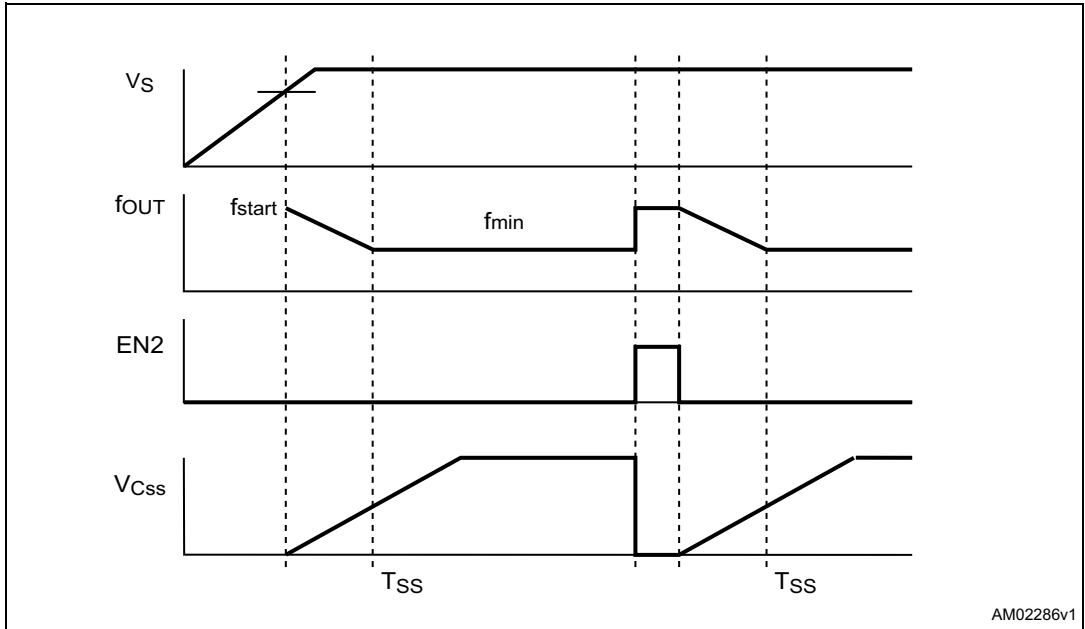


Table 5. Pin description

| Pin no. | Name | Function |
|---------|---------------------|--|
| 1 | CSS | Soft-start timing capacitor |
| 2 | R _{fstart} | Soft-start frequency setting - low impedance voltage source -see also C _f |
| 3 | C _f | Oscillator frequency setting - see also R _{fmin} , R _{fstart} |
| 4 | R _{fmin} | Minimum oscillation frequency setting - low impedance voltage source - see also C _f |
| 5 | O _{Pout} | Sense op amp output - low impedance |
| 6 | O _{Pon-} | Sense op amp inverting input -high impedance |
| 7 | O _{Pon+} | Sense op amp non inverting input - high impedance |
| 8 | EN1 | Half bridge latched enable |
| 9 | EN2 | Half bridge unlatched enable |
| 10 | GND | Ground |
| 11 | LVG | Low side driver output |
| 12 | V _s | Supply voltage with internal Zener clamp |
| 13 | N.C. | Not connected |
| 14 | OUT | High side driver reference |
| 15 | HVG | High side driver output |
| 16 | V _{boot} | Bootstrapped supply voltage |

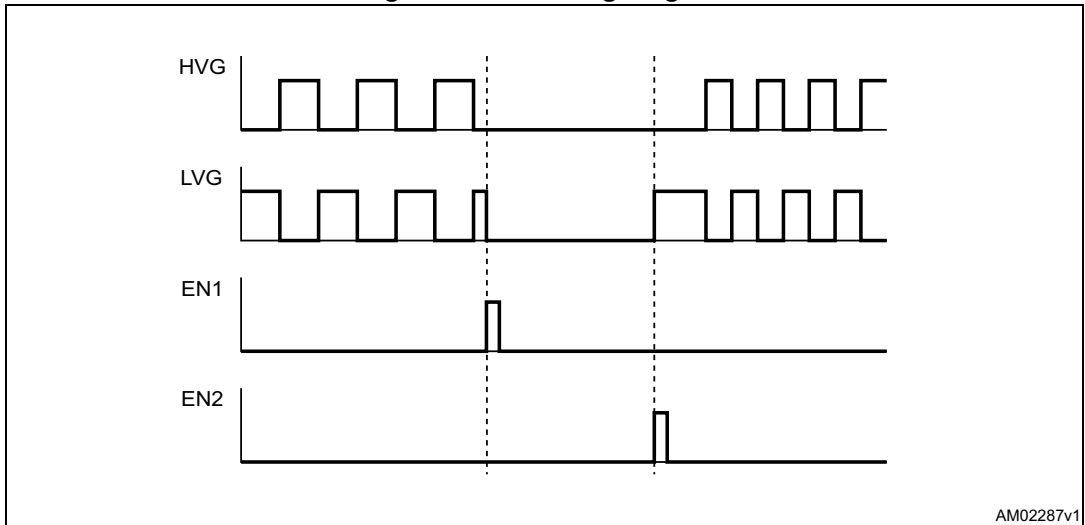
4 Timing diagrams

Figure 3. EN2 timing diagram



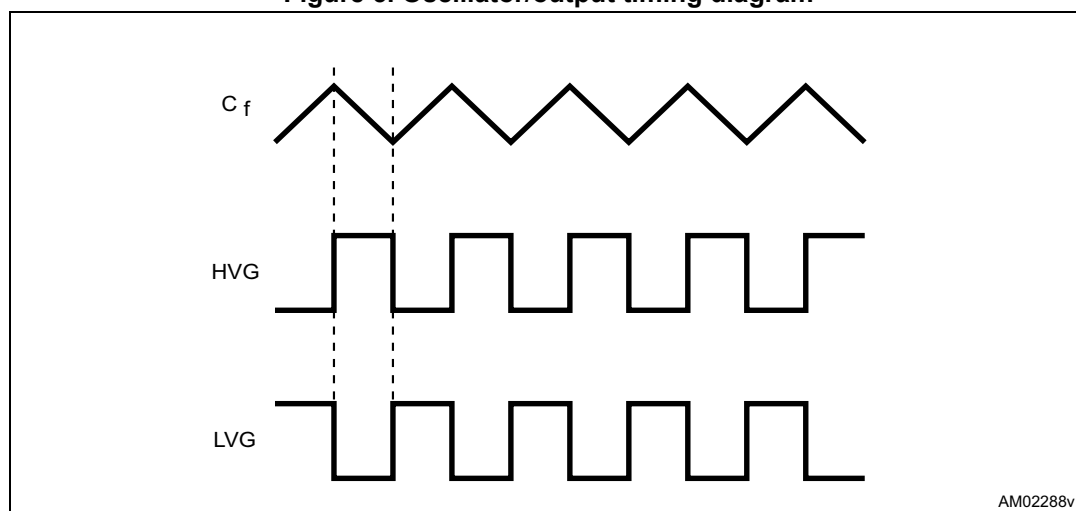
AM02286v1

Figure 4. EN1 timing diagram



AM02287v1

Figure 5. Oscillator/output timing diagram



5 Block diagram description

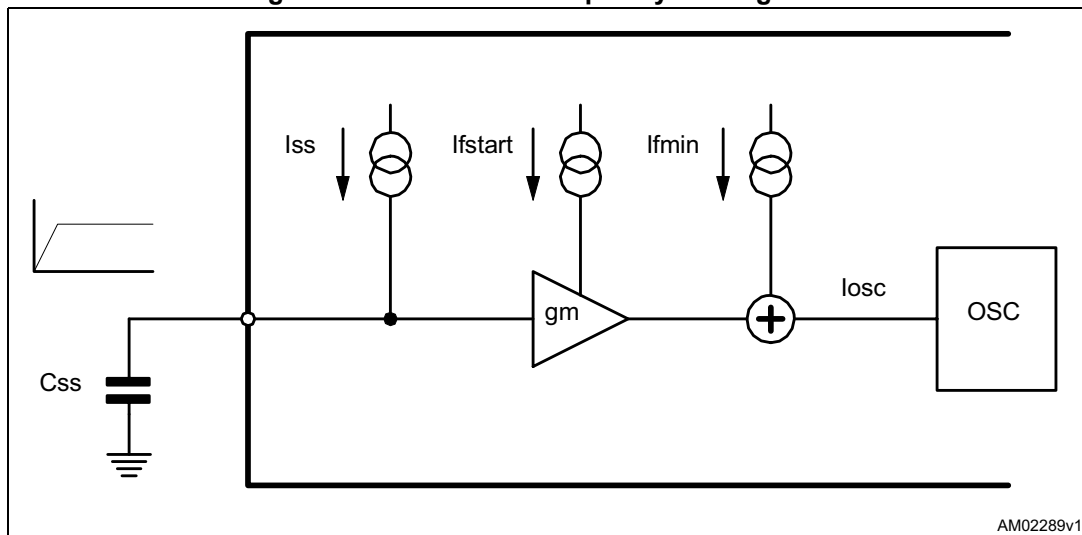
5.1 High/low side driving section

A high and low side driving section provide the proper driving to the external power MOS or IGBT. A high sink/source driving current (450/250 mA typ.) ensure fast switching times also when size for power MOS are used. The internal logic ensures a minimum deadtime to avoid cross conduction of the power devices.

5.2 Timing and oscillator section

The device is provided of a soft-start function. It consists in a period of time, T_{SS} , in which the switching frequency shifts from f_{start} to f_{min} . This feature is explained in the following description (refer to [Figure 6](#) and [Figure 7](#)).

Figure 6. Soft-start and frequency shifting block



During the soft-start time the current I_{SS} charges the capacitor C_{SS} , generating a voltage ramp which is delivered to a transconductance amplifier, as shown in [Figure 6](#). Thus this voltage signal is converted in a growing current which is subtracted to I_{fstart} . Therefore the current which drives the oscillator to set the frequency during the soft-start is equal to:

Equation 1

$$I_{osc} = I_{fmin} + (I_{fstart} - g_m V_{C_{SS}}(t)) = I_{fmin} + \left(I_{fstart} - \frac{g_m I_{SS}}{C_{SS}} \right)$$

Equation 2

$$\text{where } I_{fmin} = \frac{V_{REF}}{R_{fmin}}, I_{fstart} = \frac{V_{REF}}{R_{fstart}}, V_{REF} = 2V$$

At the startup ($t = 0$) the oscillator frequency is set by:

Equation 3

$$I_{OSC}(0) = I_{fmin} + I_{fstart} = V_{REF} \left(\frac{1}{R_{fmin}} + \frac{1}{R_{fstart}} \right)$$

At the end of the soft-start ($t = T_{SS}$) the second term of eq.1 decreases to zero and the switching frequency is set only by I_{min} (i.e. R_{fmin}):

Equation 4

$$I_{OSC}(T_{SS}) = I_{fmin} = \frac{V_{REF}}{R_{fmin}}$$

Since the second term of [Equation 1](#) is equal to zero, we have:

Equation 5

$$I_{fstart} - \frac{g_m I_{SS}}{C_{SS}} T_{SS} = 0 \rightarrow T_{SS} = \frac{C_{SS} I_{fstart}}{g_m I_{SS}}$$

Note that there is not a fixed threshold of the voltage across C_{SS} in which the soft-start finishes (i.e. the end of the frequency shifting), and T_{SS} depends on C_{SS} , I_{fstart} , g_m , and I_{SS} ([Equation 5](#)). Making T_{SS} independent of I_{fstart} , the I_{SS} current has been designed to be a fraction of I_{fstart} , so:

Equation 6

$$I_{SS} = \frac{I_{fstart}}{K} \rightarrow T_{SS} = \frac{C_{SS} I_{fstart}}{g_m I_{fstart} K} \rightarrow T_{SS} = \frac{C_{SS}}{g_m K} \rightarrow T_{SS} = k_{SS} C_{SS}$$

In this way the soft-start time depends only on the capacitor C_{SS} . The typical value of the k_{SS} constant (Soft-start timing constant) is 0.15 s/ μ F.

The current I_{OSC} is fed to the oscillator as shown in [Figure 7](#). It is twice mirrored (x4 and x8) generating the triangular wave on the oscillator capacitor C_f . Referring to the internal structure of the oscillator ([Figure 7](#)), a good relationship to compute an approximate value of the oscillator frequency in normal operation is:

Equation 7

$$f_{min} = \frac{1.41}{R_{fmin} C_f}$$

The degree of approximation depends on the frequency value, but it remains very good in the range from 30 kHz to 100 kHz (*Figure 8* to *Figure 12*).

Figure 7. Oscillator block

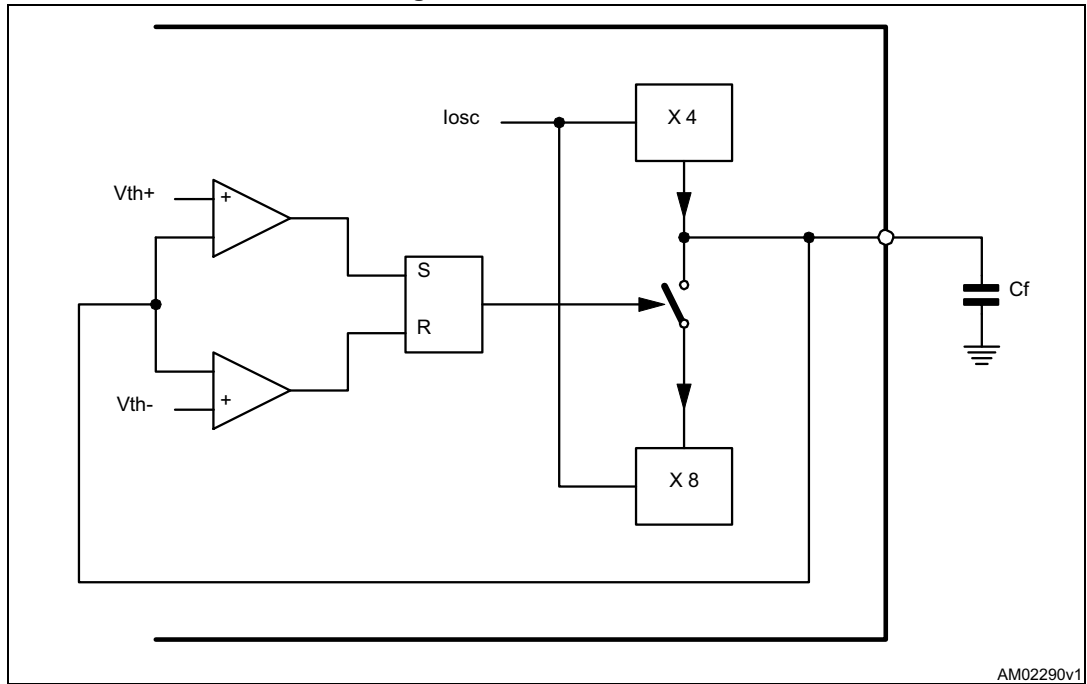


Figure 8. Typ. f_{min} vs. R_{fmin} at $C_f = 470$ pF

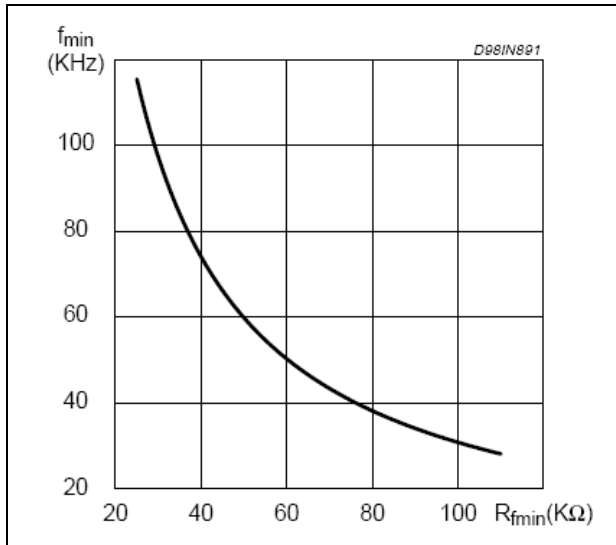


Figure 9. Typ. $(f_{start}-f_{min})$ vs. R_{fstar} at $C_f = 470$ pF

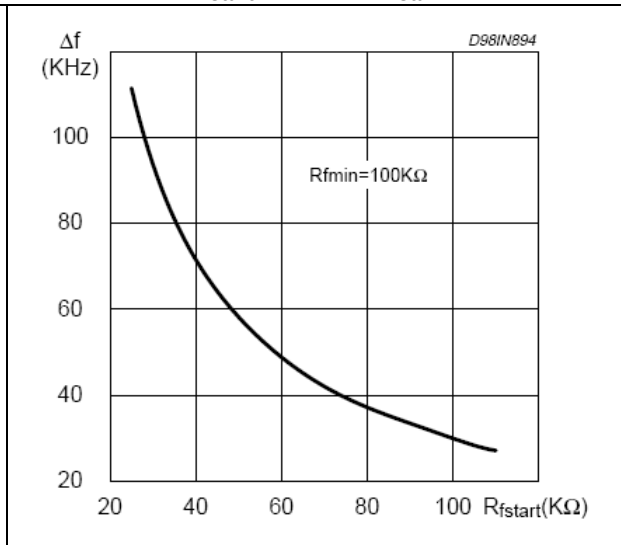


Figure 10. Typ. $(f_{start}-f_{min})$ vs. R_{fstar} at $C_f = 470$ pF

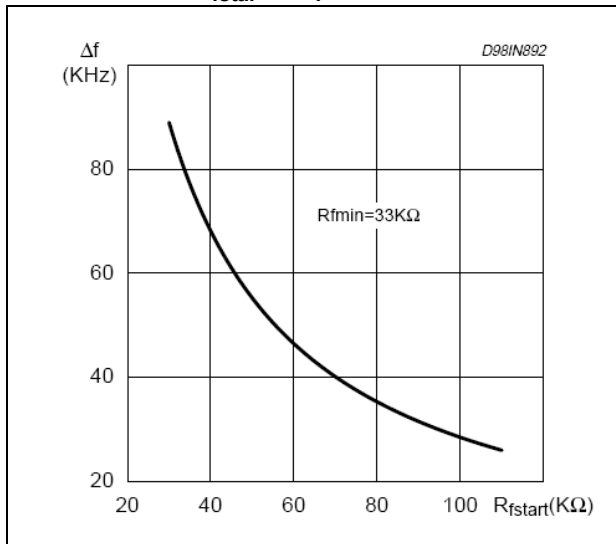


Figure 11. f_{min} at different R_f vs C_f

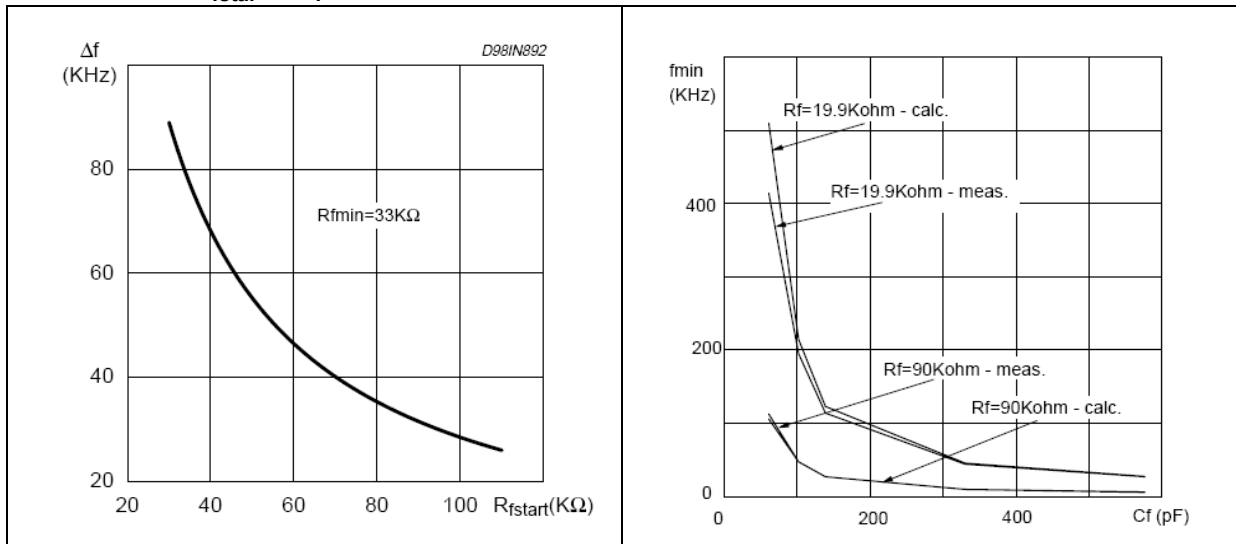
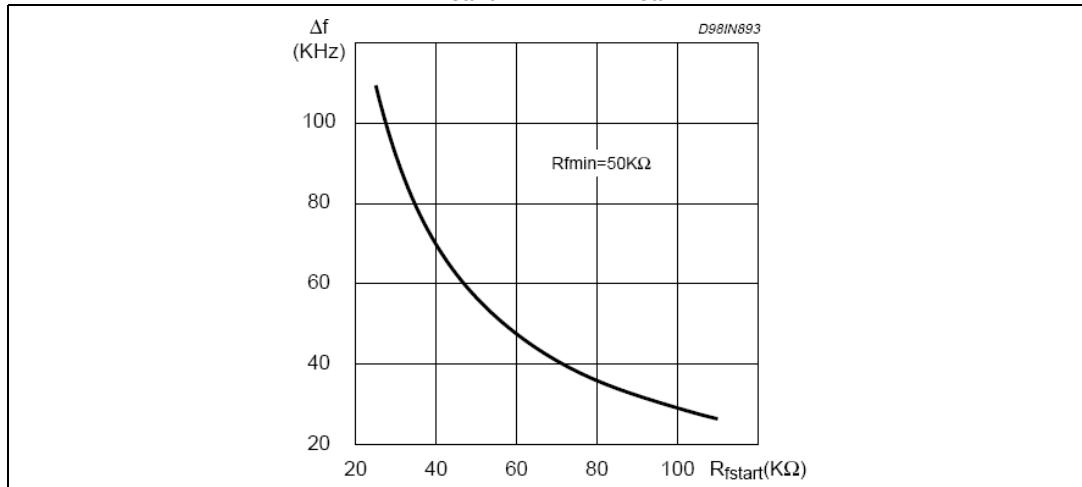
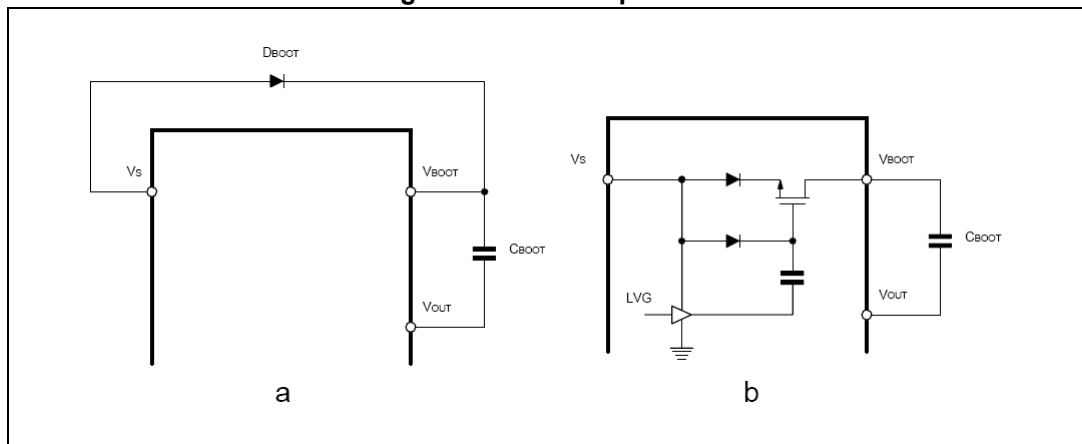


Figure 12. Typ. ($f_{start}-f_{min}$) vs. R_{fstar} at $C_f = 470$ pF

5.3 Bootstrap section

The supply of the high voltage section is obtained by means of a bootstrap circuitry. This solution normally requires a high voltage fast recovery diode for charging the bootstrap capacitor (*Figure 13* - part a). In the device a patented integrated structure replaces this external diode. It is released by means of a high voltage DMOS, driven synchronously with the low side driver (LVG), with in series a diode, as shown in *Figure 13* - part b.

Figure 13. Bootstrap driver



To drive the synchronized DMOS it is necessary a voltage higher than the supply voltage V_s . This voltage is obtained by means of an internal charge pump (*Figure 13* - part b).

The diode connected in series to the DMOS has been added to avoid undesirable turn on of it. The introduction of the diode prevents any current can flow from the V_{boot} pin to the V_S one in case that the supply is quickly turned off when the internal capacitor of the pump is not fully discharged.

The bootstrap driver introduces a voltage drop during the recharging of the capacitor C_{boot} (i.e. when the low side driver is on), which increases with the frequency and with the size of the external power MOS. It is the sum of the drop across the R_{DSON} and of the diode

threshold voltage. At low frequency this drop is very small and can be neglected. Anyway increasing the frequency it must be taken in to account. In fact the drop, reducing the amplitude of the driving signal, can significantly increase the R_{DSON} of the external power MOS (and so the dissipation).

To be considered that in resonant power supplies the current which flows in the power MOS decreases increasing the switching frequency and generally the increases of R_{DSON} is not a problem because power dissipation is negligible. [Equation 8](#) is useful to compute the drop on the bootstrap driver:

Equation 8

$$V_{\text{drop}} = I_{\text{charge}} R_{\text{dson}} + V_{\text{diode}} \rightarrow V_{\text{drop}} = \frac{Q_g}{T_{\text{charge}}} R_{\text{dson}} + V_{\text{diode}}$$

where Q_g is the gate charge of the external power MOS, R_{dson} is the on-resistance of the bootstrap DMOS, and T_{charge} is the time in which the bootstrap driver remains on (about the semi-period of the switching frequency minus the deadtime). The typical resistance value of the bootstrap DMOS is 150Ω . For example using a power MOS with a total gate charge of 30 nC the drop on the bootstrap driver is about 3 V , at a switching frequency of 200 kHz . In fact:

Equation 9

$$V_{\text{drop}} = \frac{30 \text{ nC}}{2.23 \mu\text{s}} 150 \Omega + 0.6 \text{ V} \sim 2.6 \text{ V}$$

To summaries, if a significant drop on the bootstrap driver (at high switching frequency when large power MOS are used) represents a problem, an external diode can be used, avoiding the drop on the R_{DSON} of the DMOS.

5.4 Op amp section

The integrated op amp is designed to offer low output impedance, wide band, high input impedance and wide common mode range. It can be readily used to implement protection features or a closed loop control. For this purpose the op amp output can be properly connected to R_{fmin} pin to adjust the oscillation frequency.

5.5 Comparators

Two CMOS comparators are available to perform protection schemes.

Short pulses (≥ 200 ns) on comparators input are recognized. The EN1 input (active high), has a threshold of 0.6 V (typical value) forces the device in a latched shut down state (e.g. LVG low, HVG low, oscillator stopped), as in the under voltage conditions. Normal operating conditions are resumed after a power-off power-on sequence. The EN2 input (active high), with a threshold of 1.2 V (typical value) restarts a soft-start sequence (see timing diagrams in *Figure 3*, *Figure 4*, and *Figure 5*). In addition the EN2 comparator, when activated, removes a latched shutdown caused by EN1.

Figure 14. Switching time waveform definitions

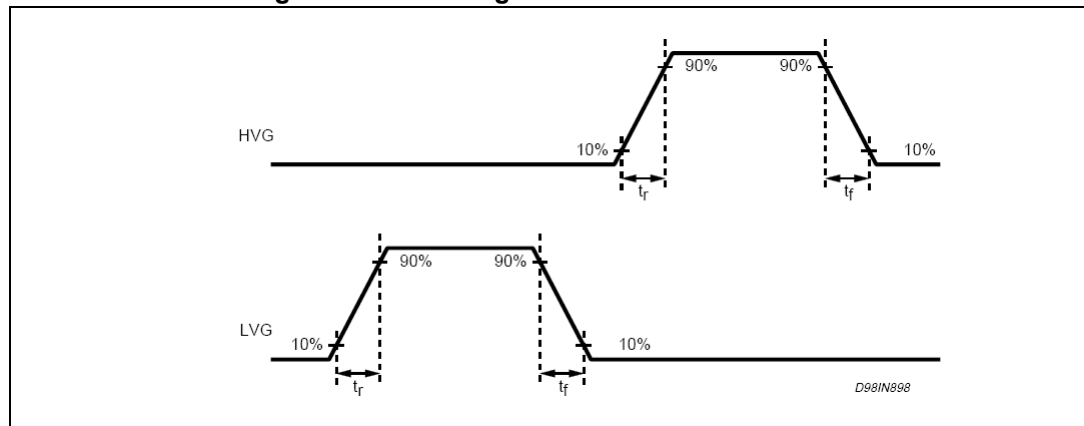


Figure 15. Deadtime and duty cycle waveform definition

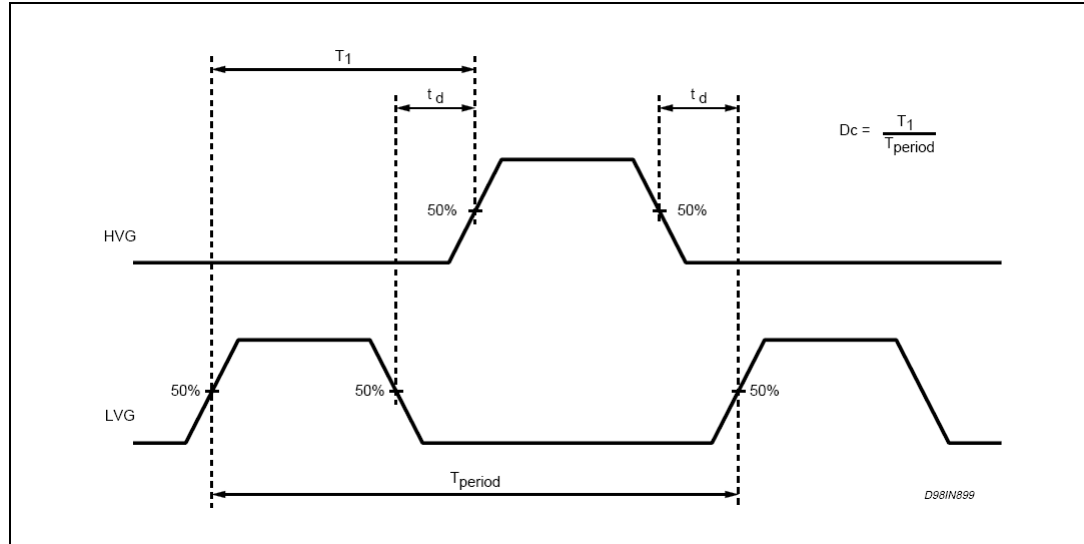


Figure 16. Typ. f_{min} vs. temperature

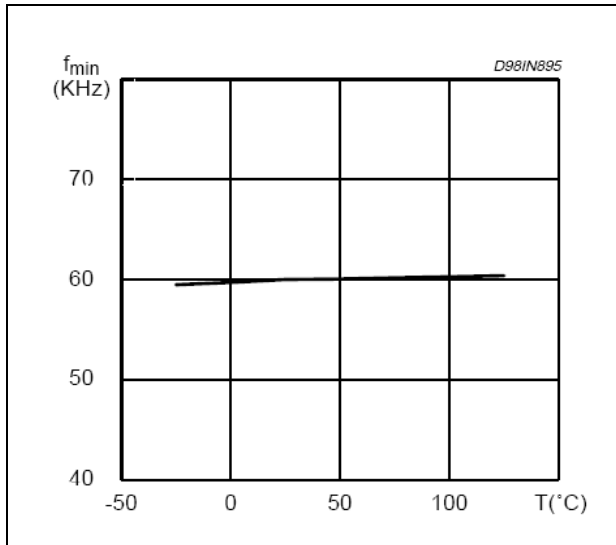


Figure 17. Startup current vs. temperature

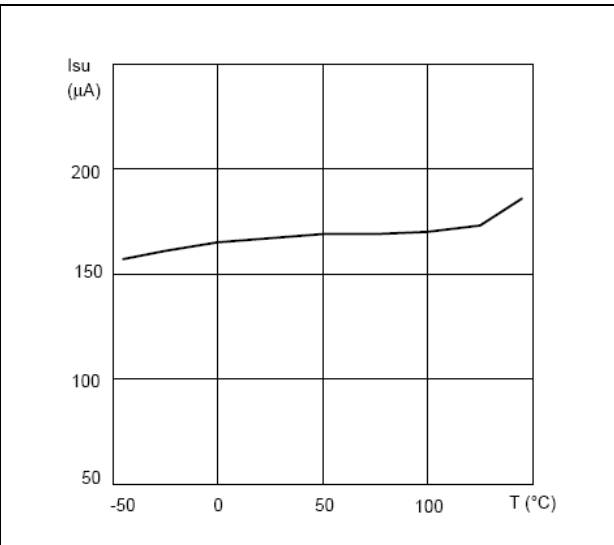


Figure 18. Typ. f_{start} vs. temperature

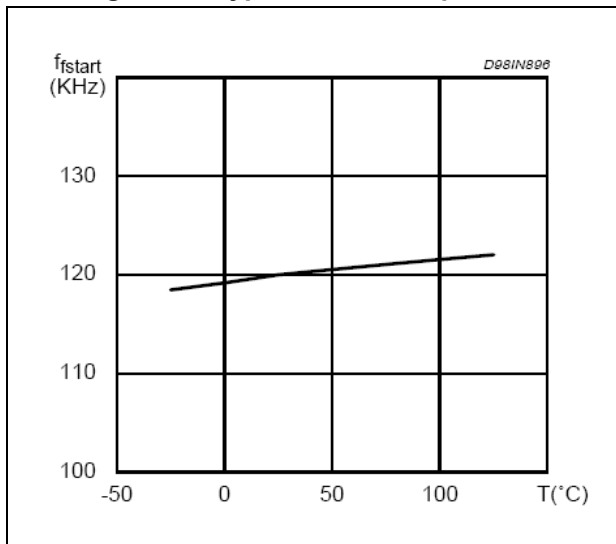


Figure 19. Quiescent current vs. temperature

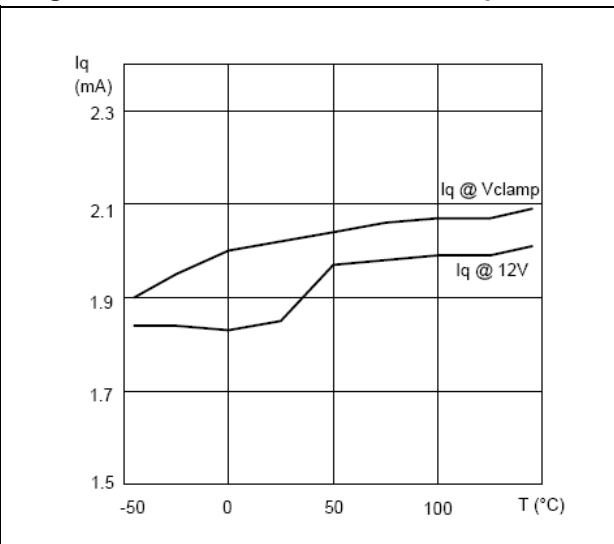


Figure 20. Vs thresholds and clamp vs. temp.

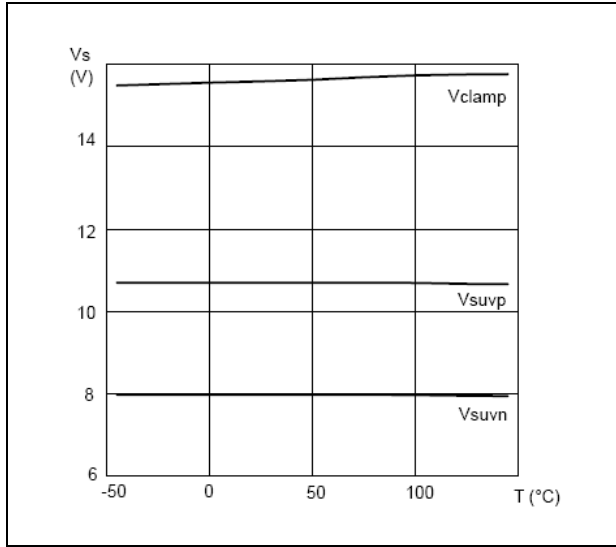


Figure 21. HVG source and sink current vs. temperature

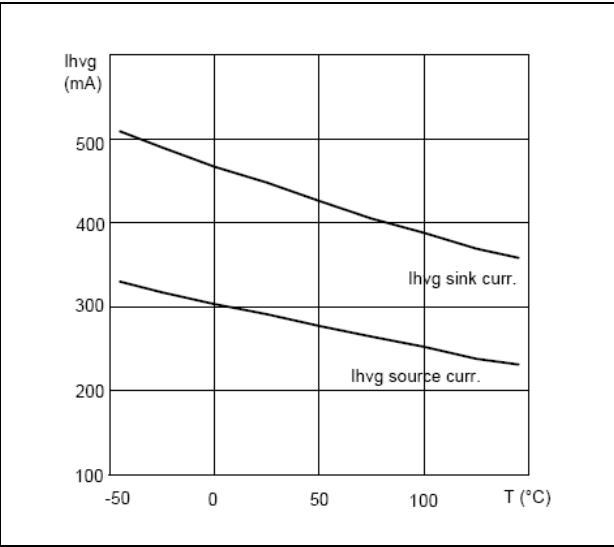


Figure 22. LVG source and sink current vs. temperature

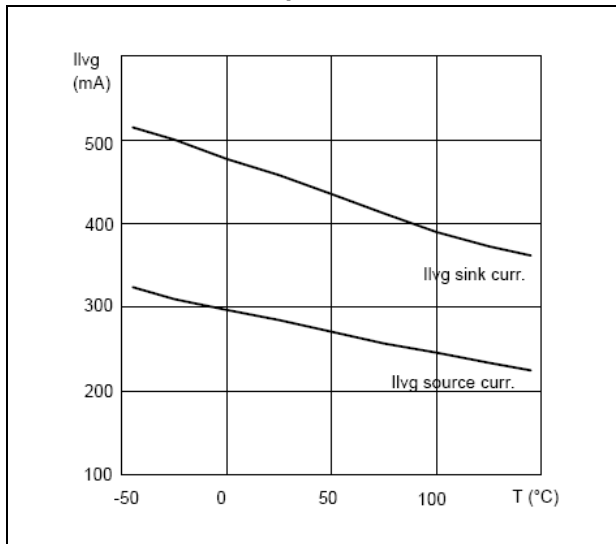


Figure 23. Soft-start timing constant vs. temperature

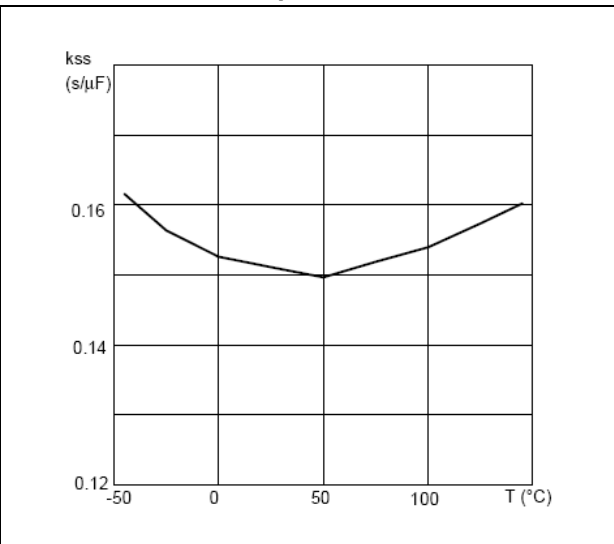
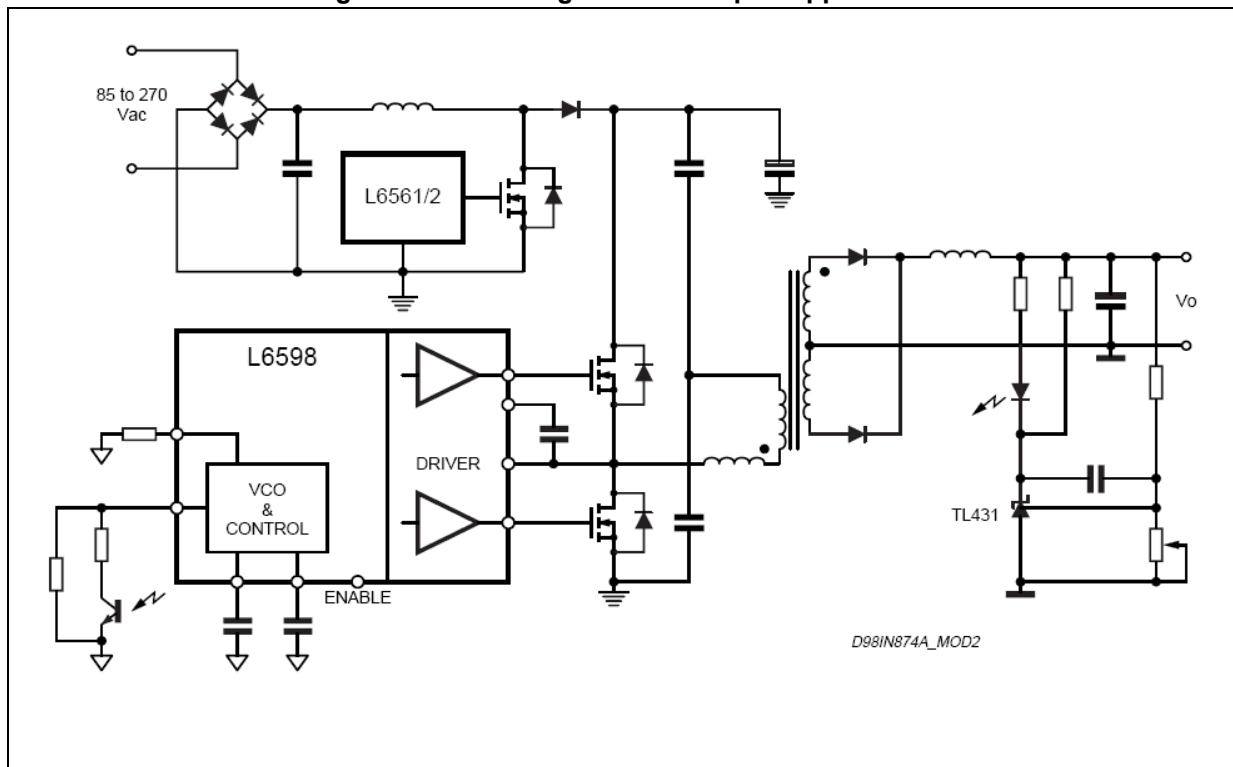


Figure 24. Wide range AC/DC adapter application



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 25. Plastic DIP16 (0.25) package outline

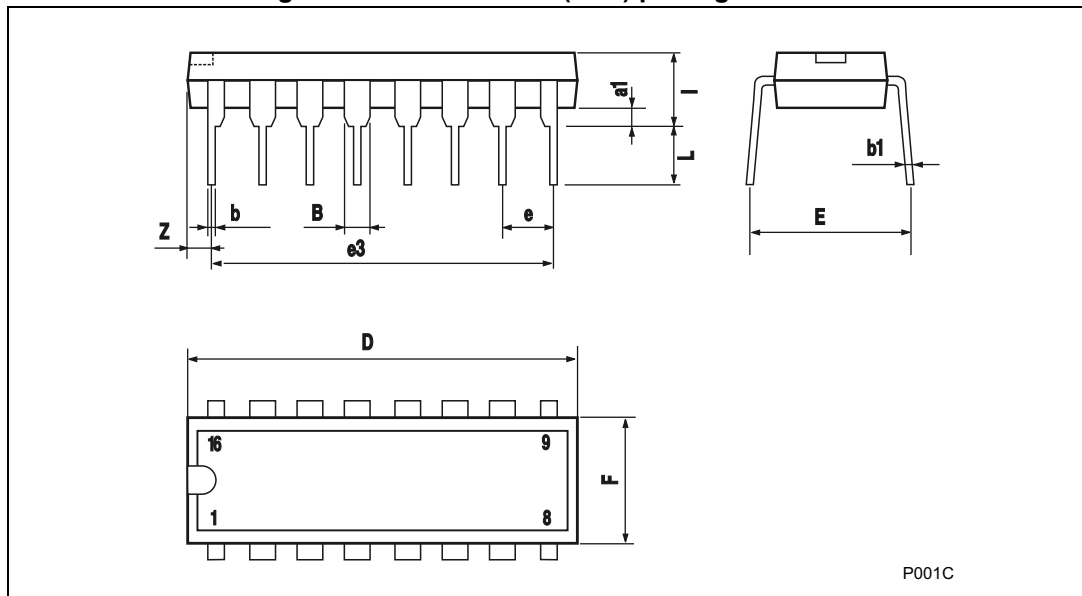
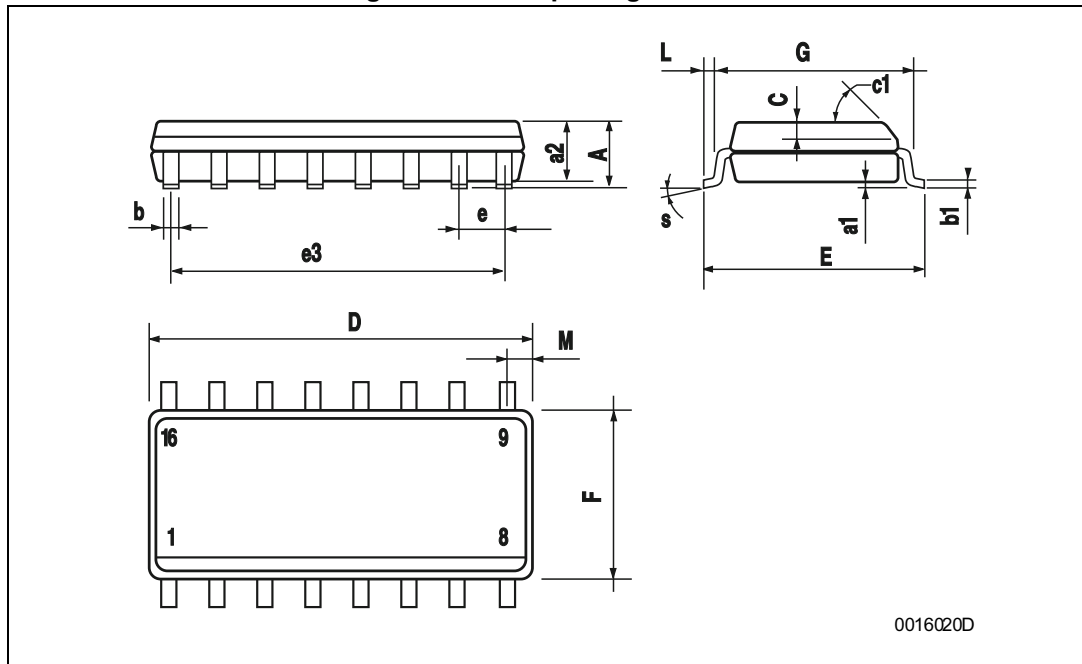


Table 6. Plastic DIP16 (0.25) package mechanical data

| Symbol | Dimensions | | | | | |
|--------|------------|-------|------|-------|-------|-------|
| | mm | | | inch | | |
| | Min. | Typ | Max. | Min. | Typ. | Max. |
| a1 | 0.51 | | | 0.020 | | |
| B | 0.77 | | 1.65 | 0.030 | | 0.065 |
| b | | 0.5 | | | 0.020 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 20 | | | 0.787 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 17.78 | | | 0.700 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 5.1 | | | 0.201 |
| L | | 3.3 | | | 0.130 | |
| Z | | | 1.27 | | | 0.050 |

Figure 26. SO16 package outline



0016020D

Table 7. SO16 package mechanical data

| Symbol | Dimensions | | | | | |
|--------|------------|------|------|-------|-------|-------|
| | mm | | | inch | | |
| | Min. | Typ | Max. | Min. | Typ. | Max. |
| A | | | 1.75 | | | 0.068 |
| a | 1.0 | | 1.27 | 0.039 | | 0.050 |
| a2 | | | 1.64 | | | 0.063 |
| b | 0.35 | | 0.46 | 0.013 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | | 0.5 | | | 0.019 | |
| c1 | 45° (typ.) | | | | | |
| D | 9.8 | | 10 | 0.385 | | 0.393 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 8.89 | | | 0.350 | |
| F | 3.8 | | 4.0 | 0.149 | | 0.157 |
| G | 4.6 | | 5.3 | 0.181 | | 0.208 |
| L | 0.5 | | 1.27 | 0.019 | | 0.050 |
| M | | | 0.62 | | | 0.024 |
| S | 8° (max.) | | | | | |

7 Ordering codes

Table 8. Ordering information

| Order codes | Package | Packing |
|-------------|---------|---------------|
| L6598 | DIP16 | Tube |
| L6598D | SO16N | Tube |
| L6598D013TR | | Tape and reel |

8 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 21-Jun-2004 | 5 | Changed the impagination following the new release of "corporate technical publication design guide". Done a few of corrections in the text. |
| 09-Sep-2004 | 6 | Added ordering number for the tape and reel version, updated Table 4 on page 4 |
| 02-Oct-2009 | 7 | Updated Table 4 on page 4 |
| 18-Nov-2013 | 8 | Added cross-reference in Section 5 . Updated Section 6: Package information (reformatted - added title of Figure 25 and Table 6 , Figure 26 and Table 7 and reversed order of <i>figures</i> and <i>tables</i> , minor modifications). Updated Table 8 (replaced L6598D016TR device by L6598D013TR device). Minor corrections throughout document. |

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