

# SN74CB3T3125 Quadruple FET Bus Switch

## 2.5-V, 3.3-V Low-Voltage Bus Switch with 5-V-Tolerant Level Shifter

### 1 Features

- Output Voltage Translation Tracks  $V_{CC}$
- Supports Mixed-Mode Signal Operation On All Data I/O Ports
  - 5-V Input Down to 3.3-V Output-Level Shift With 3.3-V  $V_{CC}$
  - 5-V/3.3-V Input Down to 2.5-V Output-Level Shift With 2.5-V  $V_{CC}$
- 5-V-Tolerant I/Os With Device Powered Up or Powered Down
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance ( $r_{on}$ ) Characteristics ( $r_{on} = 5 \Omega$  Typical)
- Low Input/Output Capacitance Minimizes Loading ( $C_{io(OFF)} = 4.5$  pF Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 20 \mu A$  Max)
- $V_{CC}$  Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- Supports Digital Applications: Level Translation, USB Interface, Bus Isolation
- Ideal for Low-Power Portable Equipment

### 3 Description

The SN74CB3T3125 is a high-speed TTL-compatible FET bus switch with low ON-state resistance ( $r_{on}$ ), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks  $V_{CC}$ . The SN74CB3T3125 supports systems using 5-V TTL, 3.3-V LVTTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see *Typical DC Voltage-Translation Characteristics*).

The SN74CB3T3125 is organized as four 1-bit bus switches with separate output-enable ( $1OE$ ,  $2OE$ ,  $3OE$ ,  $4OE$ ) inputs. It can be used as four 1-bit bus switches or as one 4-bit bus switch. When  $\overline{OE}$  is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 1-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

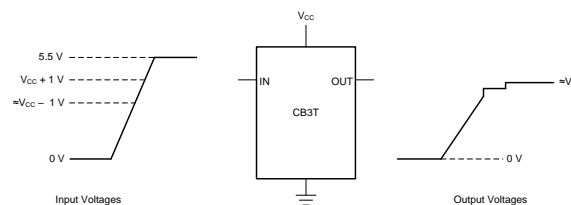
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74CB3T3125	VQFN – RGY (14)	3.50 mm x 3.50 mm
	TSSOP – PW (14)	5.00 mm x 4.40 mm
	TVSOP – DGV (14)	3.60 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Typical DC Voltage-Translation Characteristics



If the input high voltage ( $V_{IH}$ ) level is greater than or equal to  $V_{CC} + 1$  V, and less than or equal to 5.5 V, the output high voltage ( $V_{OH}$ ) level will be equal to approximately the  $V_{CC}$  voltage level.



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## 4 Revision History

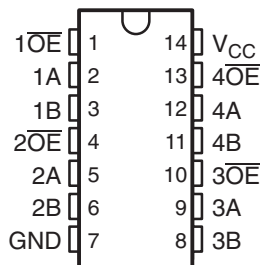
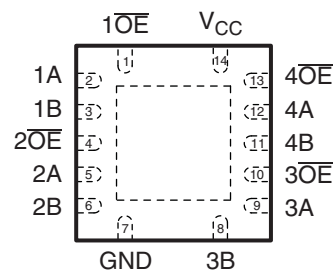
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2012) to Revision C	Page
• Added <i>Application</i> list, <i>Device Information</i> table, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Removed Ordering Information table. ....	1
• Changed $t_{en}$ $V_{CC} = 3.3$ V MAX value From: 4.4 ns To: 8 ns in the <i>Switching Characteristic</i> .....	5

Changes from Revision A (April 2009) to Revision B	Page
• Updated <i>Typical DC Voltage-Translation Characteristics</i> .....	1

## 5 Pin Configuration and Functions

**DGV OR PW PACKAGE  
(TOP VIEW)**

**RGY PACKAGE  
(TOP VIEW)**

**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{1OE}$	1	I	Active-low enable for switch 1
1A	2	I/O	Switch 1 A terminal
1B	3	I/O	Switch 1 B terminal
$\overline{2OE}$	4	I	Active-low enable for switch 2
2A	5	I/O	Switch 2 A terminal
2B	6	I/O	Switch 2 B terminal
GND	7	-	Ground
3A	8	I/O	Switch 3 A terminal
3B	9	I/O	Switch 3 B terminal
$\overline{3OE}$	10	I	Active-low enable for switch 3
4A	11	I/O	Switch 4 A terminal
4B	12	I/O	Switch 4 B terminal
$\overline{4OE}$	13	I	Active-low enable for switch 4
$V_{CC}$	14	-	Supply voltage pin

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>	-0.5	7	V
V <sub>IN</sub>	Control input voltage range <sup>(2) (3)</sup>	-0.5	7	V
V <sub>I/O</sub>	Switch I/O voltage range <sup>(2) (3) (4)</sup>	-0.5	7	V
I <sub>IK</sub>	Control input clamp current	V <sub>IN</sub> < 0	-50	mA
I <sub>I/O</sub>	I/O port clamp current	V <sub>I/O</sub> < 0	-50	mA
I <sub>I/O</sub>	ON-state switch current <sup>(5)</sup>		±128	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V<sub>I</sub> and V<sub>O</sub> are used to denote specific conditions for V<sub>I/O</sub>.
- (5) I<sub>I</sub> and I<sub>O</sub> are used to denote specific conditions for I<sub>I/O</sub>.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000
			V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.3	3.6	V
V <sub>IH</sub>	High-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	5.5
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	5.5
V <sub>IL</sub>	Low-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0	0.7
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	0.8
V <sub>I/O</sub>	Data input/output voltage	0	5.5	V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74CB3T3125			UNIT	
	VQFN (RGY)	TSSOP (PW)	TVSOP (DGV)		
	14 PINS	14 PINS	14 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	55.5	123.3	154.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	56.9	53.0	64.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	30.9	66.3	88.4	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	3.6	9.1	10.8	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	30.9	65.7	87.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	14.6	-	-	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics<sup>(1)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT	
$V_{IK}$		$V_{CC} = 3\text{ V}$ , $I_I = -18\text{ mA}$			-1.2	V	
$V_{OH}$		See <a href="#">Figure 3</a> through <a href="#">Figure 5</a>					
$I_{IN}$	Control inputs	$V_{CC} = 3.6\text{ V}$ , $V_{IN} = 3.6\text{ V to } 5.5\text{ V or GND}$			±10	μA	
$I_I$		$V_{CC} = 3.6\text{ V}$ , Switch ON, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC} - 0.7\text{ V to } 5.5\text{ V}$		±20	μA	
			$V_I = 0.7\text{ V to } V_{CC} - 0.7\text{ V}$		-40		
			$V_I = 0\text{ to } 0.7\text{ V}$		±5		
$I_{OZ}$ <sup>(3)</sup>		$V_{CC} = 3.6\text{ V}$ , $V_O = 0\text{ to } 5.5\text{ V}$ , $V_I = 0$ , Switch OFF, $V_{IN} = V_{CC}$ or GND			±10	μA	
$I_{off}$		$V_{CC} = 0$ , $V_O = 0\text{ to } 5.5\text{ V}$ , $V_I = 0$			10	μA	
$I_{CC}$		$V_{CC} = 3.6\text{ V}$ , $I_{I/O} = 0$ , Switch ON or OFF, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC}$ or GND		20	μA	
			$V_I = 5.5\text{ V}$		20		
$\Delta I_{CC}$ <sup>(4)</sup>	Control inputs	$V_{CC} = 3\text{ V to } 3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND			300	μA	
$C_{in}$	Control inputs	$V_{CC} = 3.3\text{ V}$ , $V_{IN} = V_{CC}$ or GND		3		pF	
$C_{io(OFF)}$		$V_{CC} = 3.3\text{ V}$ , $V_{I/O} = 5.5\text{ V}$ , $3.3\text{ V}$ , or GND, Switch OFF, $V_{IN} = V_{CC}$ or GND		4.5		pF	
$C_{io(ON)}$		$V_{CC} = 3.3\text{ V}$ , Switch ON, $V_{IN} = V_{CC}$ or GND	$V_{I/O} = 5.5\text{ V or } 3.3\text{ V}$		4	pF	
			$V_{I/O} = \text{GND}$		10		
$r_{on}$ <sup>(5)</sup>		$V_{CC} = 2.3\text{ V}$ , TYP at $V_{CC} = 2.5\text{ V}$ , $V_I = 0$	$I_O = 24\text{ mA}$		5	8	Ω
			$I_O = 16\text{ mA}$		5	8	
		$V_{CC} = 3\text{ V}$ , $V_I = 0$	$I_O = 64\text{ mA}$		5	7	
			$I_O = 32\text{ mA}$		5	7	

(1)  $V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.

(2) All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

(3) For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}$ <sup>(1)</sup>	A or B	B or A	0.15		0.25		ns
$t_{en}$	$\overline{OE}$	A or B	1	8.5	1	8	ns
$t_{dis}$	$\overline{OE}$	A or B	1	9	1	9	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

### 6.7 Typical Characteristics

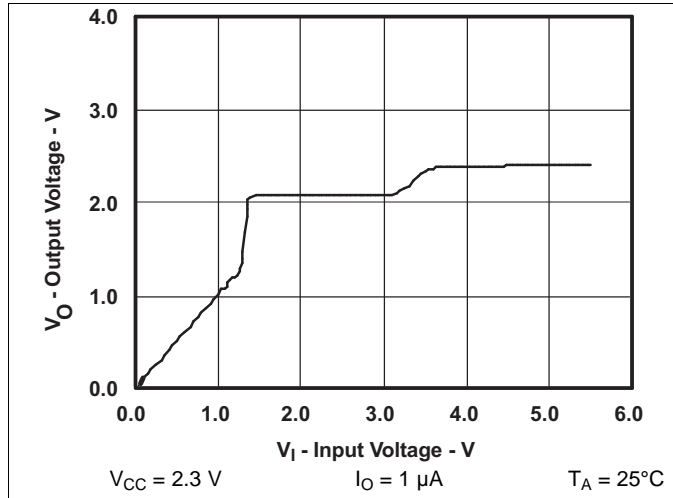


Figure 1. Data Output Voltage vs Data Input Voltage

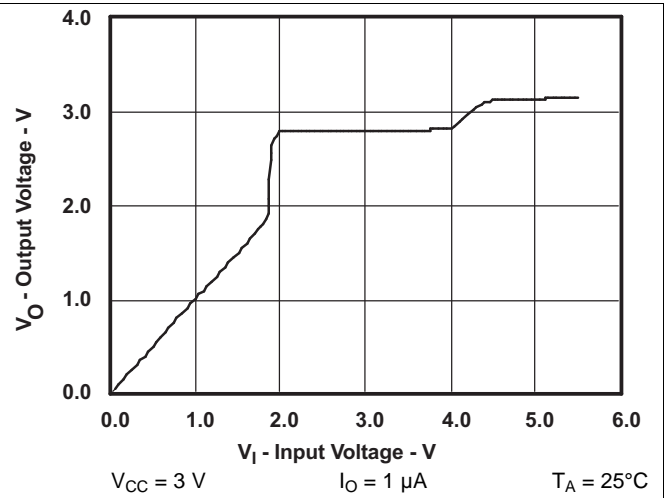


Figure 2. Data Output Voltage vs Data Input Voltage

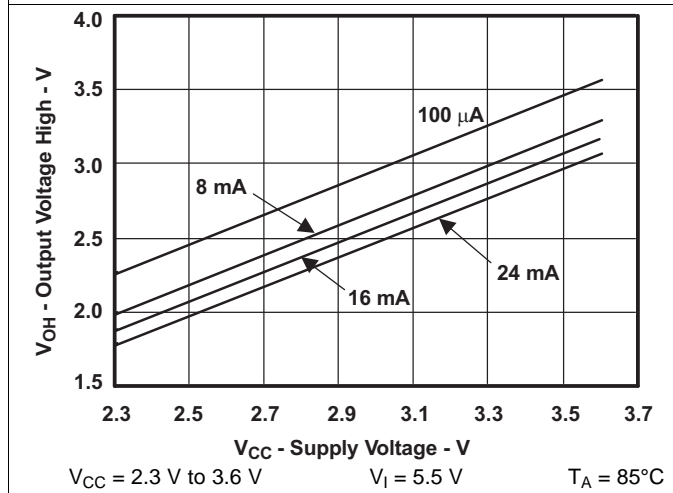


Figure 3. Output Voltage High vs Supply Voltage

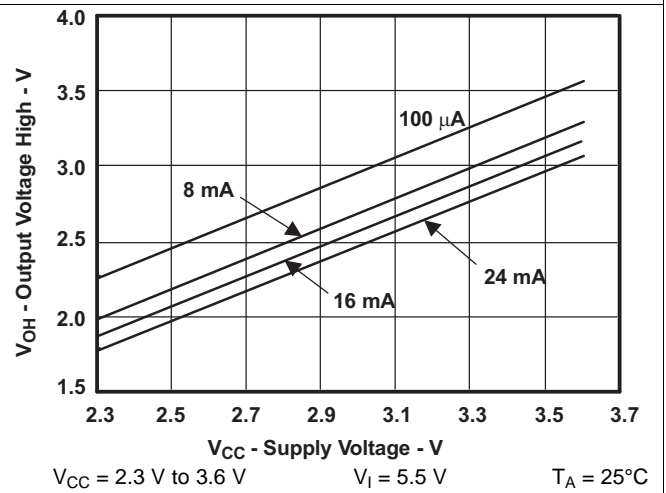


Figure 4. Output Voltage High vs Supply Voltage

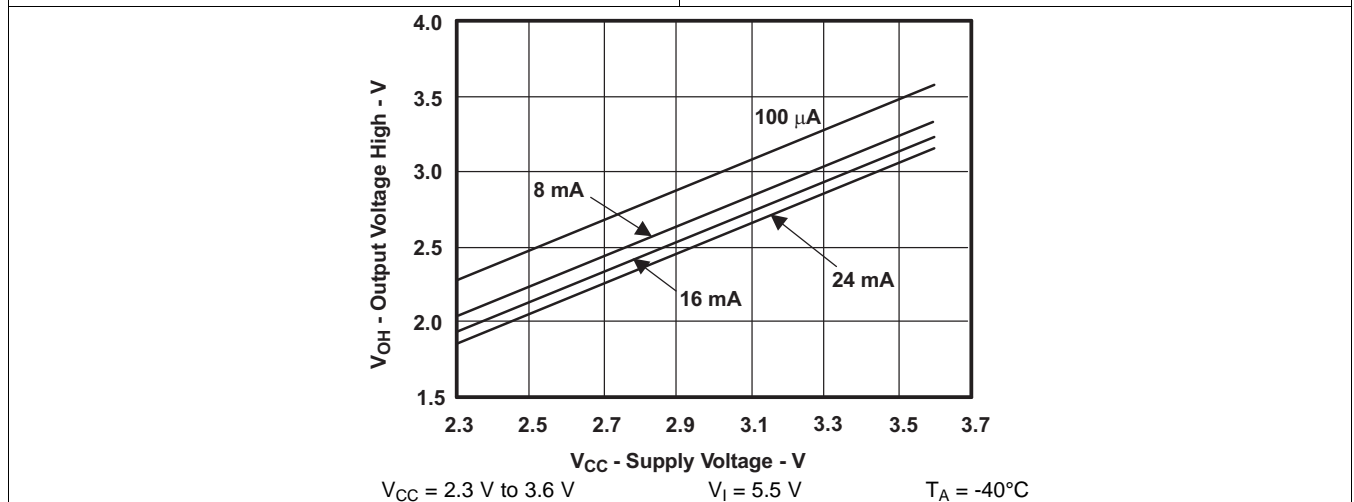
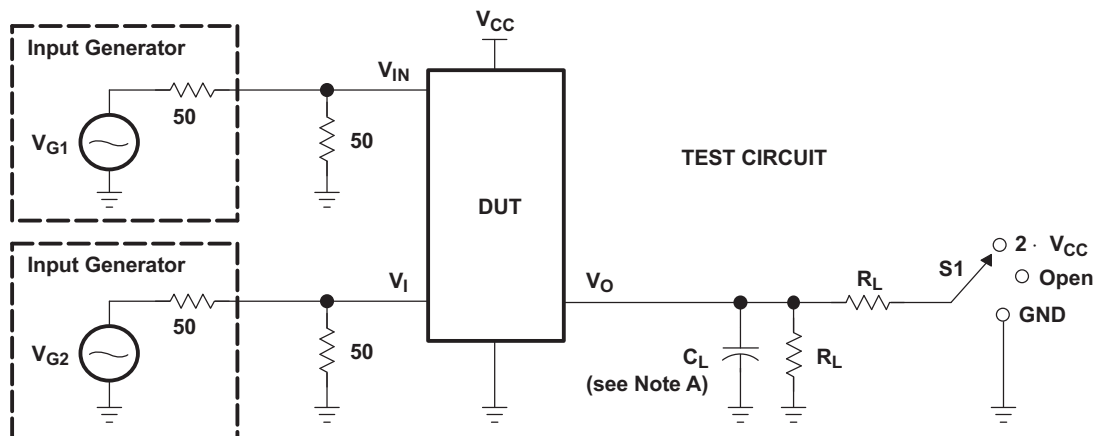
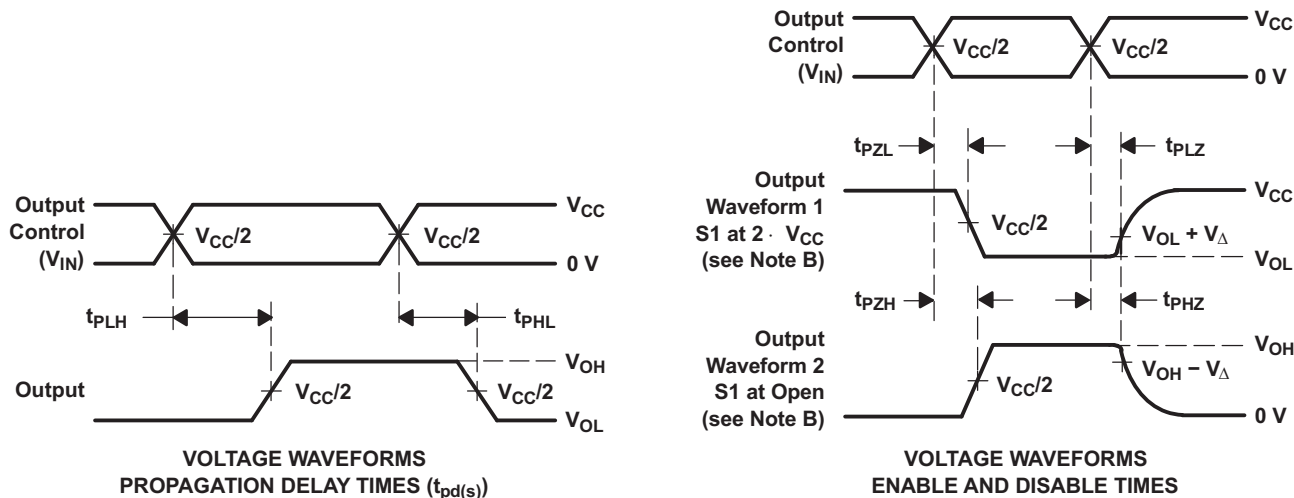


Figure 5. Output Voltage High vs Supply Voltage

## 7 Parameter Measurement Information



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V
t <sub>pd(s)</sub>	2.5 V ± 0.2 V	Open	500	3.6 V or GND	30 pF	
	3.3 V ± 0.3 V	Open	500	5.5 V or GND	50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	2.5 V ± 0.2 V	2 · V <sub>CC</sub>	500	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 · V <sub>CC</sub>	500	GND	50 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	2.5 V ± 0.2 V	Open	500	3.6 V	30 pF	0.15 V
	3.3 V ± 0.3 V	Open	500	5.5 V	50 pF	0.3 V



- NOTES:
- A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR = 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> = 2.5 ns, t<sub>f</sub> = 2.5 ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd(s)</sub>. The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - H. All parameters and waveforms are not applicable to all devices.

Figure 6. Test Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

The SN74CB3T3125 device is organized as four 1-bit bus switches with separate output-enable (1OE, 2OE, 3OE, and 4 OE) inputs. When OE is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is high, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports. This device is fully specified for partial-power-down applications using Ioff. The Ioff feature ensures that damaging current will not backflow through the device when it is powered down. The SN74CB3T3125 device has isolation during power off. To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 8.2 Functional Block Diagram

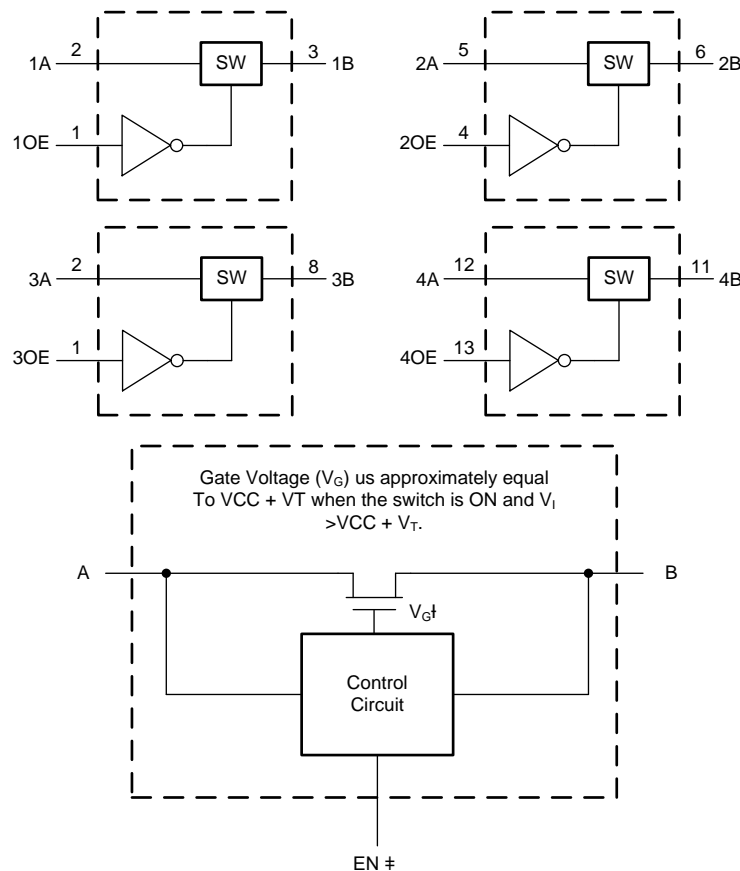


Figure 7. Simplified Schematic, Each FET Switch (SW)



### 8.3 Feature Description

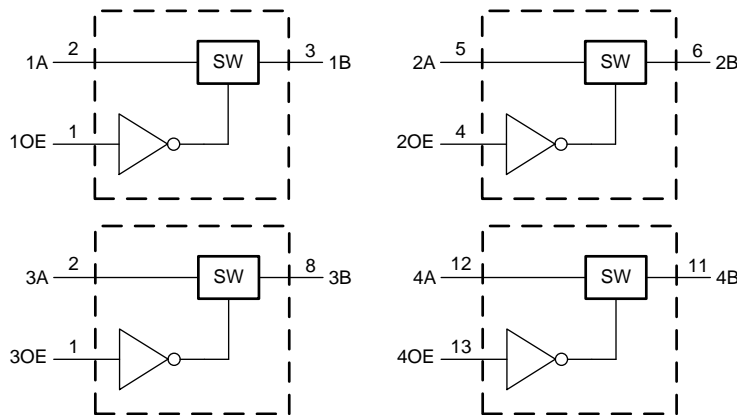
The SN74CB3T3125 is ideal for low-power portable equipment. Power consumption is low by design,  $I_{CC} = 20 \mu A$ , On-state resistance is low ( $r_{on} = 5 \Omega$ ) It has bidirectional data flow with near zero propagation delay. The device minimizes loading due to the low input/output capacitance  $C_{io(OFF)} = 4.5 \text{ pF}$  Typical. Operating VCC range from 2.3 V to 3.6 V. The output tracks VCC. Data and control inputs provide undershoot clamp diodes. Control inputs can be driven by TTL or 5-V/3.3-V CMOS outputs. It supports mixed-mode signal operation on all data I/O ports. Data I/Os support 0- to 5-V signaling levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V). The device is protected from damaging current, Ioff supports partial shutdown which prevents the current from flowing back through the device when it is powered down. In addition, it has 5-V tolerant I/Os with device powered up or powered down. The device is latch-up resistant with 250 mA exceeding the JESD 17 standard, providing protection from destruction due to latch-up. This device is protected against electrostatic discharge. It is tested per JESD 22 using 2000-V Human-Body Model (A114-B, Class II), and 1000-V Charged-Device Model (C101).

### 8.4 Device Functional Modes

Table 1 lists the functional modes for the SN74CB3T3125.

**Table 1. Function Table  
(Each Bus Switch)**

INPUT OE	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect



**Figure 8. Logic Diagram (Positive Logic)**

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

This application is specifically to connect a 5-V bus to a 3.3 V device. Ideally, set VCC to 3.3 V. It is assumed that communication in this particular application is one-directional, going from the bus controller to the device.

### 9.2 Typical Application

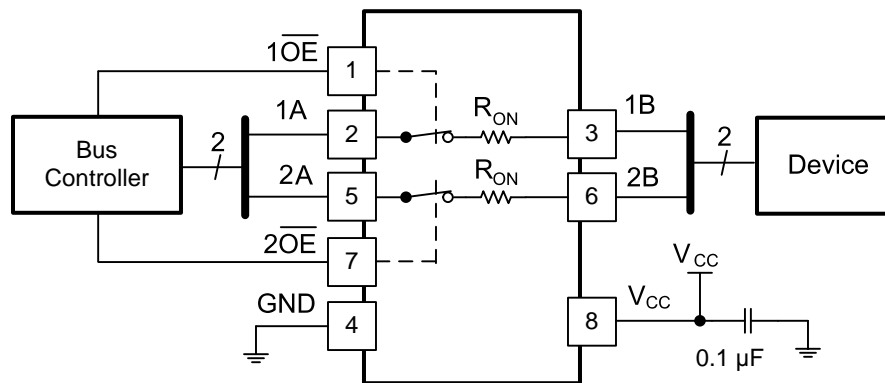


Figure 9. Application Circuit

#### 9.2.1 Design Requirements

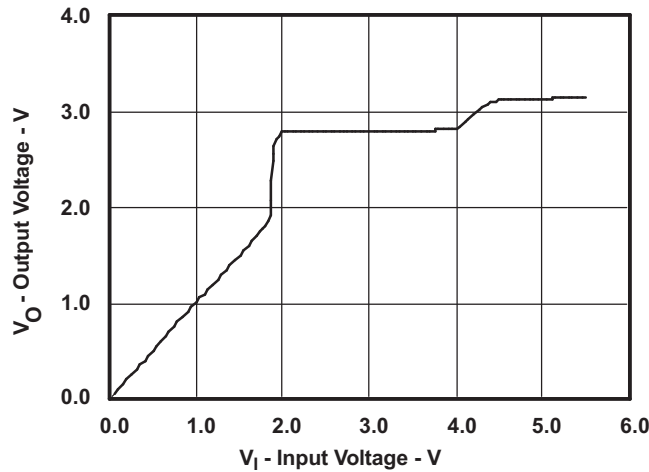
This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Because this design is for down-translating voltage, no pull-up resistors are required.

#### 9.2.2 Detailed Design Procedure

1. Recommended Input conditions – Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in *Recommended Operating Conditions* – Inputs are overvoltage tolerant allowing them to go as high as 7 V at any valid VCC.
2. Recommend output conditions – Load currents should not exceed 128 mA on each channel.

**Typical Application (continued)**

**9.2.3 Application Curves**



V<sub>CC</sub> = 3 V

I<sub>O</sub> = 1 μA

T<sub>A</sub> = 25°C

**Figure 10. Data Output Voltage vs Data Input Voltage**

**10 Power Supply Recommendations**

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Recommended Operating Conditions.

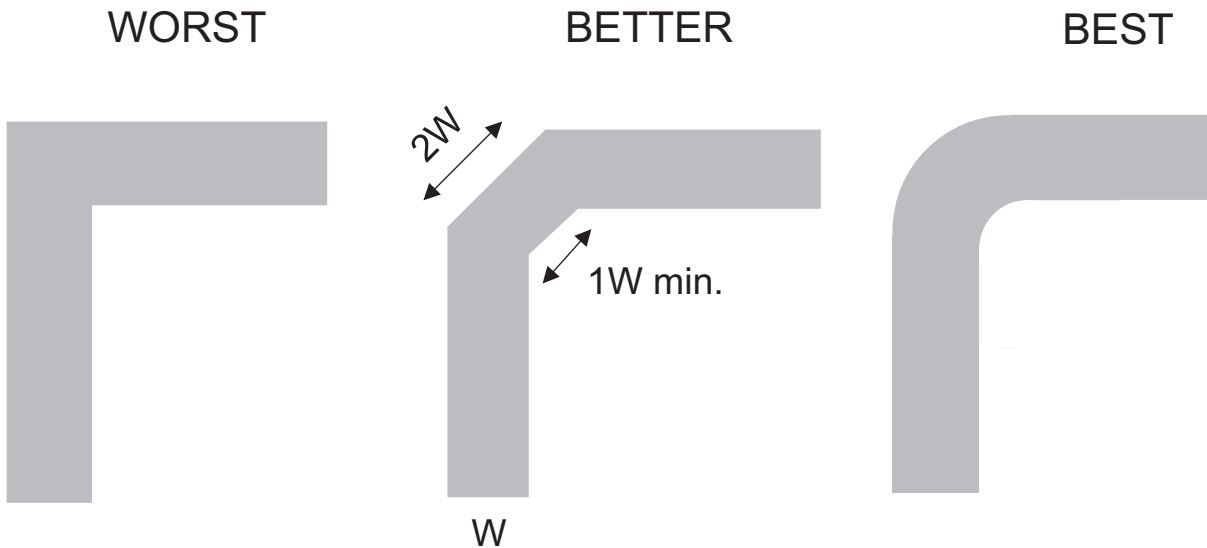
Each VCC terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled VCC, then a 0.01-μF or 0.022-μF capacitor is recommended for each VCC because the VCC pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example VCC and VDD, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 11 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

### 11.2 Layout Example



**Figure 11. Example Layout**

## 12 Device and Documentation Support

### 12.1 Device Support

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CB3T3125DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS125	<a href="#">Samples</a>
SN74CB3T3125PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS125	<a href="#">Samples</a>
SN74CB3T3125PWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS125	<a href="#">Samples</a>
SN74CB3T3125PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS125	<a href="#">Samples</a>
SN74CB3T3125PWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS125	<a href="#">Samples</a>
SN74CB3T3125RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	KS125	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T3125DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CB3T3125PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3T3125RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T3125DGVR	TVSOP	DGV	14	2000	367.0	367.0	35.0
SN74CB3T3125PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74CB3T3125RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

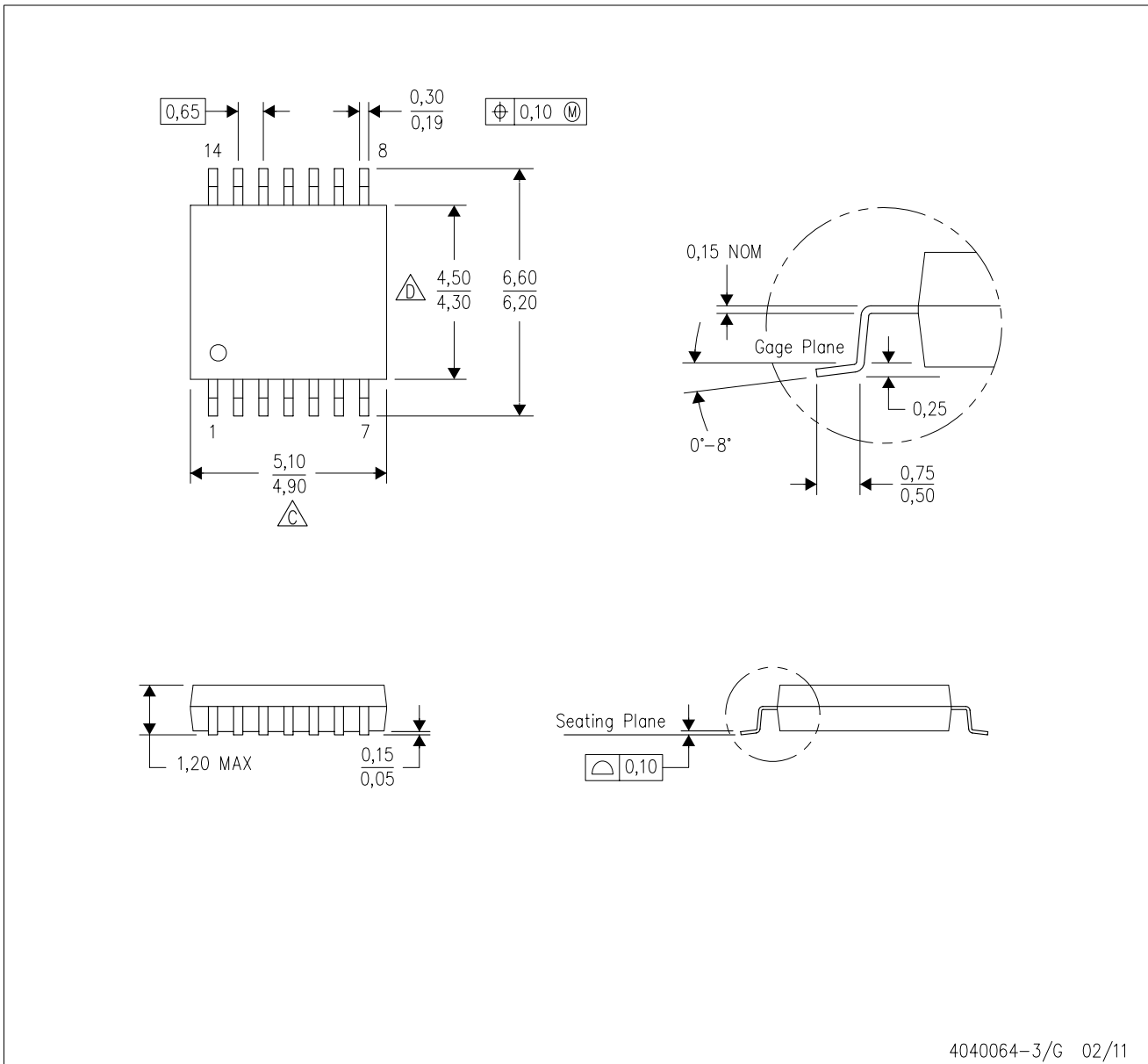


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



# MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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