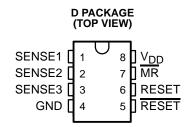
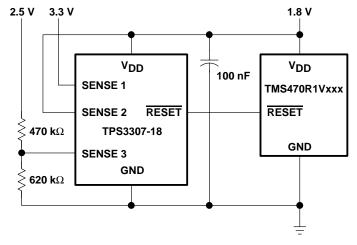
- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Triple Supervisory Circuits for DSP and Processor-Based Systems
- Power-On Reset Generator with Fixed Delay Time of 200 ms, No External Capacitor Needed

- Temperature-Compensated Voltage Reference
- Maximum Supply Current of 40 μA
- Supply Voltage Range . . . 2 V to 6 V
- Defined RESET Output from V_{DD} ≥ 1.1 V
- SO-8 Package
- Temperature Range . . . –40°C to 125°C



typical applications

Figure 1 lists some of the typical applications for the TPS3307 family, and a schematic diagram for a processor-based system application. This application uses TI part numbers TPS3307–18 and TMS470R1Vxxx.



- Automotive applications using DSPs, Microcontrollers or Microprocessors
- Industrial Equipment
- Programmable Controls
- Automotive Systems

Figure 1. Applications Using the TPS3307-18

description

The TPS3307-18 is a micropower supply voltage supervisor designed for circuit initialization primarily in automotive DSP and processor-based systems, which require more than one supply voltage.

The TPS3307-18 is designed for monitoring three independent supply voltages: 3.3 V/1.8 V/adj,. The adjustable SENSE input allows the monitoring of any supply voltage >1.25 V.

The various supply voltage supervisors are designed to monitor the nominal supply voltage as shown in the following supply voltage monitoring table.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



[†] Contact factory for details. Q100 qualification data available on request.

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description (continued)

SUPPLY VOLTAGE MONITORING

DEVICE	NOMINA	L SUPERVISED	VOLTAGE	THRESHOLD VOLTAGE (TYP)		
DEVICE	SENSE1	SENSE2	SENSE3	SENSE1	SENSE2	SENSE3
TPS3307-18	3.3 V	1.8 V	User defined	2.93 V	1.68 V	1.25 V [†]

[†]The actual sense voltage has to be adjusted by an external resistor divider according to the application requirements.

During power-on, \overline{RESET} is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors the SENSEn inputs and keeps \overline{RESET} active as long as SENSEn remain below the threshold voltage V_{IT+} .

An internal timer delays the return of the \overline{RESET} output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d\,typ}$ = 200 ms, starts after all SENSEn inputs have risen above the threshold voltage V_{IT+} . When the voltage at any SENSE input drops below the threshold voltage V_{IT-} , the \overline{RESET} output becomes active (low) again.

The TPS3307-18 incorporates a manual reset input, \overline{MR} . A low level at \overline{MR} causes \overline{RESET} to become active. In addition to the active-low \overline{RESET} output, the TPS3307-18 includes an active-high RESET output.

The device is available in a standard 8-pin SO package, and is characterized for operation over a temperature range of –40°C to 125°C.

ORDERING INFORMATION

TA	PACKA	GE‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	Small Outline (D)	Tape and Reel	TPS3307-18QDRQ1	30718Q

[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION/TRUTH TABLES

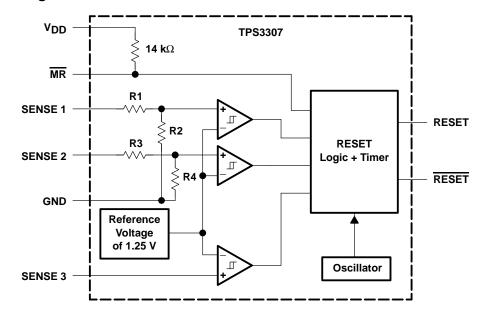
MR	SENSE1>VIT1	SENSE2>VIT2	SENSE3>VIT3	RESET	RESET
L	X	X	X	L	Н
Н	0	0	0	L	Н
Н	0	0	1	L	Н
Н	0	1	0	L	Н
Н	0	1	1	L	Н
Н	1	0	0	L	Н
Н	1	0	1	L	Н
Н	1	1	0	L	Н
Н	1	1	1	Н	L

X = Don't care

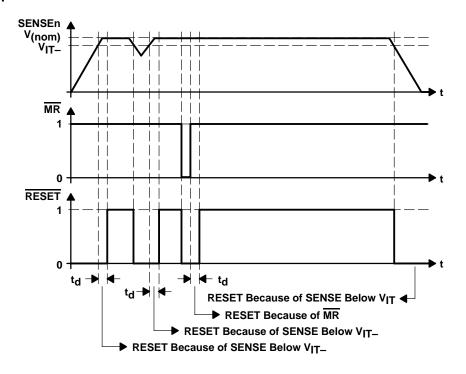
PowerPAD is a trademark of Texas Instruments Incorporated.



functional block diagram



timing diagram



TPS3307-18-Q1 TRIPLE PROCESSOR SUPERVISORS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{DD} (see Note1)	
All other pins (see Note 1)	
Maximum low output current, I _{OL}	5 mA
Maximum high output current, I _{OH}	
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD})	±20 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T _A	–40°C to 125°C
Storage temperature range, T _{stg}	–65°C to 150°C
Soldering temperature	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_{\mbox{A}} \le 25^{\circ}\mbox{C}$ POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V _{DD}	2	6	V
Input voltage at MR and SENSE3, V _I	0	V _{DD} +0.3	V
Input voltage at SENSE1 and SENSE2, VI	0	(V _{DD} +0.3)V _{IT} /1.25V	V
High-level input voltage at MR, VIH	0.7xV _{DD}		V
Low-level input voltage at MR, V _{IL}		0.3×V _{DD}	V
Input transition rise and fall rate at \overline{MR} , $\Delta t/\Delta V$		50	ns/V
Operating free-air temperature range, TA	-40	125	°C



NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t = 1000 h continuously.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CON	MIN	TYP	MAX	UNIT			
			$V_{DD} = 2 V \text{ to } 6 V$,	I _{OH} = -20 μA	V _{DD} - 0.2V				
Vон	VOH High-level output voltage		$V_{DD} = 3.3 V$,	$I_{OH} = -2 \text{ mA}$	V _{DD} - 0.4V			V	
			$V_{DD} = 6 V$,	$I_{OH} = -3 \text{ mA}$	V _{DD} - 0.4V				
			$V_{DD} = 2 V \text{ to } 6 V$,	$I_{OL} = 20 \mu A$			0.2		
VOL	Low-level output voltage		$V_{DD} = 3.3 \text{ V},$	$I_{OL} = 2 \text{ mA}$			0.4	V	
			V _{DD} = 6 V,	$I_{OL} = 3 \text{ mA}$			0.4		
	Power-up reset voltage (see Note 2)		$V_{DD} \ge 1.1 \text{ V},$	I _{OL} = 20 μA			0.4	V	
					1.2	1.25	1.29	V	
V _{IT} _	Negative-going input threshold voltage (see Note 3)	VSENSE2	$V_{DD} = 2 \text{ V to 6 V},$ $T_{A} = -40^{\circ}\text{C} \text{ to 125}$	50C	1.6	1.68	1.73	.,	
	(see Note 3)	VSENSE1	1A = -40 C 10 125	2.8	2.93	3.02	V		
			V _{IT} _ = 1.25 V		2	10	30		
V _{hys}	Hysteresis at VSENSEn input		V _{IT} _ = 1.68 V	2	15	40	mV		
			V _{IT} _ = 2.93 V		3	30	60		
		MR	$\overline{MR} = 0.7 \times V_{DD}$	V _{DD} = 6 V		-130	-180		
١.	18.1.1.1.1.	SENSE1	VSENSE1 = V _{DD}	= 6 V		5	8		
lн	High-level input current	SENSE2	VSENSE2 = V _{DD}	= 6 V		6	9	μΑ	
		SENSE3	VSENSE3 = V _{DD}		-1		1		
	I am land in an a summer	MR	$\overline{MR} = 0 \text{ V},$	V _{DD} = 6 V		-430	-600		
<u> </u>	IL Low-level input current		VSENSE1,2,3 = 0	V	-1		1	μΑ	
I _{DD}	Supply current						40	μΑ	
Ci	Input capacitance		$V_I = 0 V \text{ to } V_{DD}$			10	_	pF	

NOTES: 2. The lowest supply voltage at which RESET becomes active. t_r, V_{DD} ≥ 15 μs/V
 3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1 μF) should be placed close to the supply terminals.

TPS3307-18-Q1 TRIPLE PROCESSOR SUPERVISORS

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timing requirements at $\rm V_{DD}$ = 2 V to 6 V, $\rm R_{L}$ = 1 M $\Omega,\, C_{L}$ = 50 pF, $\rm T_{A}$ = 25°C

	PARAMETER TEST CONDITIONS				MIN	TYP	MAX	UNIT
	Pulse width	SENSEn	VSENSEnL = VIT0.2 V,	VSENSEnH = VIT+ +0.2 V	6	10		μs
١W	Puise width	MR	$V_{IH} = 0.7 \times V_{DD}$	$V_{IL} = 0.3 \times V_{DD}$	100	150		ns

switching characteristics at V_DD = 2 V to 6 V, R_L = 1 M Ω , C_L = 50 pF, T_A = 25°C

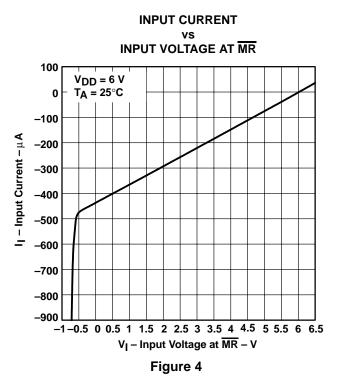
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t _d	Delay time		$\frac{VI(SENSEn)}{MR} \ge V_{IT+} + 0.2 \text{ V},$ $\frac{VI(SENSEn)}{MR} \ge 0.7 \times V_{DD}, \text{ See timing diagram}$	140	200	280	ms
tPHL	Propagation (delay) time, high-to-low level output	MR to RESET MR to RESET	VI(SENSEn) ≥ VIT+ +0.2 V,		000	000	
^t PLH	Propagation (delay) time, low-to-high level output	MR to RESET MR to RESET	$V_{IH} = 0.7 \times V_{DD}, V_{IL} = 0.3 \times V_{DD}$	200		600	ns
^t PHL	Propagation (delay) time, high-to-low level output	SENSEn to RESET	V _{IH} = V _{IT+} +0.2 V, V _{IL} = V _{IT-} -0.2 V,			_	
^t PLH	Propagation (delay) time, low-to-high level output	SENSEn to RESET	$\overline{MR} \ge 0.7 \times V_{DD}$		1	5	μs

TYPICAL CHARACTERISTICS

NORMALIZED SENSE THRESHOLD VOLTAGE FREE-AIR TEMPERATURE AT V_{DD} Normalized Input Threshold Voltage – VIT(TA), VIT(25 $^\circ$ C) 1.005 <u>V_{DD}</u> = 2 V MR = Open 1.004 1.003 1.002 1.001 0.999 0.998 0.997 0.996 0.995 -40 -15 60 85

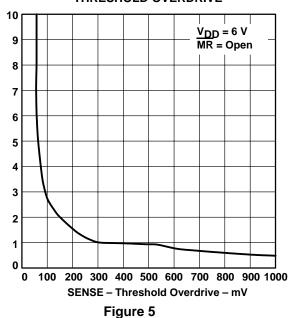
Figure 2

T_A - Free-Air Temperature - °C



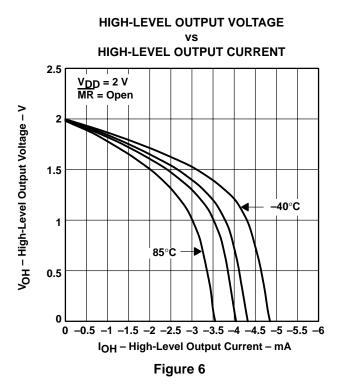
SUPPLY CURRENT SUPPLY VOLTAGE 18 16 14 12 TPS3307-33 I_{DD} – Supply Current – μA 10 8 6 2 0 SENSEn = V_{DD} -6 MR = Open -8 T_A = 25°C -0.5 0 0.5 1 1.5 2 2.5 3 3.5 4 4.5 5 5.5 6 6.5 7 V_{DD} - Supply Voltage - V Figure 3

MINIMUM PULSE DURATION AT SENSE vs THRESHOLD OVERDRIVE

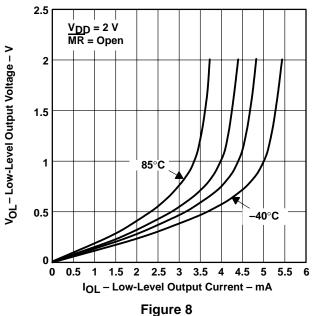


 t_{W} – Minimum Pulse Duration at V_{Sense} – μ s

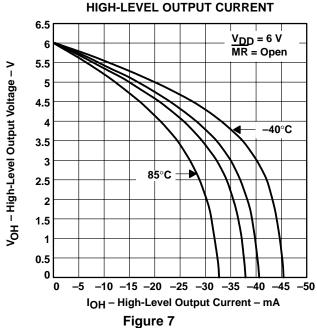
TYPICAL CHARACTERISTICS



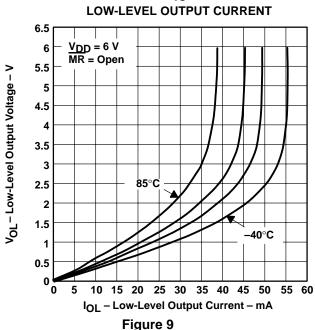




HIGH-LEVEL OUTPUT VOLTAGE



LOW-LEVEL OUTPUT VOLTAGE VS LOW-LEVEL OUTPUT CURRENT

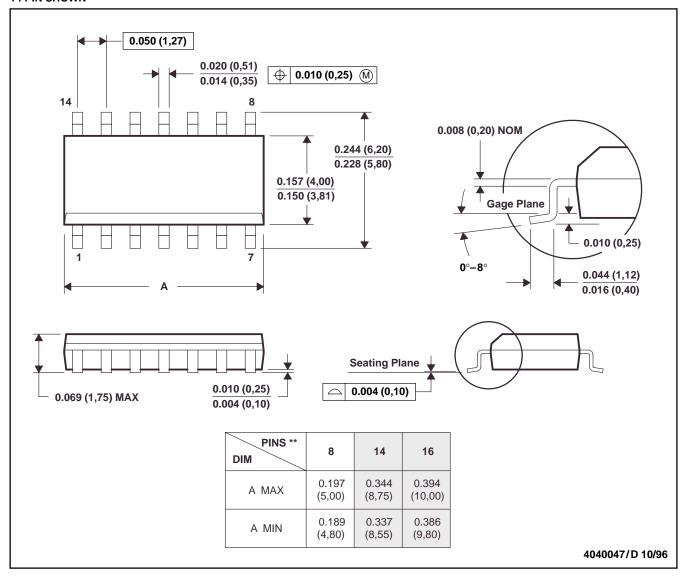


MECHANICAL DATA

D (R-PDSO-G**)

14 PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-012



PACKAGE OPTION ADDENDUM

25-Feb-2005

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Pa	ckage Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS3307-18QDRQ1	ACTIVE	SOIC	D	8 2	2500	None	CU NIPDAU	Level-1-220C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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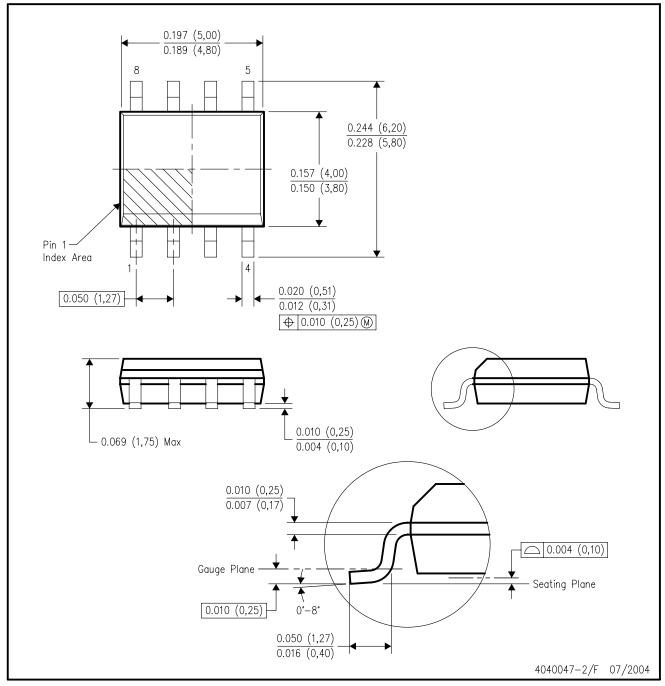
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



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- D. Falls within JEDEC MS-012 variation AA.



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