TEXAS INSTRUMENTS
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TPS79901, TPS79915, TPS79918 TPS79925, TPS79928, TPS799285 TPS79929, TPS79930, TPS79933

SBVS056A – JANUARY 2005 – REVISED FEBRUARY 2005

200mA Low Quiescent Current, Ultra-Low Noise, High PSRR, Low Dropout Linear Regulator

FEATURES

- **200mA Low Dropout Regulator with EN**
- **Low I_Q: 40µA**
- **Available in 1.5V, 1.8V, 2.5V, 2.8V, 2.85V, 2.9V, 3.0V, 3.3V, and Adjustable (1.2V to 6.5V) Versions**
- **High PSRR: 66dB at 1kHz**
- **Ultra-low Noise: 29.5µV_{RMS}**
- **Fast Start-Up Time: 45µs**
- **Stable with a 2.0µF Ceramic Output Capacitance**
- **Excellent Load/Line Transient Response**
- **2% Overall Accuracy (Load/Line/Temp)**
- **Very Low Dropout: 100mV**
- **Small ThinSOT-23 and WCSP (Available June 2005) Packages**

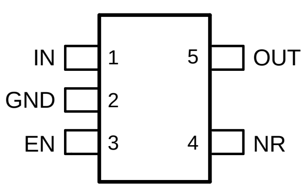
APPLICATIONS

- **Cellular Phones**
- **Wireless LAN, Bluetooth™**
- **VCOs, RF**
- **Handheld Organizers, PDAs**

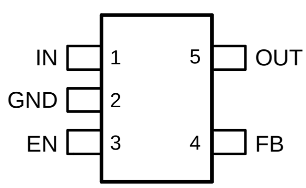
DESCRIPTION

The TPS799xx family of low-dropout (LDO) low-power linear regulators offer excellent AC performance with very low ground current. High power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient response are provided while consuming a very low 40µA (typical) ground current. The TPS799xx is stable with ceramic capacitors and uses an advanced BiCMOS fabrication process to yield dropout voltage typically 110mV at 200mA output. The TPS799xx uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% over all load, line, process, and temperature variations. It is fully specified from T_J = -40°C to +125°C and is offered in low profile ThinSOT23 and Wafer Chip-Scale packages, ideal for wireless handsets and WLAN cards.

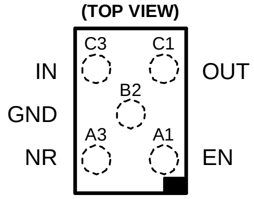
TPS799xxDDC
TSOT23−5
(TOP VIEW)



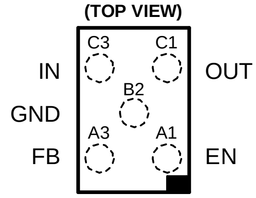
TPS79901DDC
TSOT23−5
(TOP VIEW)

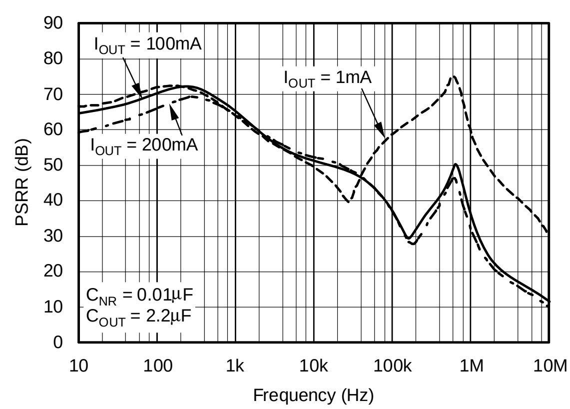


TPS799xxYZU
WCSP PACKAGE
(TOP VIEW)



TPS79901YZU
WCSP PACKAGE
(TOP VIEW)





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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT} (2)
TPS799**xx*yyy****z***	**XX** is nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, 01 = Adjustable). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Output voltages from 1.2V to 4.8V in 50mV increments are available; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS

Over operating temperature range (unless otherwise noted)(1)

PARAMETER	TPS799xx	UNIT
V_{IN} range	-0.3 to +7.0	V
V_{EN} range	-0.3 to V_{IN} +0.3	V
V_{OUT} range	-0.3 to V_{IN} +0.3	V
Peak output current	Internally limited	
Continuous total power dissipation	See Dissipation Ratings Table	
Junction temperature range, T_J	-55 to +150	°C
Storage junction temperature range , T_{STG}	-55 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	T_A < 25°C	T_A = 70°C	T_A = 85°C
Low-K(1)	DDC	90°C/W	280°C	3.6mW/°C	360mW	200mW	145mW
High-K(2)	DDC	90°C/W	200°C	5.0mW/°C	500mW	275mW	200mW
Low-K(1)	YZU	27°C/W	255°C	3.9mW/°C	390mW	215mW	155mW
High-K(2)	YZU	27°C/W	190°C	5.3mW/°C	530mW	295mW	215mW

(1) The JEDEC low-K (1s) board used to derive this data was a 3in x 3in, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3in x 3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = – 40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3V or 2.7V, whichever is greater; I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{OUT} = 2.2µF, C_{NR} = 0.01µF, unless otherwise noted. For TPS79901, V_{OUT} = 3.0V.
Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			2.7		6.5	V
V_{FB}	Internal reference (TPS79901)			1.169	1.193	1.217	V
V_{OUT}	Output voltage range (TPS79901)			V_{FB}		6.5-V_{DO}	V
V_{OUT}	Output accuracy	Nominal	T_J = +25°C	-1.0		+1.0	%
V_{OUT}	Output accuracy(1)	Over V_{IN}, I_{OUT}, Temp	V_{OUT} + 0.3V ≤ V_{IN} ≤ 6.5V 500µA ≤ I_{OUT} ≤ 200mA	-2.0	±1.0	+2.0	%
ΔV_{OUT}%/ ΔV_{IN}	Line regulation(1)		$V_{OUT(NOM)}$ + 0.3V ≤ V_{IN}≤ 6.5V		0.02		%/V
ΔV_{OUT}%/ ΔI_{OUT}	Load regulation		500µA ≤ I_{OUT}≤ 200mA		0.002		%/mA
V_{DO}	Dropout voltage(2) (V_{IN} = $V_{OUT(NOM)}$ - 0.1V)	V_{OUT} < 3.3V	I_{OUT} = 200mA		100	175	mV
V_{DO}	Dropout voltage (V_{IN} = $V_{OUT(NOM)}$ - 0.1V)	V_{OUT}≥ 3.3V	I_{OUT} = 200mA		90	160	mV
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(NOM)}$	200	400	600	mA
I_{GND}	Ground pin current		500µA ≤ I_{OUT} ≤ 200mA		40	60	µA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4V, 2.7V ≤ V_{IN} ≤ 6.5V		0.15	1.0	µA
I_{FB}	Feedback pin current (TPS79901)			-0.5		0.5	µA
PSRR	Power-supply rejection ratio V_{IN} = 3.85V, V_{OUT} = 2.85V, C_{NR} = 0.01µF, I_{OUT} = 100mA		f = 100Hz		70		dB
			f = 1kHz		66		dB
			f = 10kHz		51		dB
			f = 100kHz		38		dB
V_N	Output noise voltage BW = 10Hz – 100kHz, V_{OUT} = 2.8V		C_{NR} = 0.01µF		29.5		µV_{RMS}
			C_{NR} = none		263		µV_{RMS}
T_{STR}	Startup time V_{OUT} = 2.85V, R_L = 14Ω, C_{OUT} = 2.2µF		C_{NR} = 0.001µF		45		µs
			C_{NR} = 0.047µF		45		µs
			C_{NR} = 0.01µF		50		µs
			C_{NR} = none		50		µs
$V_{EN(HI)}$	Enable high (enabled)			1.2		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)			0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled		V_{EN} = V_{IN} = 6.5V		0.03	1.0	µA
TSD	Thermal shutdown temperature		Shutdown, temperature increasing		165		°C
			Reset, temperature decreasing		145		°C
T_J	Operating junction temperature			-40		+125	°C
UVLO	Under voltage lockout		V_{IN} rising	1.90	2.20	2.50	V
	Hysteresis		V_{IN} falling		70		mV

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.7V, whichever is greater.
(2) V_{DO} is not measured for devices with $V_{OUT(NOM)}$ < 2.8V because minimum V_{IN} = 2.7V.

DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAMS

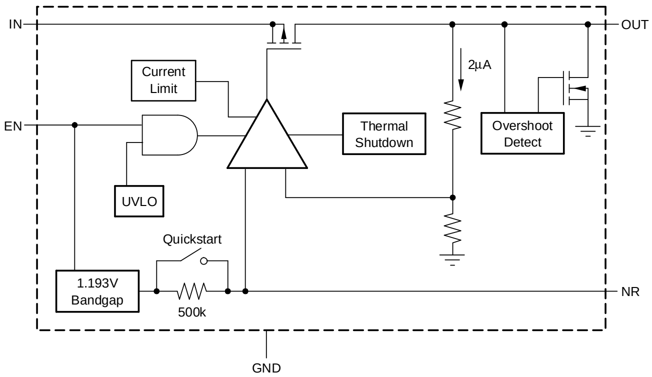


Figure 1. Fixed Voltage Versions

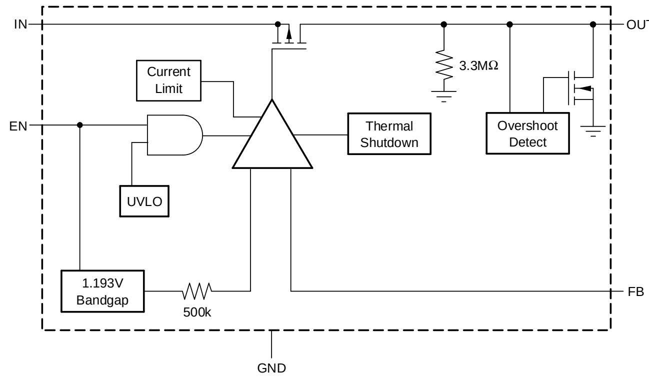


Figure 2. Adjustable Voltage Versions

Table 1. PIN DESCRIPTIONS

TPS799xx			DESCRIPTION
NAME	DDC	YZU	
IN	1	C3	Unregulated input supply.
GND	2	B2	Ground
EN	3	A1	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
NR	4	A3	Fixed voltage versions only; connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This allows output noise to be reduced to very low levels.
FB	4	A3	Adjustable version only; this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	5	C1	Output of the regulator. A small capacitor (total typical capacitance ≥ 2.0µF ceramic) is needed from this pin to ground to assure stability.

TYPICAL CHARACTERISTICS

Over operating temperature range (T_J=- 40°C to +125°C), V_{IN}=$V_{OUT(TYP)}$ + 0.3V or 2.7V, whichever is greater; I_{OUT}=1mA, V_{EN} = V_{IN}, C_{OUT}=2.2µF, C_{NR}=0.01µF, unless otherwise noted. For TPS79901, V_{OUT}=3.0V. Typical values are at T_J=+25°C.

LOAD REGULATION

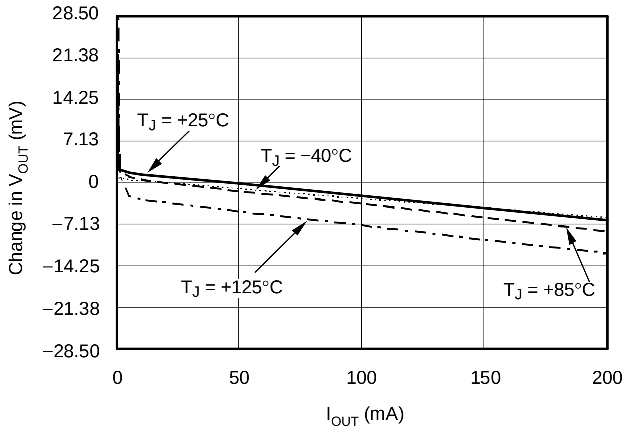


Figure 3.

LINE REGULATION

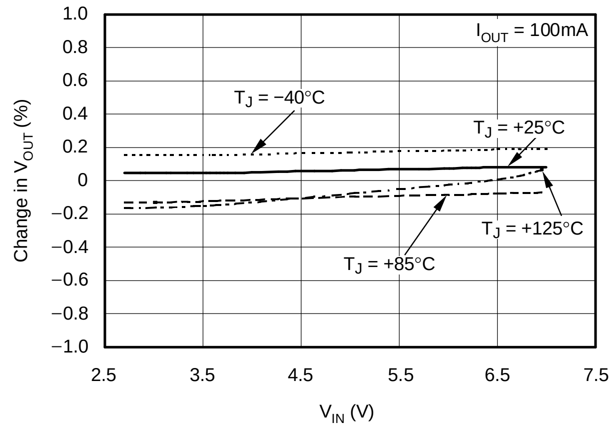


Figure 4.

OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

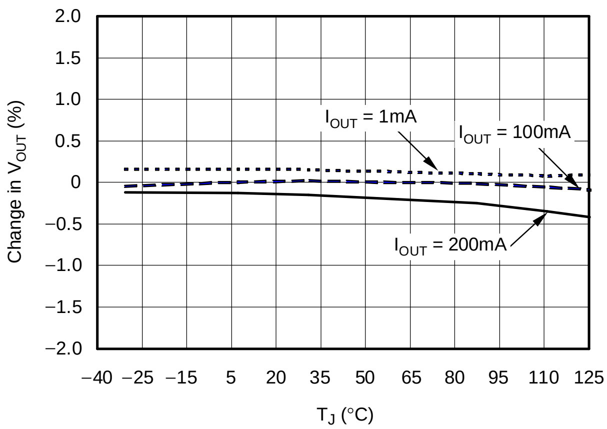


Figure 5.

TPS799285 DROPOUT VOLTAGE vs OUTPUT CURRENT

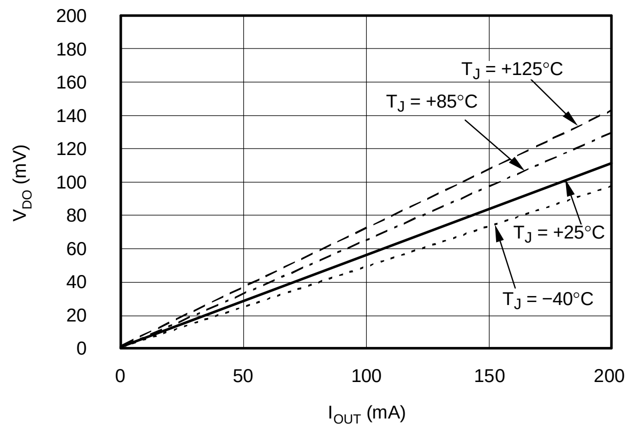


Figure 6.

TPS799285 DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

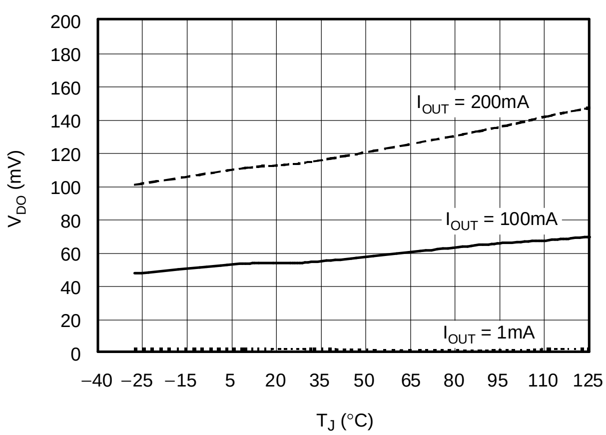


Figure 7.

TPS79901 DROPOUT vs INPUT VOLTAGE

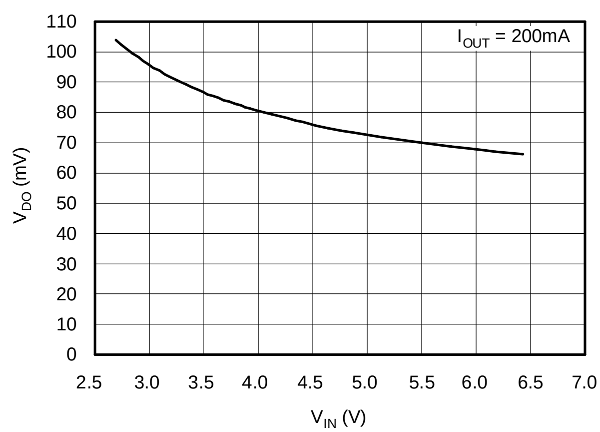


Figure 8.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J=- 40°C to +125°C), V_{IN}=$V_{OUT(TYP)}$ + 0.3V or 2.7V, whichever is greater; I_{OUT}=1mA, V_{EN} = V_{IN}, C_{OUT}=2.2µF, C_{NR}=0.01µF, unless otherwise noted. For TPS79901, V_{OUT}=3.0V. Typical values are at T_J=+25°C.

GROUND PIN CURRENT vs INPUT VOLTAGE

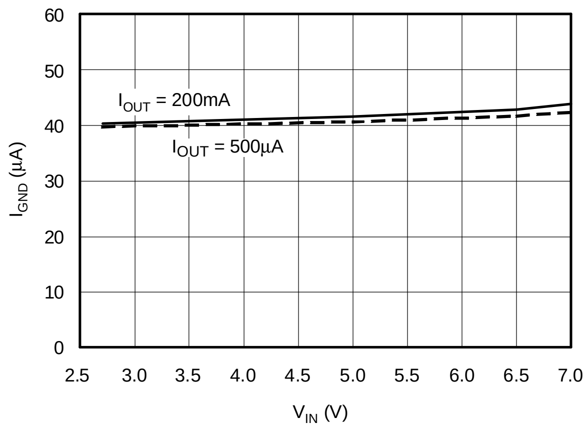


Figure 9.

TPS799285 GROUND PIN CURRENT vs JUNCTION TEMPERATURE

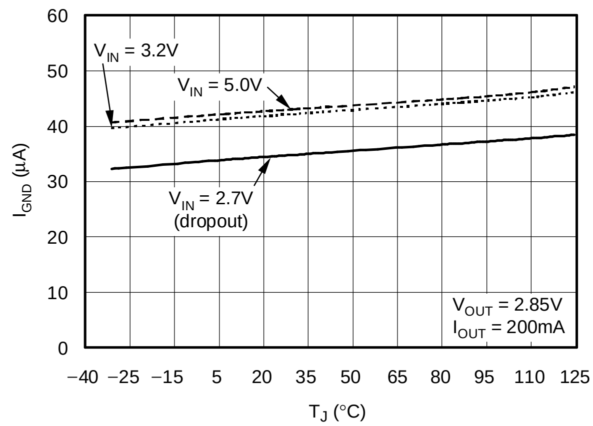


Figure 10.

GROUND PIN CURRENT (DISABLED) vs JUNCTION TEMPERATURE

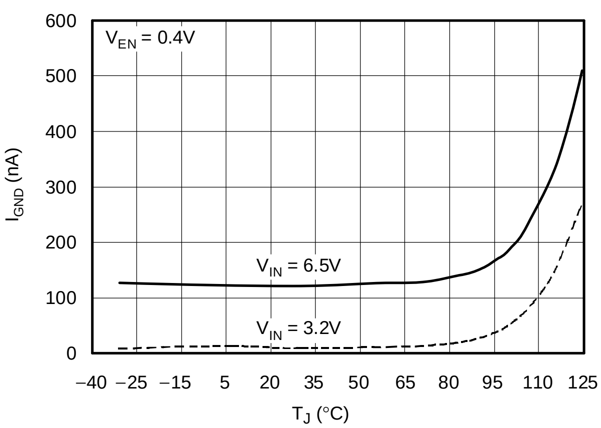


Figure 11.

TPS799285 POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN}- V_{OUT} = 1.0V)

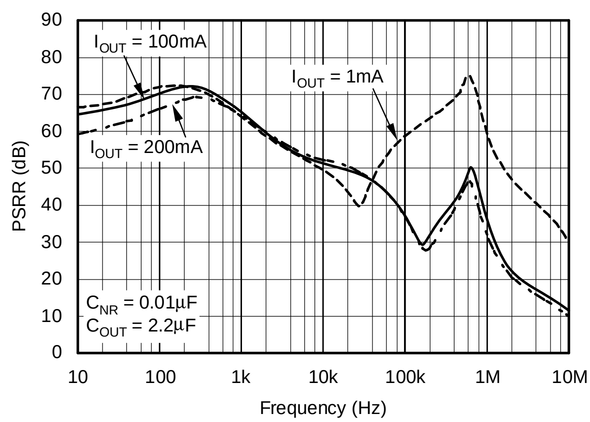


Figure 12.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J=- 40°C to +125°C), V_{IN}=$V_{OUT(TYP)}$ + 0.3V or 2.7V, whichever is greater; I_{OUT}=1mA, V_{EN} = V_{IN}, C_{OUT}=2.2µF, C_{NR}=0.01µF, unless otherwise noted. For TPS79901, V_{OUT}=3.0V. Typical values are at T_J=+25°C.

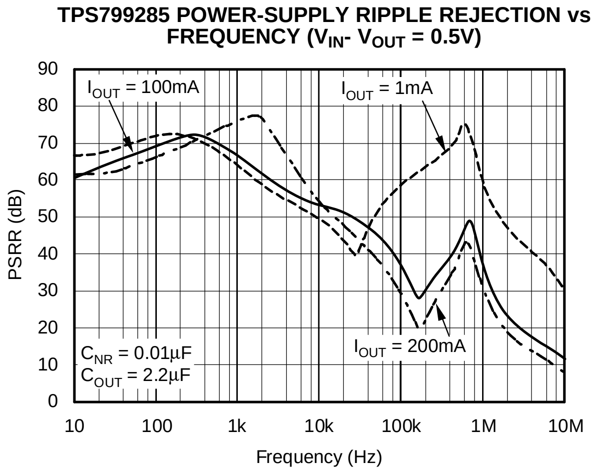


Figure 13.

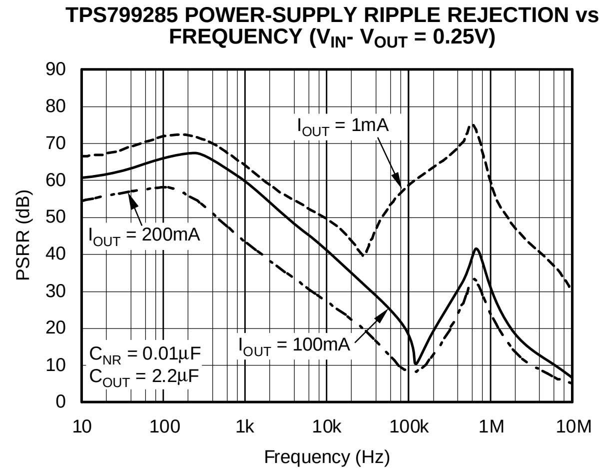


Figure 14.

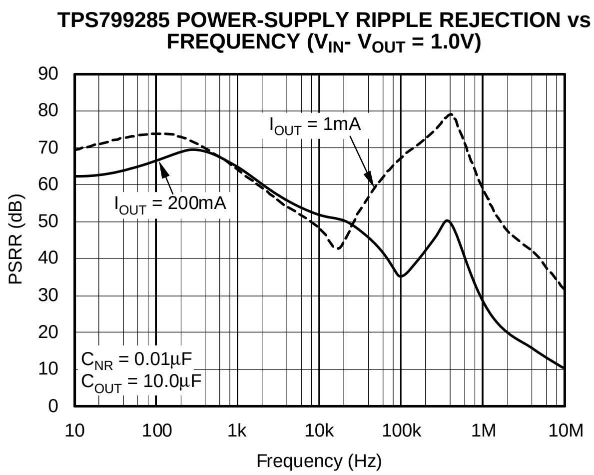


Figure 15.

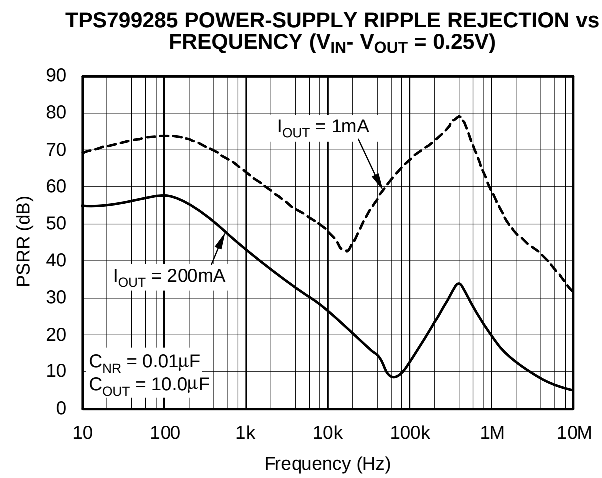


Figure 16.

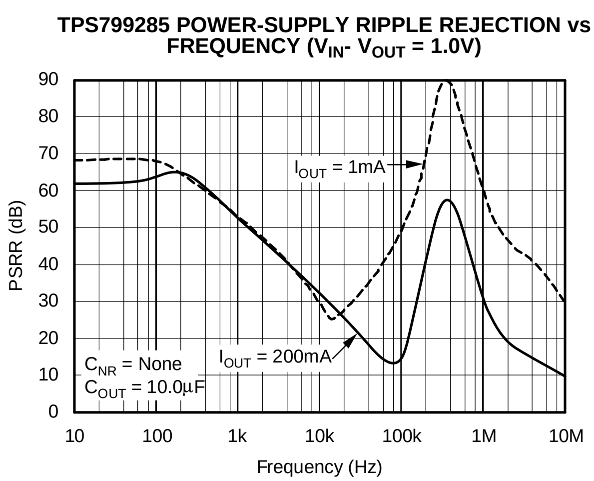


Figure 17.

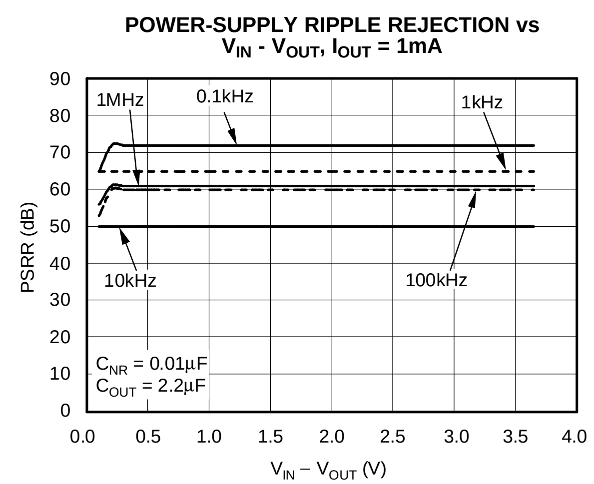


Figure 18.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J=- 40°C to +125°C), V_{IN}=$V_{OUT(TYP)}$ + 0.3V or 2.7V, whichever is greater; I_{OUT}=1mA, V_{EN} = V_{IN}, C_{OUT}=2.2µF, C_{NR}=0.01µF, unless otherwise noted. For TPS79901, V_{OUT}=3.0V. Typical values are at T_J=+25°C.

POWER-SUPPLY RIPPLE REJECTION vs V_{IN} - V_{OUT}, I_{OUT} = 100mA

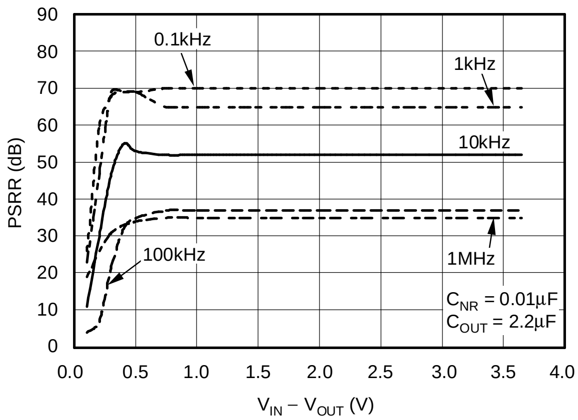


Figure 19.

POWER-SUPPLY RIPPLE REJECTION vs V_{IN}- V_{OUT}, I_{OUT} = 200mA

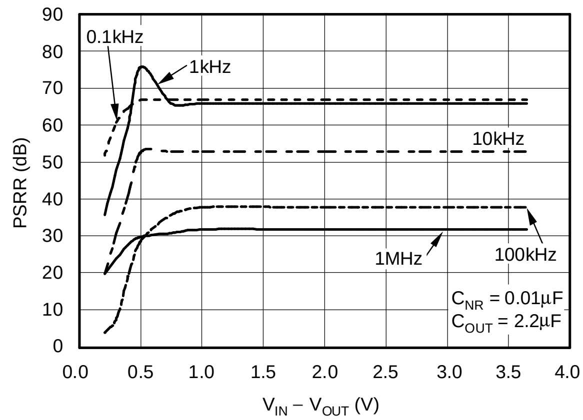


Figure 20.

**TPS799285
TOTAL NOISE vs C_{NR}**

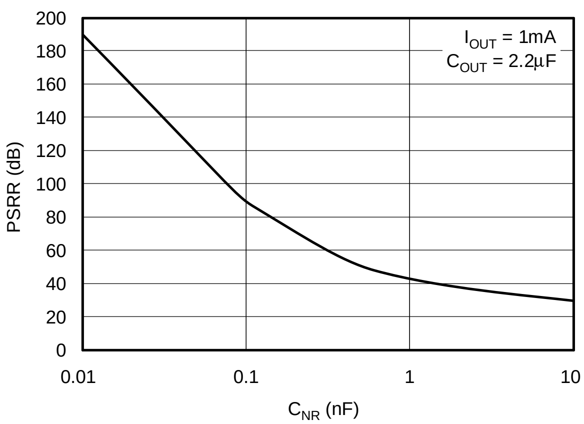


Figure 21.

**TPS799285
TOTAL NOISE vs C_{OUT}**

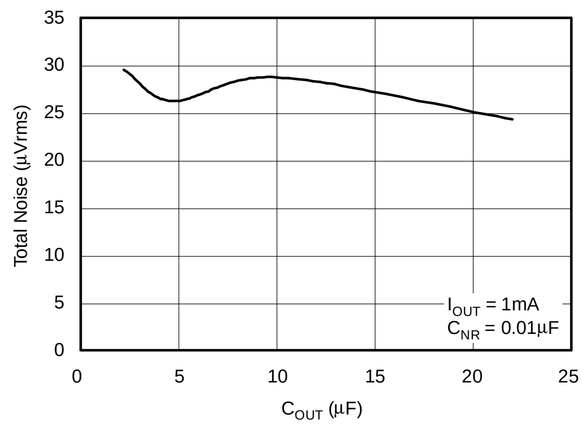


Figure 22.

**TPS799285
LINE TRANSIENT RESPONSE**

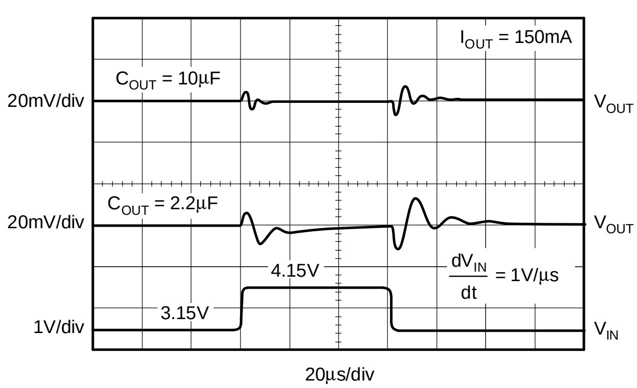


Figure 23.

**TPS799285
LOAD TRANSIENT RESPONSE**

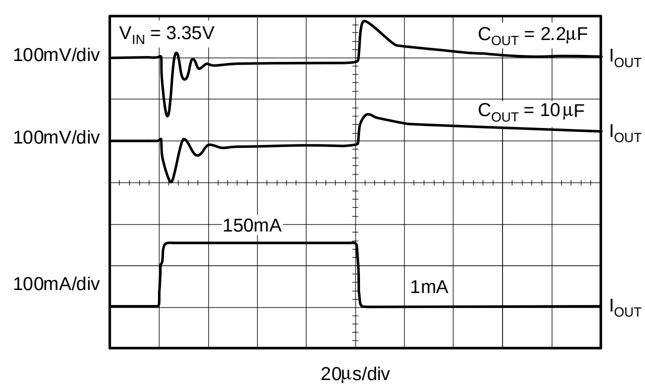


Figure 24.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J=- 40°C to +125°C), V_{IN}=$V_{OUT(TYP)}$ + 0.3V or 2.7V, whichever is greater; I_{OUT}=1mA, V_{EN} = V_{IN}, C_{OUT}=2.2µF, C_{NR}=0.01µF, unless otherwise noted. For TPS79901, V_{OUT}=3.0V. Typical values are at T_J=+25°C.

TPS799285
TURN-ON RESPONSE (V_{EN} = V_{IN})

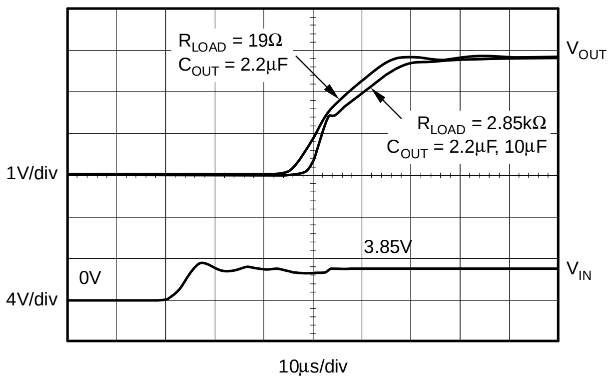


Figure 25.

TPS799285
ENABLE RESPONSE

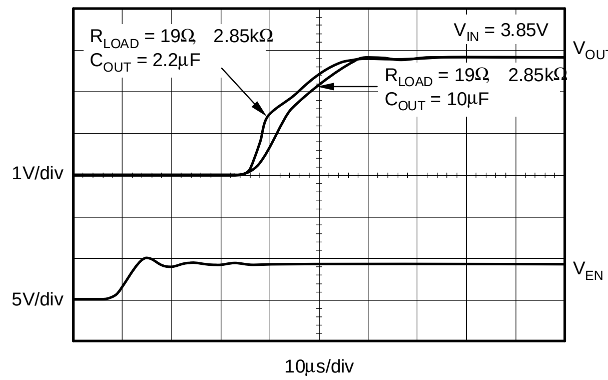


Figure 26.

TPS799285
POWER-UP / POWER-DOWN

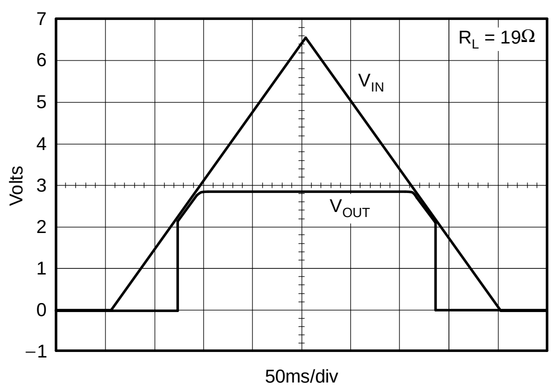


Figure 27.

APPLICATION INFORMATION

The TPS799xx family of LDO regulators combines the high performance required of many RF and precision analog applications with ultra-low current consumption. High PSRR is provided by a high gain, high bandwidth error loop with good supply rejection at very low headroom (V_{IN} – V_{OUT}). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the bandgap reference and to improve PSRR while a quick-start circuit fast-charges this capacitor at startup for quick startup times. The combination of high performance and low ground current also make the TPS799xx an excellent choice for portable applications. All versions have thermal and over-current protection and are fully specified from –40°C to +125°C.

Figure 28 shows the basic circuit connections for fixed voltage models. Figure 29 gives the connections for the adjustable output version (TPS79901). R_1 and R_2 can be calculated for any output voltage using the formula in Figure 29. Sample resistor values for common output voltages are shown in Figure 29.

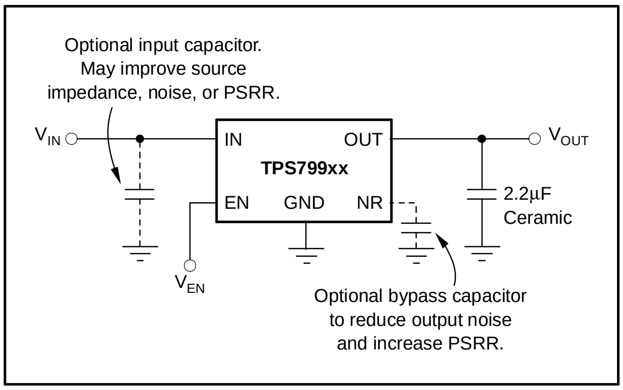


Figure 28. Typical Application Circuit for Fixed Voltage Versions

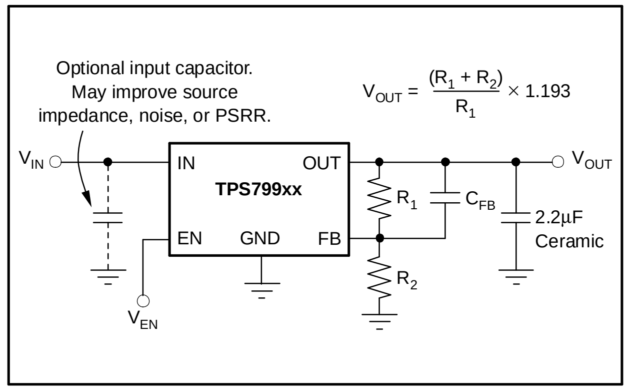


Figure 29. Typical Application Circuit for Adjustable Voltage Version

Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 1µF low ESR capacitor across the input supply near the regulator. This will counteract reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1µF input capacitor may be necessary to ensure stability.

The TPS799xx is designed to be stable with standard ceramic capacitors of values 2.2µF or larger. X5R and X7R type capacitors are best as they have minimal variation in value and ESR over temperature. Maximum ESR should be < 1.0Ω.

Feedback Capacitor Requirements (TPS79901 only)

The feedback capacitor, C_{FB}, shown in Figure 29 is required for stability. For a parallel combination of R_1 and R_2 equal to 250kΩ, any value from 3pF to 1nF can be used. Fixed voltage versions have an internal 30pF feedback capacitor which is quick-charged at start-up. The adjustable version does not have this quick-charge circuit, so values below 5pF should be used to ensure fast startup; values above 47pF can be used to implement an output voltage soft-start. Larger value capacitors also improve noise slightly. The TPS79901 is stable in unity-gain configuration (OUT tied to FB) without C_{FB}.

Output Noise

In most LDOs, the bandgap is the dominant noise source. If a noise reduction capacitor (C_{NR}) is used with the TPS799xx, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01µF noise reduction capacitor; for the adjustable version, use smaller value resistors in the output resistor divider. A parallel combination that gives 2µA of divider current will have the same noise performance as a fixed voltage version. To further optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2Ω. This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

Noise can be referred to the feedback point (FB pin) such that with C_{NR} = 0.01µF total noise is approximately given by Equation 1:

$$V_N = \frac{10.7\mu V_{RMS}}{V} \times V_{OUT} \quad (1)$$

The TPS79901 adjustable version does not have the noise-reduction pin available, so ultra-low noise operation is not possible. Noise can be minimized according to the above recommendations.

Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Internal Current Limit

The TPS799xx internal current limit helps protect the regulator during fault conditions. During current limit, the output will source a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in current limit for extended periods of time.

The PMOS pass element in the TPS799xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

Dropout Voltage

The TPS799xx uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS,ON}$ of the PMOS pass element. Because the PMOS device behaves like a resistor in dropout, V_{DO} will approximately scale with output current.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 18 through Figure 20 in the ***Typical Characteristics*** section.

Startup

Fixed voltage versions of the TPS799xx use a quick-start circuit to fast-charge the noise reduction capacitor, C_{NR}, if present (see *Functional Block Diagrams*, Figure 1). This allows the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate in this configuration.

Note that for fastest startup, V_{IN} should be applied first, then the enable pin (EN) driven high. If EN is tied to IN, startup will be somewhat slower. Refer to Figure 25 and Figure 26 in the ***Typical Characteristics*** section. The quick-start switch is closed for approximately 135µs. To ensure that C_{NR} is fully charged during the quick-start time, a 0.01µF or smaller capacitor should be used.

Transient Response

As with any regulator, increasing the size of the output capacitor will reduce over/undershoot magnitude but increase duration of the transient response. In the adjustable version, adding C_{FB} between OUT and FB will improve stability and transient response. The transient response of the TPS799xx is enhanced by an active pull-down that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pull-down device behaves like a 350Ω resistor to ground.

Under-Voltage Lock-Out (UVLO)

The TPS799xx utilizes an under-voltage lock-out circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a de-glitch feature so that it will typically ignore undershoot transients on the input if they are less than 50µs duration.

Minimum Load

The TPS799xx is stable and well-behaved with no output load. To meet the specified accuracy, a minimum load of 500µA is required. Below 500µA at junction temperatures near +125°C, the output can drift up enough to cause the output pull-down to turn on. The output pull-down will limit voltage drift to 5% typically but ground current could increase by approximately 50µA. In typical applications, the junction cannot reach high temperatures at light loads since there is no appreciable dissipated power. The specified ground current would then be valid at no load in most applications.

Thermal Information

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS799xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS799xx into thermal shutdown will degrade device reliability.

Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the head from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Dissipation Ratings* table. Using heavier copper will increase the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers will also improve the heatsink effectiveness.

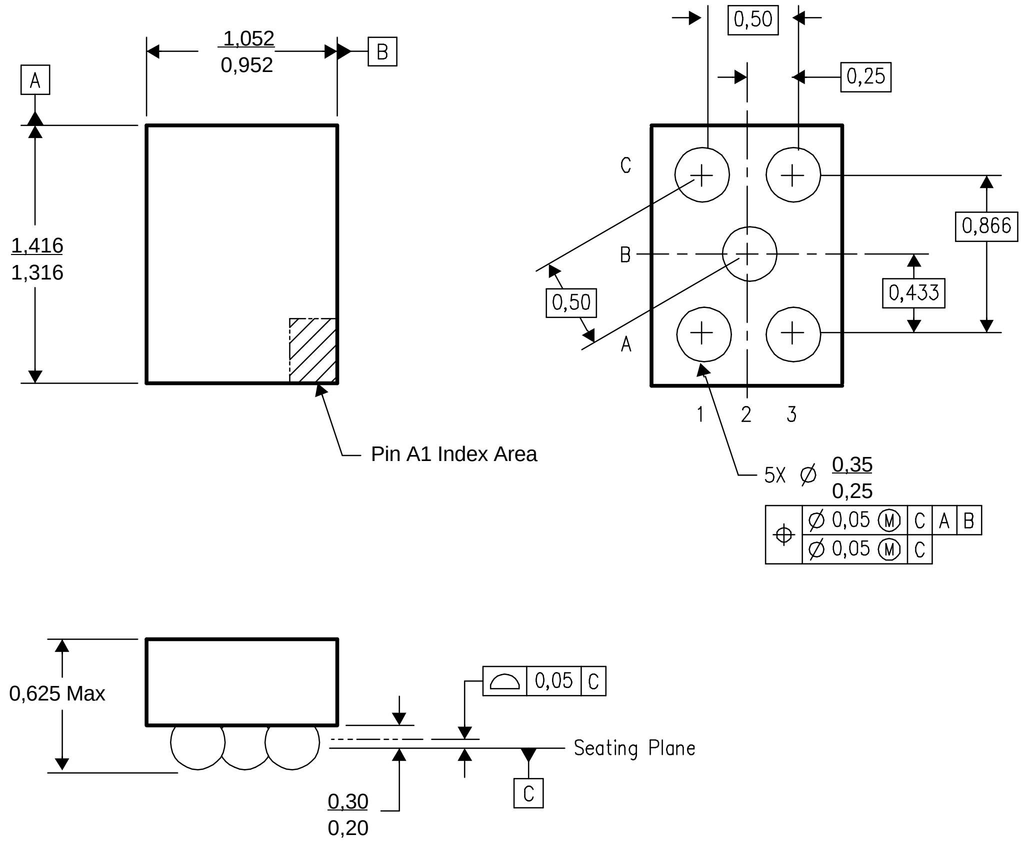
Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current time the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = \left(V_{IN} - V_{OUT}\right) \cdot I_{OUT} \quad (2)$$

Package Mounting

Solder pad footprint recommendations for the TPS799xx are available from the Texas Instruments' web site at www.ti.com.

Thermal Information (continued)



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.

NanoStar is a trademark of Texas Instruments.

Figure 30. YZU Wafer Chip-Scale Preliminary Package Dimensions (mm)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS79901DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79901DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	None	Call TI	Call TI
TPS79901DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79901DDCTG4	ACTIVE	TO/SOT	DDC	5	250	None	Call TI	Call TI
TPS79915DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79915DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	None	Call TI	Call TI
TPS79915DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79915DDCTG4	ACTIVE	TO/SOT	DDC	5	250	None	Call TI	Call TI
TPS79918DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79918DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	None	Call TI	Call TI
TPS79918DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79918DDCTG4	ACTIVE	TO/SOT	DDC	5	250	None	Call TI	Call TI
TPS79925DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79925DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	None	Call TI	Call TI
TPS79925DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79925DDCTG4	ACTIVE	TO/SOT	DDC	5	250	None	Call TI	Call TI
TPS799285DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS799285DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	None	Call TI	Call TI
TPS799285DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS799285DDCTG4	ACTIVE	TO/SOT	DDC	5	250	None	Call TI	Call TI
TPS79928DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79928DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	None	Call TI	Call TI
TPS79928DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79928DDCTG4	ACTIVE	TO/SOT	DDC	5	250	None	Call TI	Call TI
TPS79930DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79930DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	None	Call TI	Call TI
TPS79930DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79930DDCTG4	ACTIVE	TO/SOT	DDC	5	250	None	Call TI	Call TI
TPS79933DDCR	ACTIVE	TO/SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79933DDCRG4	ACTIVE	TO/SOT	DDC	5	3000	None	Call TI	Call TI
TPS79933DDCT	ACTIVE	TO/SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS79933DDCTG4	ACTIVE	TO/SOT	DDC	5	250	None	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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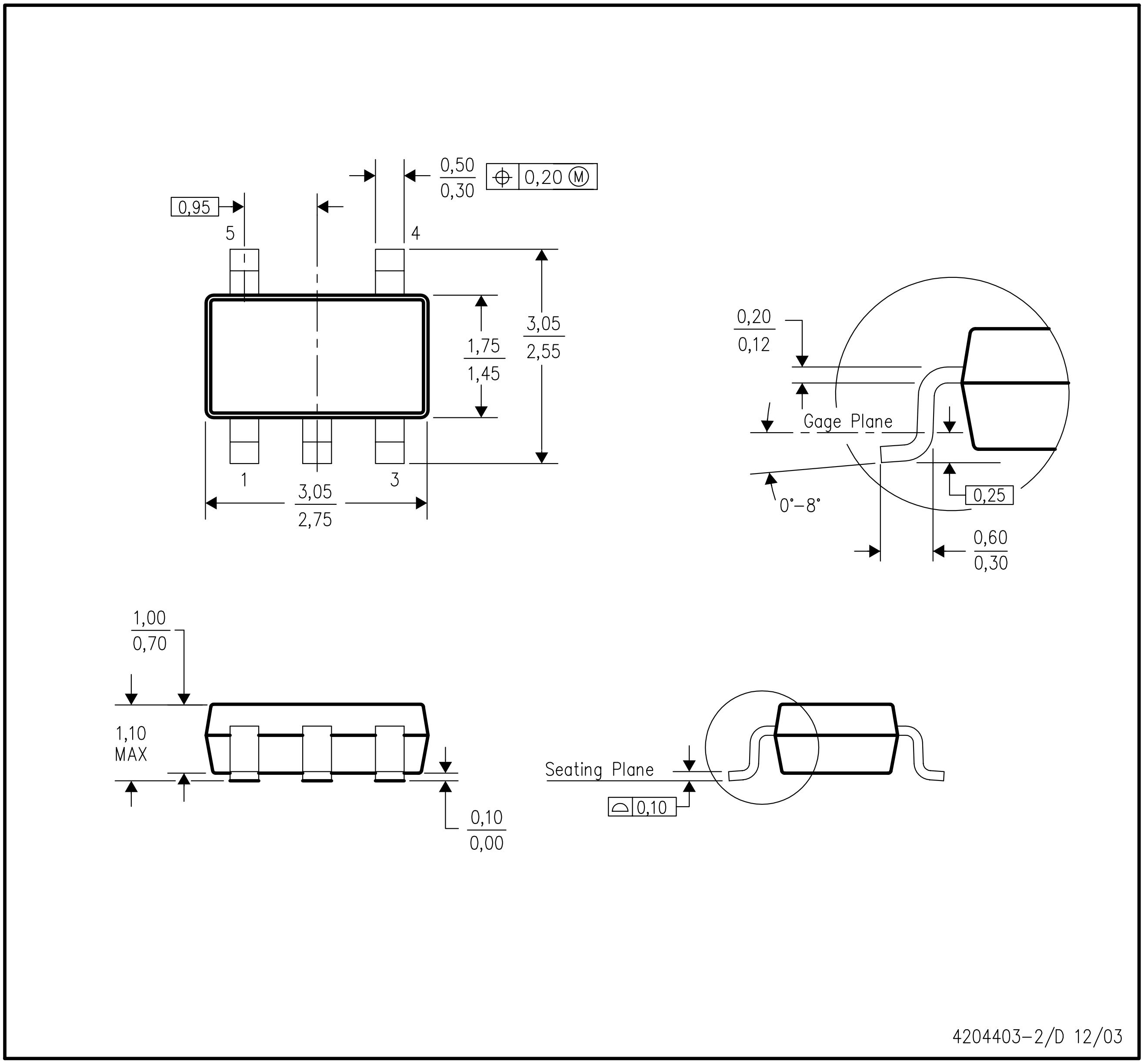
DDC (R-PDSO-G5) PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-193 variation AB (5 pin).

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