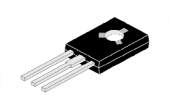
PNP EPITAXIAL SILICON POWER TRANSISTORS

TME_2N5194



TO-126

TO-126
Plastic Package
RoHS compliant

APPLICATIONS: Use in Medium Power Amplifier and Switching Applications.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	Value	UNIT
Collector Base Voltage	V_{CBO}	60	V
Collector Emitter Voltage	V_{CEO}	60	V
Emitter Base Voltage	V_{EBO}	5.0	V
Collector Current	I_C	4.0	A
Collector Peak Current	I_{CM}	7.0	A
Total Dissipation @ T_C=25ºC	P_D	40	W
Operating and Storage Junction Temperature Range	T_j, T_{stg}	-65 to +150	°C

THERMAL RESISTANCE

Junction to Case	$R_{th\ (j-c)}$	3.12	°C/W

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
Collector Cut off Current	I_{CBO}	V_{CB}=rated $V_{CB,}$	--	--	100	µA
	I_{CEV}	V_{CE}=rated V_{CEO}, V_{EB}=1.5V,	--	--	100	µA
	I_{CEO}	V_{CE}=rated V_{CEO}	--	--	1	mA
Emitter Cut off Current	I_{EBO}	V_{EB}=5V, I_C=0	--	--	1.0	mA
Collector Emitter Sustaining Voltage	$V_{CEO\ (sus)}$ [1]	I_C=100mA, I_B=0	60	--	--	V
Collector Emitter Saturation Voltage	$V_{CE\ (sat)}$ [1]	I_C=1.5A, I_B=0.15A	--	--	0.6	V
		I_C=4A, I_B=1A	--	--	1.2	
Base Emitter Voltage	$V_{BE\ (on)}$ [1]	I_C=1.5A, V_{CE}=2V	--	--	1.2	V
DC Current Gain	h_{FE} [1]	I_C=1.5A, V_{CE}=2V	25	--	120	
		I_C=4A, V_{CE}=2V	10	--	--	
Current Gain Bandwidth Product	f_T	I_C=1A, V_{CE}=10V, f=1MHz	2	--	--	MHz

Note:

1. Pulsed Pulse Duration=300µs, Duty Cycle=1.5%

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

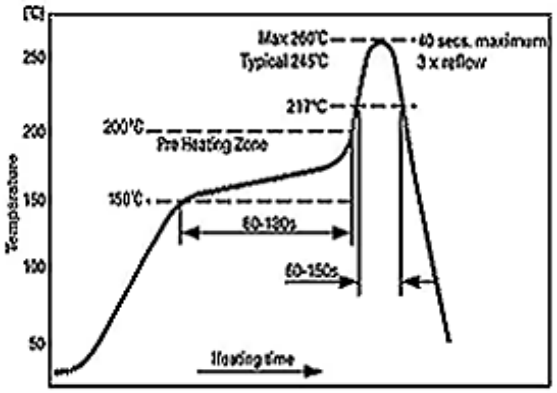
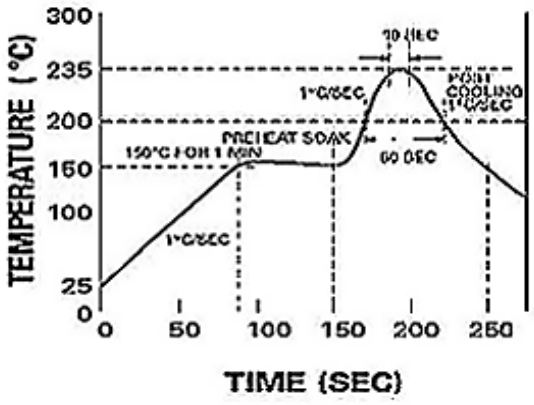


Figure 2

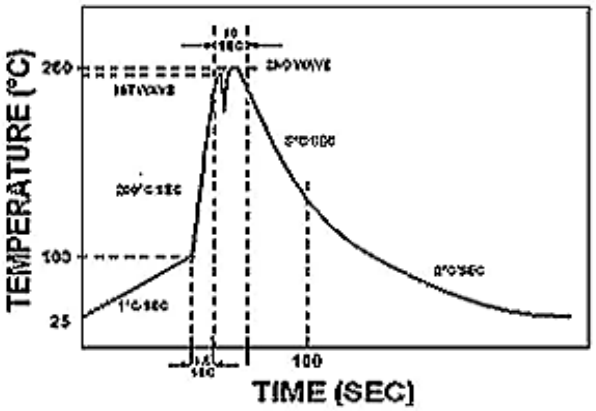


Reflow profiles in tabular form

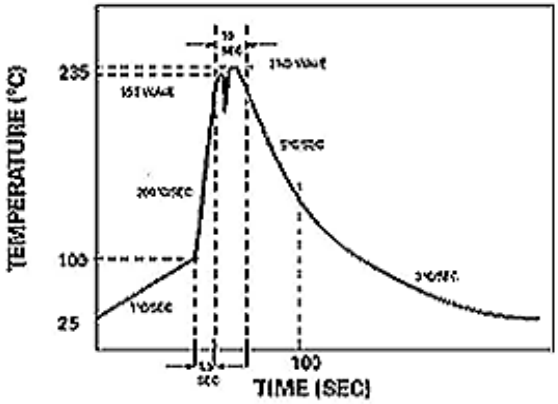
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder

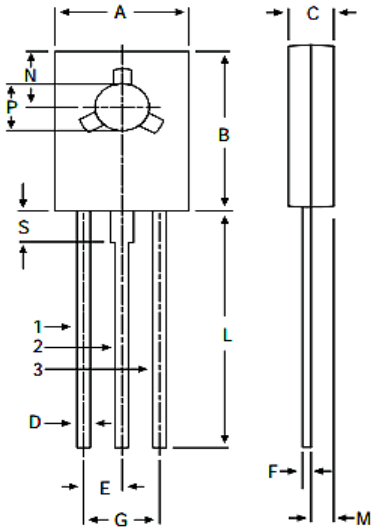


Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

PACKAGE DETAILS

TO-92 Leaded Plastic Package

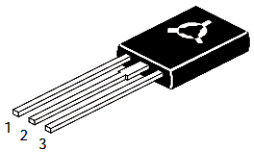


DIM	MIN	MAX
A	7.4	7.8
B	10.5	10.8
C	2.4	2.7
D	0.7	0.9
E	2.25 TYP	
F	0.49	0.75
G	4.5 TYP	
L	15.7 TYP	
M	1.27 TYP	
N	3.75 TYP	
P	3.0	3.2
S	2.5 TYP	

All dimensions are in mm

PIN CONFIGURATION

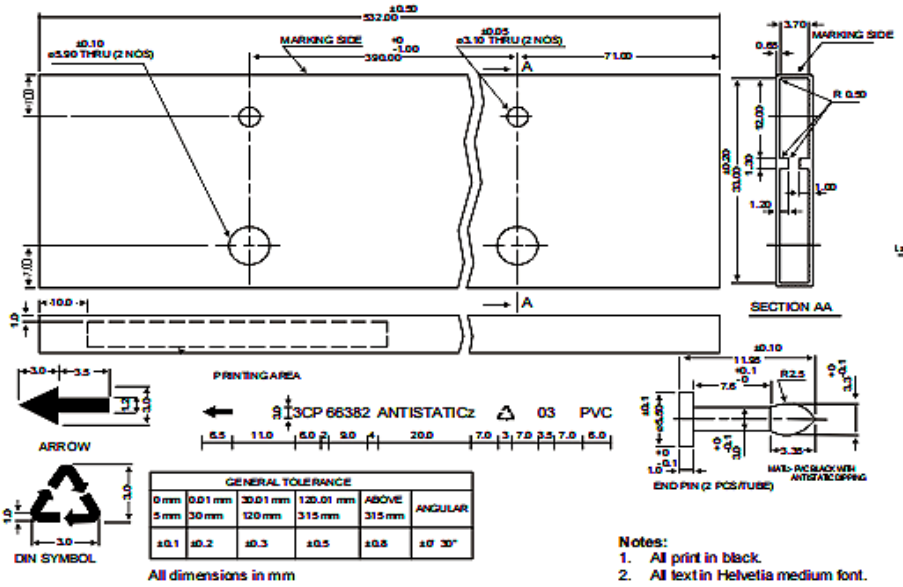
1. Emitter
2. Collector
3. Base



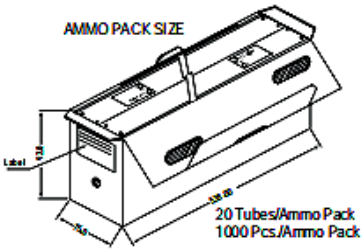
Packaging Information

PACKAGE	STANDARD PACK		INNER CARTON BOX		OUTER CARTON BOX		
	Details	Net Weight/Qty	Size	Qty	Size	Qty	Gr Wt
TO-126 Bulk	500 pcs/polybag	340 gm/500 pcs	3" x 7.5" x 7.5"	2K	17" x 15" x 13.5"	32K	31 kgs
TO-126 Tube	50 pcs/tube	73 gm/50 pcs	3" x 3.7" x 21.5"	1K	19" x 19" x 19"	10K	15 kgs

TO-126 TUBE PACKING



Notes:
1. All print in black.
2. All text in Helvetia medium font.



Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.

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