

### Features

- 800 V avalanche rugged power section
- PWM operation with frequency jittering for low EMI
- Operating frequency:
  - 30 kHz for VIPER06Xx
  - 60 kHz for VIPER06Lx
  - 115 kHz for VIPER06Hx
- No need for an auxiliary winding in low-power applications
- Standby power < 30 mW at 265 V<sub>AC</sub>
- Limiting current with adjustable set point
- On-board soft-start
- Safe auto-restart after a fault condition
- Hysteretic thermal shutdown

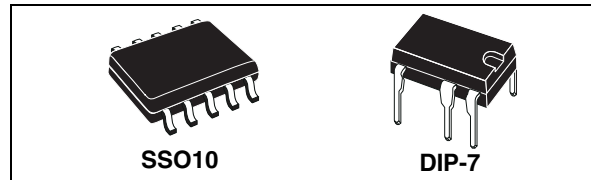
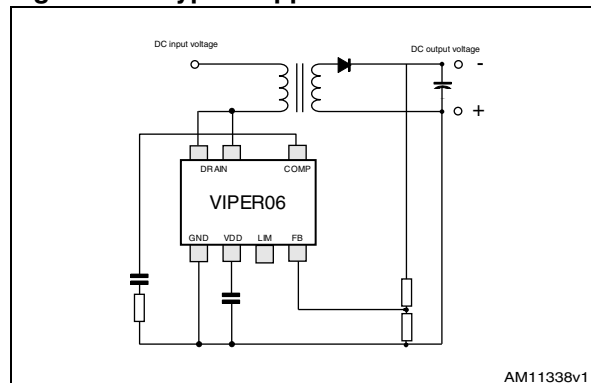


Figure 1. Typical application



### Applications

- Replacement of capacitive power supplies
- Home appliances
- Power metering
- LED drivers

### Description

The VIPER06 is an offline converter with an 800 V avalanche rugged power section, a PWM controller, a user-defined overcurrent limit, open-loop failure protection, hysteretic thermal protection, soft startup and safe auto-restart after any fault condition. The device is able to power itself directly from the rectified mains, eliminating the need for an auxiliary bias winding. Advanced frequency jittering reduces EMI filter cost. Burst mode operation and the device's very low power consumption both help to meet the standards set by energy-saving regulations.

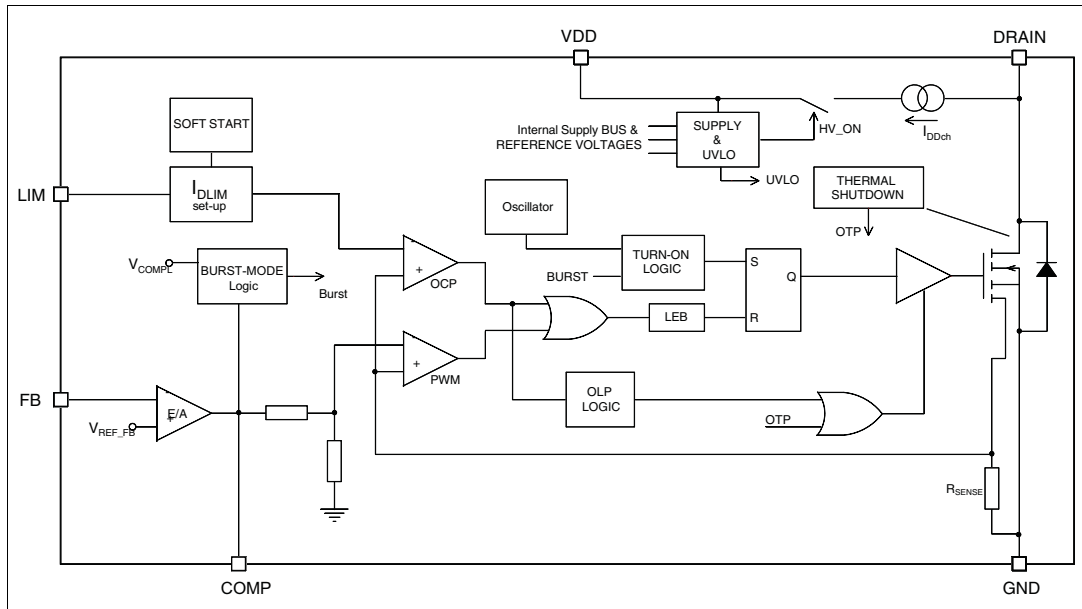
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# 1 Block diagram

Figure 2. Block diagram



# 2 Typical power

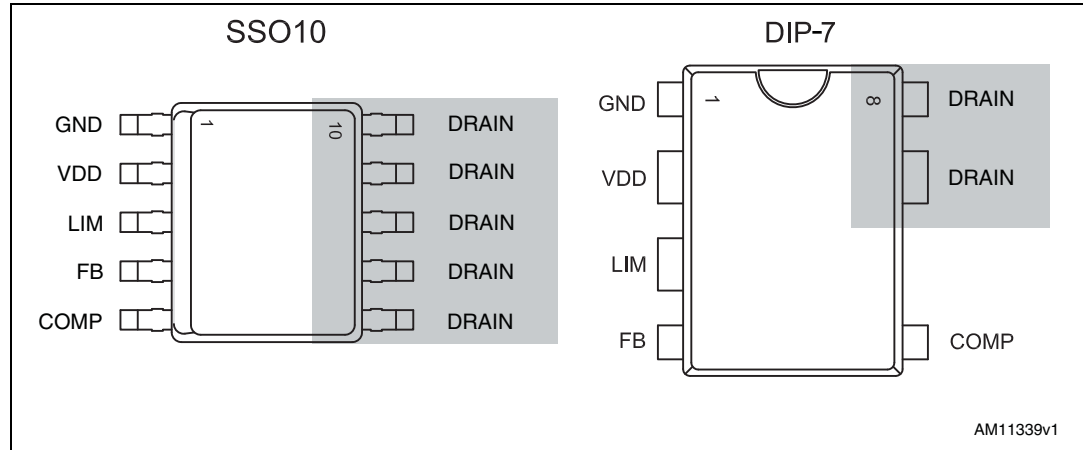
Table 1. Typical power

Part number	230 V <sub>AC</sub>		85-265 V <sub>AC</sub>	
	Adapter <sup>(1)</sup>	Open frame <sup>(2)</sup>	Adapter <sup>(1)</sup>	Open frame <sup>(2)</sup>
VIPER06	6 W	8 W	4 W	5 W

1. Typical continuous power in non-ventilated enclosed adapter measured at 50 °C ambient.
2. Maximum practical continuous power in an open-frame design at 50 °C ambient, with adequate heat sinking.

### 3 Pin settings

Figure 3. Connection diagram (top view)



Note: The copper area for heat dissipation has to be designed under the DRAIN pins.

Table 2. Pin description

Pin		Name	Function
DIP-7	SSO10		
1	1	GND	Connected to the source of the internal power MOSFET and controller ground reference.
2	2	VDD	Supply voltage of the control section. This pin provides the charging current of the external capacitor.
3	3	LIM	This pin allows setting the drain current limitation. The limit can be reduced by connecting an external resistor between this pin and GND. Pin left open if default drain current limitation is used.
4	4	FB	Inverting input of the internal transconductance error amplifier. Connecting the converter output to this pin through a single resistor results in an output voltage equal to the error amplifier reference voltage (see $V_{FB\_REF}$ in Table 6). An external resistor divider is required for higher output voltages.
5	5	COMP	Output of the internal transconductance error amplifier. The compensation network has to be placed between this pin and GND to achieve stability and good dynamic performance of the voltage control loop. The pin is used also to directly control the PWM with an optocoupler. The linear voltage range extends from $V_{COMPL}$ to $V_{COMPH}$ (Table 6).
7, 8	6-10	DRAIN	High-voltage drain pins. The built-in high-voltage switched startup bias current is drawn from these pins too. Pins connected to the metal frame to facilitate heat dissipation.

## 4 Electrical data

### 4.1 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Pin (DIP-7)	Parameter	Value		Unit
			Min	Max	
V <sub>DRAIN</sub>	7, 8	Drain-to-source (ground) voltage		800	V
E <sub>AV</sub>	7, 8	Repetitive avalanche energy (limited by T <sub>J</sub> = 150 °C)		2	mJ
I <sub>AR</sub>	7, 8	Repetitive avalanche current (limited by T <sub>J</sub> = 150 °C)		1	A
I <sub>DRAIN</sub>	7, 8	Pulse drain current (limited by T <sub>J</sub> = 150 °C)		2.5	A
V <sub>COMP</sub>	5	Input pin voltage	-0.3	3.5	V
V <sub>FB</sub>	4	Input pin voltage	-0.3	4.8	V
V <sub>LIM</sub>	3	Input pin voltage	-0.3	2.4	V
V <sub>DD</sub>	2	Supply voltage	-0.3	Self-limited	V
I <sub>DD</sub>	2	Input current		20	mA
P <sub>TOT</sub>		Power dissipation at T <sub>A</sub> < 40 °C (DIP-7)		1	W
		Power dissipation at T <sub>A</sub> < 50 °C (SSO10)		1	W
T <sub>J</sub>		Operating junction temperature range	-40	150	°C
T <sub>STG</sub>		Storage temperature	-55	150	°C

### 4.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max value SSO10	Max value DIP-7	Unit
R <sub>thJP</sub>	Thermal resistance junction pin (dissipated power = 1 W)	35	40	°C/W
R <sub>thJA</sub>	Thermal resistance junction ambient (dissipated power = 1 W)	100	110	°C/W
R <sub>thJA</sub>	Thermal resistance junction ambient <sup>(1)</sup> (dissipated power = 1 W)	80	90	°C/W

1. When mounted on a standard single side FR4 board with 100 mm<sup>2</sup> (0.155 sq in) of Cu (35 μm thick).

### 4.3 Electrical characteristics

( $T_J = -25$  to  $125$  °C,  $V_{DD} = 14$  V <sup>(a)</sup> unless otherwise specified).

**Table 5. Power section**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$V_{BVDSS}$	Breakdown voltage	$I_{DRAIN} = 1$ mA, $V_{COMP} = GND$ , $T_J = 25$ °C	800			V
$I_{OFF}$	OFF state drain current	$V_{DRAIN} = \text{max rating}$ , $V_{COMP} = GND$			60	μA
$R_{DS(on)}$	Drain-source on-state resistance	$I_{DRAIN} = 0.2$ A, $T_J = 25$ °C			32	Ω
		$I_{DRAIN} = 0.2$ A, $T_J = 125$ °C			67	Ω
$C_{OSS}$	Effective (energy related) output capacitance	$V_{DRAIN} = 0$ to 640 V		10		pF

**Table 6. Supply section**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
<b>Voltage</b>						
$V_{DRAIN\_START}$	Drain-source startup voltage		25		45	V
$I_{DDch1}$	Startup charging current	$V_{DRAIN} = 100$ V to 640 V, $V_{DD} = 4$ V	-0.6		-1.8	mA
$I_{DDch2}$	Charging current during operation	$V_{DRAIN} = 100$ V to 640 V, $V_{DD} = 9$ V falling edge	-7		-14	mA
$V_{DD}$	Operating voltage range		11.5		23.5	V
$V_{DDclamp}$	$V_{DD}$ clamp voltage	$I_{DD} = 15$ mA	23.5			V
$V_{DDon}$	$V_{DD}$ startup threshold		12	13	14	V
$V_{DDCSon}$	VDD on internal high-voltage current generator threshold		9.5	10.5	11.5	V
$V_{DDoff}$	$V_{DD}$ undervoltage shutdown threshold		7	8	9	V
<b>Current</b>						
$I_{DD0}$	Operating supply current, not switching	$F_{OSC} = 0$ kHz, $V_{COMP} = GND$			0.6	mA
$I_{DD1}$	Operating supply current, switching	$V_{DRAIN} = 120$ V, $F_{OSC} = 30$ kHz			1.3	mA
		$V_{DRAIN} = 120$ V, $F_{OSC} = 60$ kHz			1.45	mA
		$V_{DRAIN} = 120$ V, $F_{OSC} = 115$ kHz			1.6	mA
$I_{DDoff}$	Operating supply current with $V_{DD} < V_{DDoff}$	$V_{DD} < V_{DDoff}$			0.35	mA
$I_{DDol}$	Open-loop failure current threshold	$V_{DD} = V_{DDclamp}$ $V_{COMP} = 3.3$ V,	4			mA

a. Adjust  $V_{DD}$  above  $V_{DDon}$  startup threshold before setting to 14 V.

Table 7. Controller section

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
<b>Error amplifier</b>						
$V_{REF\_FB}$	FB reference voltage		3.2	3.3	3.4	V
$I_{FB\_PULL\ UP}$	Current pull-up			-1		$\mu$ A
$G_M$	Transconductance			2		mA/V
<b>Current setting (LIM) pin</b>						
$V_{LIM\_LOW}$	Low-level clamp voltage	$I_{LIM} = -100 \mu$ A		0.5		V
<b>Compensation (COMP) pin</b>						
$V_{COMPH}$	Upper saturation limit	$T_J = 25 \text{ }^\circ\text{C}$		3		V
$V_{COMPL}$	Burst mode threshold	$T_J = 25 \text{ }^\circ\text{C}$	1	1.1	1.2	V
$V_{COMPL\_HYS}$	Burst mode hysteresis	$T_J = 25 \text{ }^\circ\text{C}$		40		mV
$H_{COMP}$	$\Delta V_{COMP} / \Delta I_{DRAIN}$		4		9	V/A
$R_{COMP(DYN)}$	Dynamic resistance	$V_{FB} = GND$		15		k $\Omega$
$I_{COMP}$	Source / sink current	$V_{FB} > 100 \text{ mV}$		150		$\mu$ A
	Max source current	$V_{COMP} = GND, V_{FB} = GND$		220		$\mu$ A
<b>Current limitation</b>						
$I_{Dlim}$	Drain current limitation	$I_{LIM} = -10 \mu$ A, $V_{COMP} = 3.3 \text{ V}$ , $T_J = 25 \text{ }^\circ\text{C}$	0.32	0.35	0.38	A
$t_{SS}$	Soft-start time			8.5		ms
$T_{ON\_MIN}$	Minimum turn-on time				450	ns
$I_{Dlim\_bm}$	Burst mode current limitation	$V_{COMP} = V_{COMPL}$		85		mA
<b>Overload</b>						
$t_{OVL}$	Overload time			50		ms
$t_{RESTART}$	Restart time after fault			1		s
<b>Oscillator section</b>						
$F_{OSC}$	Switching frequency	VIPER06Xx	27	30	33	kHz
		VIPER06Lx	54	60	66	kHz
		VIPER06Hx	103	115	127	kHz
$F_D$	Modulation depth	$F_{OSC} = 30 \text{ kHz}$		$\pm 3$		kHz
		$F_{OSC} = 60 \text{ kHz}$		$\pm 4$		kHz
		$F_{OSC} = 115 \text{ kHz}$		$\pm 8$		kHz
$F_M$	Modulation frequency			230		Hz
$D_{MAX}$	Maximum duty cycle		70		80	%



Table 7. Controller section (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
<b>Thermal shutdown</b>						
$T_{SD}$	Thermal shutdown temperature		150	160		°C
$T_{HYST}$	Thermal shutdown hysteresis			30		°C

# 5 Typical electrical characteristics

Figure 4.  $I_{Dim}$  vs.  $T_J$

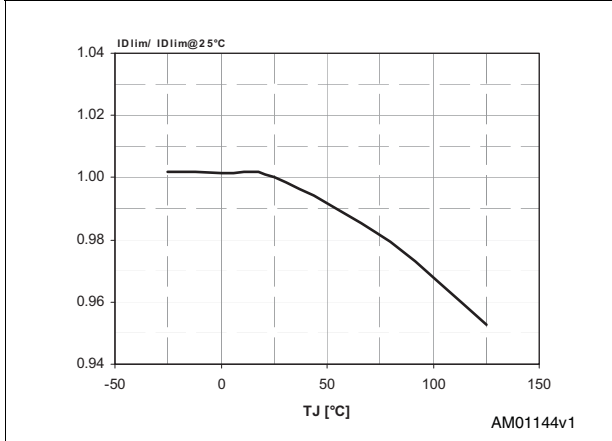


Figure 5.  $F_{OSC}$  vs.  $T_J$

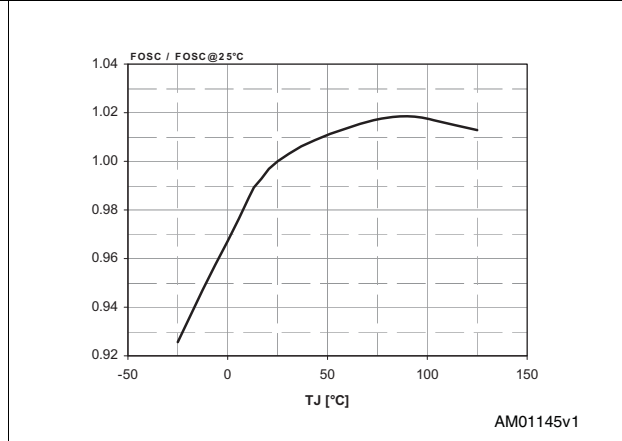


Figure 6.  $V_{DRAIN\_START}$  vs.  $T_J$

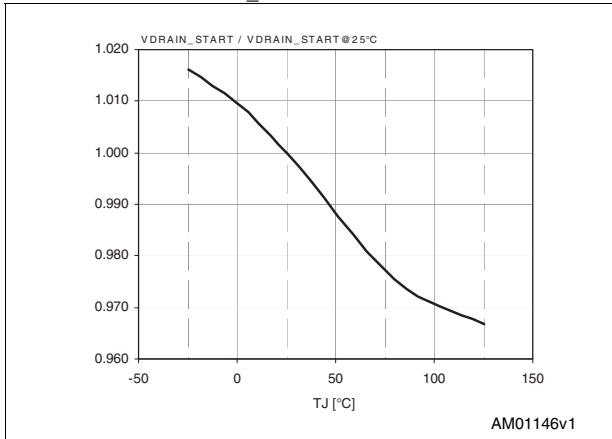


Figure 7.  $H_{COMP}$  vs.  $T_J$

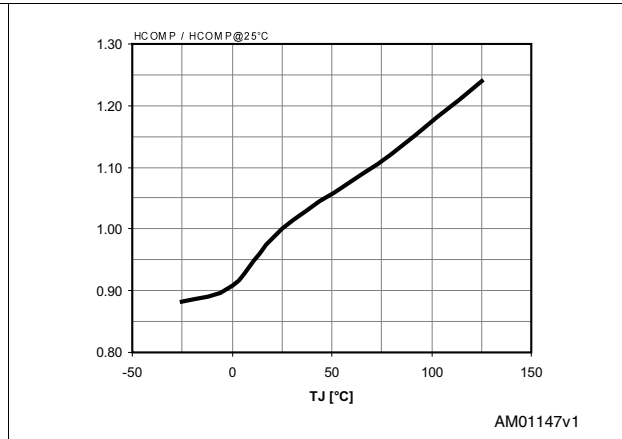


Figure 8.  $G_M$  vs.  $T_J$

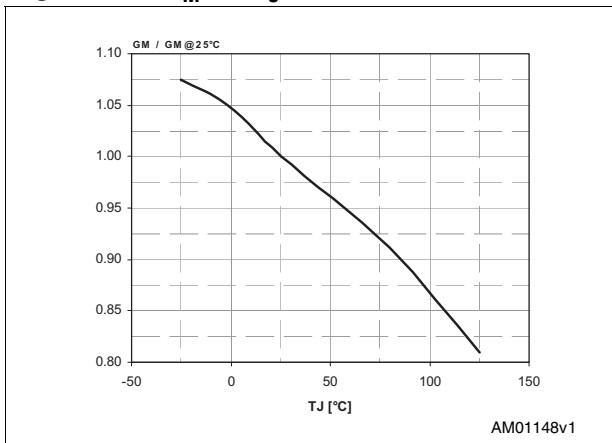


Figure 9.  $V_{REF\_FB}$  vs.  $T_J$

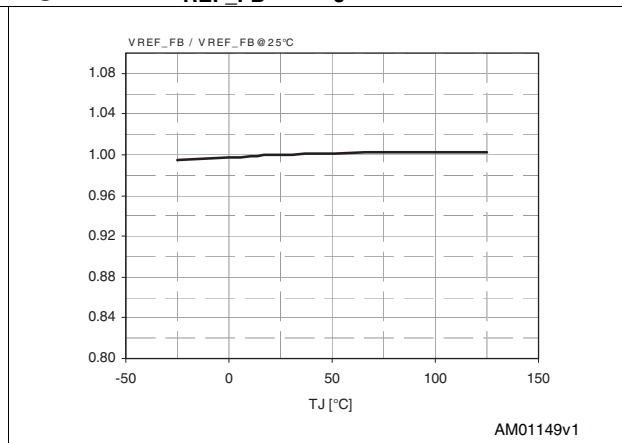


Figure 10.  $I_{COMP}$  vs.  $T_J$

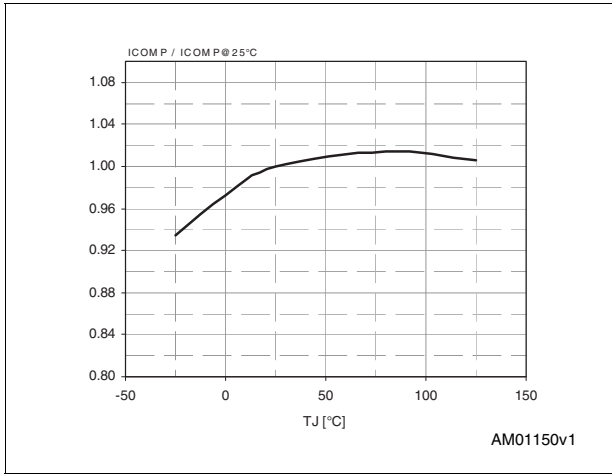


Figure 11. Operating supply current (no switching) vs.  $T_J$

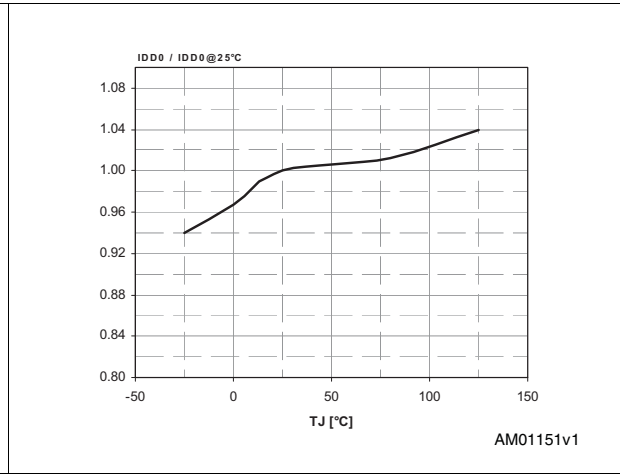


Figure 12. Operating supply current (switching) vs.  $T_J$

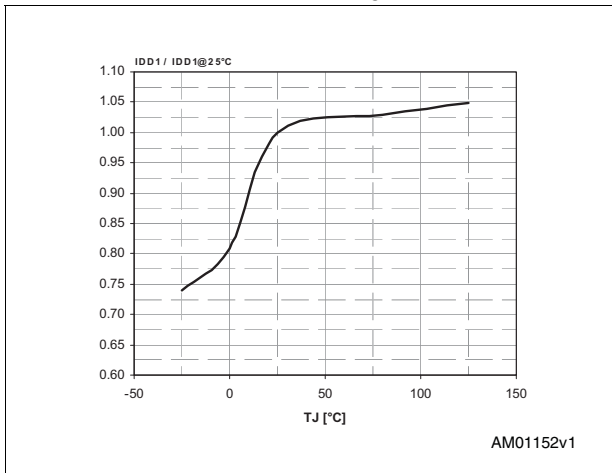


Figure 13.  $I_{Dlim}$  vs.  $R_{LIM}$

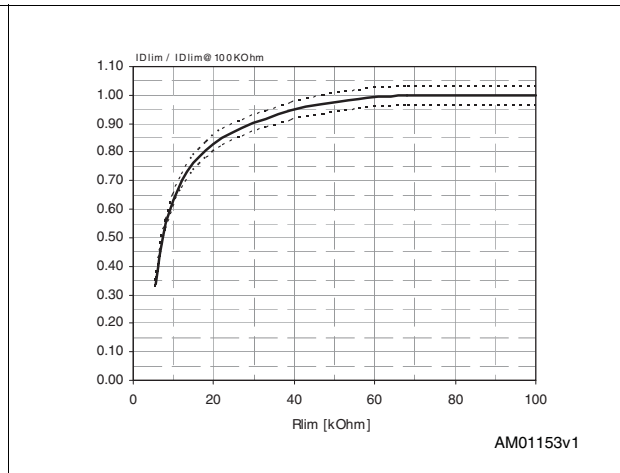


Figure 14. Power MOSFET on-resistance vs.  $T_J$

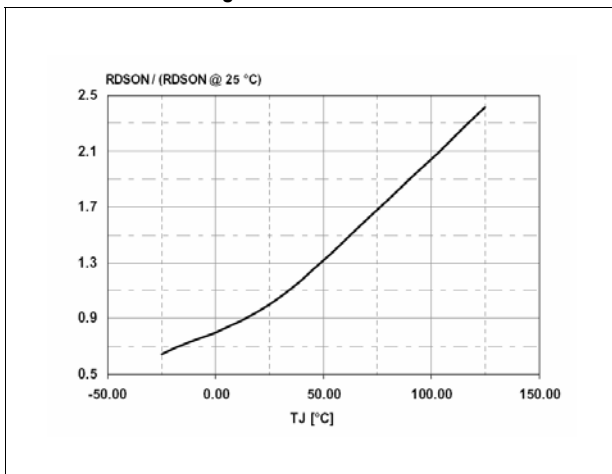


Figure 15. Power MOSFET breakdown voltage vs.  $T_J$

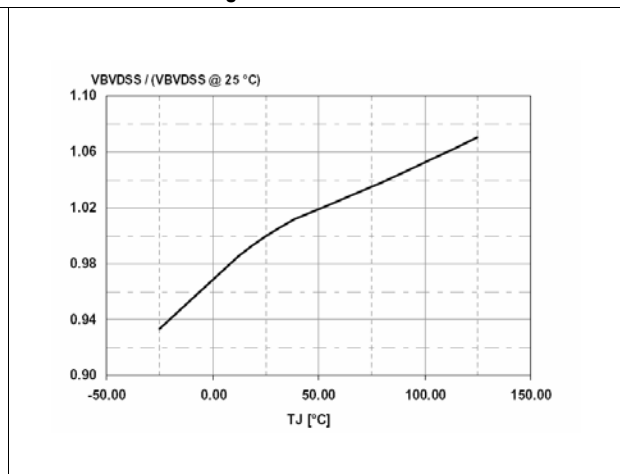
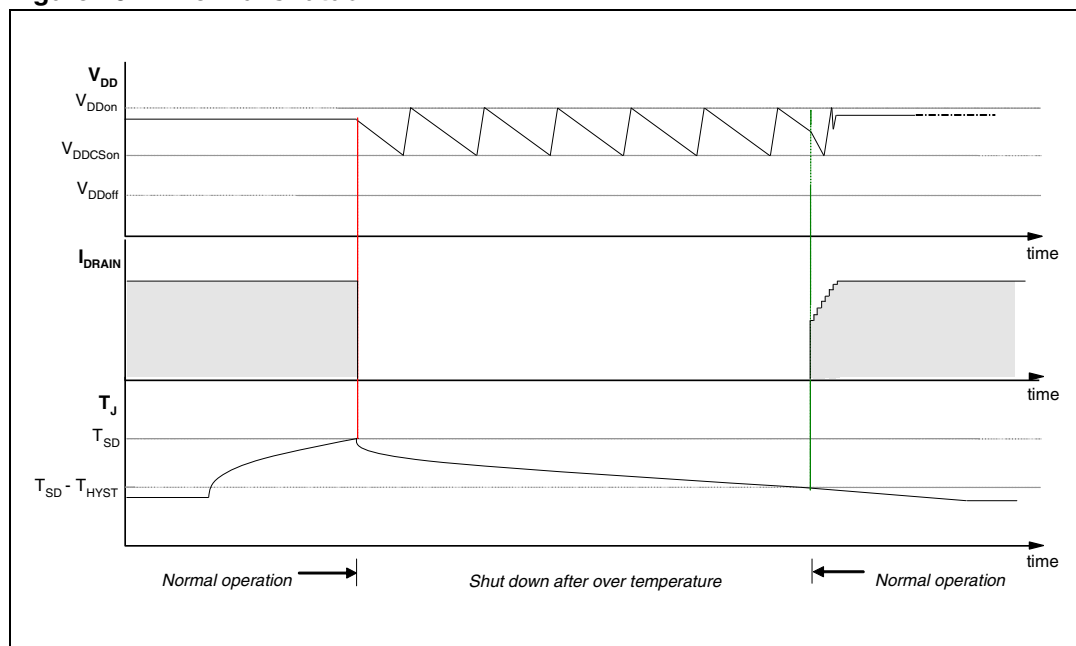


Figure 16. Thermal shutdown



# 6 Typical circuit

Figure 17. Flyback converter (non-isolated output)

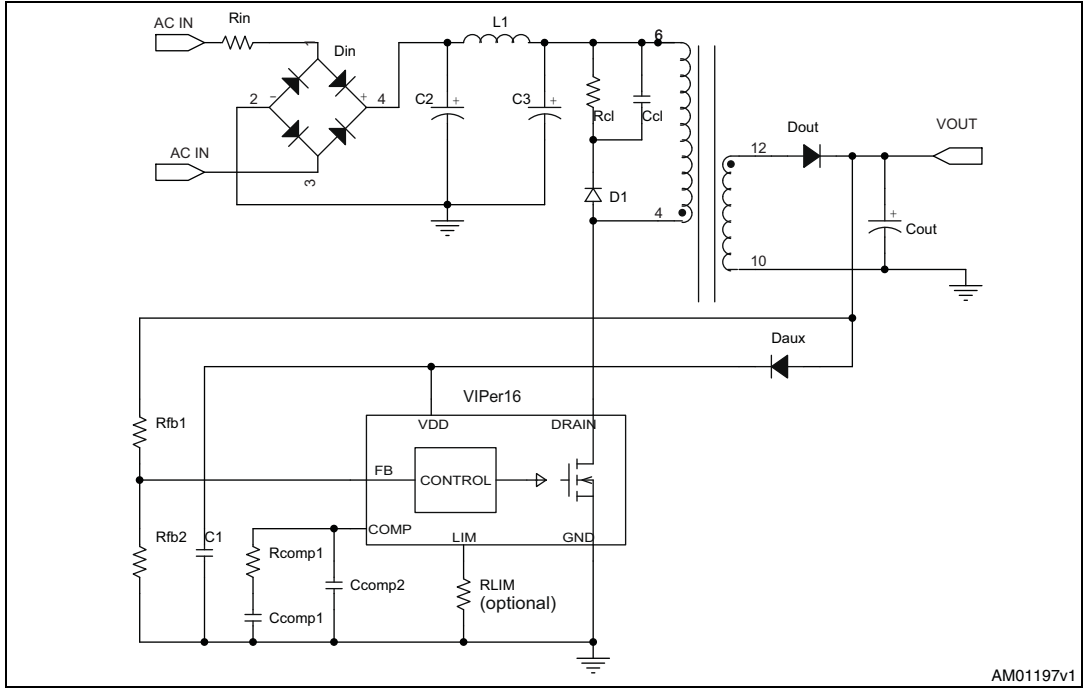


Figure 18. Flyback converter (isolated output)

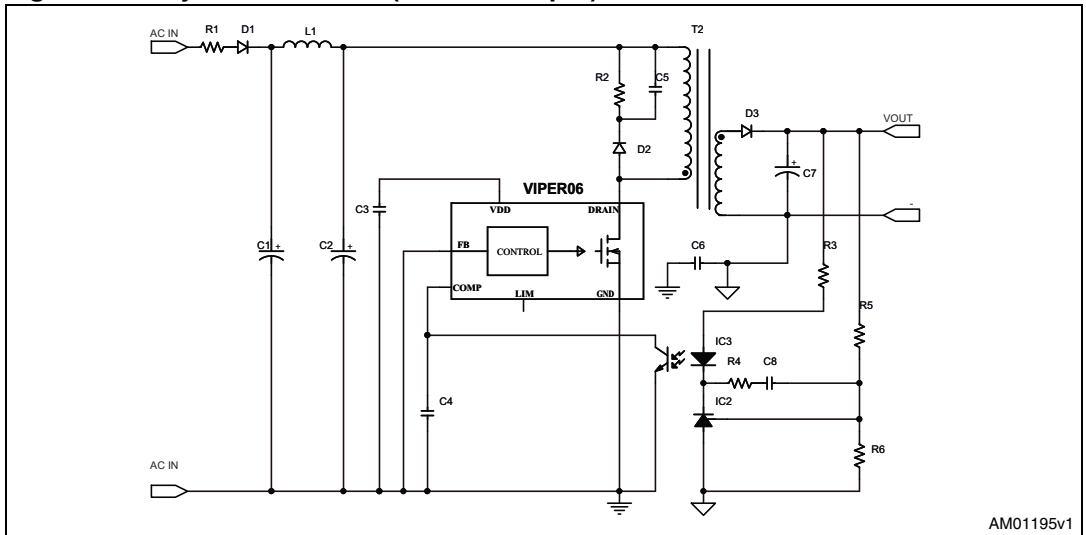
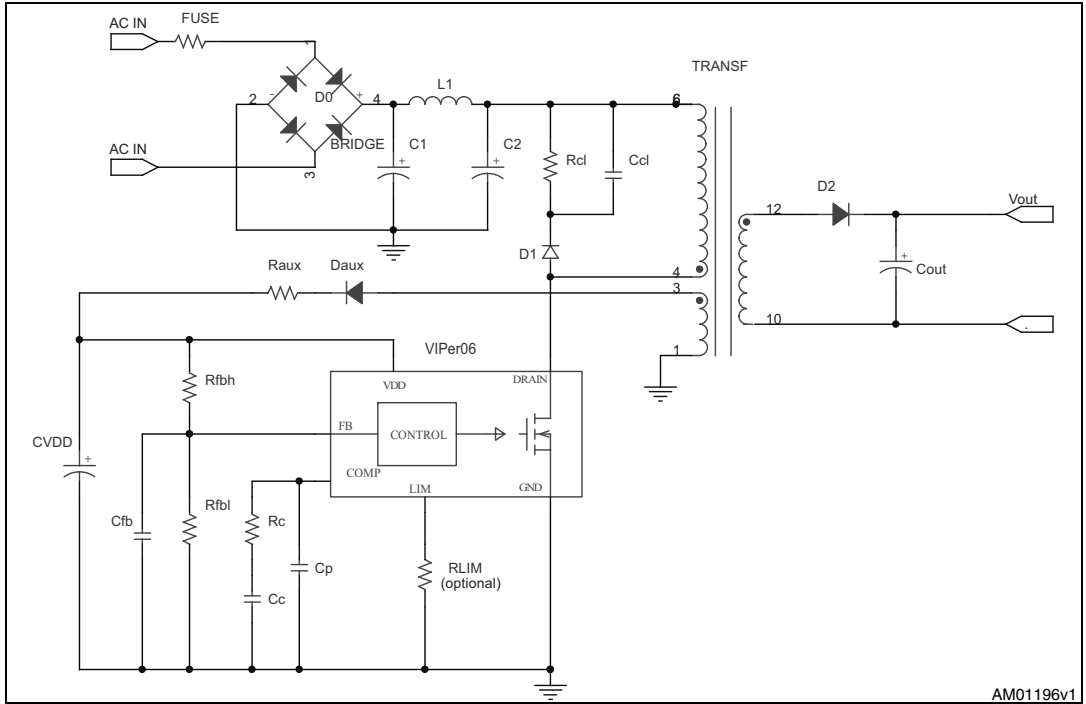
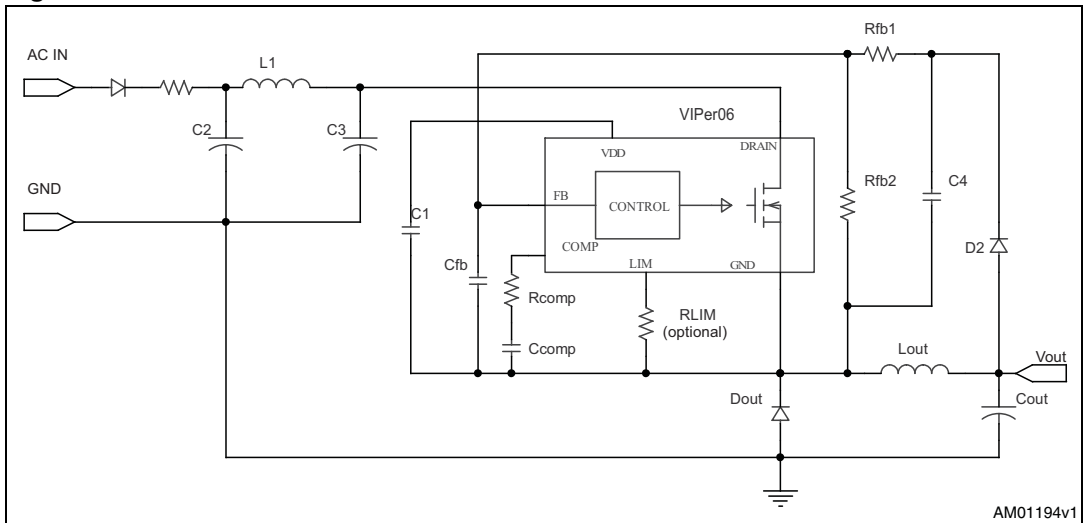


Figure 19. Flyback converter (isolated output without optocoupler)



AM01196v1

Figure 20. Buck converter



AM01194v1

## 7 Power section

The power section is implemented with an N-channel power MOSFET with a breakdown voltage of 800 V min. and a typical  $R_{DS(on)}$  of 32  $\Omega$ . It includes a SenseFET structure to allow virtually lossless current sensing and the thermal sensor.

The gate driver of the power MOSFET is designed to supply a controlled gate current during both turn-ON and turn-OFF in order to minimize common-mode EMI. During UVLO conditions, an internal pull-down circuit holds the gate low in order to ensure that the power MOSFET cannot be turned ON accidentally.

## 8 High voltage current generator

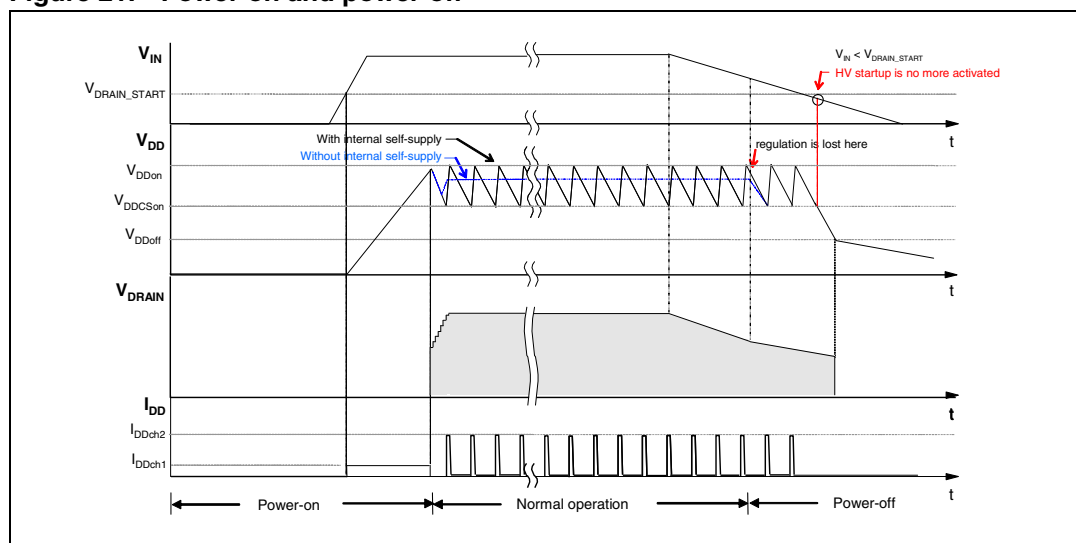
The high-voltage current generator is supplied by the DRAIN pin. At the first startup of the converter it is enabled when the voltage across the input bulk capacitor reaches the  $V_{DRAIN\_START}$  threshold, sourcing a  $I_{DDch1}$  current (see [Table 6 on page 7](#)). As the  $V_{DD}$  voltage reaches the  $V_{DDon}$  threshold, the power section starts switching and the high-voltage current generator is turned OFF. The VIPER06 is powered by the energy stored in the  $V_{DD}$  capacitor.

In a steady-state condition, if the self-biasing function is used, the high-voltage current generator is activated between  $V_{DDCSon}$  and  $V_{DDon}$  (see [Table 6 on page 7](#)), delivering  $I_{DDch2}$ , see [Table 6 on page 7](#) to the  $V_{DD}$  capacitor during the MOSFET off-time (see [Figure 21](#)).

The device can also be supplied through the auxiliary winding in which case the high-voltage current source is disabled during steady-state operation, provided that  $V_{DD}$  is above  $V_{DDCSon}$ .

At converter power-down, the  $V_{DD}$  voltage drops and the converter activity stops as it falls below the  $V_{DDoff}$  threshold (see [Table 6 on page 7](#)).

**Figure 21. Power-on and power-off**



## 9 Oscillator

The switching frequency is internally fixed at 30 kHz or 60 kHz or 115 kHz (respectively part numbers VIPER06Xx, VIPER06Lx and VIPER06Hx).

The switching frequency is modulated by approximately  $\pm 3$  kHz (30 kHz version) or  $\pm 4$  kHz (60 kHz version) or  $\pm 8$  kHz (115 kHz version) at 230 Hz (typical) rate, so that the resulting spread spectrum action distributes the energy of each harmonic of the switching frequency over a number of sideband harmonics having the same energy on the whole, but smaller amplitudes.

## 10 Soft startup

During the converter's startup phase, the soft-start function progressively increases the cycle-by-cycle drain current limit, up to the default value  $I_{Dlim}$ . In this way the drain current is further limited and the output voltage is progressively increased, reducing the stress on the secondary diode. The soft-start time is internally fixed to  $t_{SS}$ , see typical value in [Table 7 on page 8](#), and the function is activated for any attempt of converter startup and after a fault event.

This function helps prevent saturation of the transformer during startup and short-circuit.

## 11 Adjustable current limit set point

The VIPER06 includes a current-mode PWM controller. The drain current is sensed cycle-by-cycle through the integrated resistor  $R_{SENSE}$  and the voltage is applied to the non-inverting input of the PWM comparator, see [Figure 2 on page 4](#). As soon as the sensed voltage is equal to the voltage derived from the COMP pin, the power MOSFET is switched OFF.

In parallel with the PWM operations, the comparator OCP, see [Figure 2 on page 4](#), checks the level of the drain current and switches OFF the power MOSFET in case the current is higher than the threshold  $I_{Dlim}$ , see [Table 7 on page 8](#).

The level of the drain current limit  $I_{Dlim}$  can be reduced using a resistor  $R_{LIM}$  connected between the LIM and GND pins. Current is sunk from the LIM pin through the resistor  $R_{LIM}$  and the setup of  $I_{Dlim}$  depends on the level of this current. The relation between  $I_{Dlim}$  and  $R_{LIM}$  is shown in [Figure 13 on page 11](#).

When the LIM pin is left open or if  $R_{LIM}$  has a high value (i.e.  $> 80$  k $\Omega$ ), the current limit is fixed to its default value,  $I_{Dlim}$ , as given in [Table 7 on page 8](#).



## 12 FB pin and COMP pin

The device can be used both in non-isolated and isolated topology. In non-isolated topology, the feedback signal from the output voltage is applied directly to the FB pin as the inverting input of the internal error amplifier having the reference voltage,  $V_{REF\_FB}$ , see [Table 7 on page 8](#).

The output of the error amplifier sources and sinks the current,  $I_{COMP}$  respectively to and from the compensation network connected on the COMP pin. This signal is then compared in the PWM comparator with the signal coming from the SenseFET in order to switch off the power MOSFET on a cycle-by-cycle basis. See the [Figure 2 on page 4](#) and the [Figure 22](#).

When the power supply output voltage is equal to the error amplifier reference voltage,  $V_{REF\_FB}$ , a single resistor has to be connected from the output to the FB pin. For higher output voltages the external resistor divider is needed. If the voltage on the FB pin is accidentally left floating, an internal pull-up protects the controller.

The output of the error amplifier is externally accessible through the COMP pin and it's used for the loop compensation, usually an RC network.

As shown in [Figure 22](#), in case of an isolated power supply, the internal error amplifier has to be disabled (FB pin shorted to GND). In this case an internal resistor is connected between an internal reference voltage and the COMP pin, see [Figure 22](#). The current loop has to be closed on the COMP pin through the opto-transistor in parallel with the compensation network. The  $V_{COMP}$  dynamic range is between  $V_{COMPL}$  and  $V_{COMPH}$  shown in [Figure 23 on page 18](#).

When the voltage  $V_{COMP}$  drops below the voltage threshold  $V_{COMPL}$ , the converter enters burst mode, see [Section 13 on page 18](#).

When the voltage  $V_{COMP}$  rises above the  $V_{COMPH}$  threshold, the peak drain current, as well as the deliverable output power, will reach its limit.

**Figure 22. Feedback circuit**

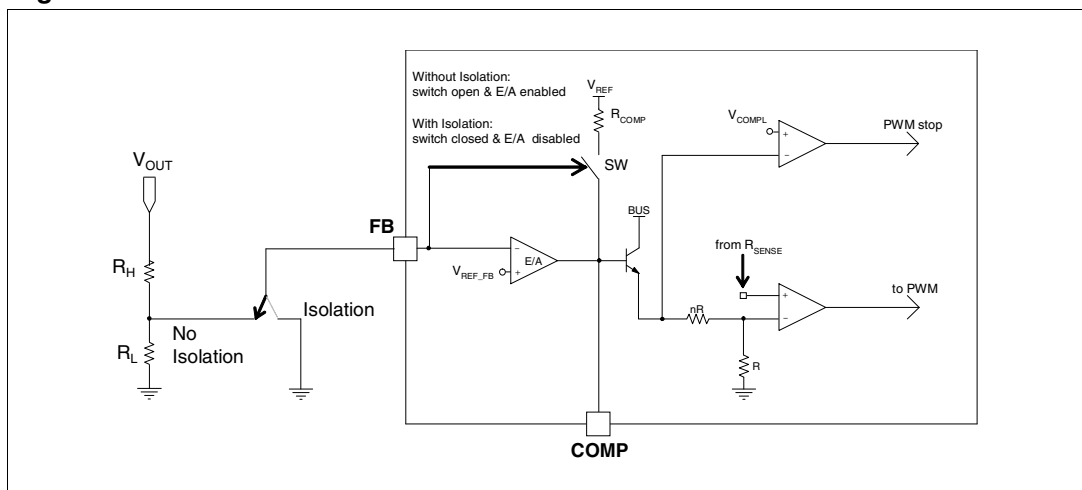
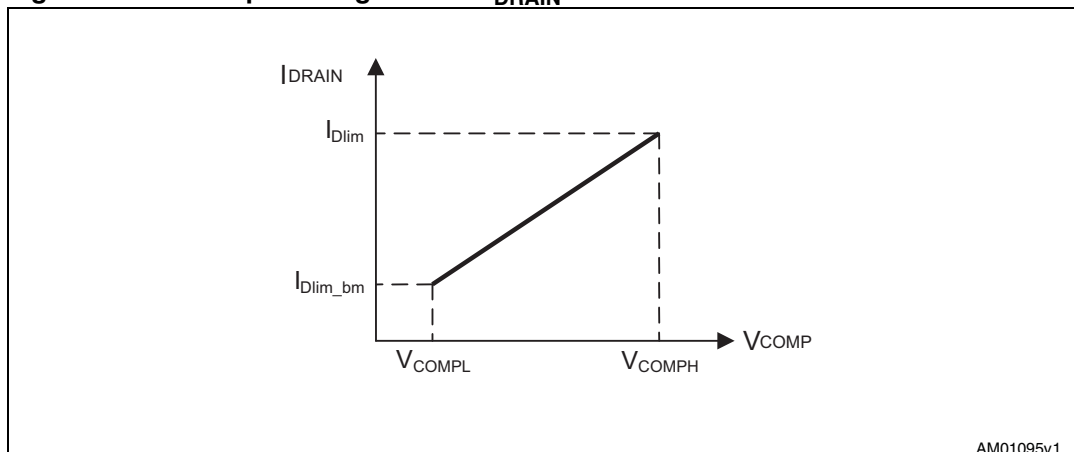


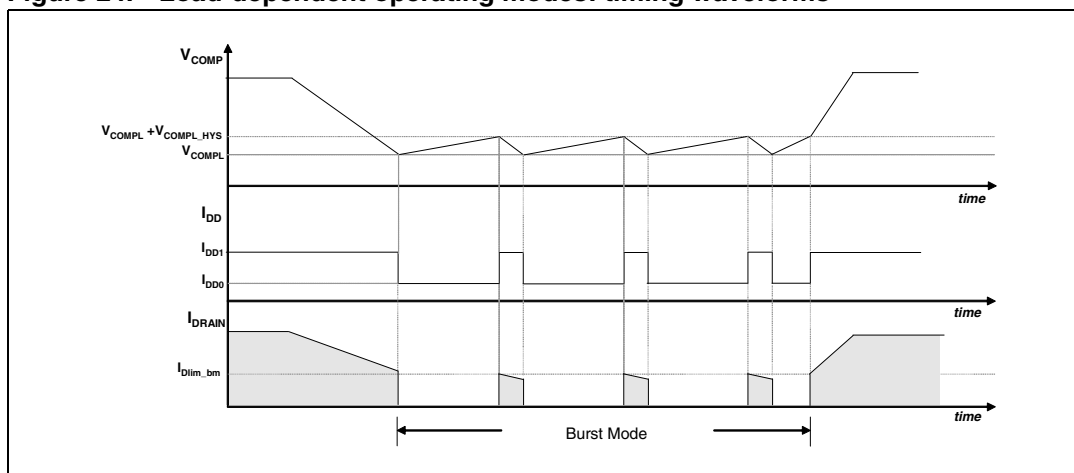
Figure 23. COMP pin voltage versus  $I_{DRAIN}$



### 13 Burst mode

When the voltage  $V_{COMP}$  drops below the threshold,  $V_{COMPL}$ , the power MOSFET is kept in the OFF state and the consumption is reduced to the  $I_{DD0}$  current, as reported on [Table 6 on page 7](#). In reaction to the loss of energy, the  $V_{COMP}$  voltage increases and as soon as it exceeds the threshold  $V_{COMPL} + V_{COMPL\_HYS}$ , the converter starts switching again with a level of consumption equal to the  $I_{DD1}$  current. This ON-OFF operation mode, referred to as “burst mode” and shown in [Figure 24 on page 18](#), reduces the average frequency, which can go down even to a few hundreds hertz, thus minimizing all frequency-related losses and making it easier to comply with energy-saving regulations. During burst mode, the drain current limit is reduced to the value  $I_{Dlim\_bm}$  (given in [Table 7 on page 8](#)) in order to avoid the audible noise issue.

Figure 24. Load-dependent operating modes: timing waveforms

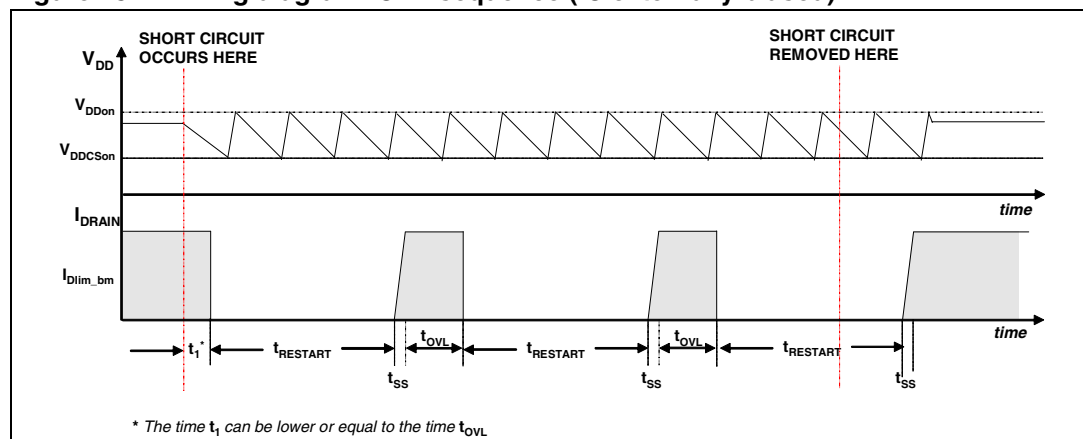


## 14 Automatic auto-restart after overload or short-circuit

The overload protection is implemented automatically using the integrated up-down counter. Every cycle, it is incremented or decremented depending upon the current logic detection of the limit condition or not. The limit condition is the peak drain current,  $I_{Dlim}$ , given in [Table 7 on page 8](#) or the one set by the user through the  $R_{LIM}$  resistor, shown in [Figure 13 on page 11](#). After the reset of the counter, if the peak drain current is continuously equal to the level  $I_{Dlim}$ , the counter will be incremented until the fixed time,  $t_{OVL}$ , at which point the power MOSFET switch ON will be disabled. It will be activated again through the soft-start after the  $t_{RESTART}$  time (see [Figure 25](#) and [Figure 26 on page 19](#)) and the time values mentioned in [Table 7 on page 8](#).

For overload or short-circuit events, the power MOSFET switching will be stopped after a period of time dependent upon the counter with a maximum equal to  $t_{OVL}$ . The protection sequence continues until the overload condition is removed, see [Figure 25](#) and [Figure 26](#). This protection ensures a low repetition rate of restart attempts of the converter, so that it works safely with extremely low power throughput and avoids overheating the IC in case of repeated overload events. If the overload is removed before the protection tripping, the counter will be decremented cycle-by-cycle down to zero and the IC will not be stopped.

**Figure 25. Timing diagram: OLP sequence (IC externally biased)**



**Figure 26. Timing diagram: OLP sequence (IC internally biased)**

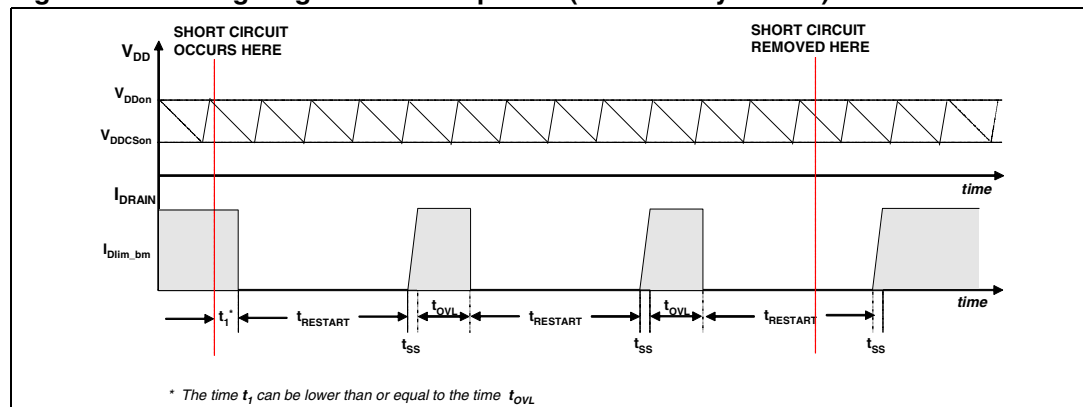
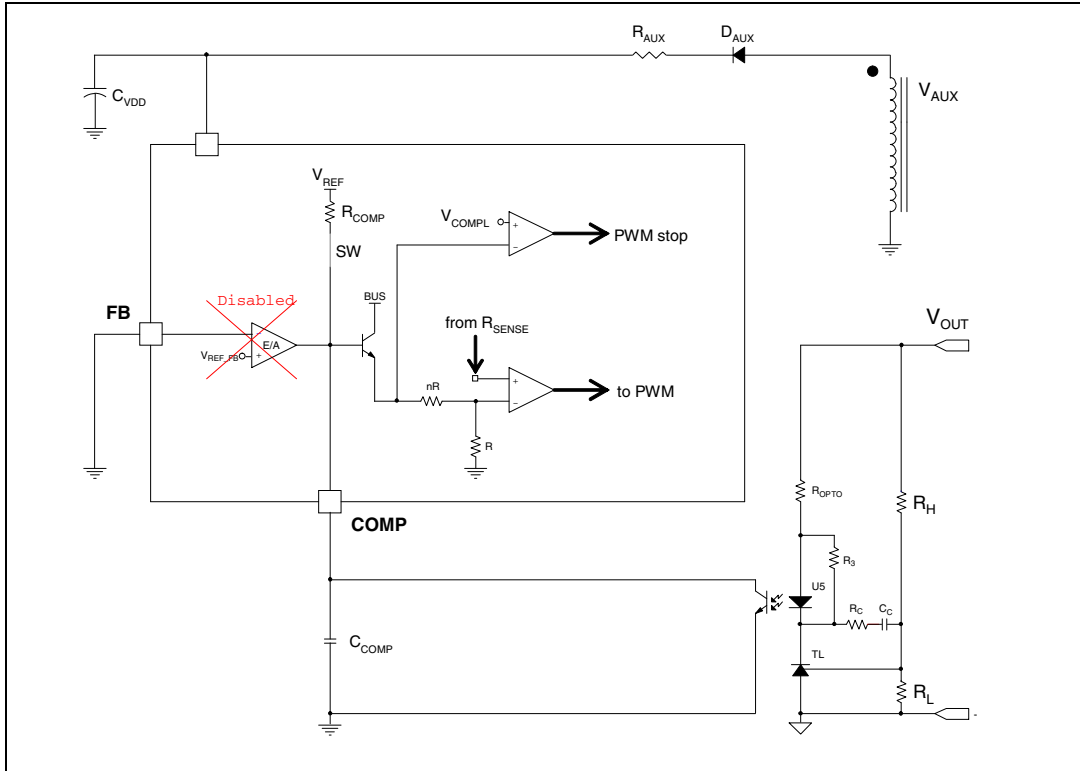




Figure 28. FB pin connection for isolated flyback



## 16 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

**Table 8. DIP-7 mechanical data**

Dim.	mm		
	Typ	Min	Max
A			5.33
A1		0.38	
A2	3.30	2.92	4.95
b	0.46	0.36	0.56
b2	1.52	1.14	1.78
c	0.25	0.20	0.36
D	9.27	9.02	10.16
E	7.87	7.62	8.26
E1	6.35	6.10	7.11
e	2.54		
eA	7.62		
eB			10.92
L	3.30	2.92	3.81
M <sup>(1)(2)</sup>	2.508		
N	0.50	0.40	0.60
N1			0.60
O <sup>(2)(3)</sup>	0.548		

1. Creepage distance > 800 V.
2. Creepage distance as given in the 664-1 CEI / IEC standard.
3. Creepage distance 250 V.

- Note:*
- 1 The lead size includes the thickness of the lead finishing material.
  - 2 Dimensions do not include mold protrusion, not to exceed 0.25 mm in total (both sides).
  - 3 Package outline exclusive of metal burr dimensions.
  - 4 Datum plane "H" coincident with the bottom of lead, where lead exits body (refer to [Figure 29 on page 23](#)).

Figure 29. DIP-7 package dimensions

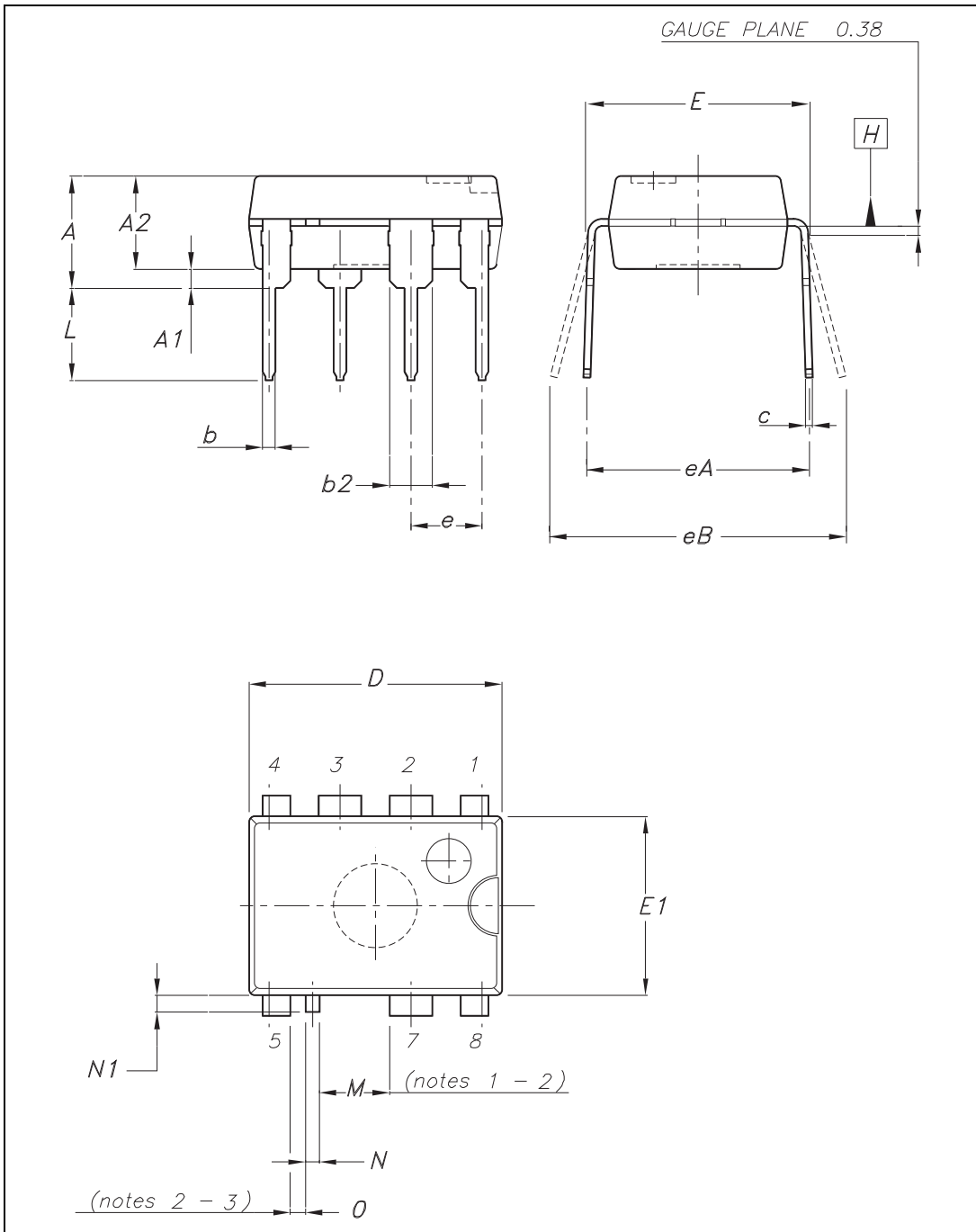
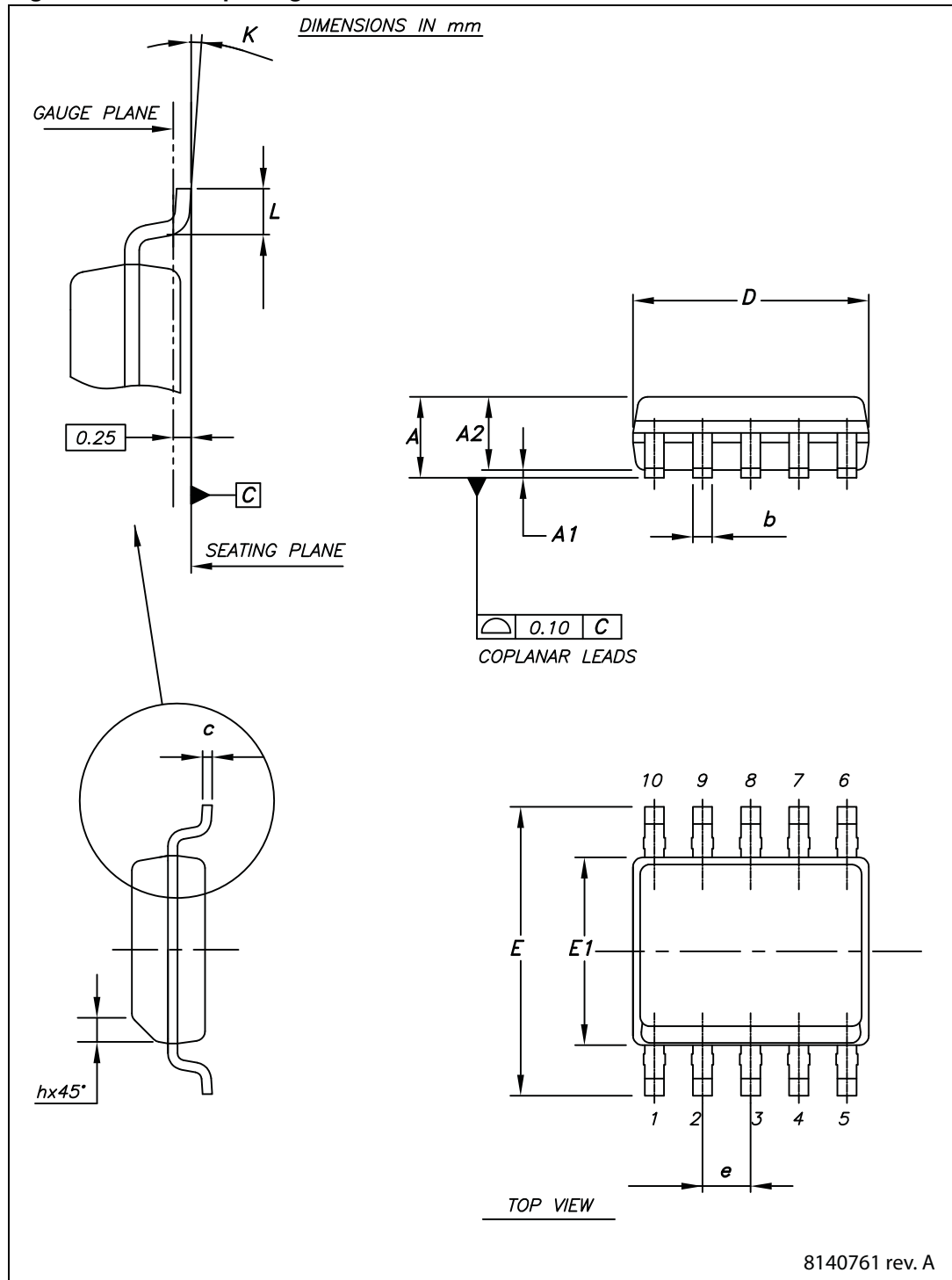


Table 9. SSO10 mechanical data

Dim.	Databook (mm.)		
	Typ	Min.	Max
A			1.75
A1		0.10	0.25
A2		1.25	
b		0.31	0.51
c		0.17	0.25
D	4.90	4.80	5
E	6	5.80	6.20
E1	3.90	3.80	4
e	1		
h		0.25	0.50
L		0.40	0.90
K		0°	8°



Figure 30. SSO10 package dimensions



## 17 Order codes

**Table 10. Ordering information**

Order code	Package	Packaging
VIPER06XN	DIP-7	Tube
VIPER06LN		
VIPER06HN		
VIPER06XS	SSO10	Tube
VIPER06XSTR		Tape and reel
VIPER06LS		Tube
VIPER06LSTR		Tape and reel
VIPER06HS		Tube
VIPER06HSTR		Tape and reel

## 18 Revision history

Table 11. Document revision history

Date	Revision	Changes
08-Mar-2012	1	Initial release.

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