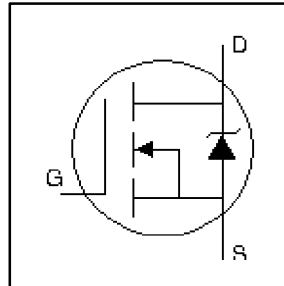


HEXFET® Power MOSFET

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30V  $V_{GS}$  Rating
- Reduced  $C_{ISS}$ ,  $C_{OSS}$ ,  $C_{RSS}$
- Isolated Central Mounting Hole
- Dynamic  $dv/dt$  Rated
- Repetitive Avalanche Rated



$$V_{DSS} = 500V$$

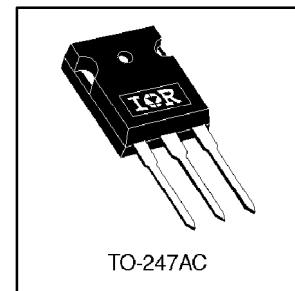
$$R_{DS(on)} = 0.27\Omega$$

$$I_D = 20A$$

**Description**

This new series of Low Charge HEXFET Power MOSFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing advanced Hexfet technology the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings. These device improvements combined with the proven ruggedness and reliability of HEXFETs offer the designer a new standard in power transistors for switching applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	20	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	12	
$I_{DM}$	Pulsed Drain Current ①	80	
$P_D @ T_C = 25^\circ C$	Power Dissipation	280	W
	Linear Derating Factor	2.2	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	960	mJ
$I_{AR}$	Avalanche Current ③	20	A
$E_{AR}$	Repetitive Avalanche Energy ①	28	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ ③	3.5	V/ns
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1Nm)	


**Thermal Resistance**

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	40	

# IRFP460LC



## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	500	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.59	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(ON)</sub>	Static Drain-to-Source On-Resistance	—	—	0.27	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 12A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	12	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 12A
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 500V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 400V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	—	120	nC	I <sub>D</sub> = 20A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	32		V <sub>DS</sub> = 400V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	49		V <sub>GS</sub> = 10V, See Fig. 6 and 13 ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	18	—		ns
t <sub>r</sub>	Rise Time	—	77	—	I <sub>D</sub> = 20A	
t <sub>d(off)</sub>	Turn-Off Delay Time	—	40	—	R <sub>G</sub> = 4.3Ω	
t <sub>f</sub>	Fall Time	—	43	—	R <sub>D</sub> = 12Ω, See Fig. 10 ④	
L <sub>D</sub>	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	13	—		
C <sub>iss</sub>	Input Capacitance	—	3600	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	440	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	39	—		f = 1.0MHz, See Fig. 5

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	20	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	80		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.8	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 20A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	570	860	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 20A
Q <sub>rr</sub>	Reverse Recovery Charge	—	6.6	9.9	μC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Notes:

① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )

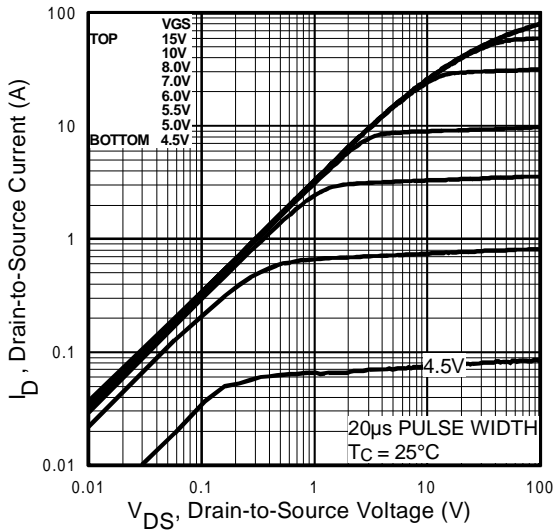
③ I<sub>SD</sub> ≤ 20A, di/dt ≤ 160A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 150°C

② V<sub>DD</sub> = 25V, starting T<sub>J</sub> = 25°C, L = 4.3mH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 20A. (See Figure 12)

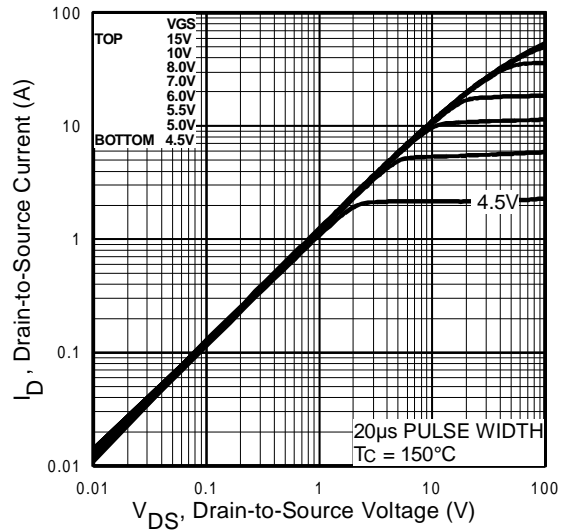
④ Pulse width ≤ 300μs; duty cycle ≤ 2%.



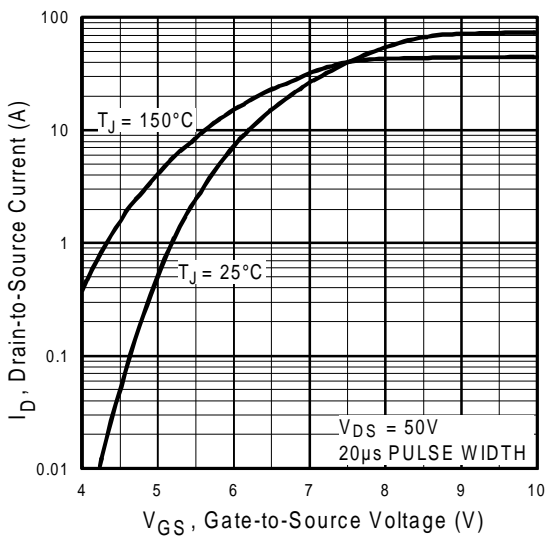
# IRFP460LC



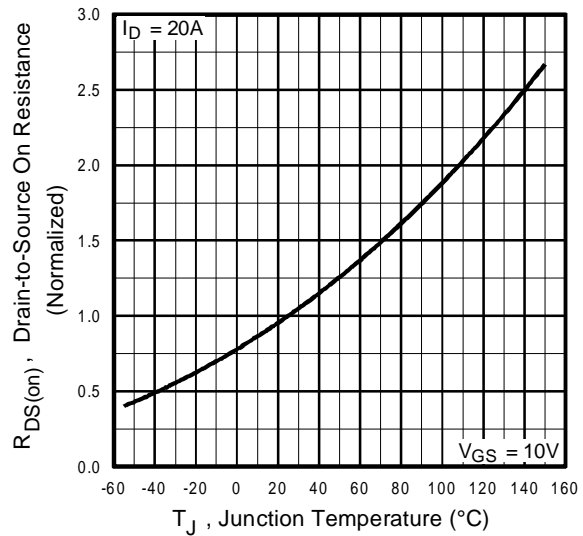
**Fig 1.** Typical Output Characteristics,  
 $T_C = 25^\circ\text{C}$



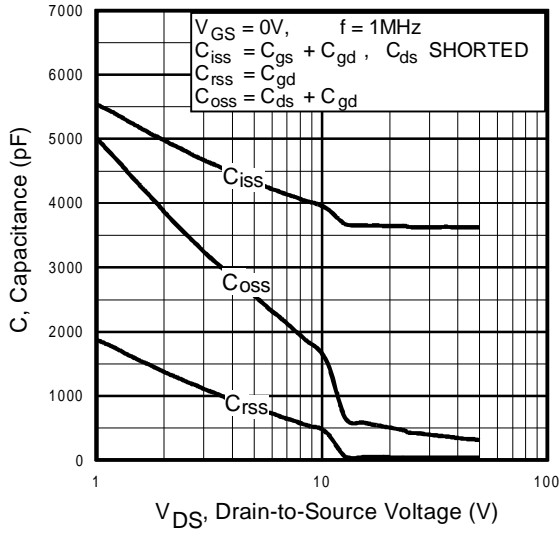
**Fig 2.** Typical Output Characteristics,  
 $T_C = 150^\circ\text{C}$



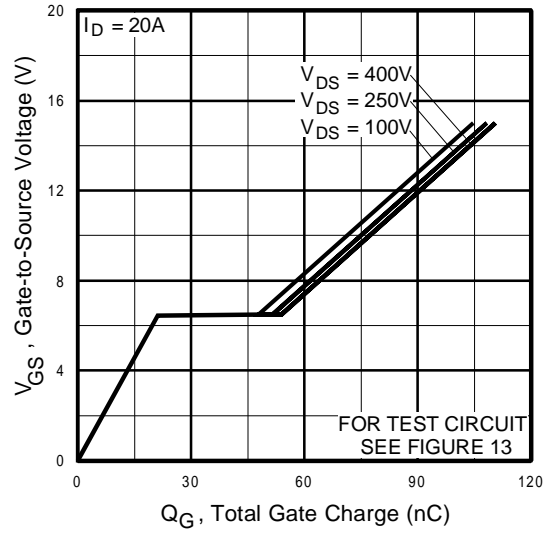
**Fig 3.** Typical Transfer Characteristics



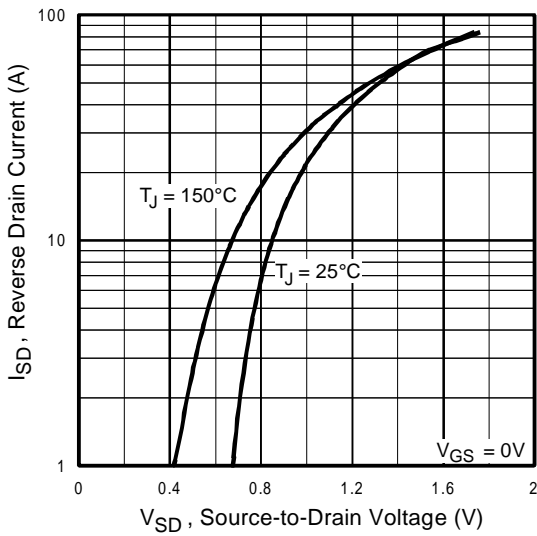
**Fig 4.** Normalized On-Resistance  
Vs. Temperature



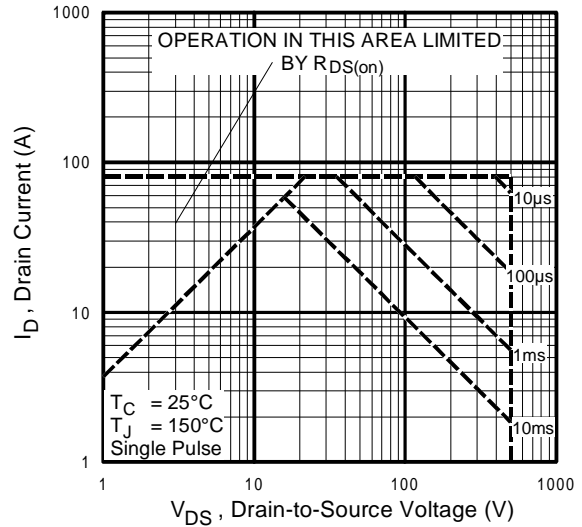
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



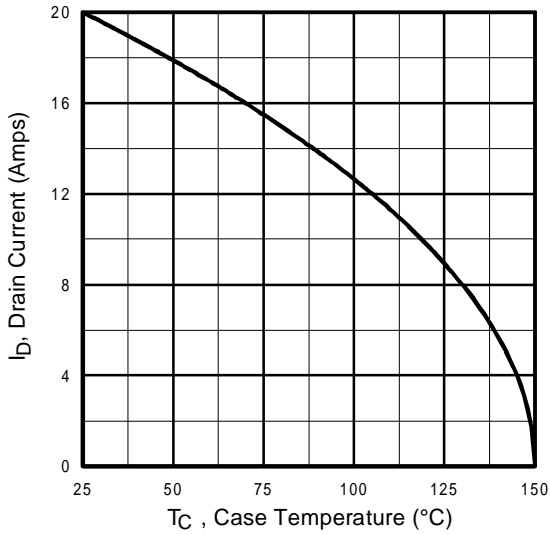
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



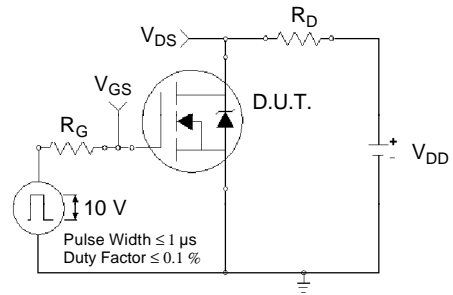
**Fig 7.** Typical Source-Drain Diode Forward Voltage



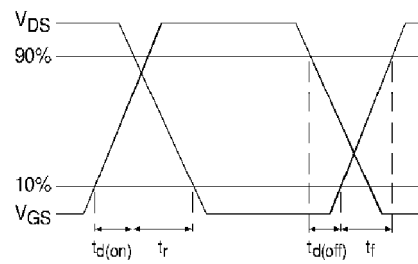
**Fig 8.** Maximum Safe Operating Area



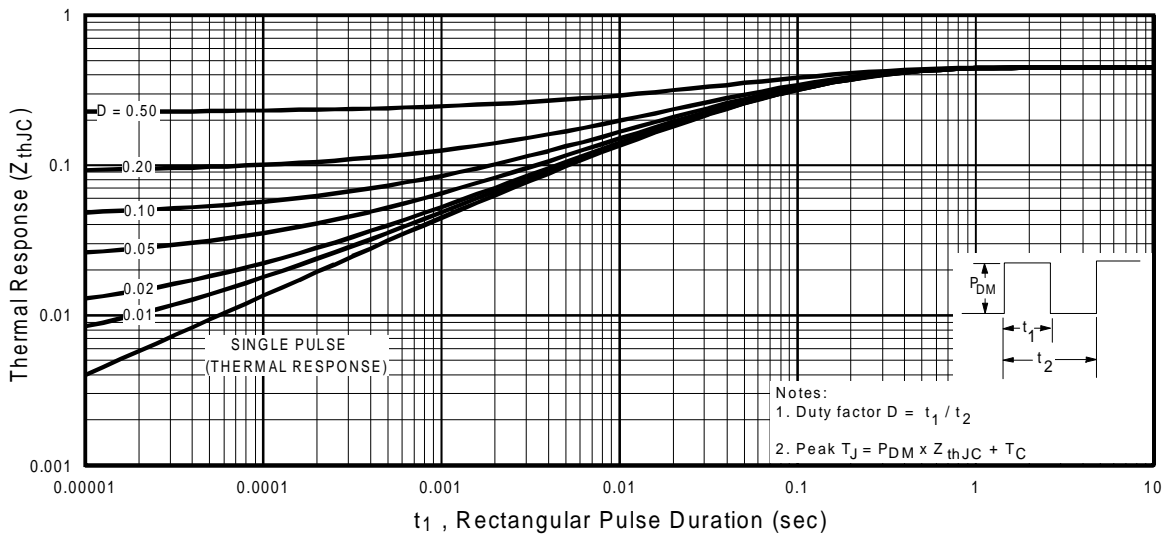
**Fig 9.** Maximum Drain Current Vs. Case Temperature



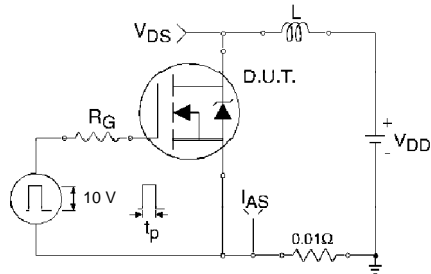
**Fig 10a.** Switching Time Test Circuit



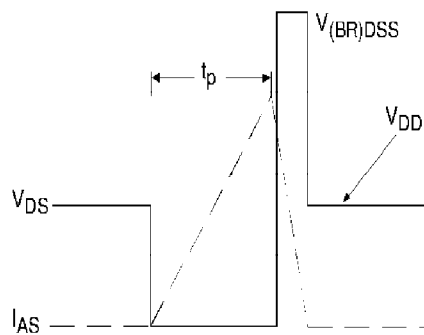
**Fig 10b.** Switching Time Waveforms



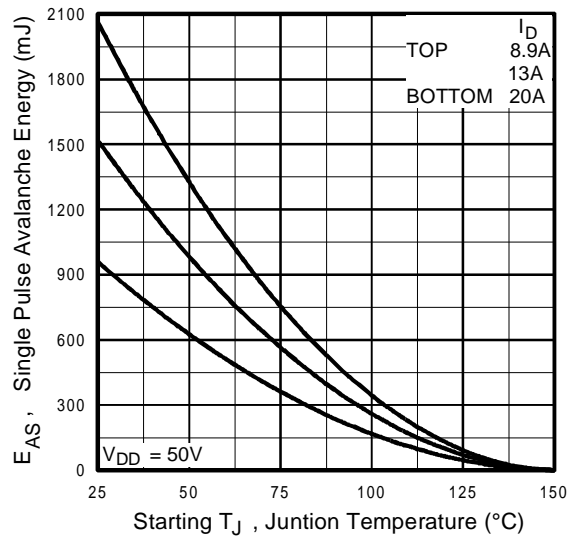
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



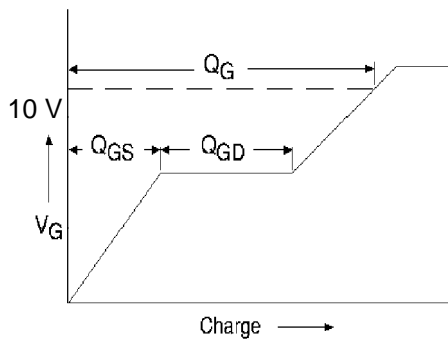
**Fig 12a.** Unclamped Inductive Test Circuit



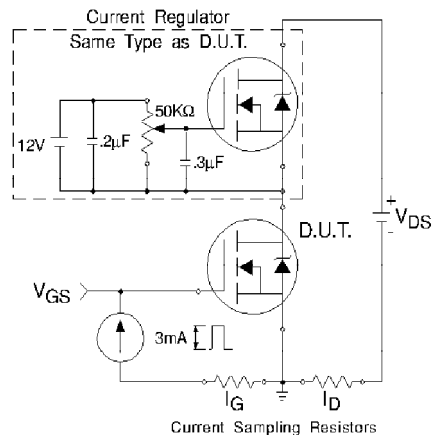
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

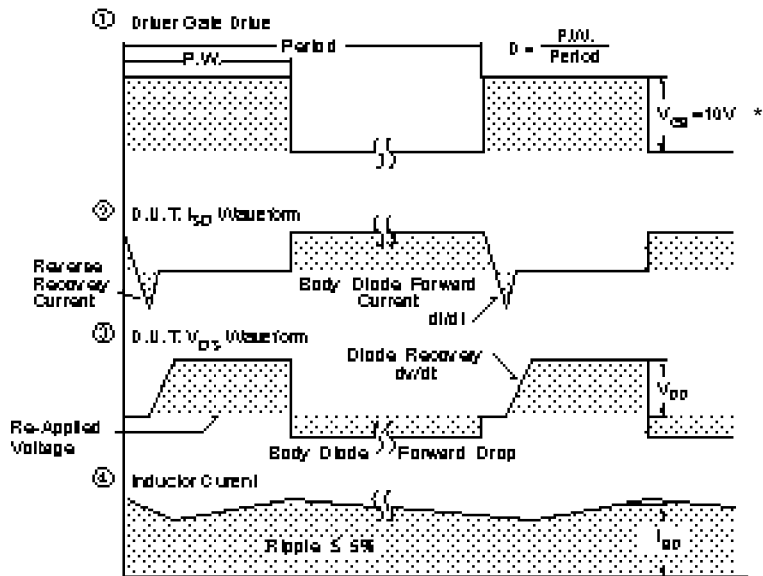
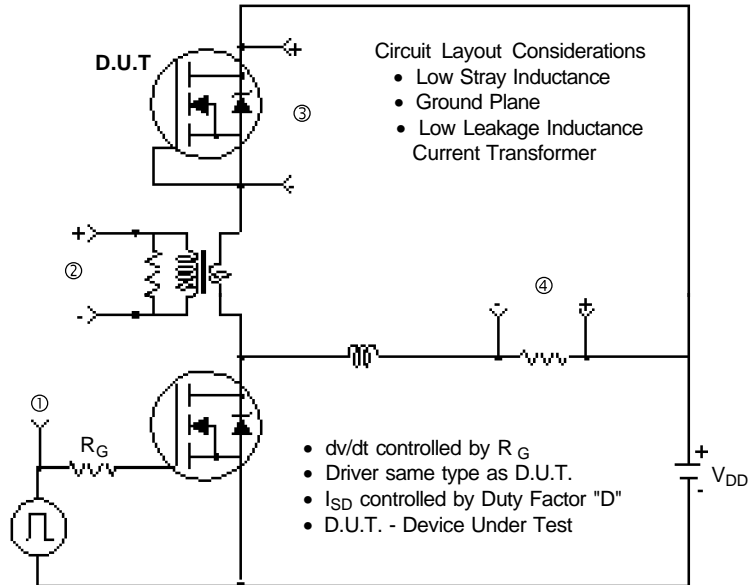


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



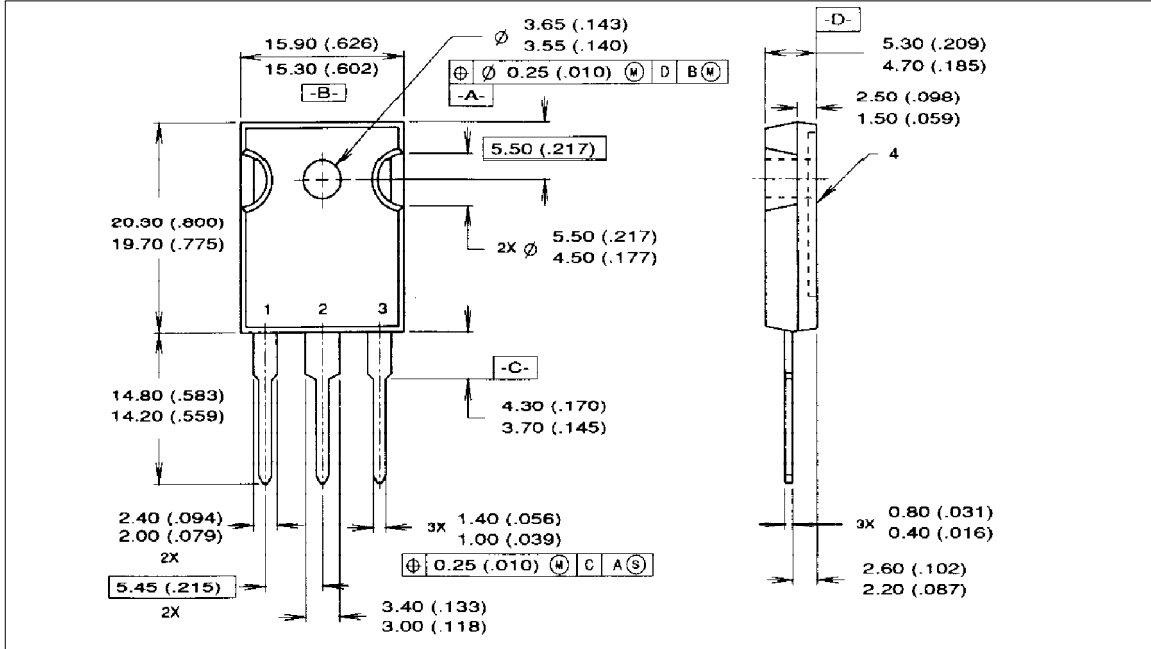
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFETS

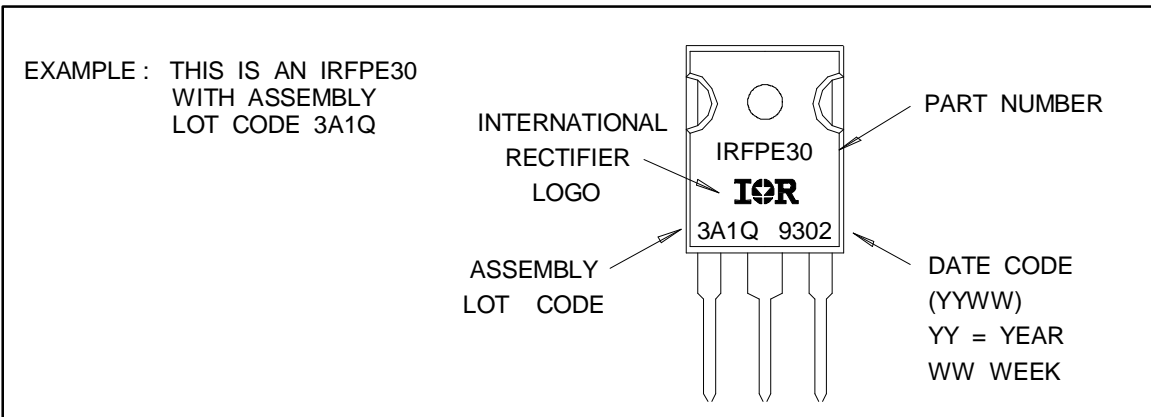
# IRF460LC



## Package Outline TO-247AC



## Part Marking Information TO-247AC



**WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331  
**EUROPEAN HEADQUARTERS:** Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: (44) 0883 713215  
**IR CANADA:** 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 3L1, Tel: (905) 475 1897  
**IR GERMANY:** Saalburgstrasse 157, 61350 Bad Homburg Tel: 6172 37066  
**IR ITALY:** Via Liguria 49, 10071 Borgaro, Torino Tel: (39) 1145 10111  
**IR FAR EAST:** K&H Bldg., 2F, 3-30-4 Nishi-Ikeburo 3-Chome, Toshima-Ki, Tokyo 171 Tel: (03)3983 0641  
**IR SOUTHEAST ASIA:** 315 Outram Road, #10-02 Tan Boon Liat Building, 0316 Tel: 65 221 8371

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