

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4516B**

## **MSI**

## **Binary up/down counter**

Product specification  
File under Integrated Circuits, IC04

January 1995

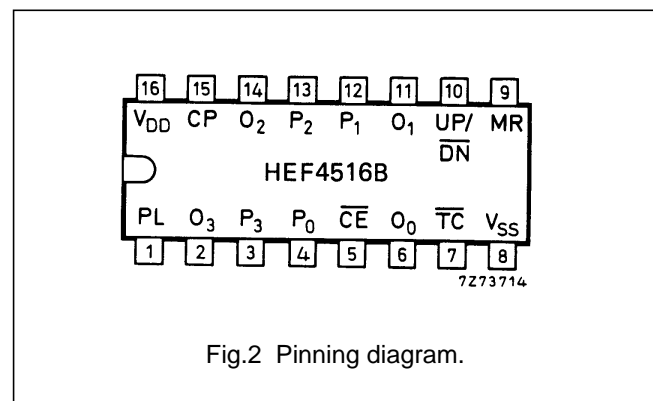
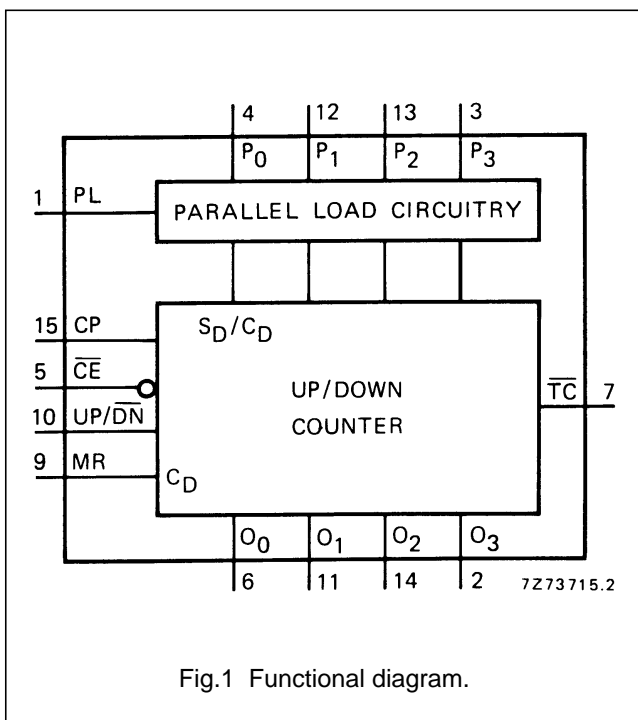
# Binary up/down counter

# HEF4516B MSI

### DESCRIPTION

The HEF4516B is an edge-triggered synchronous up/down 4-bit binary counter with a clock input (CP), an up/down count control input (UP/DN), an active LOW count enable input ( $\overline{CE}$ ), an asynchronous active HIGH parallel load input (PL), four parallel inputs (P<sub>0</sub> to P<sub>3</sub>), four parallel outputs (O<sub>0</sub> to O<sub>3</sub>), an active LOW terminal count output ( $\overline{TC}$ ), and an overriding asynchronous master reset input (MR).

Information on P<sub>0</sub> to P<sub>3</sub> is loaded into the counter while PL is HIGH, independent of all other input conditions except MR which must be LOW. When PL and  $\overline{CE}$  are LOW, the counter changes on the LOW to HIGH transition of CP. Input UP/DN determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up,  $\overline{TC}$  is LOW when O<sub>0</sub> and O<sub>3</sub> are HIGH and  $\overline{CE}$  is LOW. When counting down,  $\overline{TC}$  is LOW when O<sub>0</sub> to O<sub>3</sub> and  $\overline{CE}$  are LOW. A HIGH on MR resets the counter (O<sub>0</sub> to O<sub>3</sub> = LOW) independent of all other input conditions.



- HEF4516BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4516BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4516BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

### PINNING

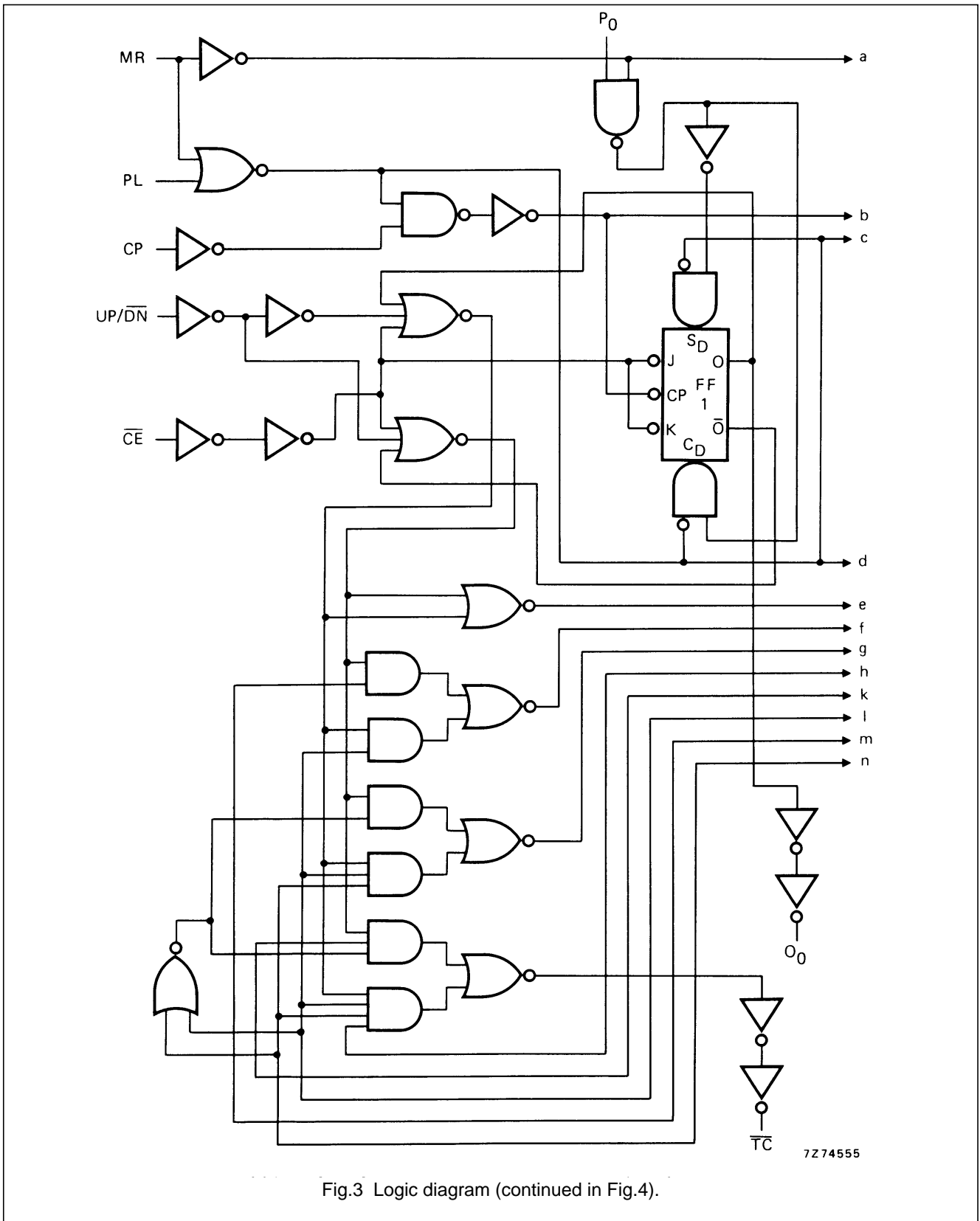
- PL parallel load input (active HIGH)
- P<sub>0</sub> to P<sub>3</sub> parallel inputs
- $\overline{CE}$  count enable input (active LOW)
- CP clock pulse input (LOW to HIGH, edge triggered)
- UP/DN up/down count control input
- MR master reset input
- $\overline{TC}$  terminal count output (active LOW)
- O<sub>0</sub> to O<sub>3</sub> parallel outputs

### FAMILY DATA, I<sub>DD</sub> LIMITS category MSI

See Family Specifications

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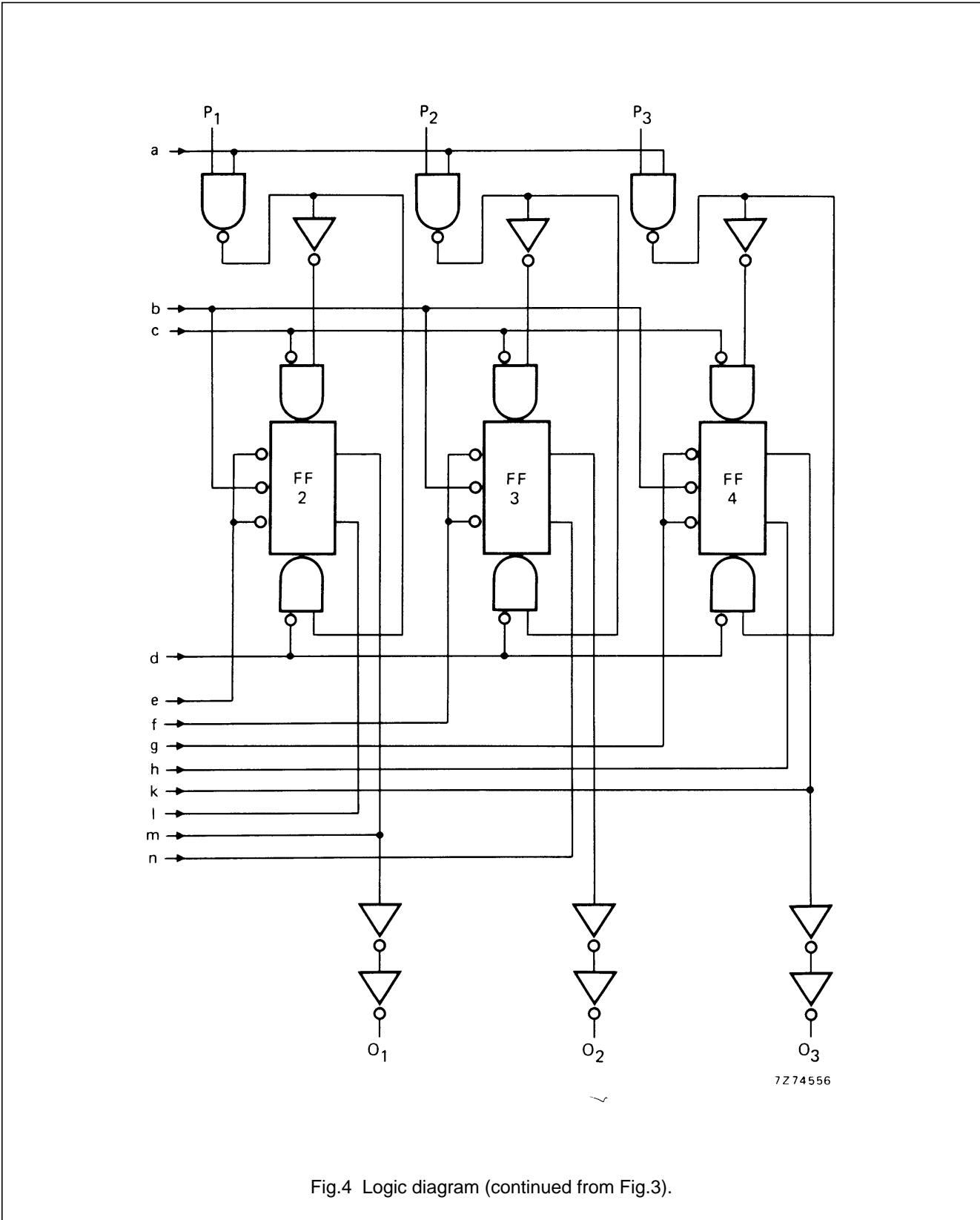


Fig.4 Logic diagram (continued from Fig.3).

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FUNCTION TABLE

| MR | PL | UP/DN | $\overline{CE}$ | CP         | MODE          |
|----|----|-------|-----------------|------------|---------------|
| L  | H  | X     | X               | X          | parallel load |
| L  | L  | X     | H               | X          | no change     |
| L  | L  | L     | L               | $\nearrow$ | count down    |
| L  | L  | H     | L               | $\searrow$ | count up      |
| H  | X  | X     | X               | X          | reset         |

Notes

- H = HIGH state (the more positive voltage)  
L = LOW state (the less positive voltage)  
X = state is immaterial  
 $\nearrow$  = positive-going transition

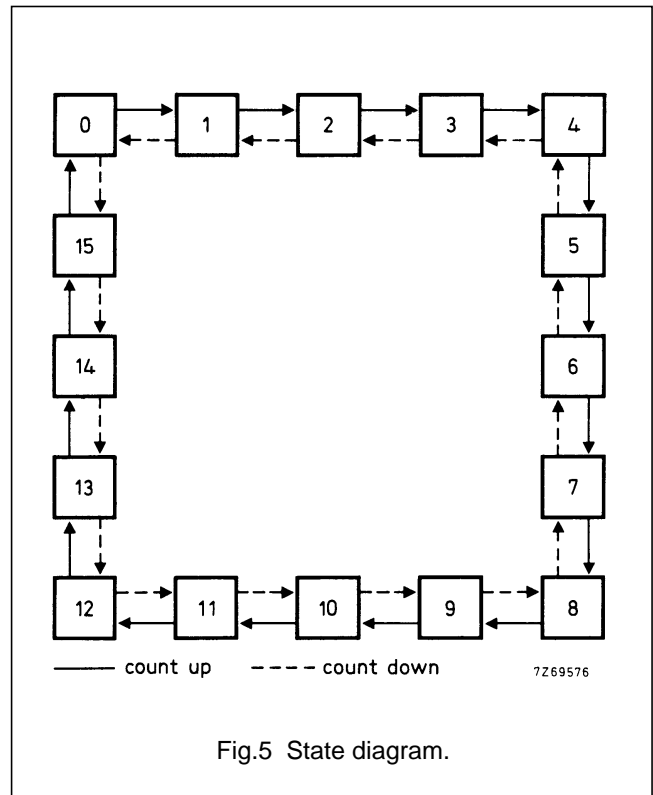


Fig.5 State diagram.

Logic equation for terminal count:

$$\overline{TC} = \overline{CE} \cdot \{ (UP/DN) \cdot O_0 \cdot O_1 \cdot O_2 \cdot O_3 + (\overline{UP/DN}) \cdot \overline{O_0} \cdot \overline{O_1} \cdot \overline{O_2} \cdot \overline{O_3} \}$$

AC CHARACTERISTICS

$V_{SS} = 0 V$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; input transition times  $\leq 20 \text{ ns}$

|   | $V_{DD}$<br>V | TYPICAL FORMULA FOR P ( $\mu\text{W}$ )  |   |
|---|---------------|--|---|
| Dynamic power dissipation per package (P) | 5<br>10<br>15 | $1000 f_i + \sum (f_o C_L) \times V_{DD}^2$<br>$4500 f_i + \sum (f_o C_L) \times V_{DD}^2$<br>$11\ 200 f_i + \sum (f_o C_L) \times V_{DD}^2$ | where<br>$f_i$ = input freq. (MHz)<br>$f_o$ = output freq. (MHz)<br>$C_L$ = load capacitance (pF)<br>$\sum (f_o C_L)$ = sum of outputs<br>$V_{DD}$ = supply voltage (V) |

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## AC CHARACTERISTICS

 $V_{SS} = 0$  V;  $T_{amb} = 25$  °C;  $C_L = 50$  pF; input transition times  $\leq 20$  ns

|   | $V_{DD}$<br>V | SYMBOL    | MIN. | TYP. | MAX.   | TYPICAL EXTRAPOLATION<br>FORMULA |
|---|---------------|-----------|------|------|--------|----------------------------------|
| Propagation delays                        |               |           |      |      |        |                                  |
| CP $\rightarrow$ $O_n$                    | 5             |           |      | 145  | 290 ns | 118 ns + (0,55 ns/pF) $C_L$      |
| HIGH to LOW                               | 10            | $t_{PHL}$ |      | 60   | 120 ns | 49 ns + (0,23 ns/pF) $C_L$       |
|   | 15            |           |      | 45   | 90 ns  | 37 ns + (0,16 ns/pF) $C_L$       |
| LOW to HIGH                               | 5             | $t_{PLH}$ |      | 155  | 310 ns | 128 ns + (0,55 ns/pF) $C_L$      |
|   | 10            |           |      | 65   | 130 ns | 54 ns + (0,23 ns/pF) $C_L$       |
|   | 15            |           |      | 45   | 90 ns  | 37 ns + (0,16 ns/pF) $C_L$       |
| CP $\rightarrow$ $\overline{TC}$          | 5             |           |      | 260  | 525 ns | 233 ns + (0,55 ns/pF) $C_L$      |
| HIGH to LOW                               | 10            | $t_{PHL}$ |      | 105  | 210 ns | 94 ns + (0,23 ns/pF) $C_L$       |
|   | 15            |           |      | 75   | 150 ns | 67 ns + (0,16 ns/pF) $C_L$       |
| LOW to HIGH                               | 5             | $t_{PLH}$ |      | 180  | 360 ns | 153 ns + (0,55 ns/pF) $C_L$      |
|   | 10            |           |      | 75   | 150 ns | 64 ns + (0,23 ns/pF) $C_L$       |
|   | 15            |           |      | 55   | 115 ns | 47 ns + (0,16 ns/pF) $C_L$       |
| PL $\rightarrow$ $O_n$                    | 5             |           |      | 125  | 255 ns | 98 ns + (0,55 ns/pF) $C_L$       |
| HIGH to LOW                               | 10            | $t_{PHL}$ |      | 55   | 110 ns | 44 ns + (0,23 ns/pF) $C_L$       |
|   | 15            |           |      | 40   | 85 ns  | 32 ns + (0,16 ns/pF) $C_L$       |
| LOW to HIGH                               | 5             | $t_{PLH}$ |      | 170  | 340 ns | 143 ns + (0,55 ns/pF) $C_L$      |
|   | 10            |           |      | 70   | 140 ns | 59 ns + (0,23 ns/pF) $C_L$       |
|   | 15            |           |      | 50   | 105 ns | 42 ns + (0,16 ns/pF) $C_L$       |
| PL $\rightarrow$ $\overline{TC}$          | 5             |           |      | 250  | 500 ns | 223 ns + (0,55 ns/pF) $C_L$      |
| HIGH to LOW                               | 10            | $t_{PHL}$ |      | 110  | 220 ns | 99 ns + (0,23 ns/pF) $C_L$       |
|   | 15            |           |      | 80   | 160 ns | 72 ns + (0,16 ns/pF) $C_L$       |
| LOW to HIGH                               | 5             | $t_{PLH}$ |      | 250  | 500 ns | 223 ns + (0,55 ns/pF) $C_L$      |
|   | 10            |           |      | 110  | 220 ns | 99 ns + (0,23 ns/pF) $C_L$       |
|   | 15            |           |      | 80   | 160 ns | 72 ns + (0,16 ns/pF) $C_L$       |
| $\overline{CE} \rightarrow \overline{TC}$ | 5             |           |      | 165  | 330 ns | 138 ns + (0,55 ns/pF) $C_L$      |
| HIGH to LOW                               | 10            | $t_{PHL}$ |      | 65   | 135 ns | 54 ns + (0,23 ns/pF) $C_L$       |
|   | 15            |           |      | 50   | 100 ns | 42 ns + (0,16 ns/pF) $C_L$       |
| LOW to HIGH                               | 5             | $t_{PLH}$ |      | 145  | 290 ns | 118 ns + (0,55 ns/pF) $C_L$      |
|   | 10            |           |      | 60   | 125 ns | 49 ns + (0,23 ns/pF) $C_L$       |
|   | 15            |           |      | 45   | 95 ns  | 37 ns + (0,16 ns/pF) $C_L$       |
| MR $\rightarrow$ $O_n, \overline{TC}$     | 5             |           |      | 205  | 405 ns | 178 ns + (0,55 ns/pF) $C_L$      |
| HIGH to LOW                               | 10            | $t_{PHL}$ |      | 65   | 130 ns | 54 ns + (0,23 ns/pF) $C_L$       |
|   | 15            |           |      | 45   | 85 ns  | 37 ns + (0,16 ns/pF) $C_L$       |
| MR $\rightarrow$ $\overline{TC}$          | 5             |           |      | 225  | 450 ns | 198 ns + (0,55 ns/pF) $C_L$      |
| LOW to HIGH                               | 10            | $t_{PLH}$ |      | 75   | 150 ns | 64 ns + (0,23 ns/pF) $C_L$       |
|   | 15            |           |      | 50   | 100 ns | 42 ns + (0,16 ns/pF) $C_L$       |

## Binary up/down counter

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MSI**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$ 

|  | $V_{DD}$<br>V | SYMBOL    | MIN. | TYP. | MAX.   | TYPICAL<br>EXTRAPOLATION<br>FORMULA     |
|--|---------------|-----------|------|------|--------|---|
| Output transition times<br>HIGH to LOW | 5             | $t_{THL}$ |      | 60   | 120 ns | $10\text{ ns} + (1,0\text{ ns/pF}) C_L$ |
|  | 10            |           |      | 30   | 60 ns  | $9\text{ ns} + (0,42\text{ ns/pF}) C_L$ |
|  | 15            |           |      | 20   | 40 ns  | $6\text{ ns} + (0,28\text{ ns/pF}) C_L$ |
| LOW to HIGH                            | 5             | $t_{TLH}$ |      | 60   | 120 ns | $10\text{ ns} + (1,0\text{ ns/pF}) C_L$ |
|  | 10            |           |      | 30   | 60 ns  | $9\text{ ns} + (0,42\text{ ns/pF}) C_L$ |
|  | 15            |           |      | 20   | 40 ns  | $6\text{ ns} + (0,28\text{ ns/pF}) C_L$ |

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|                                   | V <sub>DD</sub><br>V | SYMBOL            | MIN. | TYP. | MAX. | TYPICAL<br>EXTRAPOLATION<br>FORMULA |    |
|-----------------------------------|----------------------|-------------------|------|------|------|-------------------------------------|----|
| Minimum clock<br>pulse width; LOW | 5                    | t <sub>WCPL</sub> | 95   | 45   | ns   | see also waveforms<br>Figs 6 and 7  |    |
|                                   | 10                   |                   | 35   | 20   | ns   |                                     |    |
|                                   | 15                   |                   | 25   | 15   | ns   |                                     |    |
| Minimum PL<br>pulse width; HIGH   | 5                    | t <sub>WPLH</sub> | 105  | 55   | ns   |                                     |    |
|                                   | 10                   |                   | 45   | 25   | ns   |                                     |    |
|                                   | 15                   |                   | 35   | 15   | ns   |                                     |    |
| Minimum MR<br>pulse width; HIGH   | 5                    | t <sub>WMRH</sub> | 120  | 60   | ns   |                                     |    |
|                                   | 10                   |                   | 50   | 25   | ns   |                                     |    |
|                                   | 15                   |                   | 40   | 20   | ns   |                                     |    |
| Recovery time<br>for MR           | 5                    | t <sub>RMR</sub>  | 130  | 65   | ns   |                                     |    |
|                                   | 10                   |                   | 45   | 20   | ns   |                                     |    |
|                                   | 15                   |                   | 30   | 15   | ns   |                                     |    |
| Recovery time<br>for PL           | 5                    | t <sub>RPL</sub>  | 150  | 75   | ns   |                                     |    |
|                                   | 10                   |                   | 50   | 25   | ns   |                                     |    |
|                                   | 15                   |                   | 30   | 15   | ns   |                                     |    |
| Set-up times                      | P <sub>n</sub> → PL  | t <sub>su</sub>   | 100  | 50   | ns   |                                     |    |
|                                   |                      |                   | 10   | 50   | 25   |                                     | ns |
|                                   |                      |                   | 15   | 40   | 20   |                                     | ns |
|                                   | UP/DN → CP           | t <sub>su</sub>   | 5    | 250  | 125  |                                     | ns |
|                                   |                      |                   | 10   | 100  | 50   |                                     | ns |
|                                   |                      |                   | 15   | 75   | 35   |                                     | ns |
|                                   | CE → CP              | t <sub>su</sub>   | 5    | 120  | 60   | ns                                  |    |
|                                   |                      |                   | 10   | 40   | 20   | ns                                  |    |
|                                   |                      |                   | 15   | 25   | 10   | ns                                  |    |
| Hold times                        | P <sub>n</sub> → PL  | t <sub>hold</sub> | 10   | -40  | ns   |                                     |    |
|                                   |                      |                   | 10   | 5    | -20  | ns                                  |    |
|                                   |                      |                   | 15   | 0    | -20  | ns                                  |    |
|                                   | UP/DN → CP           | t <sub>hold</sub> | 5    | 35   | -90  | ns                                  |    |
|                                   |                      |                   | 10   | 15   | -35  | ns                                  |    |
|                                   |                      |                   | 15   | 15   | -25  | ns                                  |    |
|                                   | CE → CP              | t <sub>hold</sub> | 5    | 20   | -40  | ns                                  |    |
|                                   |                      |                   | 10   | 5    | -15  | ns                                  |    |
|                                   |                      |                   | 15   | 5    | -10  | ns                                  |    |
| Maximum clock<br>pulse frequency  | 5                    | f <sub>max</sub>  | 3    | 6    | MHz  |                                     |    |
|                                   | 10                   |                   | 7    | 14   | MHz  |                                     |    |
|                                   | 15                   |                   | 9    | 18   | MHz  |                                     |    |



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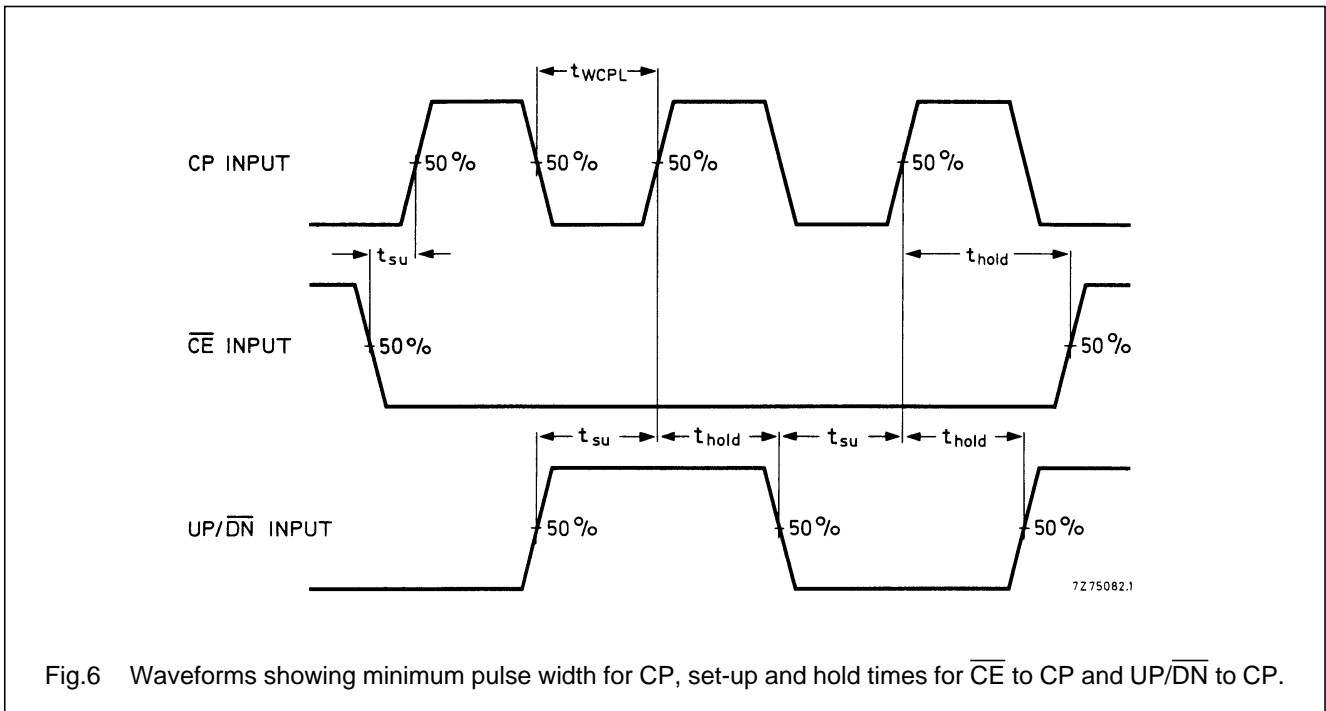


Fig.6 Waveforms showing minimum pulse width for CP, set-up and hold times for  $\overline{CE}$  to CP and UP/ $\overline{DN}$  to CP.

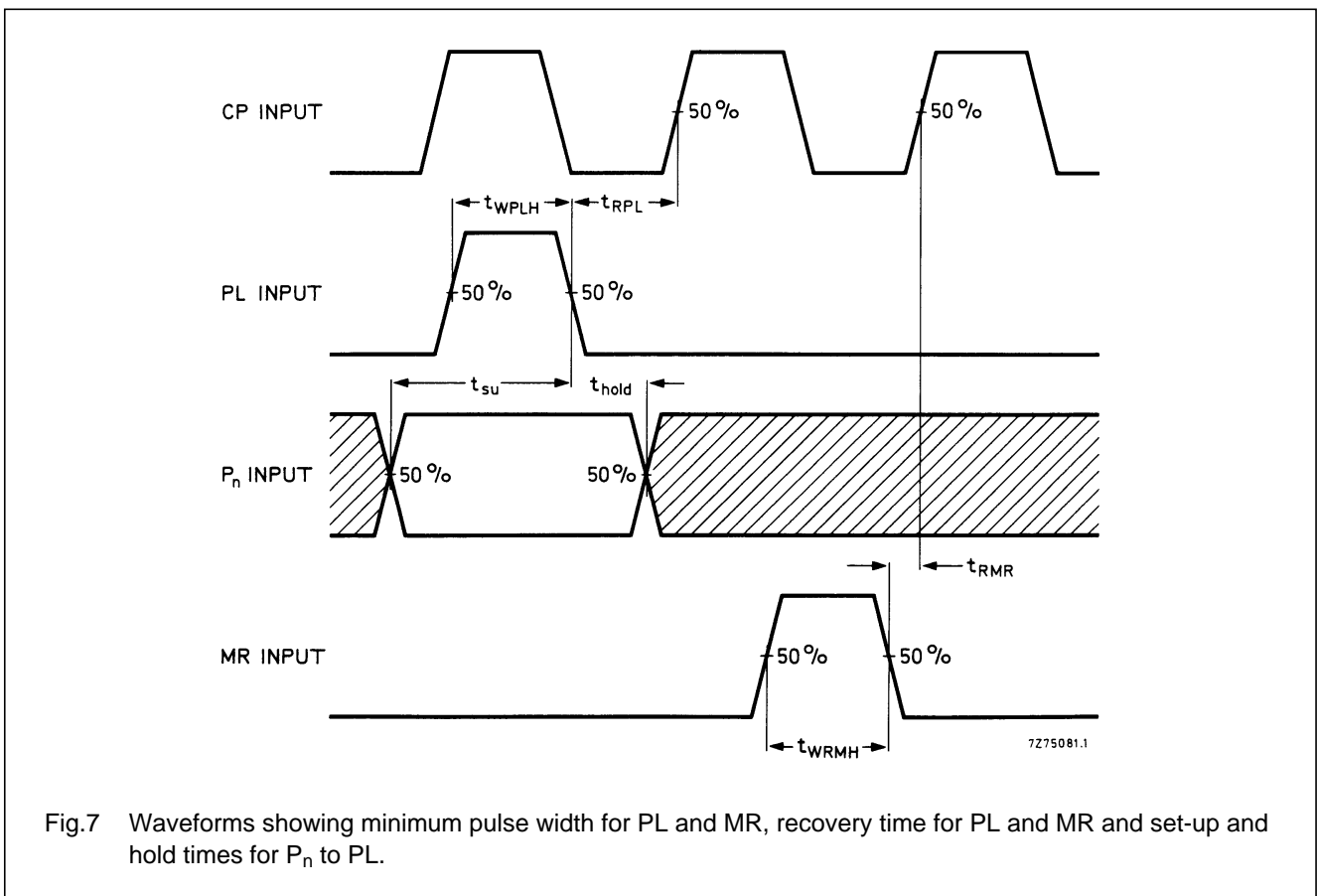


Fig.7 Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR and set-up and hold times for  $P_n$  to PL.

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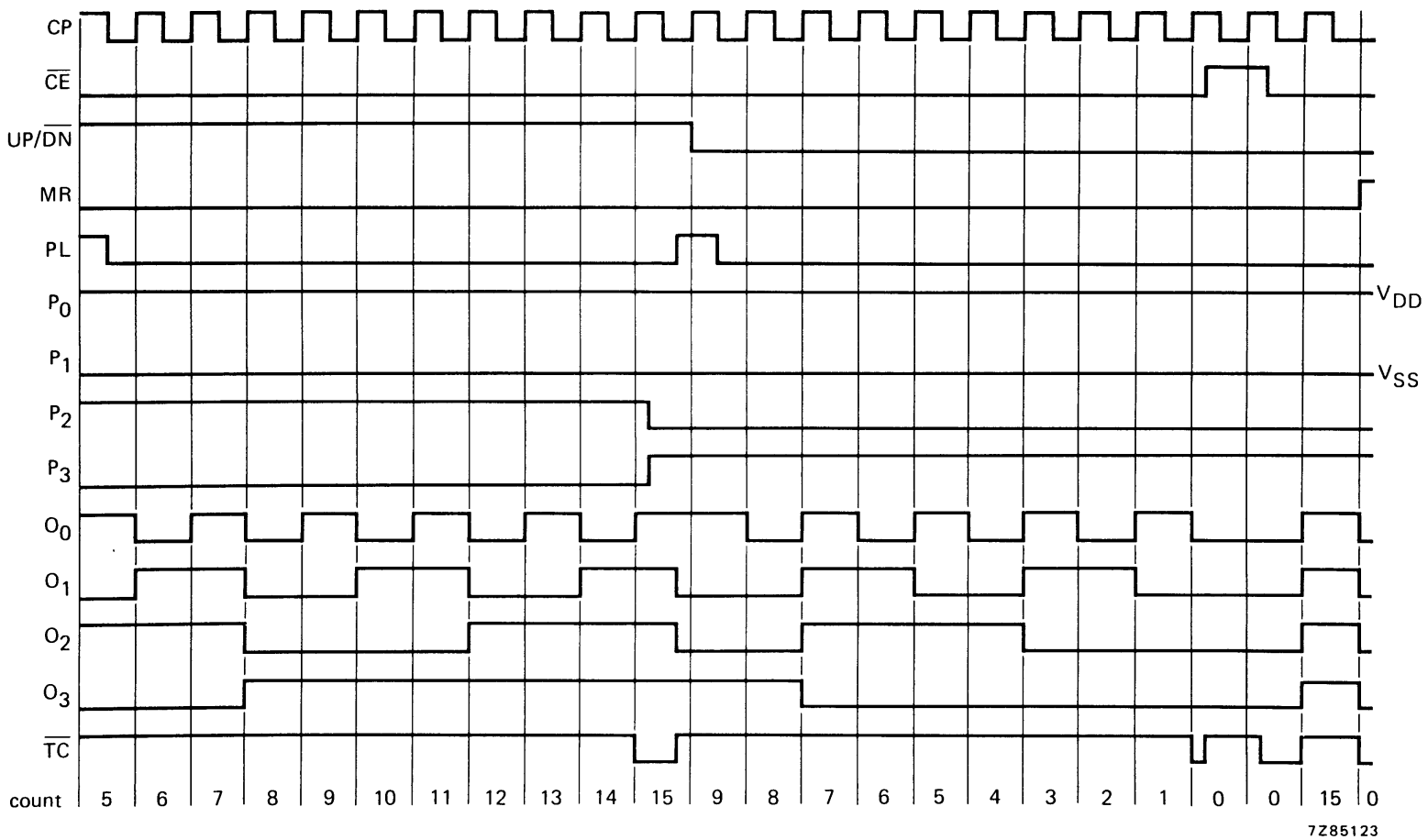


Fig.8 Timing diagram.