

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40098B **buffers** 3-state hex inverting buffer

Product specification
File under Integrated Circuits, IC04

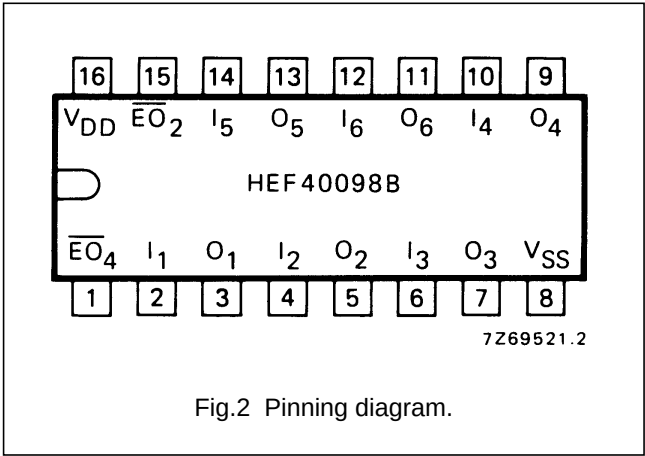
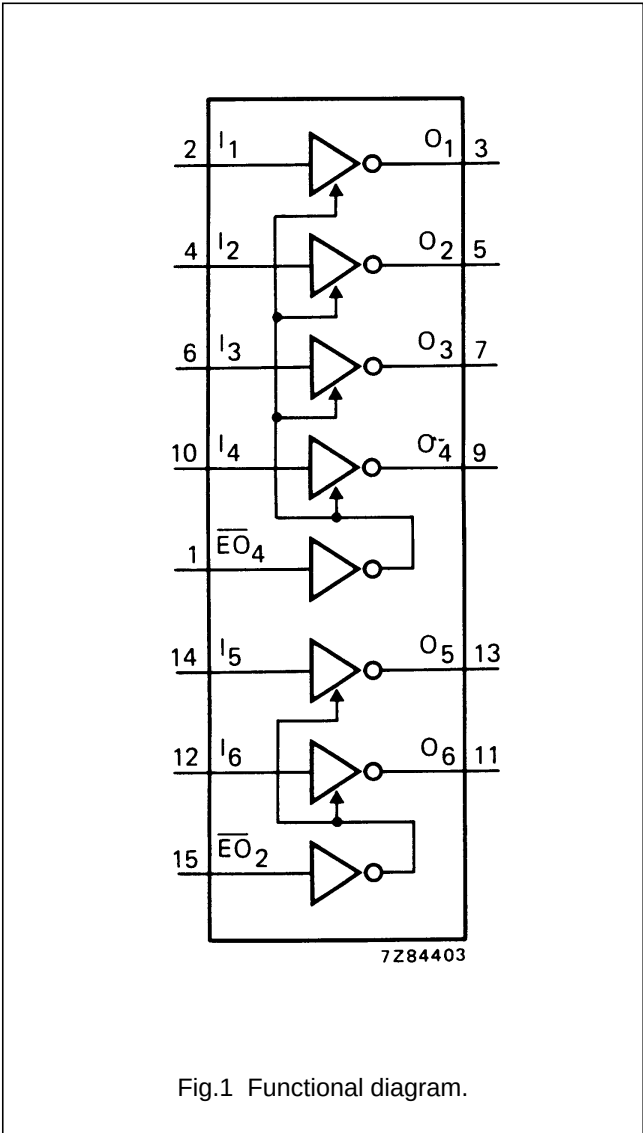
January 1995

3-state hex inverting buffer

HEF40098B
buffers

DESCRIPTION

The HEF40098B is a hex inverting buffer with 3-state outputs. The 3-state outputs are controlled by two enable inputs ($\overline{EO}_4$ and $\overline{EO}_2$). A HIGH on $\overline{EO}_4$ causes four of the six buffer elements to assume a high impedance or OFF-state regardless of the other input conditions and a HIGH on $\overline{EO}_2$ causes the outputs of the remaining two buffer elements to assume a high impedance or OFF-state regardless of the other input conditions.



- HEF40098BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF40098BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF40098BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

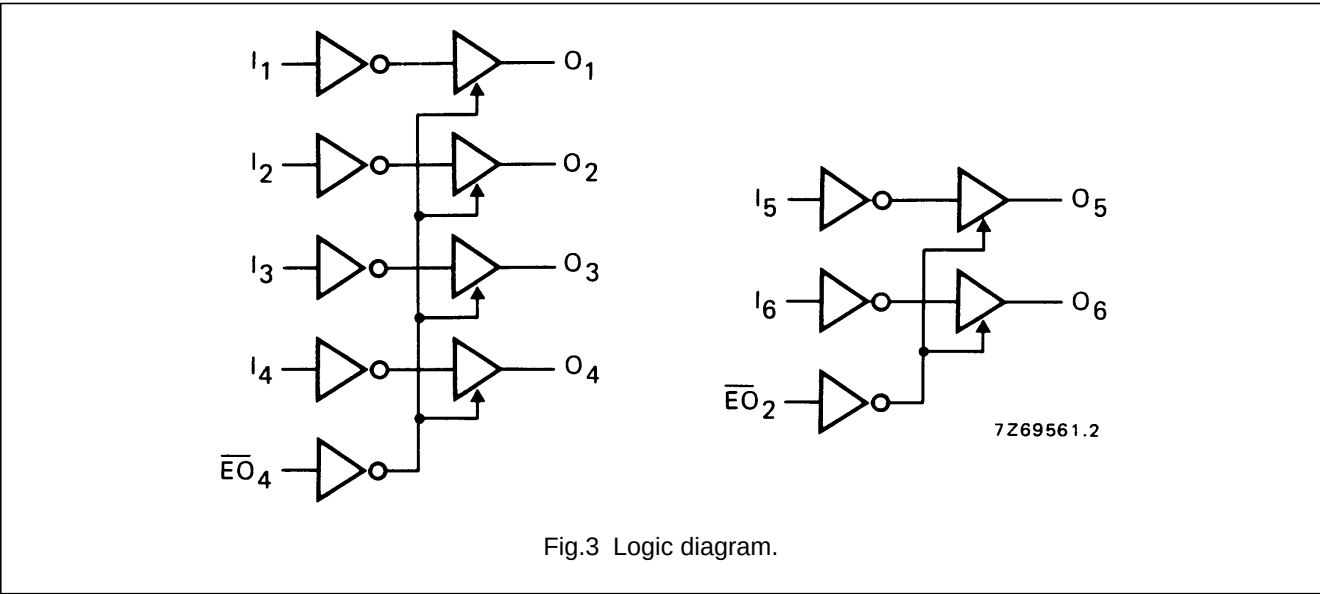
- I_1 to I_6 buffer inputs
- $\overline{EO}_4$, $\overline{EO}_2$ enable inputs (active LOW)
- O_1 to O_6 buffer outputs (active LOW)

FAMILY DATA, I_{DD} LIMITS category BUFFERS

See Family Specifications

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DC CHARACTERISTICS

V_{SS} = 0 V

HEF	V _{DD} V	V _{OH} V	V _{OL} V	SYMBOL	T _{amb} (°C)					
					-40		+25		+85	
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Output current HIGH	5	4,6		-I _{OH}	1,2		1,0		0,8	mA
	10	9,5			3,8		3,2		2,5	mA
	15	13,5			12,0		10,0		8,0	mA
HIGH	5	2,5		-I _{OH}	3,8		3,2		2,5	mA
Output current LOW	4,75		0,4	I _{OL}	3,5		2,9		2,3	mA
	10		0,5		12,0		10,0		8,0	mA
	15		1,5		24,0		20,0		16,0	mA

HEC	V _{DD} V	V _{OH} V	V _{OL} V	SYMBOL	T _{amb} (°C)					
					-55		+25		+125	
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Output current HIGH	5	4,6		-I _{OH}	1,25		1,0		0,6	mA
	10	9,5			4,0		3,2		2,1	mA
	15	12,5			12,5		10,0		6,7	mA
HIGH	5	2,5		-I _{OH}	4,0		3,2		2,1	mA
Output current LOW	4,75		0,4	I _{OL}	3,6		2,9		1,9	mA
	10		0,5		12,5		10,0		6,7	mA
	15		1,5		25,0		20,0		13,0	mA

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AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5 10 15	t_{PHL}	80 35 25	160 70 50 ns	$70\text{ ns} + (0,20\text{ ns/pF}) C_L$ $31\text{ ns} + (0,08\text{ ns/pF}) C_L$ $22\text{ ns} + (0,06\text{ ns/pF}) C_L$
LOW to HIGH	5 10 15	t_{PLH}	65 30 25	130 60 50 ns	$50\text{ ns} + (0,30\text{ ns/pF}) C_L$ $24\text{ ns} + (0,13\text{ ns/pF}) C_L$ $23\text{ ns} + (0,05\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5 10 15	t_{THL}	30 15 10	60 30 20 ns	$15\text{ ns} + (0,30\text{ ns/pF}) C_L$ $10\text{ ns} + (0,11\text{ ns/pF}) C_L$ $7\text{ ns} + (0,07\text{ ns/pF}) C_L$
LOW to HIGH	5 10 15	t_{TLH}	35 20 15	70 40 30 ns	$10\text{ ns} + (0,50\text{ ns/pF}) C_L$ $8\text{ ns} + (0,24\text{ ns/pF}) C_L$ $6\text{ ns} + (0,18\text{ ns/pF}) C_L$
3-state propagation delays Output disable times $\overline{EO}_2, \overline{EO}_4 \rightarrow O_n$ HIGH	5 10 15	t_{PHZ}	45 35 30	85 65 60 ns	
LOW	5 10 15	t_{PLZ}	65 40 35	135 80 70 ns	
Output enable times $\overline{EO}_2, \overline{EO}_4 \rightarrow O_n$ HIGH	5 10 15	t_{PZH}	70 35 30	140 75 65 ns	
LOW	5 10 15	t_{PZL}	90 40 35	185 85 70 ns	

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	$5\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$ $22\,800 f_i + \sum (f_o C_L) \times V_{DD}^2$ $81\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)