TEXAS INSTRUMENTS

**SN74CBTLV3257-EP**

SCDS271A – MAY 2008 – REVISED MAY 2019

# SN74CBTLV3257-EP Low-Voltage 4-Bit 1-of-2 FET Multiplexer/Demultiplexer

## 1 Features

- Controlled baseline
  - One assembly site
  - One test site
  - One fabrication site
- Extended temperature performance of –55°C to 125°C
- Enhanced diminishing manufacturing sources (DMS) support
- Enhanced product-change notification
- Qualification pedigree [1]
- 5-Ω switch connection between two ports
- Rail-to-rail switching on data I/O ports
- $I_{off}$ supports partial-power-down mode operation
- Latch-up performance exceeds 100 mA per JESD 78, class II
- ESD protection exceeds JESD 22
  - 2000-V human-body model (A114-A)
  - 200-V machine model (A115-A)

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

## 2 Applications

- Supports defense, aerospace, and medical applications

## 3 Description

The SN74CBTLV3257 is a 4-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The select (S) input controls the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable ($\overline{OE}$) input is high.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ feature ensures that damaging current does not backflow through the device when it is powered down. The device has isolation during power off.
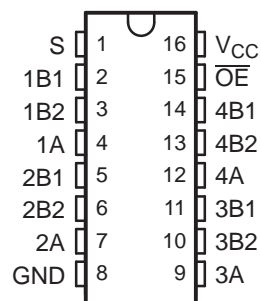
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### Device Information[1]

| PART NUMBER | GRADE | PACKAGE |
|---|---|---|
| CCBTLV3257MPWREP | $T_A$ = –55°C to 125°C | TSSOP – PW Tape and Reel |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**PW PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| S | 1 | 16 | $V_{CC}$ |
| 1B1 | 2 | 15 | $\overline{OE}$ |
| 1B2 | 3 | 14 | 4B1 |
| 1A | 4 | 13 | 4B2 |
| 2B1 | 5 | 12 | 4A |
| 2B2 | 6 | 11 | 3B1 |
| 2A | 7 | 10 | 3B2 |
| GND | 8 | 9 | 3A |

# Table of Contents

# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Original (May 2008) to Revision A** **Page**

* Changed *ORDERING INFORMATION* table to *Device Information* table.................................................................................. 1

* Added *Applications* section, *Table of Contents*, *Revision History* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.................................................................................. 1

## 5 Pin Configuration and Functions

**Table 1. Function Table**

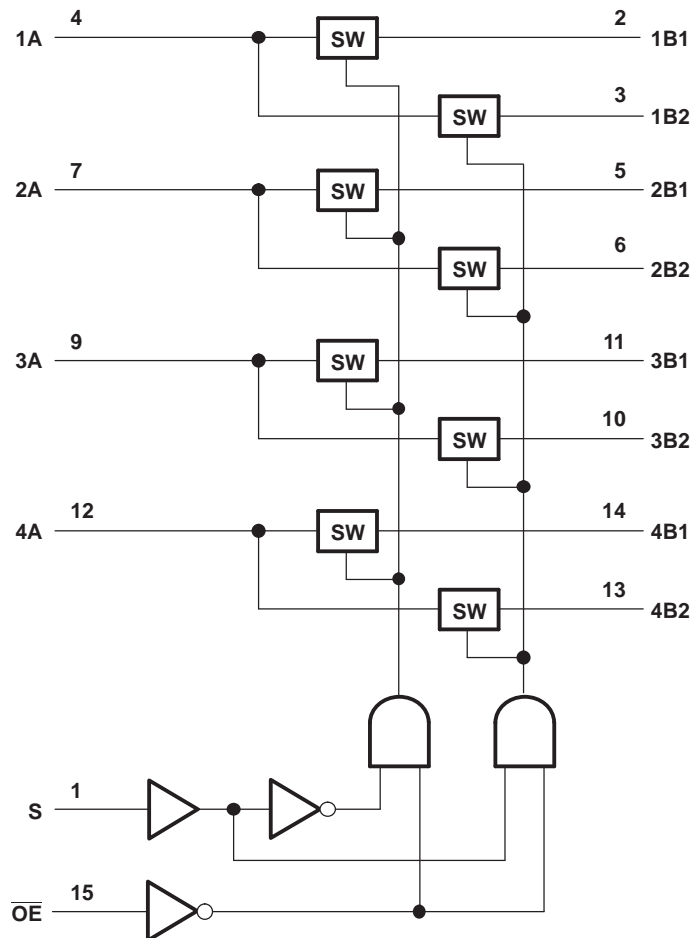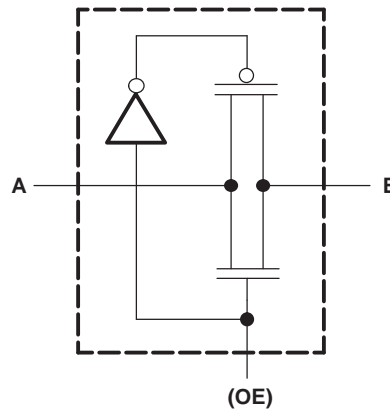| INPUTS | | FUNCTION |
|---|---|---|
| $\overline{OE}$ | S | |
| L | L | A port = B1 port |
| L | H | A port = B2 port |
| H | X | Disconnect |



**Figure 1.  Logic Diagram (Positive Logic)**

**Figure 2. Simplified Schematic, Each FET Switch**

# 6 Specifications

## 6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

|  |  |  | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 | 4.6 | V |
| $V_I$ | Input voltage[2] | | −0.5 | 4.6 | V |
| | Continuous channel current | | | 128 | mA |
| $I_{IK}$ | Input clamp current | $V_{IO} < 0$ | | −50 | mA |
| $\theta_{JA}$ | Package thermal impedance | PW package[3] | | 108 | °C/W |
| $T_{stg}$ | Storage temperature | | −65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

## 6.2 Recommended Operating Conditions[1]

|  |  |  | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.3 | 3.6 | V |
| $V_{IH}$ | High-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $T_A$ | Operating free-air temperature | | −55 | 125 | °C |

(1) All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

Product Folder Links: *SN74CBTLV3257-EP*

## 6.3 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 3 V, $I_I$ = −18 mA | | | | | −1.2 | V |
| $I_I$ | | $V_{CC}$ = 3.6 V, $V_I$ = $V_{CC}$ or GND | | | | | ±1 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, $V_I$ or $V_O$ = 0 to 3.6 V | | | | | 15 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | | | | | 10 | µA |
| $\Delta I_{CC}$[2] | Control inputs | $V_{CC}$ = 3.6 V, one input at 3 V, other inputs at $V_{CC}$ or GND | | | | | 300 | µA |
| $C_i$ | Control inputs | $V_I$ = 3 V or 0 | | | | 3 | | pF |
| $C_{io(OFF)}$ | A port | $V_O$ = 3 V or 0, $\overline{OE}$ = $V_{CC}$ | | | | 10.5 | | pF |
| | B port | | | | | 5.5 | | |
| $r_{on}$[3] | | $V_{CC}$ = 2.3 V, TYP at $V_{CC}$ = 2.5 V | $V_I$ = 0 | $I_I$ = 64 mA | | 5 | 8 | Ω |
| | | | | $I_I$ = 24 mA | | 5 | 8 | |
| | | | $V_I$ = 1.7 V | $I_I$ = 15 mA | | 27 | 40 | |
| | | $V_{CC}$ = 3 V | $V_I$ = 0 | $I_I$ = 64 mA | | 5 | 7 | |
| | | | | $I_I$ = 24 mA | | 5 | 7 | |
| | | | $V_I$ = 2.4 V | $I_I$ = 15 mA | | 10 | 15 | |

(1) All typical values are at $V_{CC}$ = 3.3 V (unless otherwise noted), $T_A$ = 25°C.
(2) This is the increase in supply current for each input that is at the specified voltage level, rather than $V_{CC}$ or GND.
(3) Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## 6.4 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

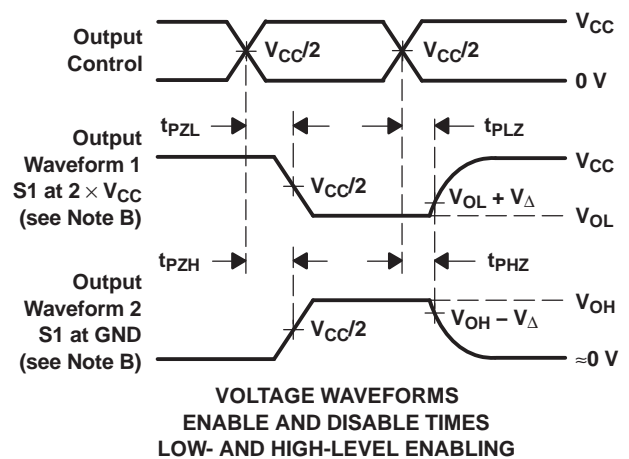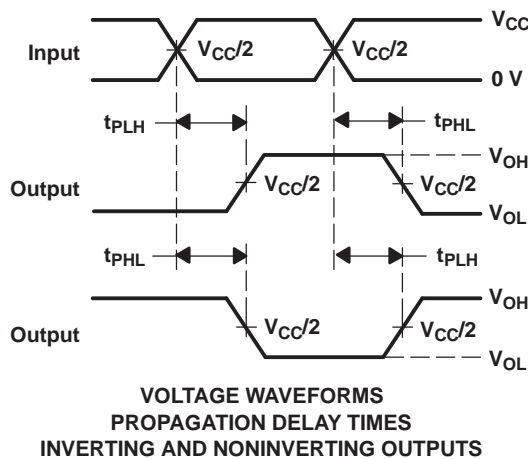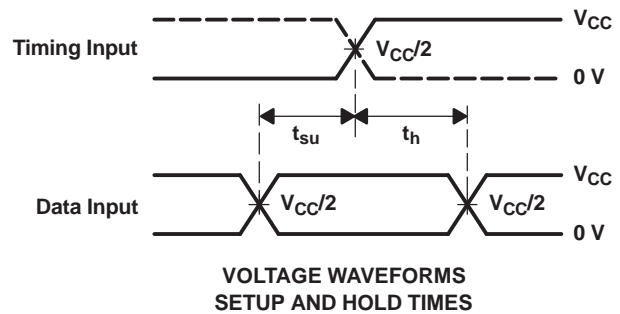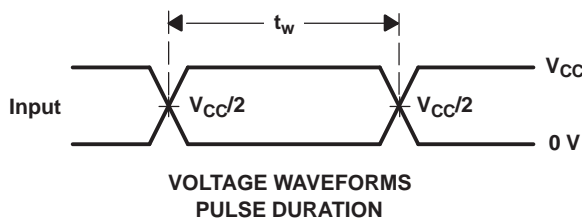| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A or B[1] | B or A | | 0.15 | | 0.25 | ns |
| | S | A or B | 1.8 | 8.1 | 1.8 | 7.3 | |
| $t_{en}$ | S | A or B | 1.7 | 7.5 | 1.7 | 6.5 | ns |
| $t_{dis}$ | S | A or B | 1 | 6.3 | 1 | 6.0 | ns |
| $t_{en}$ | $\overline{OE}$ | A or B | 1.9 | 7.1 | 2 | 6.2 | ns |
| $t_{dis}$ | $\overline{OE}$ | A or B | 1 | 7.0 | 1.6 | 6.5 | ns |

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## 7 Parameter Measurement Information

**LOAD CIRCUIT**
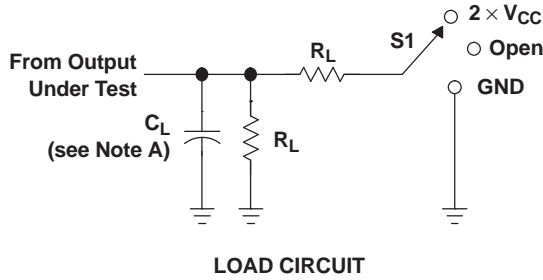
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

| $V_{CC}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|
| $2.5\ V \pm 0.2\ V$ | 30 pF | 500 $\Omega$ | 0.15 V |
| $3.3\ V \pm 0.3\ V$ | 50 pF | 500 $\Omega$ | 0.3 V |

**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. $C_L$ includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, $Z_O$ = 50 $\Omega$, $t_r \leq$ 2 ns, $t_f \leq$ 2 ns.
   D. The outputs are measured one at a time with one transition per measurement.
   E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
   F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
   G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
   H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

Product Folder Links: *SN74CBTLV3257-EP*

# 8 Device and Documentation Support

## 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 8.3 Trademarks

E2E is a trademark of Texas Instruments.
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## 8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *SN74CBTLV3257-EP*

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CCBTLV3257MPWREP | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CL257EP | Samples |
| V62/08615-01XE | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CL257EP | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74CBTLV3257-EP :**

- Catalog: SN74CBTLV3257

NOTE: Qualified Version Definitions:

  - Catalog - TI's standard catalog product

![Texas Instruments logo]

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CCBTLV3257MPWREP | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CCBTLV3257MPWREP | TSSOP | PW | 16 | 2000 | 853.0 | 449.0 | 35.0 |

SEATING PLANE

C

6.6
6.2 TYP

A

PIN 1 INDEX AREA

14X 0.65

16

2X

4.55

5.1
4.9
NOTE 3

8

9

B

4.5
4.3
NOTE 4

16X 0.30
0.19

⊕ 0.1 Ⓜ C A B

0.1 C

1

16

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0.75
0.50

0°-8°

DETAIL A
TYPICAL

4220204/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

**LAND PATTERN EXAMPLE**
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

**SOLDER MASK DETAILS**

4220204/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

**SOLDER PASTE EXAMPLE**
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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