

FDMC2523P

P-Channel QFET®

-150V, -3A, 1.5Ω

Features

- Max $r_{DS(on)} = 1.5\Omega$ at $V_{GS} = -10V$, $I_D = -1.5A$
- Low C_{rss} (typical 10pF)
- Fast Switching
- Low gate charge (typical 6.2 nC)
- Improved dv/dt capability
- RoHS Compliant

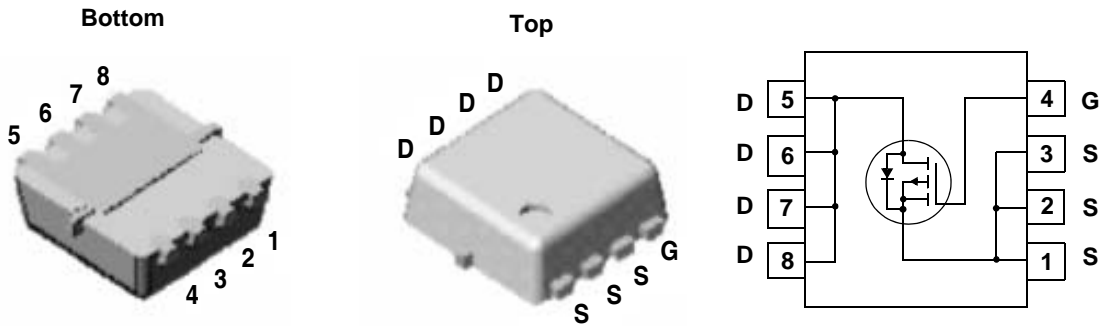


General Description

These P-Channel MOSFET enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

Application

- Active Clamp Switch



Power 33

MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-150	V
V_{GS}	Gate to Source Voltage	± 30	V
I_D	Drain Current -Continuous $T_C = 25^\circ\text{C}$	-3	A
	-Continuous $T_C = 100^\circ\text{C}$	-1.8	
	-Pulsed	-12	
P_D	Power Dissipation (Steady State) $T_C = 25^\circ\text{C}$	42	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$
dv/dt	Peak Diode Recovery dv/dt (Note 2)	-5	V/ns

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	3.0	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	60	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC2523P	FDMC2523P	Power 33	7"	8mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		-138		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -150\text{V}, V_{GS} = 0\text{V}$ $T_J = 125^\circ\text{C}$			-1 -10	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-3	-3.8	-5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		6		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{V}, I_D = -1.5\text{A}$ $V_{GS} = -10\text{V}, I_D = -1.5\text{A}, T_J = 125^\circ\text{C}$		1.1 2.0	1.5 3.6	Ω
g_{FS}	Forward Transconductance	$V_{DS} = -40\text{V}, I_D = -1.5\text{A}$ (Note 4)		1.4		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -25\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$		200	270	pF
C_{oss}	Output Capacitance			60	80	pF
C_{rss}	Reverse Transfer Capacitance			10	15	pF
R_g	Gate Resistance	$f = 1\text{MHz}$		7.5		Ω

Switching Characteristics

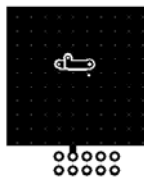
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -75\text{V}, I_D = -3\text{A}$ $V_{GS} = -10\text{V}, R_{GEN} = 25\Omega$ (Note 3,4)		15	27	ns
t_r	Rise Time			11	20	ns
$t_{d(off)}$	Turn-Off Delay Time			19	35	ns
t_f	Fall Time			13	24	ns
Q_g	Total Gate Charge	$V_{GS} = -10\text{V}$		6.2	9	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = -75\text{V}$ $I_D = -3\text{A}$		1.4		nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 3,4)		3.3		nC

Drain-Source Diode Characteristics

I_S	Maximum continuous Drain - Source Diode Forward Current				-3	A
I_{SM}	Maximum Pulse Drain - Source Diode Forward Current				-12	A
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -3.0\text{A}$		-1.8	-5	V
t_{rr}	Reverse Recovery Time	$I_F = -3.0\text{A}, di/dt = 100\text{A}/\mu\text{s}$		93		ns
Q_{rr}	Reverse Recovery Charge	(Note 3)		0.27		nC

Notes:

- 1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $60^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper



b. $135^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

- 2: $I_{SD} \leq -3\text{A}, di/dt \leq 300\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
 3: Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty cycle $< 2.0\%$.
 4: Essentially independent of operating temperature.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

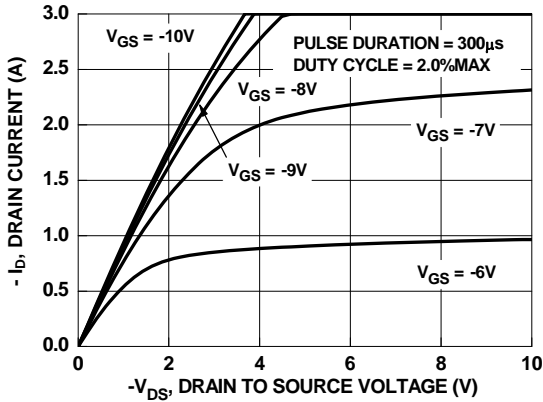


Figure 1. On-Region Characteristics

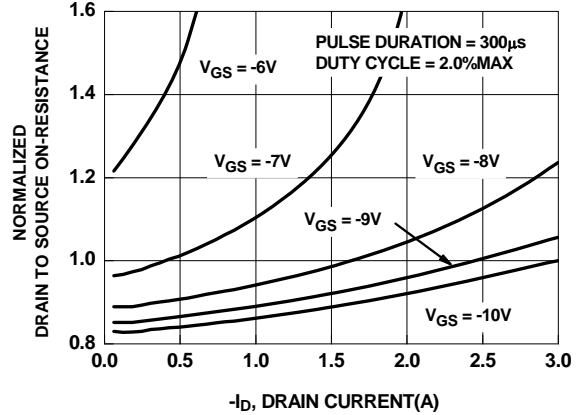


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

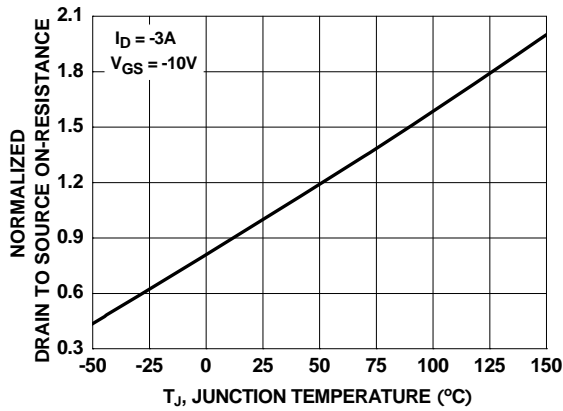


Figure 3. Normalized On-Resistance vs Junction Temperature

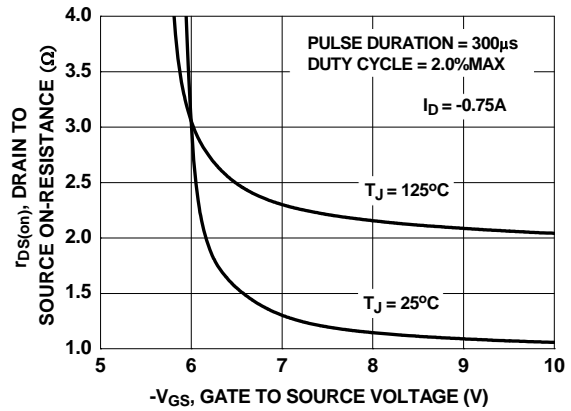


Figure 4. On-Resistance vs Gate to Source Voltage

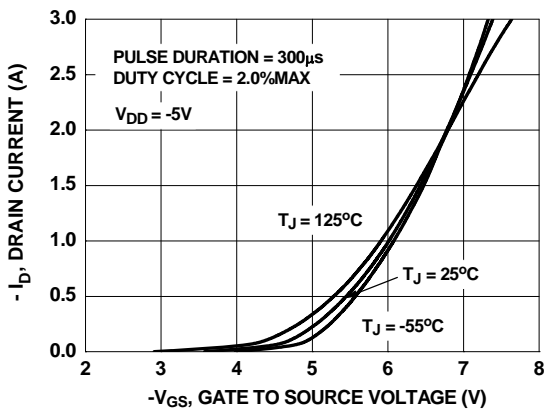


Figure 5. Transfer Characteristics

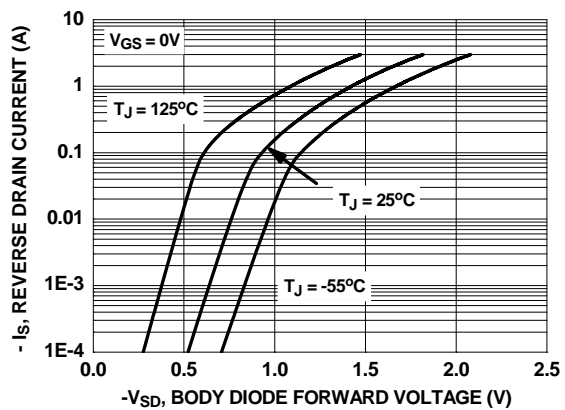


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

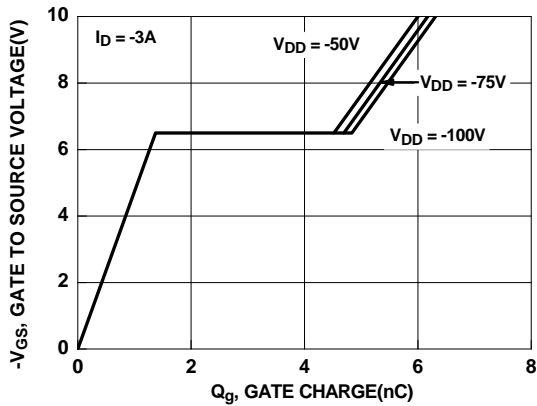


Figure 7. Gate Charge Characteristics

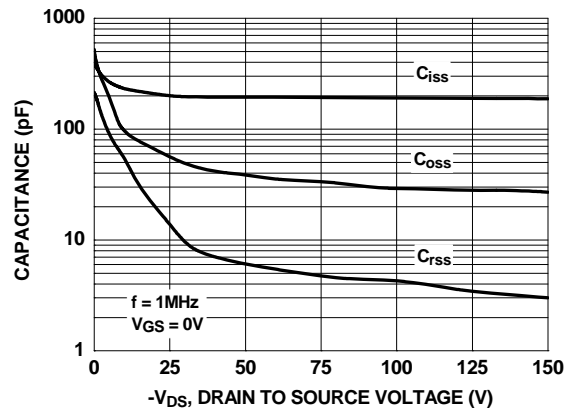


Figure 8. Capacitance vs Drain to Source Voltage

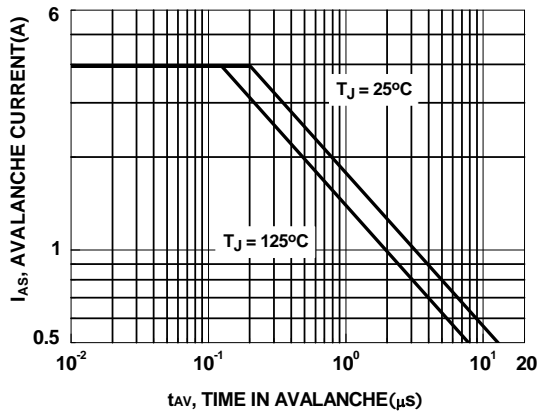


Figure 9. Unclamped Inductive Switching Capability

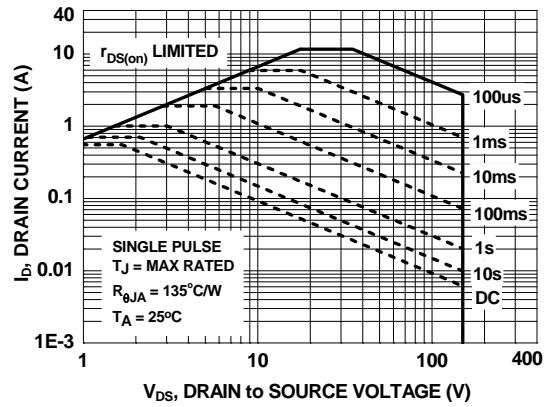


Figure 10. Forward Bias Safe Operating Area

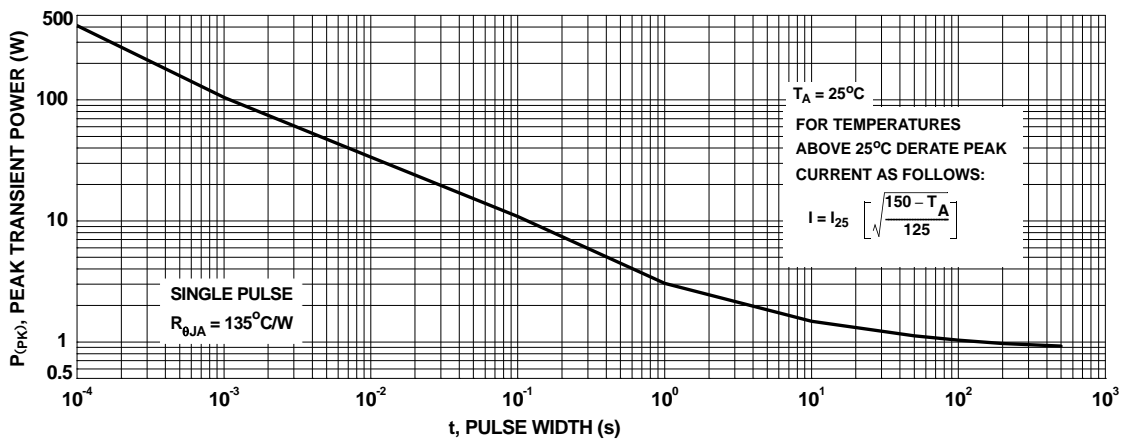


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

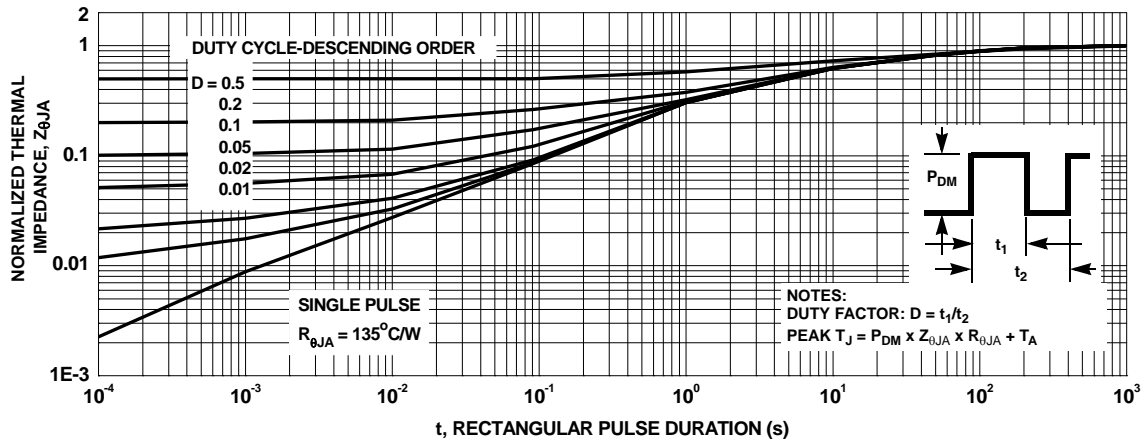
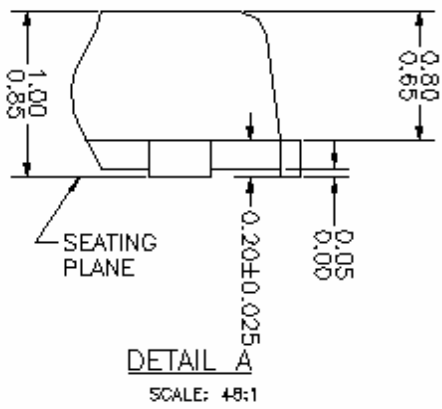
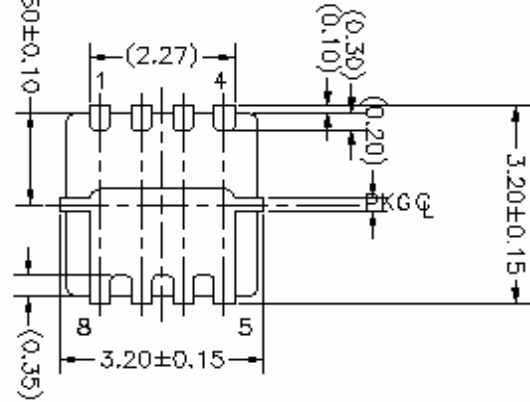
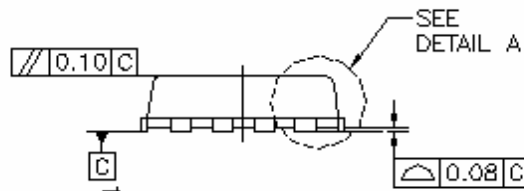
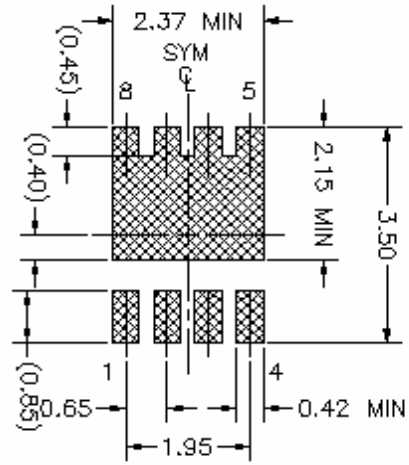
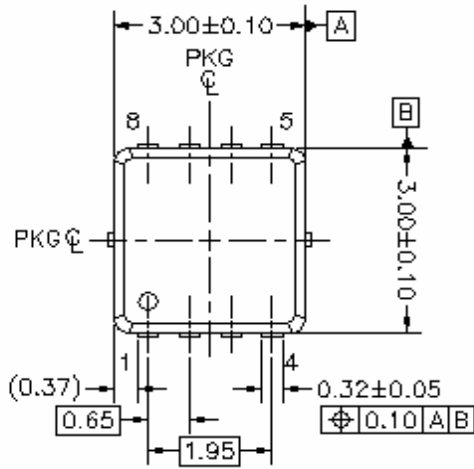


Figure 12. Transient Thermal Response Curve



NOTES: UNLESS OTHERWISE SPECIFIED

- A) NO PACKAGE STANDARD REFERENCE AS OF 29 JUNE 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FACT Quiet Series™	OCX™	SILENT SWITCHER®	UniFET™
ActiveArray™	GlobalOptoisolator™	OCXPro™	SMART START™	VCX™
Bottomless™	GTO™	OPTOLOGIC®	SPM™	Wire™
Build it Now™	HiSeC™	OPTOPLANAR™	Stealth™	
CoolFET™	I ² C™	PACMAN™	SuperFET™	
CROSSVOLT™	i-Lo™	POP™	SuperSOT™-3	
DOME™	ImpliedDisconnect™	Power247™	SuperSOT™-6	
EcoSPARK™	IntelliMAX™	PowerEdge™	SuperSOT™-8	
E ² CMOS™	ISOPLANAR™	PowerSaver™	SyncFET™	
EnSigna™	LittleFET™	PowerTrench®	TCM™	
FACT®	MICROCOUPLER™	QFET®	TinyBoost™	
FAST®	MicroFET™	QS™	TinyBuck™	
FASTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
FPS™	MICROWIRE™	Quiet Series™	TinyPower™	
FRFET™	MSX™	RapidConfigure™	TinyLogic®	
	MSXPro™	RapidConnect™	TINYOPTO™	
		µSerDes™	TruTranslation™	
		ScalarPump™	UHC®	
Across the board. Around the world.™				
The Power Franchise®				
Programmable Active Droop™				

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I22