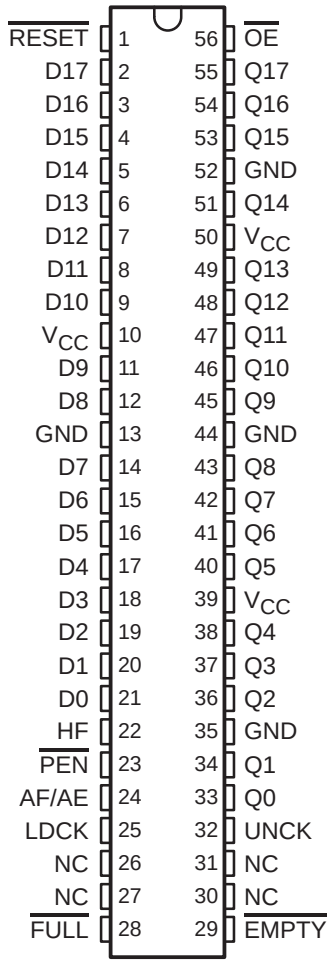
- **Operates at 3-V to 3.6-V V_{CC}**
- **Load Clock and Unload Clock Can Be Asynchronous or Coincident**
- **Low-Power Advanced CMOS Technology**
- **Full, Empty, and Half-Full Flags**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Fast Access Times of 18 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 40 MHz**
- **3-State Outputs**
- **Pin Compatible With SN74ACT7804**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing**

DL PACKAGE
(TOP VIEW)



description

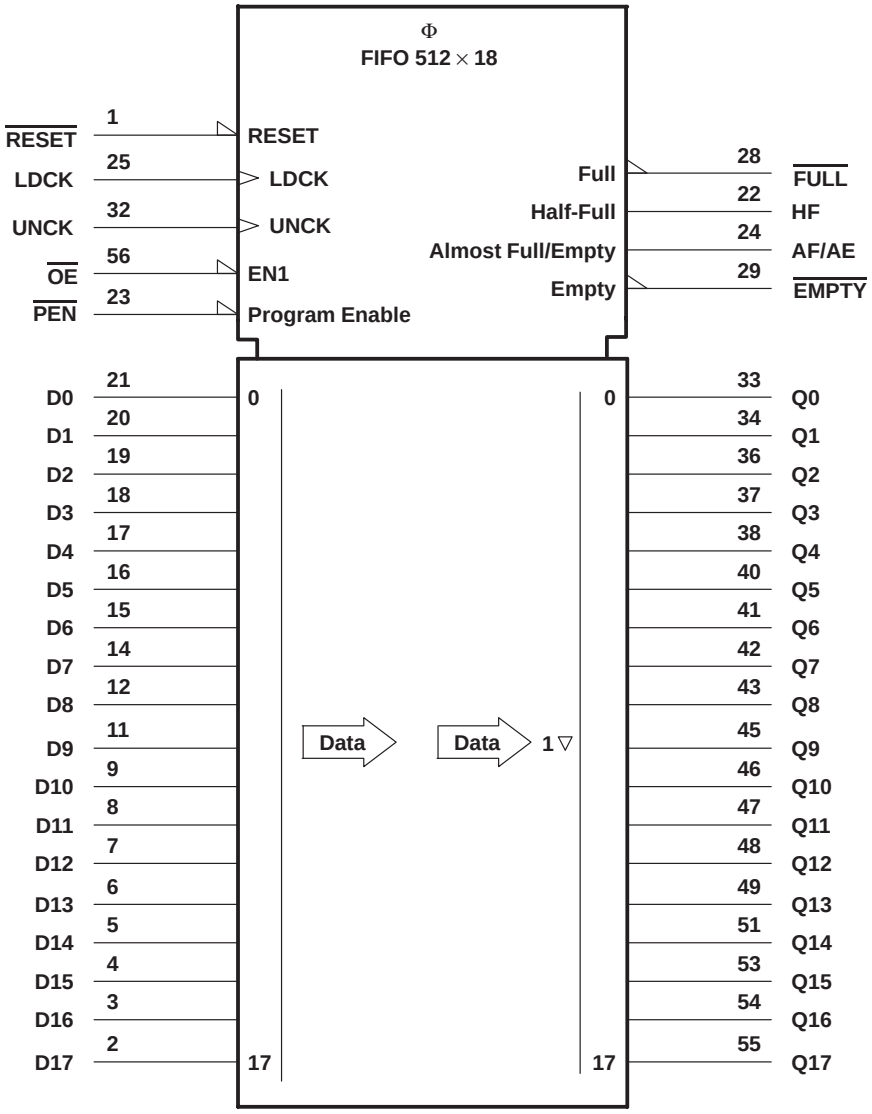
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ALVC7804 is an 18-bit FIFO with high speed and fast access times. Data is processed at rates up to 40 MHz with access times of 18 ns in a bit-parallel format. The SN74ALVC7804 is designed for 3-V to 3.6-V V_{CC} operation.

Data is written into memory on a low-to-high transition of the load clock (LDCK) and is read out on a low-to-high transition of the unload clock (UNCK). The memory is full when the number of words clocked in exceeds the number of words clocked out by 512. When the memory is full, LDCK has no effect on the data residing in memory. When the memory is empty, UNCK has no effect.

Status of the FIFO memory is monitored by the full ($\overline{FULL}$), empty ($\overline{EMPTY}$), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The $\overline{FULL}$ output is low when the memory is full and high when the memory is not full. The $\overline{EMPTY}$ output is low when the memory is empty and high when it is not empty. The HF output is high whenever the FIFO contains 256 or more words and is low when it contains 255 or less words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset are used to program the almost-empty offset value (X) and the almost-full offset value (Y), if program enable ($\overline{PEN}$) is low. The AF/AE flag is high when the FIFO contains X or less words or (512 minus Y) or more words. The AF/AE flag is low when the FIFO contains between (X plus 1) and (511 minus Y) words.

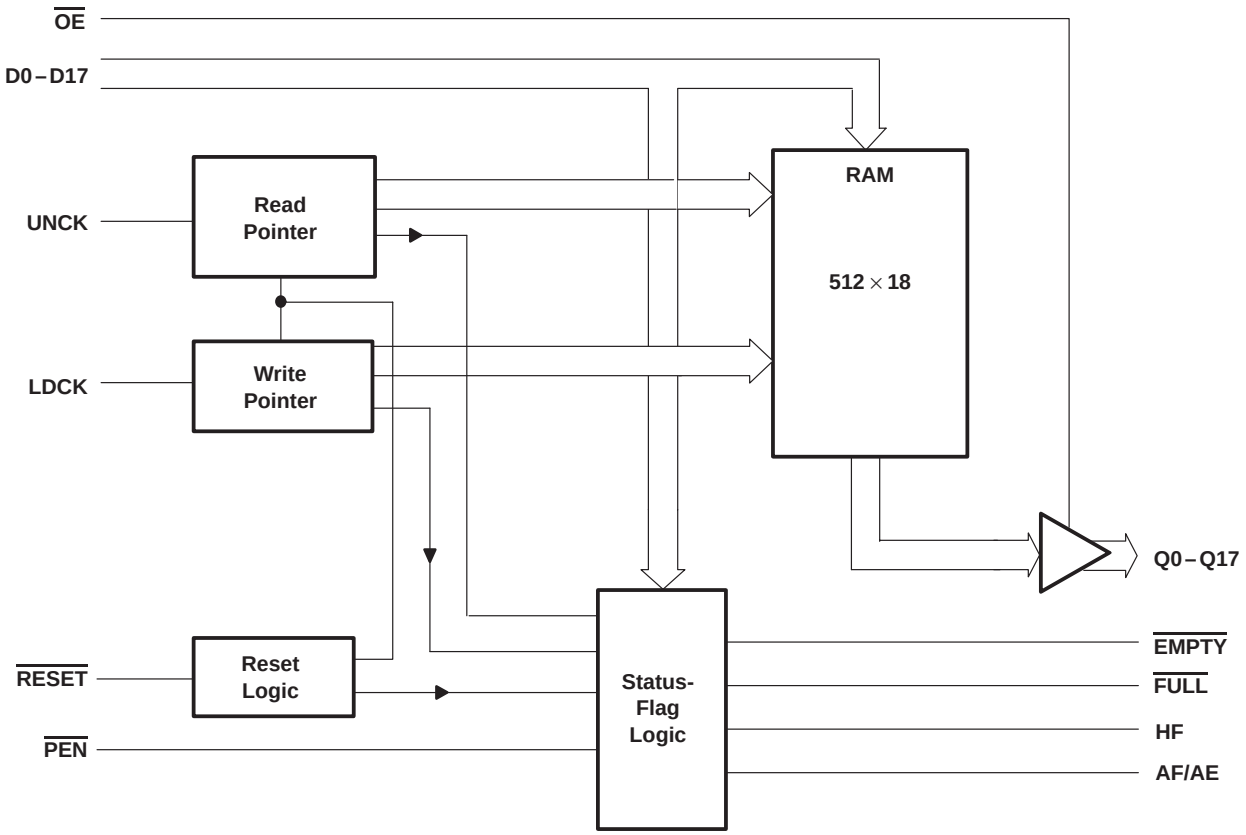
A low level on the reset ($\overline{RESET}$) resets the internal stack pointers and sets $\overline{FULL}$ high, AF/AE high, HF low, and $\overline{EMPTY}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up. The first word loaded into empty memory causes $\overline{EMPTY}$ to go high and the data to appear on the Q outputs. The data outputs are in the high-impedance state when the output-enable ($\overline{OE}$) is high.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost full/almost empty flag. Depth offset values can be programmed for AF/AE, or the default value of 64 can be used for both the almost empty offset (X) and the almost full offset (Y). AF/AE is high when memory contains X or less words or (512 – Y) or more words. AF/AE is high after reset.
D0–D17	21–14, 12–11, 9–2	I	18-bit data input port
$\overline{\text{EMPTY}}$	29	O	Empty flag. $\overline{\text{EMPTY}}$ is low when the FIFO is empty. A FIFO reset also causes $\overline{\text{EMPTY}}$ to go low.
$\overline{\text{FULL}}$	28	O	Full flag. $\overline{\text{FULL}}$ is low when the FIFO is full. A FIFO reset causes $\overline{\text{FULL}}$ to go high.
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 256 or more words. HF is low after reset.
LDCK	25	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high.
$\overline{\text{OE}}$	56	I	Output enable. When $\overline{\text{OE}}$ is high, the data outputs are in the high-impedance state.
$\overline{\text{PEN}}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D7 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	18-bit data output port
$\overline{\text{RESET}}$	1	I	Reset. A low level on $\overline{\text{RESET}}$ resets the FIFO and drives AF/AE and $\overline{\text{FULL}}$ high and HF and $\overline{\text{EMPTY}}$ low.
UNCK	32	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high.

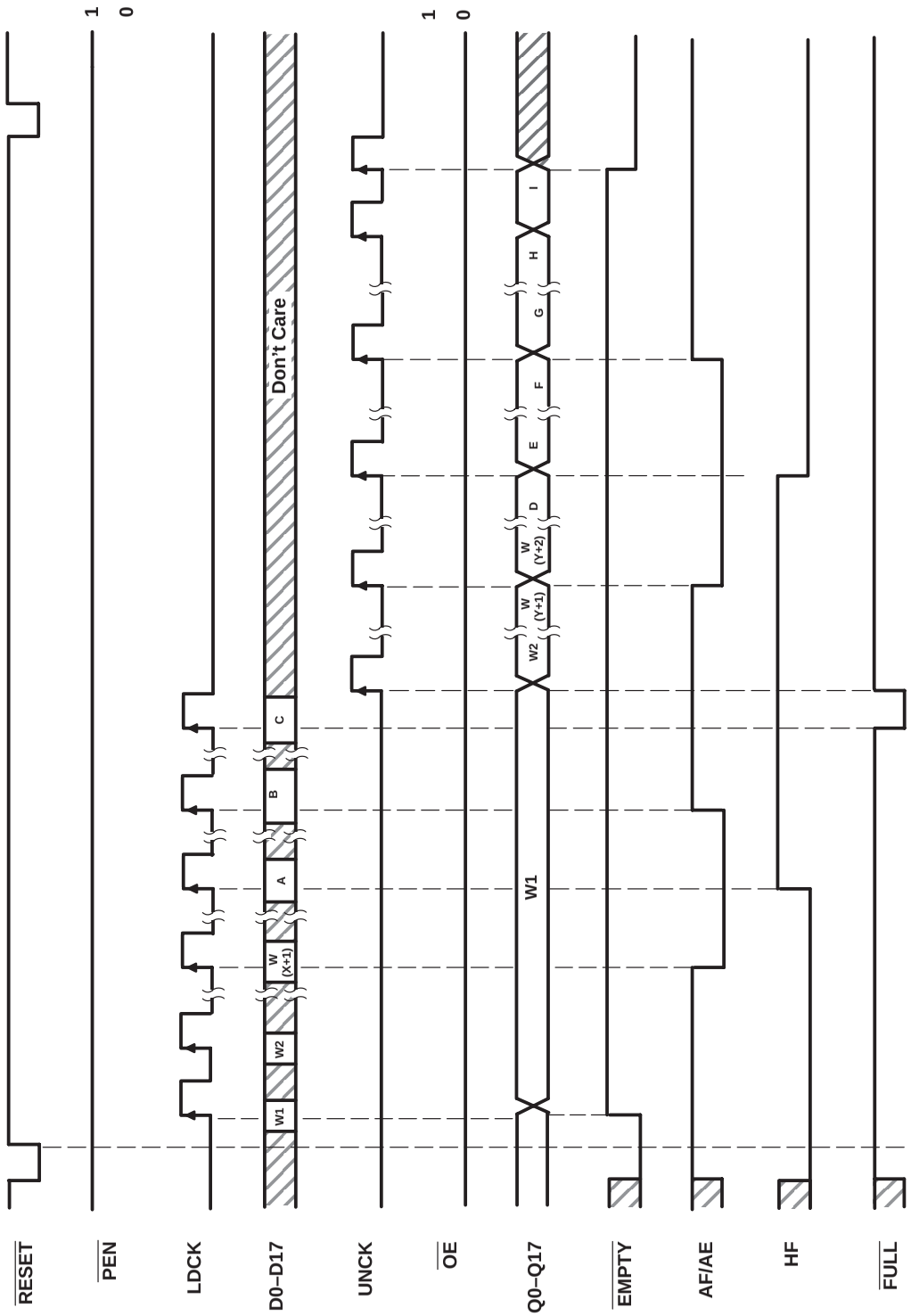


Figure 1. Write, Read, and Flag Timing Reference

DATA WORD NUMBERS FOR FLAG TRANSITIONS

DEVICE	TRANSITION WORD								
	A	B	C	D	E	F	G	H	I
SN74ALVC7804	W256	W(512–Y)	W512	W257	W258	W(512–X)	W(513–X)	W511	W512

offset values for AF/AE

The AF/AE flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. The AF/AE flag is high when the FIFO contains X or less words or (512 minus Y) or more words.

To program the offset values, $\overline{\text{PEN}}$ can be brought low after reset. On the following low-to-high transition of LDCK, the binary value on D0–D7 is stored as the almost empty offset value (X) and the almost full offset value (Y). Holding $\overline{\text{PEN}}$ low for another low-to-high transition of LDCK reprograms Y to the binary value on D0–D7 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed. A maximum value of 255 can be programmed for either X or Y (see Figure 2). To use the default values of X = Y = 64, $\overline{\text{PEN}}$ must be held high.

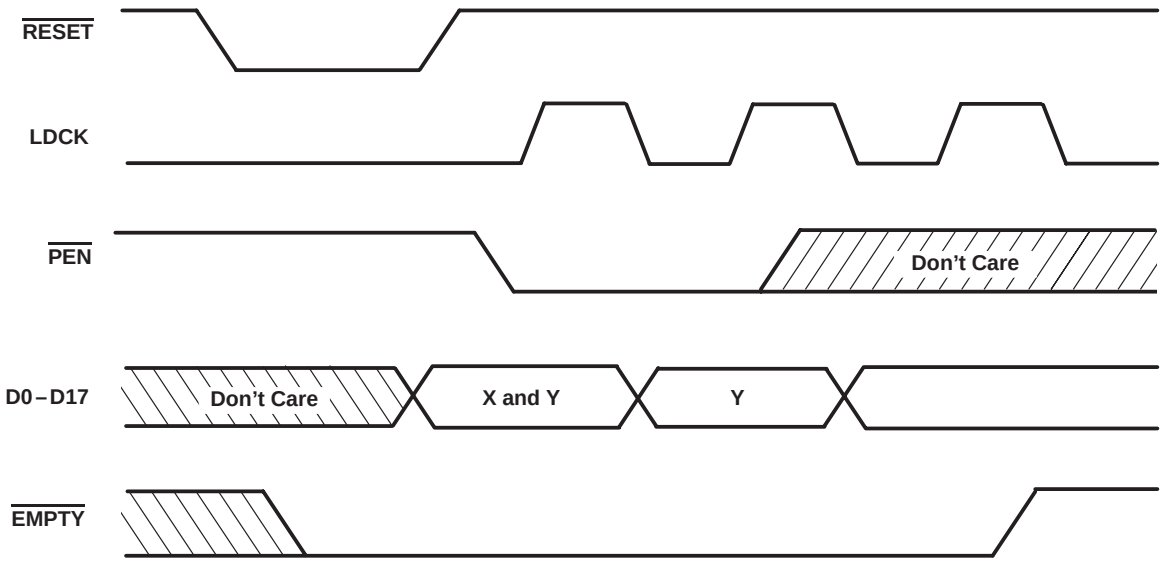


Figure 2. Programming X and Y Separately

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Voltage applied to a disabled 3-state output . . . . . 3.6 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings can be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions

			′ALVC7804-25 V_{CC} = 3.3 V ± 0.3 V		′ALVC7804-40 V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I			0	V_{CC}	0	V_{CC}	V
V_O			0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current, Q outputs, Flags	V_{CC} = 3 V		–8		–8	mA
I_{OL}	Low-level output current, Q outputs, Flags	V_{CC} = 3 V		16		16	mA
f_{clock}	Clock frequency			40		25	MHz
t_w	Pulse duration	D0–D17 high or low	8		12		ns
		LDCK high or low	8		12		
		UNCK high or low	8		12		
		$\overline{PEN}$ low	8		12		
		$\overline{RESET}$ low	10		12		
t_{su}	Setup time	D0–D17 before LDCK↑	5		5		ns
		LDCK inactive before $\overline{RESET}$ high	6		6		
		$\overline{PEN}$ before LDCK↑	8		8		
t_h	Hold time	D0–D17 after LDCK↑	0		0		ns
		$\overline{PEN}$ high after LDCK low	0		0		
		$\overline{PEN}$ low after LDCK↑	3		3		
		LDCK inactive after $\overline{RESET}$ high	6		6		
T_A	Operating free-air temperature		0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{OH}	Flags, Q outputs	V_{CC} = MIN to MAX,	I_{OH} = – 100 µA	V_{CC} – 0.2			V
		V_{CC} = 3 V,	I_{OH} = – 8 mA	2.4			
V_{OL}	Flags, Q outputs	V_{CC} = MIN to MAX,	I_{OL} = 100 µA			0.2	V
	Flags	V_{CC} = 3 V,	I_{OL} = 8 mA			0.4	
	Q outputs	V_{CC} = 3 V,	I_{OL} = 16 mA			0.55	
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±5	µA
I_{OZ}		V_{CC} = 3.6 V,	V_O = V_{CC} or GND			±10	µA
I_{CC}		V_{CC} = 3.6 V,	V_I = V_{CC} or GND and I_O = 0			40	µA
ΔI_{CC}§		V_{CC} = 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i		V_{CC} = 3.3 V,	V_I = V_{CC} or GND		3		pF
C_o		V_{CC} = 3.3 V,	V_O = V_{CC} or GND		6		pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
§ This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	′ALVC7804-25 V_{CC} = 3.3 V ± 0.3 V		′ALVC7804-40 V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	LDCK or UNCK		40		25		MHz
t_{pd}	LDCK↑	Any Q	9	22	9	24	ns
t_{pd}	UNCK↑		6	18	6	20	
t_{PLH}	LDCK↑	$\overline{EMPTY}$	6	17	6	19	ns
t_{PHL}	UNCK↑		6	17	6	19	
t_{PHL}	$\overline{RESET}$ low		4	18	4	20	
t_{PHL}	LDCK↑	$\overline{FULL}$	6	17	6	19	ns
t_{PLH}	UNCK↑		6	17	6	19	
t_{PLH}	$\overline{RESET}$ low		4	20	4	22	
t_{pd}	LDCK↑	AF/AE	7	20	7	22	ns
t_{pd}	UNCK↑		7	20	7	22	
t_{PLH}	$\overline{RESET}$ low		2	12	2	14	
t_{PLH}	LDCK↑	HF	5	20	5	22	ns
t_{PHL}	UNCK↑		7	20	7	22	
t_{PHL}	$\overline{RESET}$ low		3	14	3	16	
t_{en}	$\overline{OE}$	Any Q	2	10	2	11	ns
t_{dis}			2	11	2	12	

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C_L = 50 pF,	f = 5 MHz	53	pF

APPLICATION INFORMATION

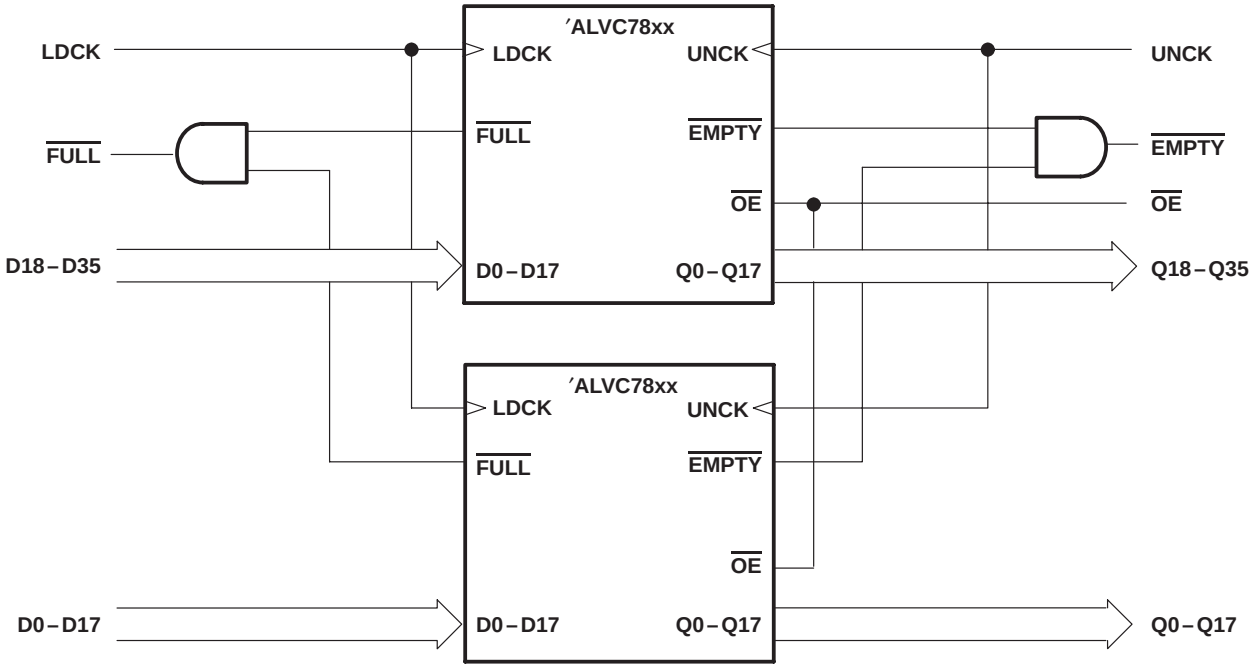


Figure 3. Word-Width Expansion: 512 × 36 Bit

TYPICAL CHARACTERISTICS

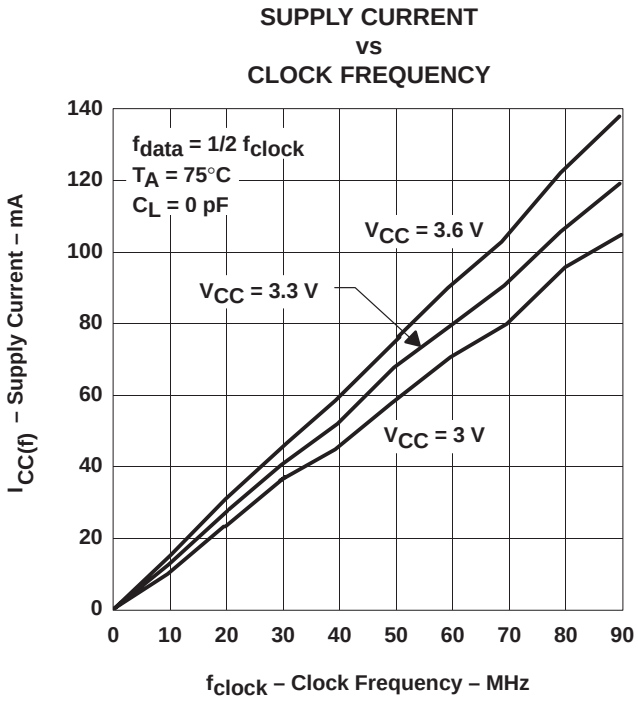


Figure 4

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 4, the dynamic power (P_d), based on all data outputs changing states on each read, can be calculated by using:

$$P_d = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

A more accurate total power (P_T) can be calculated if quiescent power (Pq) is also taken into consideration. Quiescent power (P_q) can be calculated using:

$$P_q = V_{CC} \times [I_{CCI} + (N \times \Delta I_{CC} \times dc)]$$

Total power will be:

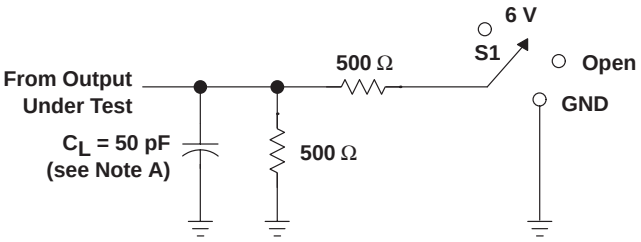
$$P_T = P_d + P_q$$

The above equations provide worst-case power calculations.

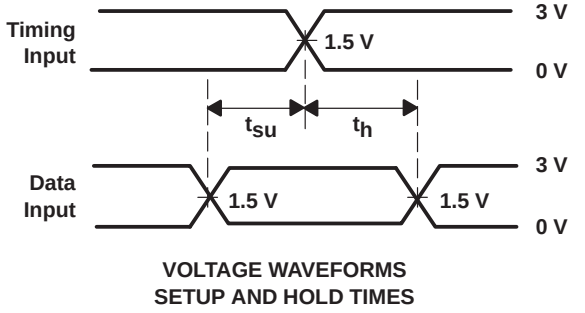
Where:

N	=	number of inputs driven by TTL levels
ΔI_{CC}	=	increase in power supply current for each input at a TTL high level
dc	=	duty cycle of inputs at a TTL high level of 3.4 V
C_L	=	output capacitance load
f_o	=	switching frequency of an output
I_{CCI}	=	idle current, supply current when FIFO is idle ≈ pF × f_{clock} = 0.2 × f_{clock} (current is due to free-running clocks)
pF	=	power factor (the slope of idle I_{CC} versus frequency)
$I_{CC(f)}$	=	active current, supply current when FIFO is transferring data

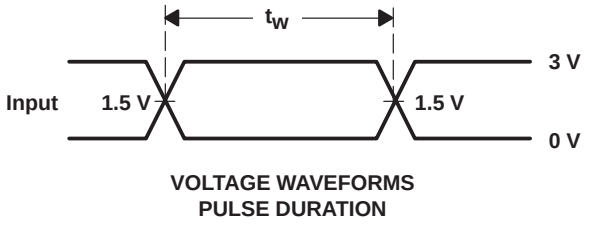
PARAMETER MEASUREMENT INFORMATION



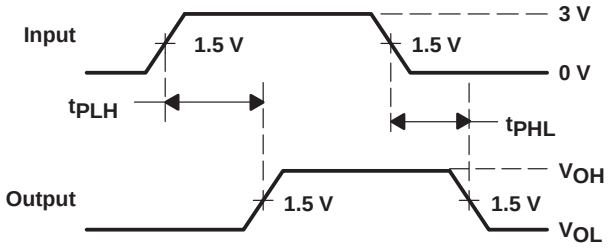
LOAD CIRCUIT FOR OUTPUTS



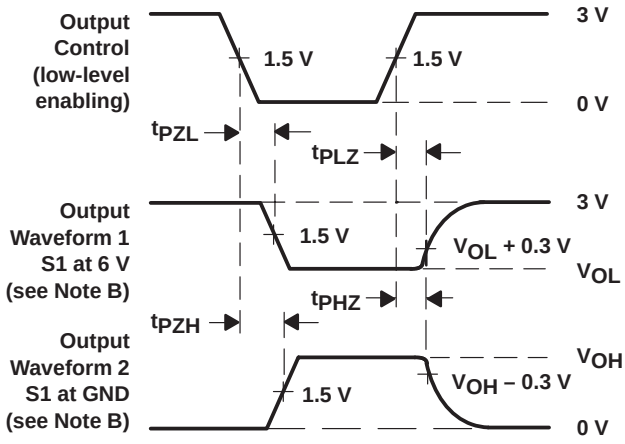
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

3-STATE OUTPUTS (ANY Q)

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	GND
	t_{PZL}			6 V
t_{dis}	t_{PHZ}	500 Ω	50 pF	GND
	t_{PLZ}			6 V
t_{pd}	t_{PLH}/t_{PHL}	500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

Figure 5. Standard CMOS Outputs (FULL, EMPTY, HF, AF/AE)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALVC7804-25DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ALVC7804-25	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

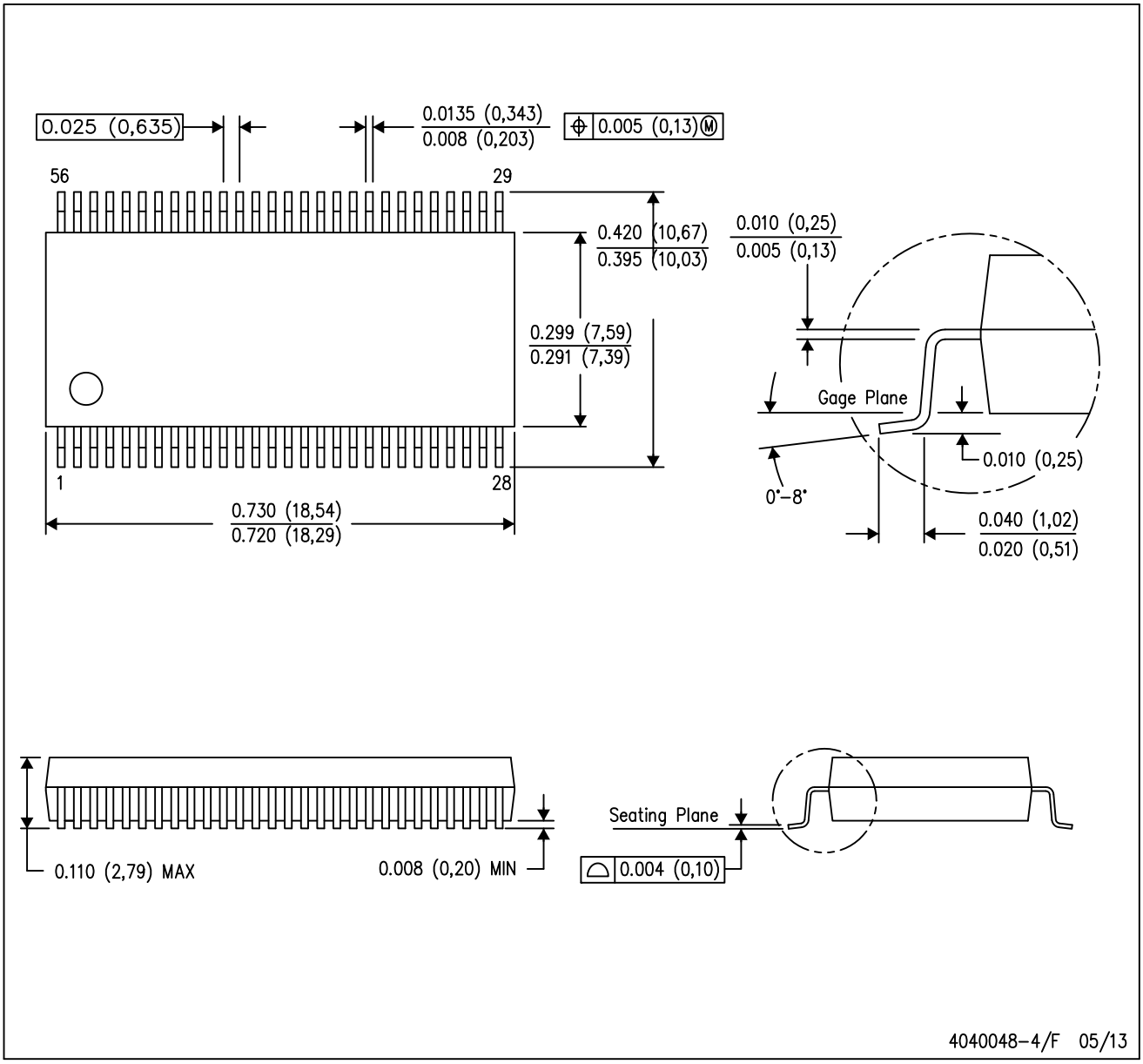
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

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