

# DUAL-CHANNEL XAUI/10GBASE-KR TRANSCEIVER WITH CROSSPOINT

Check for Samples: [TLK10232](#)

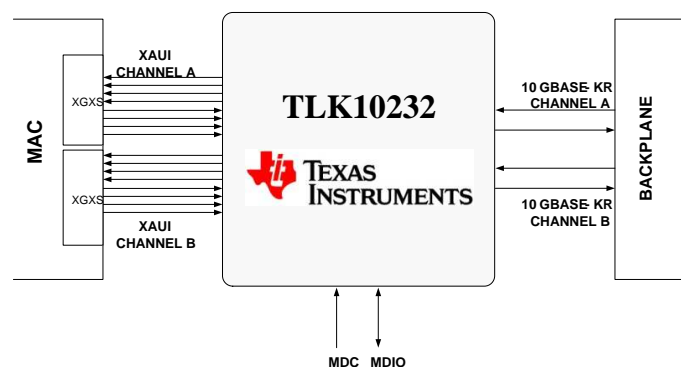
## 1 Introduction

### 1.1 Features

- Dual Channel Multi-Rate Transceiver
- Supports 10GBASE-KR, XAUI, and 1GBASE-KX Ethernet Standards
- Supports all CPRI and OBSAI Data Rates up to 10 Gbps
- Supports Multi-Rate SERDES Operation with up to 10.3125 Gbps Data Rate on the High Speed Side and up to 5 Gbps on the Low Speed Side
- Differential CML I/Os on Both High Speed and Low Speed Sides
- Interface to Backplanes, Passive and Active Copper Cables, or SFP+ Optical Modules
- Selectable Reference Clock per Channel with Multiple Output Clock Options
- Integrated Crosspoint Switch Allows for Flexible Signal Routing and Redundant Outputs
- Supports Data Retime Operation
- Supports PRBS, CRPAT, CJPAT, High/Low/Mixed-Frequency Patterns, and KR Pseudo-Random Pattern Generation and Verification, Square-Wave Generation
- Two Power Supplies: 1.0V (Core), and 1.5 or 1.8V (I/O)
- No Power Supply Sequencing Requirements
- Transmit De-emphasis and Receive Adaptive Equalization to Allow Extended Backplane/Cable Reach on Both High Speed and Low Speed Sides
- Loss of Signal (LOS) Detection
- Supports 10G-KR Link Training, Forward Error Correction, Auto-Negotiation
- Jumbo Packet Support
- JTAG; IEEE 1149.1 Test Interface
- Industry Standard MDIO Control Interface
- 65nm Advanced CMOS Technology
- Industrial Ambient Operating Temperature (–40°C to 85°C)
- Power Consumption: 800mW per Channel (Nominal)
- Device Package: 13mm x 13mm, 144-pin PBGA, 1-mm Ball-Pitch

### 1.2 Applications

- 10GBASE-KR Compliant Backplane Links
- 10 Gigabit Ethernet Switch, Router, and Network Interface Cards
- Proprietary Cable/Backplane Links
- High-Speed Point-to-Point Transmission Systems



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### 1.3 Description

The TLK10232 is a dual-channel multi-rate transceiver intended for use in high-speed bi-directional point-to-point data transmission systems. This device supports three primary modes. It can be used as a XAUI to 10GBASE-KR transceiver, as a general-purpose 8b/10b multi-rate 4:1, 2:1, or 1:1 serializer/deserializer, or can be used in 1G-KX mode.

While operating in the 10GBASE-KR mode, the TLK10232 performs serialization of the 8B/10B encoded XAUI data stream presented on its low speed (LS) side data inputs. The serialized 8B/10B encoded data is presented on the high speed (HS) side outputs in 64B/66B encoding format. Likewise, the TLK10232 performs deserialization of 64B/66B encoded data streams presented on its high speed side data inputs. The deserialized 64B/66B data is presented in XAUI 8B/10B format on the low speed side outputs. Link Training is supported in this mode as well as Forward Error Correction (FEC) for extended length applications.

While operating in the General Purpose SERDES mode, the TLK10232 performs 2:1 and 4:1 serialization of the 8B/10B encoded data streams presented on its low speed (LS) side data inputs. The serialized 8B/10B encoded data is presented on the high speed (HS) side outputs. Likewise, the TLK10232 performs 1:2 and 1:4 deserialization of 8B/10B encoded data streams presented on its high speed side data inputs. The deserialized 8B/10B encoded data is presented on the low speed side outputs. Depending on the serialization/deserialization ratio, the low speed side data rate can range from 0.5 Gbps to 5 Gbps and the high speed side data rate can range from 1 Gbps to 10 Gbps. 1:1 retimer mode is also supported but limited to 1 Gbps to 5 Gbps rates.

The TLK10232 also supports 1G-KX (1.25 Gbps) mode with PCS (CTC) capabilities. This mode can be enabled via software provisioning or via auto negotiation. If software provisioning is used, data rates up to 3.125 Gbps are supported.

The TLK10232 features a built-in crosspoint switch, allowing for redundant outputs and easy re-routing of data. Each output port (either high speed or low speed) can be configured to output data coming from any of the device's input ports. The switching can be initiated through either a hardware pin or through software control, and can be configured to occur either immediately or after the end of the current packet. This allows for switching between data sources without packet corruption.

Both low speed and high speed side data inputs and outputs are of differential current mode logic (CML) type with integrated termination resistors.

The TLK10232 provides flexible clocking schemes to support various operations. They include the support for clocking with an externally-jitter-cleaned clock recovered from the high speed side. The device is also capable of performing clock tolerance compensation (CTC) in 10GBASE-KR and 1GBASE-KX modes, allowing for asynchronous clocking.

The TLK10232 provides low speed side and high speed side loopback modes for self-test and system diagnostic purposes.

The TLK10232 has built-in pattern generators and verifiers to help in system tests. The device supports generation and verification of various PRBS, High-/Low-/Mixed-Frequency, CRPAT long/short, CJPAT, and KR pseudo-random test patterns and square wave generation. The types of patterns supported on the low speed and high speed side are dependent on the operational mode chosen.

The TLK10232 has an integrated loss of signal (LOS) detection function on both high speed and low speed sides. LOS is asserted in conditions where the input differential voltage swing is less than the LOS assert threshold.

Both TLK10232 channels are fully independent. They can be operated with different reference clocks, at different data rates, and with different serialization/deserialization ratios.

The low speed side of the TLK10232 is ideal for interfacing with an FPGA, ASIC, MAC, or network processor capable of handling lower-rate serial data streams. The high speed side is ideal for interfacing with remote systems through optical fibers, electrical cables, or backplane interfaces. The TLK10232 supports operation with SFP and SFP+ optical modules, as well as 10GBASE-KR compatible backplane systems.

## 2 Physical Characteristics

### 2.1 Block Diagram

Various interfaces of the TLK10232 device are shown in [Figure 2-1](#) for Channel A. The implementation is the same for Channel B. A simplified one-channel block diagram of both the transmit and receive data path is shown in [Figure 2-2](#). This low-power transceiver consists of two serializer/deserializer (SERDES) blocks, one on the low speed side and the other on the high speed side. The core logic block that lies between the two SERDES blocks carries out all the logic functions including channel synchronization, lane alignment, 8B/10B and 64B/66B encoding/decoding, as well as test pattern generation and verification.

The TLK10232 provides a management data input/output (MDIO Clause 22/45) interface as well as a JTAG interface for device configuration, control, and monitoring. Detailed description of the TLK10232 pin functions is provided in [Table 2-1](#).

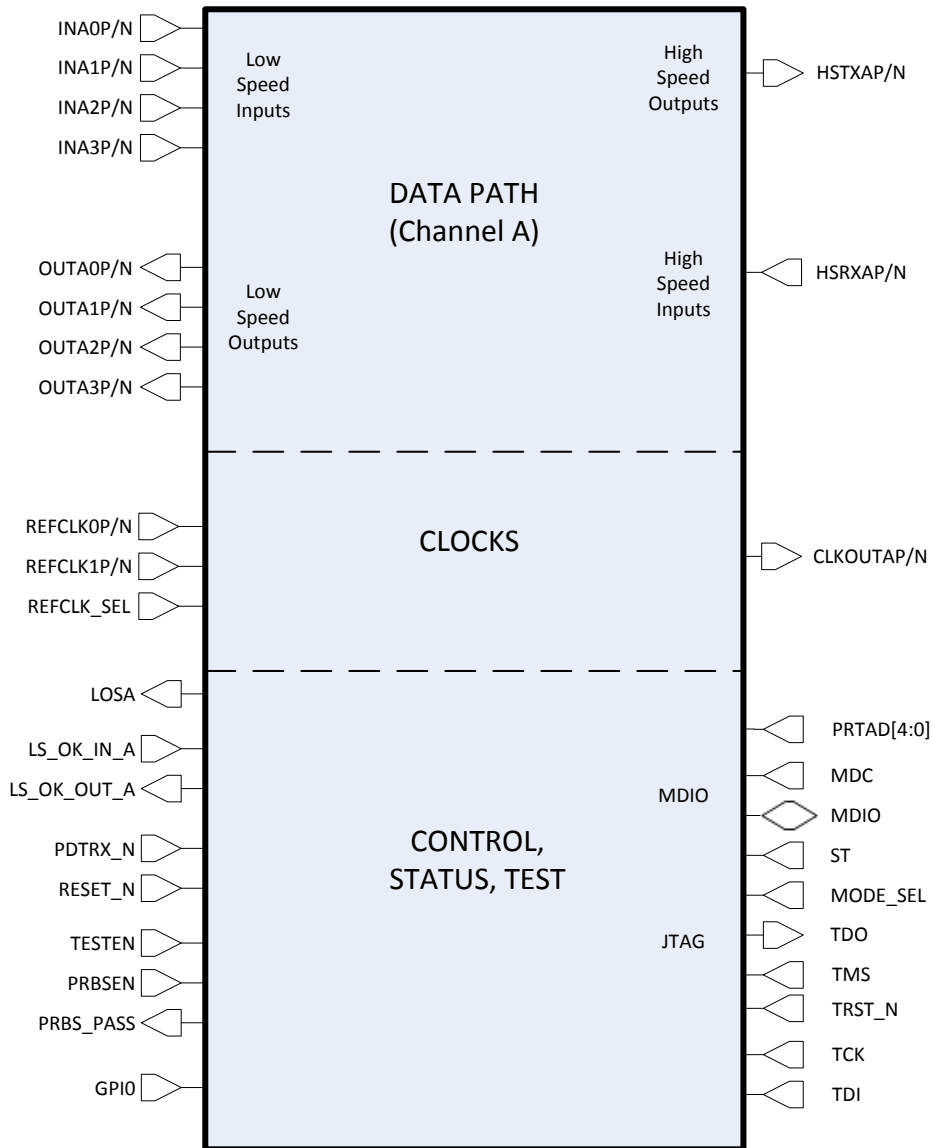


Figure 2-1. TLK10232 Interfaces

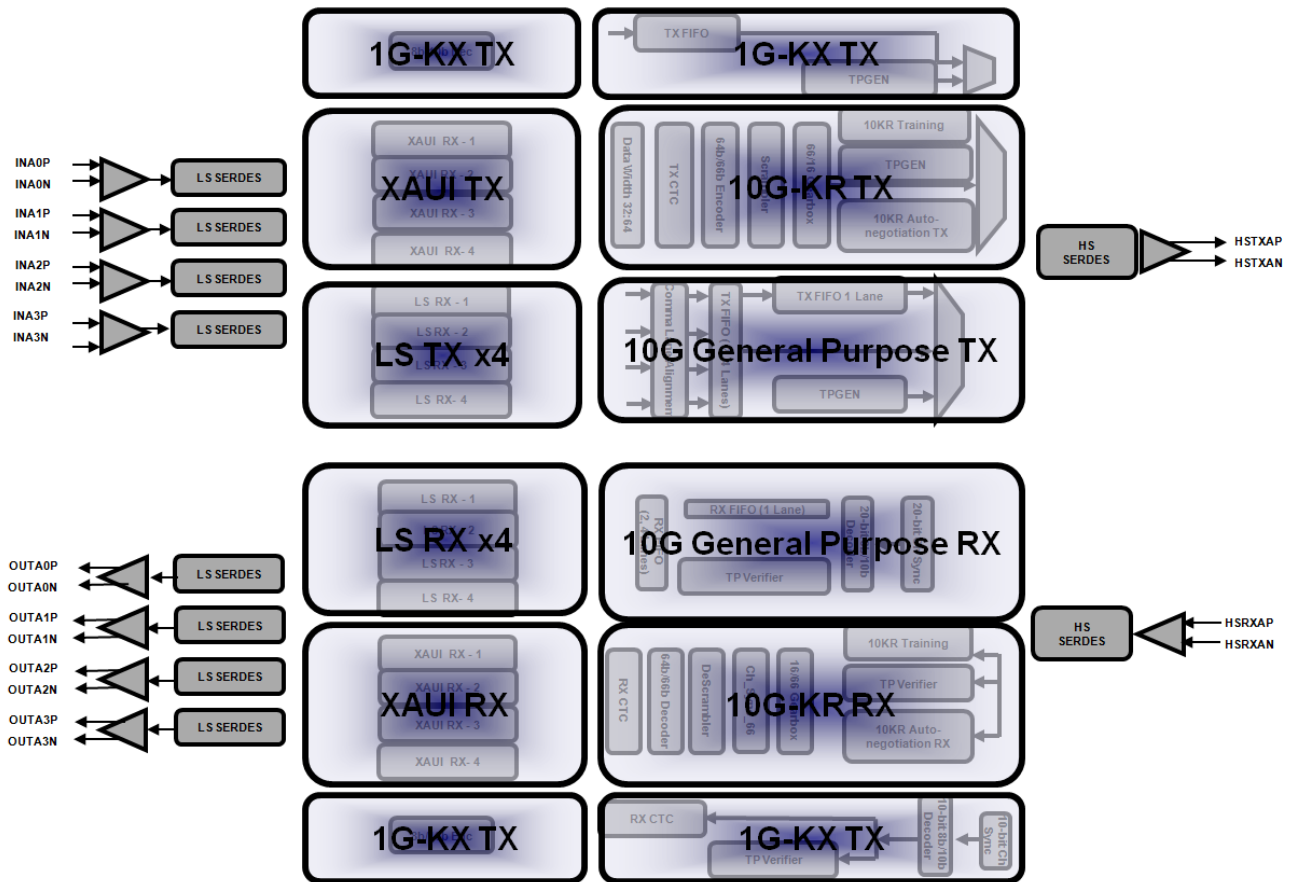


Figure 2-2. A Simplified One Channel Block Diagram of the TLK10232 Data Paths

## 2.2 Package

A 13-mm x 13-mm, 144-pin PBGA package with a ball pitch of 1 mm is used. The device pin-out is as shown in Figure 2-3 and is described in detail in Table 2-1 and Table 2-2.

|   | 1     | 2       | 3        | 4         | 5       | 6      | 7      | 8          | 9           | 10         | 11       | 12     |
|---|-------|---------|----------|-----------|---------|--------|--------|------------|-------------|------------|----------|--------|
| A | INA1P | VSS     | INA0N    | INA0P     | VSS     | OUTA0P | OUTA0N | PDTRX_A_N  | CLKOUTBP    | CLKOUTBN   | VSS      | HSRXAN |
| B | INA1N | INA2P   | VSS      | VSS       | OUTA1P  | OUTA1N | VSS    | TMS        | PRBSEN      | LS_OK_IN_A | VSS      | HSRXAP |
| C | VSS   | INA2N   | VDDRA_LS | OUTA2P    | OUTA2N  | VSS    | VDDO0  | TDI        | CLKOUTAP    | CLKOUTAN   | AMUXA    | VSS    |
| D | INA3P | VDDA_LS | VSS      | AMUXB     | VSS     | TDO    | VPP    | TCK        | LS_OK_OUT_A | VSS        | VSS      | HSTXAP |
| E | INA3N | VSS     | OUTA3N   | VSS       | TRST_N  | VDDD   | DVDD   | VDDD       | LOSA        | PRTAD0     | VDDRA_HS | HSTXAN |
| F | VSS   | VDDA_LS | OUTA3P   | VDDT_LS   | VSS     | VDDD   | DVDD   | VSS        | VDDT_HS     | VSS        | VDDA_HS  | VSS    |
| G | VSS   | VDDA_LS | VSS      | VDDT_LS   | VSS     | DVDD   | VSS    | DVDD       | PRTAD1      | VDDA_HS    | VSS      | HSRXBN |
| H | INB0P | VSS     | OUTB0N   | VSS       | RESET_N | VDDD   | DVDD   | VDDD       | LS_OK_OUT_B | MODE_SEL   | VSS      | HSRXBP |
| J | INB0N | VDDA_LS | OUTB0P   | PDTRX_B_N | VSS     | PRTAD3 | MDIO   | MDC        | PRBS_PASS   | GPI0       | VDDRB_HS | VSS    |
| K | VSS   | INB1P   | VDDRB_LS | OUTB1N    | OUTB1P  | VSS    | VDDO1  | LOSB       | REFCLK1P    | REFCLK1N   | VSS      | HSTXBP |
| L | INB2P | INB1N   | VSS      | VSS       | OUTB2N  | OUTB2P | VSS    | LS_OK_IN_B | PRTAD2      | TESTEN     | VSS      | HSTXBN |
| M | INB2N | VSS     | INB3P    | INB3N     | VSS     | OUTB3N | OUTB3P | PRTAD4     | ST          | REFCLK0P   | REFCLK0N | VSS    |

Figure 2-3. The Pin-Out of the TLK10232

## 2.3 Terminal Functions

The details of the terminal functions of the TLK10232 are provided in [Table 2-1](#) and [Table 2-2](#).

**Table 2-1. Pin Description - Signal Pins**

| TERMINAL         |                                  | DIRECTION<br>TYPE<br>SUPPLY                    | DESCRIPTION  |
|------------------|----------------------------------|--|--|
| SIGNAL           | BGA                              |  |  |
| <b>CHANNEL A</b> |                                  |  |  |
| HSTXAP<br>HSTXAN | D12<br>E12                       | Output<br>CML VDDA_HS                          | <b>High Speed Transmit Channel A Output.</b> HSTXAP and HSTXAN comprise the high speed side transmit direction Channel A differential serial output signal. During device reset (RESET_N asserted low) these pins are driven differential zero. These CML outputs must be AC coupled.  |
| HSRXAP<br>HSRXAN | B12<br>A12                       | Input<br>CML VDDA_HS                           | <b>High Speed Receive Channel A Input.</b> HSRXAP and HSRXAN comprise the high speed side receive direction Channel A differential serial input signal. These CML input signals must be AC coupled.  |
| INA[3:0]P/N      | D1/E1<br>B2/C2<br>A1/B1<br>A4/A3 | Input<br>CML VDDA_LS                           | <b>Low Speed Channel A Inputs.</b> INAP and INAN comprise the low speed side transmit direction Channel A differential input signals. These signals must be AC coupled.  |
| OUTA[3:0]P/N     | F3/E3<br>C4/C5<br>B5/B6<br>A6/A7 | Output<br>CML VDDA_LS                          | <b>Low Speed Channel A Outputs.</b> OUTAP and OUTAN comprise the low speed side receive direction Channel A differential output signals. During device reset (RESET_N asserted low) these pins are driven differential zero. These signals must be AC coupled.   |
| LOSA             | E9                               | Output LVCMOS<br>1.5V/1.8V<br>VDDO0 40Ω Driver | <b>Channel A Receive Loss Of Signal (LOS) Indicator.</b><br>LOSA=0: Signal detected.<br>LOSA=1: Loss of signal.<br>Loss of signal detection is based on the input signal level. When HSRXAP/N has a differential input signal swing of $\leq 75$ mV <sub>pp</sub> , LOSA will be asserted (if enabled). If the input signal is greater than 150 mV <sub>p-p</sub> , LOS will be deasserted. Outside of these ranges, the LOS indication is undefined.<br>Other functions can be observed on LOSA real-time, configured via MDIO<br>During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PDTRXA_N asserted low), this pin is floating. During register based power down, this pin is floating.<br>It is highly recommended that LOSA be brought to an easily accessible point on the application board (header) in the event that debug is required. |
| LS_OK_IN_A       | B10                              | Input LVCMOS<br>1.5V/1.8V VDDO0                | <b>Channel A Receive Lane Alignment Status Indicator.</b><br>Lane alignment status signal received from a Lane Alignment Slave on the link partner device. Valid in 10G General Purpose Serdes Mode.<br>LS_OK_IN_A=0: Channel A link partner receive lanes not aligned.<br>LS_OK_IN_A=1: Channel A link partner receive lanes aligned  |
| LS_OK_OUT_A      | D9                               | Output LVCMOS<br>1.5V/1.8V<br>VDDO0 40Ω Driver | <b>Channel A Transmit Lane Alignment Status Indicator.</b><br>Lane alignment status signal sent to a Lane Alignment Master on the link partner device. Valid in 10G General Purpose Serdes Mode.<br>LS_OK_OUT_A=0: Channel A link partner transmit lanes not aligned.<br>LS_OK_OUT_A=1: Channel A link partner transmit lanes aligned.   |
| PDTRXA_N         | A8                               | Input LVCMOS<br>1.5V/1.8V VDDO0                | <b>Transceiver Power Down.</b><br>When this pin is held low (asserted), Channel A is placed in power down mode. When deasserted, Channel A operates normally. After deassertion, a software data path reset should be issued through the MDIO interface.   |
| <b>CHANNEL B</b> |                                  |  |  |
| HSTXBP<br>HSTXBN | K12<br>L12                       | Output CML<br>VDDA_HS                          | <b>High Speed Transmit Channel B Output.</b> HSTXBP and HSTXBN comprise the high speed side transmit direction Channel B differential serial output signal. During device reset (RESET_N asserted low) these pins are driven differential zero. These CML outputs must be AC coupled.  |
| HSRXBP<br>HSRXBN | H12<br>G12                       | Input CML<br>VDDA_HS                           | <b>High Speed Receive Channel B Input.</b> HSRXBP and HSRXBN comprise the high speed side receive direction Channel B differential serial input signal. These CML input signals must be AC coupled.  |
| INB[3:0]P/N      | M3/M4<br>L1/M1<br>K2/L2<br>H1/J1 | Input CML<br>VDDA_LS                           | <b>Low Speed Channel B Inputs.</b> INBP and INBN comprise the low speed side transmit direction Channel B differential input signals. These signals must be AC coupled.  |
| OUTB[3:0]P/N     | M7/M6<br>L6/L5<br>K5/K4<br>J3/H3 | Output CML<br>VDDA_LS                          | <b>Low Speed Channel B Outputs.</b> OUTBP and OUTBN comprise the low speed side receive direction Channel B differential output signals. During device reset (RESET_N asserted low) these pins are driven differential zero. These signals must be AC coupled.   |

**Table 2-1. Pin Description - Signal Pins (continued)**

| TERMINAL   |                  | DIRECTION<br>TYPE<br>SUPPLY                    | DESCRIPTION   |
|--|------------------|--|---|
| SIGNAL   | BGA              |  |   |
| LOSB   | K8               | Output<br>LVCMOS 1.5V/1.8V<br>VDDO1 40Ω Driver | <p><b>Channel B Receive Loss Of Signal (LOS) Indicator.</b><br/>           LOSB=0: Signal detected.<br/>           LOSB=1: Loss of signal.<br/>           Loss of signal detection is based on the input signal level.<br/>           When HSRXBP/N has a differential input signal swing of <math>\leq 75</math> mV<sub>pp</sub>, LOSB will be asserted (if enabled). If the input signal is greater than 150 mV<sub>p-p</sub>, LOS will be deasserted. Outside of these ranges, the LOS indication is undefined.</p> <p>Other functions can be observed on LOSB real-time, configured via MDIO</p> <p>During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PDTRXB_N asserted low), this pin is floating. During register based power down, this pin is floating.</p> <p>It is highly recommended that LOSB be brought to easily accessible point on the application board (header), in the event that debug is required.</p> |
| LS_OK_IN_B   | L8               | Input<br>LVCMOS 1.5V/1.8V<br>VDDO0             | <p><b>Channel B Receive Lane Alignment Status Indicator.</b> Lane alignment status signal received from a Lane Alignment Slave on the link partner device. Valid in 10G General Purpose Serdes Mode.<br/>           LS_OK_IN_B=0: Channel B Receive lanes not aligned.<br/>           LS_OK_IN_B=1: Channel B Receive lanes aligned</p>   |
| LS_OK_OUT_B  | H9               | Output<br>LVCMOS 1.5V/1.8V<br>VDDO0 40Ω Driver | <p><b>Channel B Transmit Lane Alignment Status Indicator.</b> Lane alignment status signal sent to a Lane Alignment Master on the link partner device. Valid in 10G General Purpose Serdes Mode.<br/>           LS_OK_OUT_B=0: Channel B Transmit lanes not aligned.<br/>           LS_OK_OUT_B=1: Channel B Transmit lanes aligned.</p>  |
| PDTRXB_N   | J4               | Input<br>LVCMOS<br>1.5V/1.8V VDDO1             | <p><b>Transceiver Power Down.</b> When this pin is held low (asserted), Channel B is placed in power down mode. When deasserted, Channel B operates normally. After deassertion, a software data path reset should be issued through the MDIO interface.</p>  |
| <b>REFERENCE CLOCKS, OUTPUT CLOCKS, AND CONTROL AND MONITORING SIGNALS</b> |                  |  |   |
| REFCLK0P/N   | M10<br>M11       | Input<br>LVDS/ LVPECL<br>DVDD                  | <p><b>Reference Clock Input Zero.</b> This differential input is a clock signal used as a reference to channels A or B. The reference clock selection is done through MDIO. This input signal <b>must</b> be AC coupled. If unused, REFCLK0P/N should be pulled down to GND through a shared 100 Ω resistor.</p>  |
| REFCLK1P/N   | K9<br>K10        | Input<br>LVDS/ LVPECL<br>DVDD                  | <p><b>Reference Clock Input One.</b> This differential input is a clock signal used as a reference to channels A or B. The reference clock selection is done through MDIO. This input signal <b>must</b> be AC coupled. If unused, REFCLK1P/N should be pulled down to GND through a shared 100 Ω resistor.</p>   |
| CLKOUTAP/N<br>CLKOUTBP/N   | C9/C10<br>A9/A10 | Output<br>CML<br>DVDD                          | <p><b>Channel A/B Output Clock.</b> By default, these outputs are enabled and output the high speed side Channel A recovered byte clock (high speed line rate divided by 16 or 20). Optionally, they can be configured to output the VCO clock divided by 2. (Note: for full rates, VCO/2 pre-divided clocks will be equivalent to the line rate divided by 8; for sub-rates, VCO/2 pre-divided clocks will be equivalent to the line rate divided by 4).</p> <p>These CML outputs must be AC coupled.</p> <p>During device reset (RESET_N asserted low), pin-based power down (PDTRXA_N and PDTRXB_N asserted low), or register-based power down, these pins are floating.</p>   |
| PRBSEN   | B9               | Input<br>LVCMOS 1.5V/1.8V<br>VDDO0             | <p><b>Enable PRBS:</b> When this pin is asserted high, the internal PRBS generator and verifier circuits are enabled on both transmit and receive data paths on high speed and low speed sides of both channels.</p> <p>The PRBS 2<sup>7</sup>-1 pattern is selected by default, and can be changed through MDIO.</p>   |
| PRBS_PASS  | J9               | Output<br>LVCMOS 1.5V/1.8V<br>VDDO1 40Ω Driver | <p><b>Receive PRBS Error Free (Pass) Indicator.</b><br/>           When PRBS test is enabled (PRBSEN=1):<br/>           PRBS_PASS=1 indicates that PRBS pattern reception is error free.<br/>           PRBS_PASS=0 indicates that a PRBS error is detected. The channel, high speed or low speed side, and lane (for low speed side) that this signal refers to is chosen through MDIO.</p> <p>During device reset (RESET_N asserted low) this pin is driven high.<br/>           During pin based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is floating.<br/>           During register based power down, this pin is floating.</p> <p>It is highly recommended that PRBS_PASS be brought to easily accessible point on the application board (header), in the event that debug is required.</p>  |
| ST   | M9               | Input<br>LVCMOS 1.5V/1.8V<br>VDDO[1:0]         | <p><b>MDIO Select.</b> Used to select Clause 22 (=1) or Clause 45 (=0) operation. Note that selecting clause 22 will impact mode availability. See MODE_SEL.</p> <p>A hard or soft reset must be applied after a change of state occurs on this input signal.</p>   |
| MODE_SEL   | H10              | Input LVCMOS<br>1.5V/1.8V VDDO[1:0]            | <p><b>Device Operating Mode Select.</b><br/>           Used together with ST pin to select device operating mode. See <a href="#">Table 2-3</a> for details.</p>  |

**Table 2-1. Pin Description - Signal Pins (continued)**

| TERMINAL   |                             | DIRECTION<br>TYPE<br>SUPPLY                            | DESCRIPTION   |
|------------|-----------------------------|--|---|
| SIGNAL     | BGA                         |  |   |
| PRTAD[4:0] | M8<br>J6<br>L9<br>G9<br>E10 | Input LVCMOS<br>1.5V/1.8V VDDO[1:0]                    | <p><b>MDIO Port Address.</b> Used to select the MDIO port address.</p> <p>PRTAD[4:1] selects the MDIO port address. The TLK10232 has two different MDIO port addresses. Selecting a unique PRTAD[4:1] per TLK10232 device allows 16 TLK10232 devices per MDIO bus. Each channel can be accessed by setting the appropriate port address field within the serial interface protocol transaction.</p> <p>The TLK10232 will respond if the 4 MSB's of the port address field on MDIO protocol (PA[4:1]) matches PRTAD[4:1].<br/>If PA[0] = 1'b0, TLK10232 Channel A will respond.<br/>If PA[0] = 1'b1, TLK10232 Channel B will respond.</p> <p>PRTAD0 is not needed for port addressing, but can be used as a general purpose input pin to control the switching function or the stopwatch latency measurement. If these functions are not needed, PRTAD0 should be grounded on the application board.</p> |
| RESET_N    | H5                          | Input LVCMOS<br>1.5V/1.8V VDDO01                       | <b>Low True Device Reset.</b> RESET_N must be held asserted (low logic level) for at least 10us after device power stabilization.   |
| MDC        | J8                          | Input LVCMOS<br>with Hysteresis<br>1.5V/1.8V VDDO1     | <b>MDIO Clock Input.</b> Clock input for the MDIO interface.<br>Note that an external pullup is generally not required on MDC except if driven by an open-drain/open-collector clock source.  |
| MDIO       | J7                          | Input/ Output<br>LVCMOS 1.5V/1.8V<br>VDDO1 25Ω Driver  | <b>MDIO Data I/O.</b> MDIO interface data input/output signal for the MDIO interface. <b>This signal must be externally pulled up to VDDO using a 2kΩ resistor.</b><br>During device reset (RESET_N asserted low) this pin is floating. During software initiated power down the management interface remains active for control register writes and reads. Certain status bits will not be deterministic as their generating clock source may be disabled as a result of asserting either power down input signal. During pin based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is floating. During register based power down, this pin is driven normally.  |
| TDI        | C8                          | Input LVCMOS<br>1.5V/1.8V VDDO0<br>(Internal Pullup)   | <b>JTAG Input Data.</b> TDI is used to serially shift test data and test instructions into the device during the operation of the test port. In system applications where JTAG is not implemented, this input signal may be left floating.<br>During pin based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is not pulled up. During register based power down, this pin is pulled up normally.  |
| TDO        | D6                          | Output LVCMOS<br>1.5V/1.8V VDDO0<br>50Ω Driver         | <b>JTAG Output Data.</b> TDO is used to serially shift test data and test instructions out of the device during operation of the test port. When the JTAG port is not in use, TDO is in a high impedance state.<br>During device reset (RESET_N asserted low) this pin is floating. During pin based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is not pulled up. During register based power down, this pin is pulled up normally.  |
| TMS        | B8                          | Input LVCMOS<br>1.5V/1.8V VDDO0<br>(Internal Pullup)   | <b>JTAG Mode Select.</b> TMS is used to control the state of the internal test-port controller. In system applications where JTAG is not implemented, this input signal can be left unconnected.<br>During pin based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is not pulled up. During register based power down, this pin is pulled up normally.  |
| TCK        | D8                          | Input LVCMOS<br>with Hysteresis<br>1.5V/1.8V VDDO0     | <b>JTAG Clock.</b> TCK is used to clock state information and test data into and out of the device during boundary scan operation. In system applications where JTAG is not implemented, this input signal should be grounded.  |
| TRST_N     | E5                          | Input LVCMOS<br>1.5V/1.8V VDDO0<br>(Internal Pulldown) | <b>JTAG Test Reset.</b> TRST_N is used to reset the JTAG logic into system operational mode. This input can be left unconnected in the application and is pulled down internally, disabling the JTAG circuitry. If JTAG is implemented on the application board, this signal should be deasserted (high) during JTAG system testing, and otherwise asserted (low) during normal operation mode.<br>During pin based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is not pulled up. During register based power down, this pin is pulled up normally.   |
| TESTEN     | L10                         | Input LVCMOS<br>1.5V/1.8V VDDO1                        | <b>Test Enable.</b> This signal is used during the device manufacturing process. It should be grounded through a resistor in the device application board. The application board should allow the flexibility of easily reworking this signal to a high level if device debug is necessary (by including an uninstalled resistor to VDDO).  |
| GPIO       | J10                         | Input LVCMOS<br>1.5V/1.8V VDDO1                        | <b>General Purpose Input.</b> This signal is used during the device manufacturing process. It should be grounded through a resistor on the device application board. The application board should also allow the flexibility of easily reworking this signal to a high level if device debug is necessary (by including an uninstalled resistor to VDDO).   |
| AMUXA      | C11                         | Analog I/O   | <b>SERDES Channel A Analog Testability I/O.</b> This signal is used during the device manufacturing process. It should be left unconnected in the device application.   |
| AMUXB      | D4                          | Analog I/O   | <b>SERDES Channel B Analog Testability I/O.</b> This signal is used during the device manufacturing process. It should be left unconnected in the device application.   |



**Table 2-2. Pin Description - Power Pins**

| TERMINAL    |   | TYPE   | DESCRIPTION  |
|-------------|---|--------|--|
| SIGNAL      | BGA   |        |  |
| VDDA_LS/HS  | D2, F2, G2, J2, G10, F11  | Power  | <b>SERDES Analog Power.</b><br>VDDA_LS and VDDA_HS provide supply voltage for the analog circuits on the low-speed and high-speed sides respectively. 1.0V nominal. Can be tied together on the application board.                 |
| VDDT_LS/HS  | F4, G4, F9  | Power  | <b>SERDES Analog Power.</b><br>VDDT_LS and VDDT_HS provide termination and supply voltage for the analog circuits on the low-speed and high-speed sides respectively. 1.0V nominal. Can be tied together on the application board. |
| VDDD        | E6, F6, H6, E8, H8  | Power  | <b>SERDES Digital Power.</b><br>VDDD provides supply voltage for the digital circuits internal to the SERDES. 1.0V nominal.  |
| DVDD        | G6, E7, F7, H7, G8  | Power  | <b>Digital Core Power.</b><br>DVDD provides supply voltage to the digital core. 1.0V nominal.  |
| VDDRA_LS/HS | C3<br>E11   | Power  | <b>SERDES Analog Regulator Power.</b><br>VDDRA_LS and VDDRA_HS provide supply voltage for the internal PLL regulator for Channel A low speed and high speed sides respectively. 1.5V or 1.8V nominal.                              |
| VDDRB_LS/HS | K3<br>J11   | Power  | <b>SERDES Analog Regulator Power</b><br>VDDRB_LS and VDDRB_HS provide supply voltage for the internal PLL regulator for Channel B low speed and high speed sides respectively. 1.5V or 1.8V nominal.                               |
| VDDO[1:0]   | K7<br>C7  | Power  | <b>LVC MOS I/O Power.</b><br>VDDO0 and VDDO1 provide supply voltage for the LVC MOS inputs and outputs. 1.5V or 1.8V nominal. Can be tied together on the application board.   |
| VPP         | D7  | Power  | <b>Factory Program Voltage.</b><br>Used during device manufacturing. The application must connect this power supply directly to DVDD.  |
| VSS         | A2, A5, A11, B3, B4, B7, B11, C1, C6, C12, D3, D5, D10, D11, E2, E4, F1, F5, F8, F10, F12, G1, G3, G5, G7, G11, H2, H4, H11, J5, J12, K1, K6, K11, L3, L4, L7, L11, M2, M5, M12 | Ground | <b>Ground.</b><br>Common analog and digital ground.  |

## 2.4 Operating Modes

The TLK10232 is a versatile high-speed transceiver device that is designed to perform various physical layer functions in three operating modes: 10GBASE-KR Mode, 1G-KX Mode, and General Purpose (10G) SERDES Mode. The three modes are described in three separate sections. The device operating mode is determined by the MODE\_SEL and ST pin settings, as well as MDIO register 1E.0001 bit 10.

**Table 2-3. TLK10232 Operating Mode Selection**

|   | ST = 0 (Clause 45)                       | ST = 1 (Clause 22)     |
|---|--|------------------------|
| {MODE_SEL pin, Register 1E.0001 bit 10} |  |                        |
| 1x                                      | 10G                                      | 10G                    |
| 01                                      | 10G                                      | 10G                    |
| 00                                      | 10G-KR/1G-KX<br>(Determined by Auto Neg) | 1G-KX<br>(No Auto Neg) |

### 3 10GBASE-KR MODE FUNCTIONAL DESCRIPTION

A simplified block diagram of the transmit and receive data paths in 10GBASE-KR mode is shown in Figure 3-1. This section gives a high-level overview of how data moves through these paths, then gives a more detailed description of each block’s functionality.

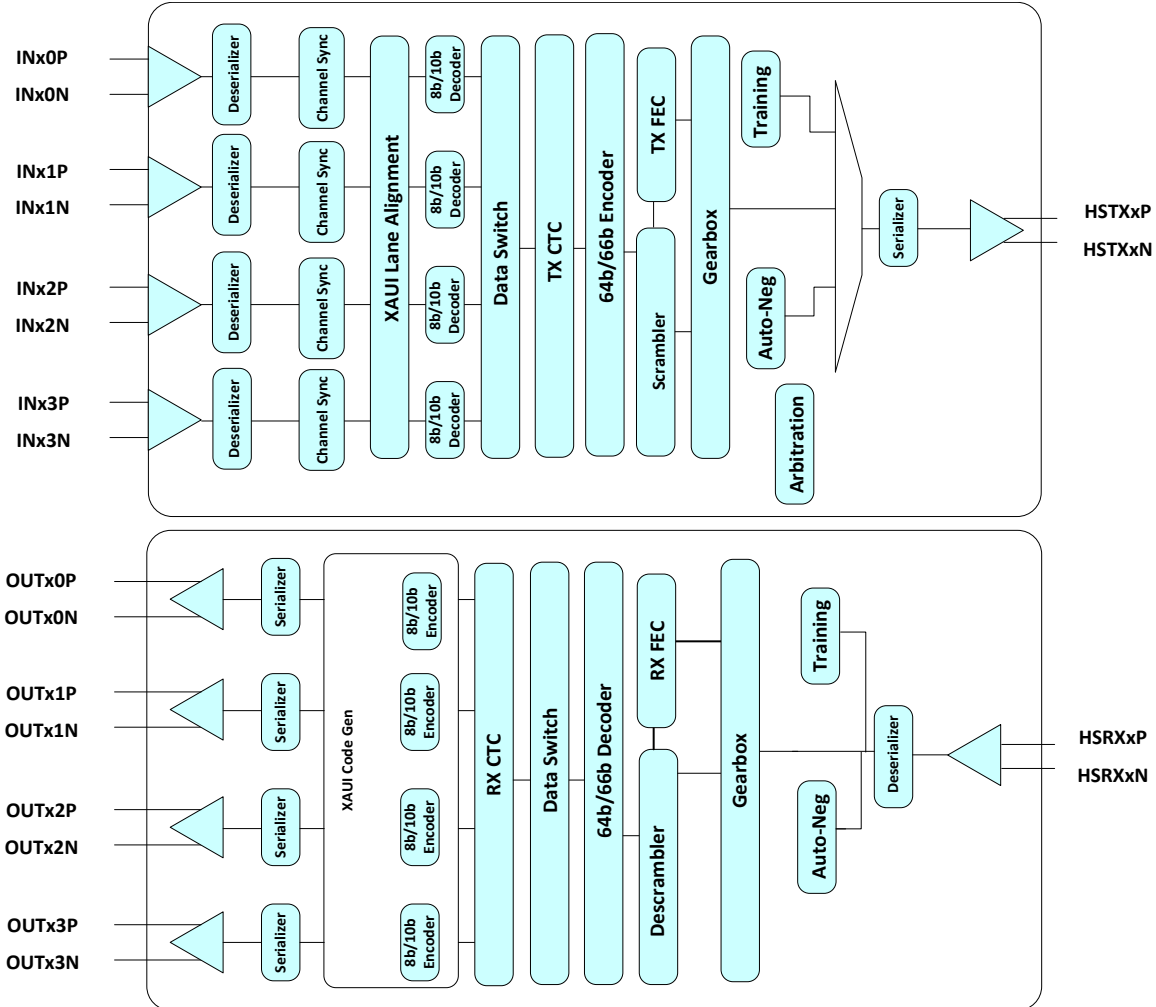


Figure 3-1. A Simplified One Channel KR Data Path Block Diagram

#### 3.1 10GBASE-KR Transmit Data Path Overview

In 10GBASE-KR Mode, the TLK10232 takes in XAUI data on the four low speed input lanes. The serial data in each lane is deserialized into 10-bit parallel data, then byte aligned (channel synchronized) based on comma detection. The four XAUI lanes are then aligned with one another, and the aligned data is input to four 8B/10B decoders. The decoded data is then input to the transmit clock tolerance compensation (CTC) block which compensates for any frequency offsets between the incoming XAUI data and the local reference clock. The CTC block then delivers the data to a 64B/66B encoder and a scrambler. The resulting scrambled 10GBASE-KR data is then input to a transmit gearbox which in turn delivers it to the high speed side SERDES for serialization and output through the HSTX\*P/N pins.

### 3.2 10GBASE-KR Receive Data Path Overview

In the receive direction, the TLK10232 will take in 64B/66B-encoded serial 10GBASE-KR data on the HSRX\*P/N pins. This data is deserialized by a high speed SERDES, then input to a receive gearbox. After the gearbox, the data is aligned to 66-bit frames, descrambled, 64B/66B decoded, and then input to the receive CTC block. After CTC, the data is encoded by four 8B/10B encoders, and the resulting four 10-bit parallel words are serialized by the low speed SERDES blocks. The four serial XAUI output lanes are transmitted out the OUT\*P/N pins.

### 3.3 Channel Synchronization Block

When parallel data is clocked into a parallel-to-serial converter, the byte boundary that was associated with the parallel data is lost in the serialization of the data. When the serial data is received and converted to parallel format again, a method is needed to be able to recognize the byte boundary again. Generally, this is accomplished through the use of a synchronization pattern. This is a unique pattern of 1's and 0's that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. 8B/10B encoding contains a character called the comma (b'0011111' or b'1100000') which is used by the comma detect circuit to align the received serial data back to its original byte boundary. The TLK10232 channel synchronization block detects the comma pattern found in the K28.5 character, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding. It is important to note that the comma can be either a (b'0011111') or the inverse (b'1100000') depending on the running disparity. The TLK10232 decoder will detect both patterns.

The TLK10232 performs channel synchronization per lane as shown in the flowchart of [Figure 3-2](#).

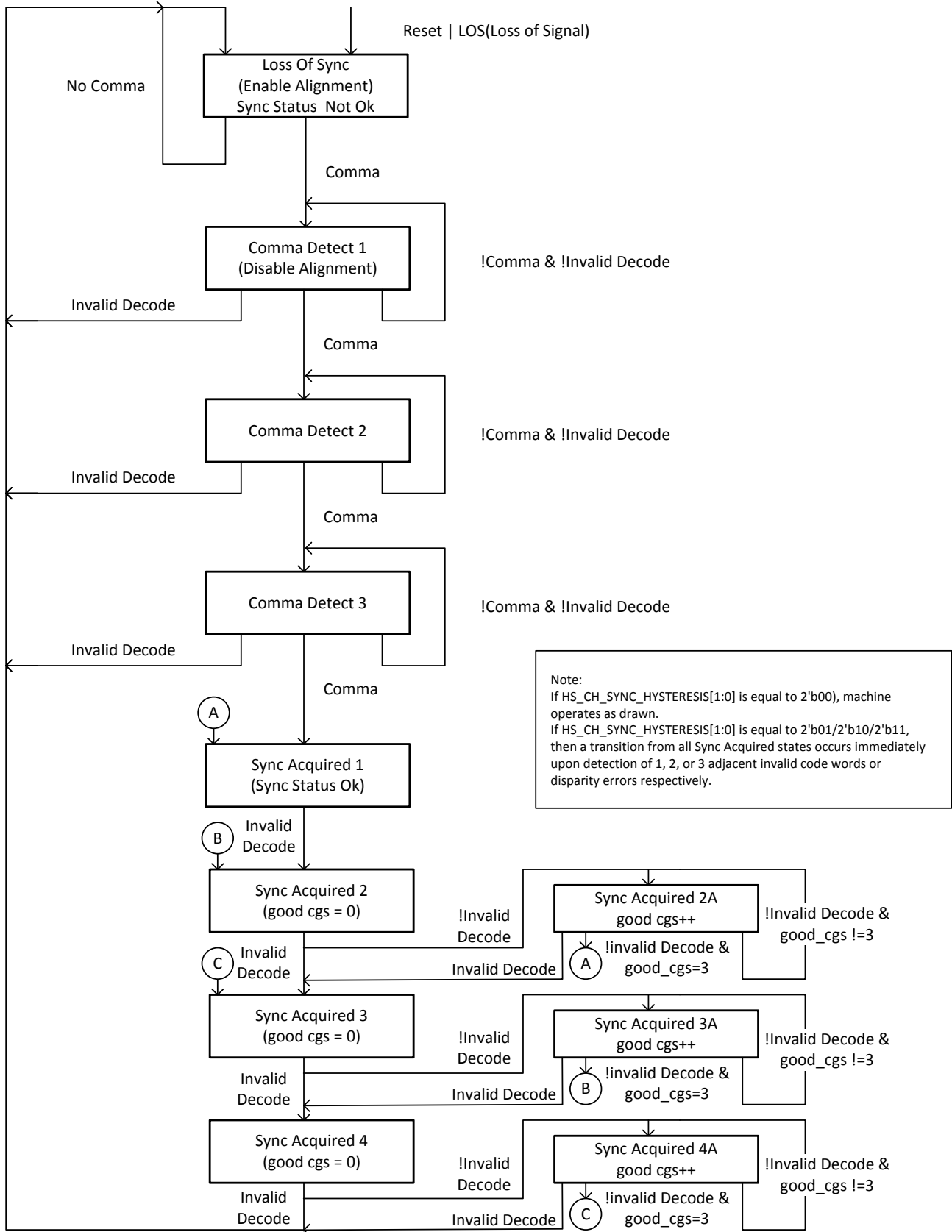


Figure 3-2. Channel Synchronization Flowchart

### 3.4 8B/10B Encoder

Embedded-clock serial interfaces require a method of encoding to ensure sufficient transition density for the receiving CDR to acquire and maintain lock. The encoding scheme also maintains the signal DC balance by keeping the number of ones and zeros balanced which allows for AC coupled data transmission. The TLK10232 uses the 8B/10B encoding algorithm that is used by the 10 Gbps and 1 Gbps Ethernet and Fibre Channel standards. This provides good transition density for clock recovery and improves error checking.

The 8B/10B encoder converts each 8-bit wide data to a 10-bit wide encoded data character to improve its transition density. This transmission code includes /D/ characters, used for transmitting data, and /K/ characters, used for transmitting protocol information. Each /K/ or /D/ character code word can also have both a positive and a negative disparity version. The disparity of a code word is selected by the encoder to balance the running disparity of the serialized data stream.

### 3.5 8B/10B Decoder

Once the Channel Synchronization block has identified the byte boundaries from the received serial data stream, the 8B/10B decoder converts 10-bit 8B/10B-encoded characters into their respective 8-bit formats. When a code word error or running disparity error is detected in the decoded data, the error is reported in the status register (1E.000F) and the LOS pin is asserted (depending on the LOS overlay selection).

### 3.6 64B/66B Encoder/Scrambler

To facilitate the transmission of data received from the media access control (MAC) layer, the TLK10232 encodes data received from the MAC using the 64B/66B encoding algorithm defined in the IEEE802.3-2008 standard. The TLK10232 takes two consecutive transfers from the XAUI interface and encodes them into a 66-bit code word. The information from the two XAUI transfers includes 64 bits of data and 8 bits of control information after 8B/10B decoding.

If the 64B/66B encoder detects an invalid packet format from the XAUI interface, it replaces erroneous information with appropriately-encoded error information. The resulting 66-bit code word is then sent on to the transmit gearbox.

The encoding process implemented in the TLK10232 includes two steps:

1. an encoding step, which converts the 72 bits of data (8 data bytes plus 8 control-code indicators) received from the transmit CTC FIFO into a 66-bit code word
2. a scrambling step, which scrambles 64 bits of encoded data using the scrambler polynomial  $x^{58}+x^{39}+1$ . The 66 bits created by the encoder consists of 64 bits of data and a 2-bit synchronization field consisting of either 01 or 10. Only the 64 bits of data are scrambled, leaving the two synchronization bits unmodified. The two synchronization bits allow the receive gearbox to obtain frame alignment and, in addition, ensure an edge transition of at least once in 66 bits of data. The encoding process allows a limited amount of control information to be sent in-line with the data.

### 3.7 Forward Error Correction

Optionally enabled, Forward Error Correction (FEC) follows the IEEE 802.3-2008 standard, and is able to correct a burst errors up to 11 bits. In the TX data path, the FEC logic resides between the scrambler and gearbox. In the RX datapath, FEC resides between the gearbox and descrambler. Frame alignment is handled inside the RX FEC block during FEC operation, and the RX gearbox sync header alignment is bypassed. Because latency is increased in both the TX and RX data paths with FEC enabled, it is disabled by default and must be enabled through MDIO programming. Note that FEC by nature will add latency due to frame storage.

### 3.8 64B/66B Decoder/Descrambler

The data received from the serial 10GBASE-KR is 64B/66B-encoded data. The TLK10232 decodes the data received using the 64B/66B decoding algorithm defined in the IEEE 802.3-2008 standard. The TLK10232 creates consecutive 72-bit data words from the encoded 66-bit code words for transfer over the XAUI interface to the MAC. The information for the two XAUI transfers includes 64 bits of data and 8 bits of control information before 8B/10B encoding.

Not all 64B/66B block payloads are valid. Invalid block payloads are handled by the 64B/66B decoder block and appropriate error handling is provided, as defined in the IEEE 802.3-2008 standard. The decoding algorithm includes two steps: a descrambling step which descrambles 64 bits of the 66-bit code word with the scrambling polynomial  $x^{58}+x^{39}+1$ , and a decoding step which converts the 66 bits of data received into 64 bits of data and 8 bits of control information. These words are sent to the receive CTC FIFO.

### 3.9 Transmit Gearbox

The function of the transmit gearbox is to convert the 66-bit encoded, scrambled data stream into a 16-bit-wide data stream to be sent out to the serializer and ultimately to the physical medium attachment (PMA) device. The gearbox is needed because while the effective bit rate of the 66-bit data stream is equal to the effective bit rate of the 16-bit data, the clock rates of the two buses are of different frequencies.

### 3.10 Receive Gearbox

While the transmit gearbox only performs the task of converting 66-bit data to be transported on to the 16-bit serializer, the receive gearbox has more to do than just the reverse of this function. The receive gearbox must also determine where within the incoming data stream the boundaries of the 66-bit code words are.

The receive gearbox has the responsibility of initially synchronizing the header field of the code words and continuously monitoring the ongoing synchronization. After obtaining synchronization to the incoming data stream, the gearbox assembles 66-bit code words and presents these to the 64B/66B decoder.

Note that in FEC mode, the Receive Gearbox blindly converts 16-bit data to 66-bit data and depends on the RX FEC logic to frame align the data.

### 3.11 XAUI Lane Alignment / Code Gen (XAUI PCS)

The XAUI interface standard is defined to allow for 21 UI of skew between lanes. This block is implemented to handle up to 30 UI (XAUI UI) of skew between lanes using /A/ characters. The state machine follows the standard 802.3-2008 defined state machine.

### 3.12 Inter-Packet Gap (IPG) Characters

The XAUI interface transports information that consists of packets and inter-packet gap (IPG) characters. The IEEE 802.3-2008 standard defines that the IPG, when transferred over the XAUI interface, consists of alignment characters (/A/), control characters (/K/) and replacement characters (/R/).

TLK10232 converts all AKR characters to IDLE characters, performs insertions or deletions on the IDLE characters, and transmits only encoded IDLE characters out to the 10GBASE-KR interface. The receive channel expects encoded IDLE characters to enter the 10GBASE-KR interface, and performs insertions and deletions on IDLE characters and then converts IDLE characters back to AKR characters. Any AKR characters received on the high speed interface are by default converted to IDLE characters for reconversion to AKR columns.

Both the transmit and receive FIFOs rely upon a valid IDLE stream to perform clock tolerance compensation (CTC).

### 3.13 Clock Tolerance Compensation (CTC)

The XAUI interface is defined to allow for separate clock domains on each side of the link. Though the reference clocks for two devices on a XAUI link have the same specified frequencies, there can be slight differences that, if not compensated for, will lead to over or under run of the FIFO's on the receive/transmit data path. The TLK10232 provides compensation for these differences in clock frequencies via the insertion or the removal of idle (I) characters on all lanes, as shown in Figure 3-3 and Figure 3-4.

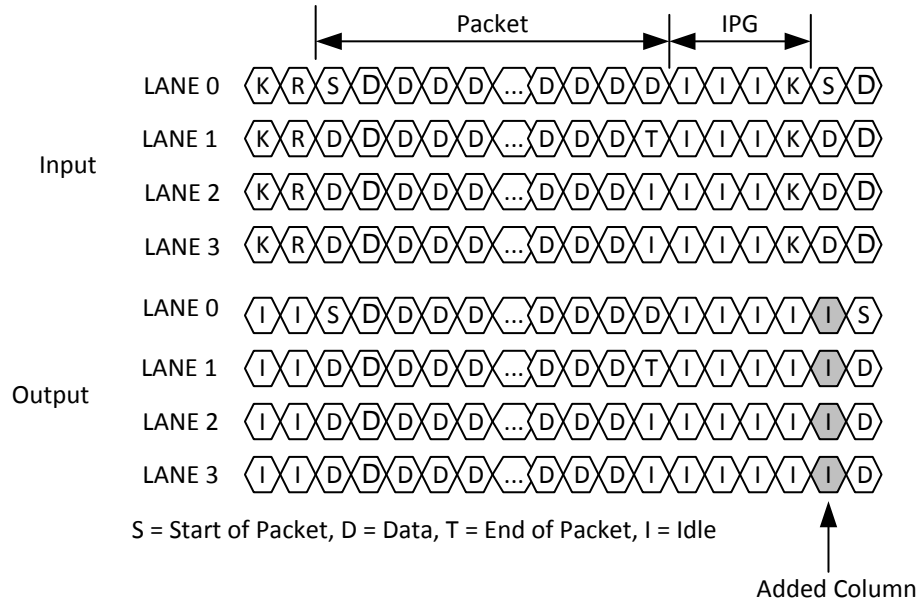


Figure 3-3. Clock Tolerance Compensation: Add

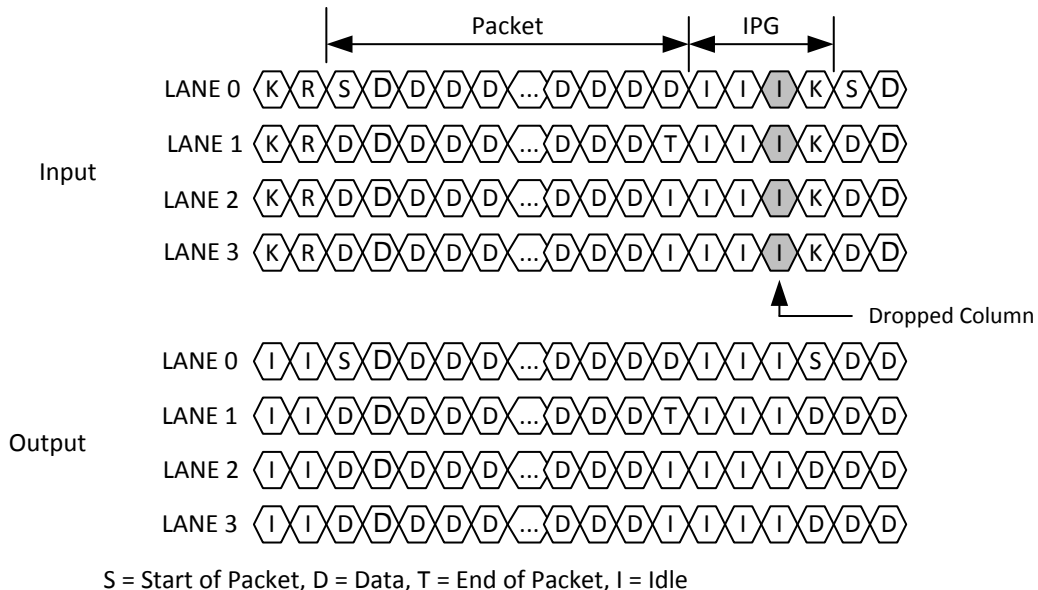


Figure 3-4. Clock Tolerance Compensation: Drop

The TLK10232 allows for provisioning of both the CTC FIFO depth and the low/high watermark thresholds that trigger idle insertion/deletion beyond the standard requirements. This allows for optimization between maximum clock tolerance and packet length. For more information on the TLK10232 CTC provisioning, see Appendix A.

### 3.14 10GBASE-KR Auto-Negotiation

When TLK10232 is selected to operate in 10GKR/1G-KX mode (MODE\_SEL pin held low), Clause 73 Auto-Negotiation will commence after power up or hardware or software reset. The data path chosen from the result of Auto-Negotiation will be the highest speed of 10G-KR or 1G-KX as advertised in the MDIO ability fields (set to 10G-KR by default). If 10G-KR is chosen, link training will commence immediately following the completion of Auto-Negotiation. Legacy devices that operate in 1G-KX mode and do not support Clause 73 Auto Negotiation will be recognized through the Clause 73 parallel detection mechanism.

### 3.15 10GBASE-KR Link Training

Link training for 10G-KR mode is performed after auto-negotiation, and follows the procedure described in IEEE 802.3-2008. The high speed TX SERDES side will update pre-emphasis tap coefficients as requested through the Coefficient update field. Received training patterns are monitored for bit errors (MDIO configurable), and requests are made to update partner channel TX coefficients until optimal settings are achieved.

The RX link training algorithm consists of sending a series of requests to move the link partner's transmitter tap coefficients to the center point of an error free region. Once link training has completed, the 10G-KR data path is enabled. If link is lost, the entire process repeats with auto-negotiation, link training, and 10G-KR mode.

TLK10232 also offers a manual mode whereby coefficient update requests are handled through external software management.

### 3.16 10GBASE-KR Line Rate, PLL Settings, and Reference Clock Selection

The TLK10232 includes internal low-jitter high quality oscillators that are used as frequency multipliers for the low speed and high speed SERDES and other internal circuits of the device. Specific MDIO registers are available for SERDES rate and PLL multiplier selection to match line rates and reference clock (REFCLK0/1) frequencies for various applications.

The external differential reference clock has a large operating frequency range allowing support for many different applications. A low-jitter reference clock should be used, and its frequency accuracy should be within  $\pm 200$  PPM of the incoming serial data rate ( $\pm 100$  PPM of nominal data rate).

When the TLK10232 device is set to operate in the 10GBASE-KR mode with a low speed side line rate of 3.125 Gbps and a high speed side line rate of 10.3125 Gbps, the reference clock choices are as shown in [Table 3-1](#). In general, using a higher reference clock frequency results in improved jitter performance.

**Table 3-1. Specific Line Rate and Reference Clock Selection for the 10GBASE-KR Mode:**

| LOW SPEED SIDE   |                       |      |                 | HIGH SPEED SIDE  |                       |      |                 |
|------------------|-----------------------|------|-----------------|------------------|-----------------------|------|-----------------|
| Line Rate (Mbps) | SERDES PLL Multiplier | Rate | REFCLKP/N (MHz) | Line Rate (Mbps) | SERDES PLL Multiplier | Rate | REFCLKP/N (MHz) |
| 3125             | 10                    | Full | 156.25          | 10312.5          | 16.5                  | Full | 156.25          |
| 3125             | 5                     | Full | 312.5           | 10312.5          | 8.25                  | Full | 312.5           |

### 3.17 10GBASE-KR Test Pattern Support

The TLK10232 has the capability to generate and verify various test patterns for self-test and system diagnostic measurements. The following test patterns are supported:

- High Speed (HS) Side: PRBS  $2^7 - 1$ , PRBS  $2^{23} - 1$ , PRBS  $2^{31} - 1$ , Square Wave with Provisionable Length, and KR Pseudo-Random Pattern
- Low Speed (LS) Side: PRBS  $2^7 - 1$ , PRBS  $2^{23} - 1$ , PRBS  $2^{31} - 1$ , High Frequency, Low Frequency, Mixed Frequency, CRPAT, CJPAT.



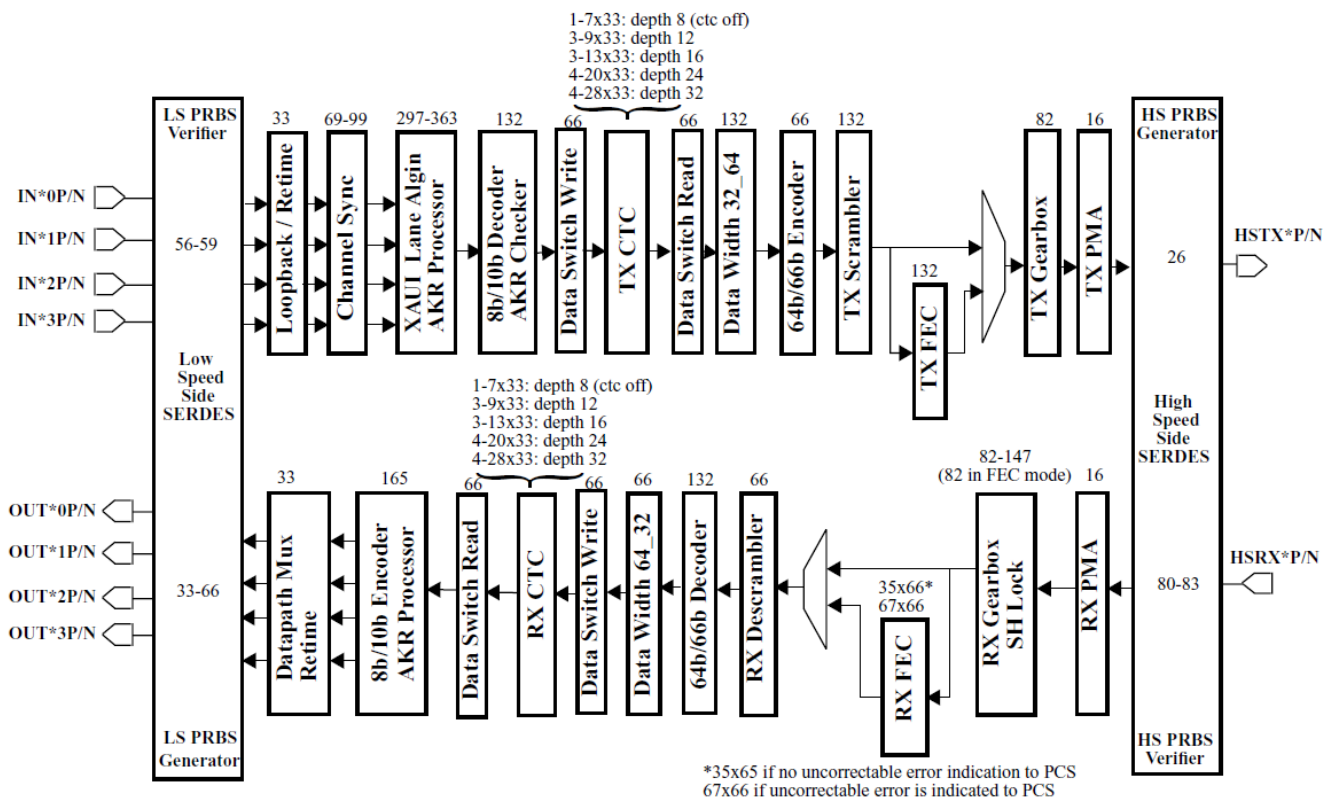
The TLK10232 provides two pins: PRBSEN and PRBS\_PASS, for additional control and monitoring of PRBS pattern generation and verification. When PRBSEN is asserted high, the internal PRBS generator and verifier circuits are enabled on both transmit and receive data paths on high speed and low speed sides of all channels. PRBS 2<sup>7</sup>-1 is selected by default, and can be changed through MDIO.

When PRBS test is enabled (PRBSEN=1):

- PRBS\_PASS = 1 indicates that PRBS pattern reception is error free.
- PRBS\_PASS = 0 indicates that a PRBS error is detected. The channel, the side (high speed or low speed), and the lane (for low speed side) that this signal refers to is chosen through MDIO.

### 3.18 10GBASE-KR Latency

The latency through the TLK10232 in 10GBASE-KR mode is as shown in Figure 3-5. Note that the latency ranges shown indicate static rather than dynamic latency variance, i.e., the range of possible latencies when the serial link is initially established. During normal operation, the latency through the device is fixed.



TX, FEC bypassed, CTC depth 12: 1269-1569 UI (123ns - 152ns)

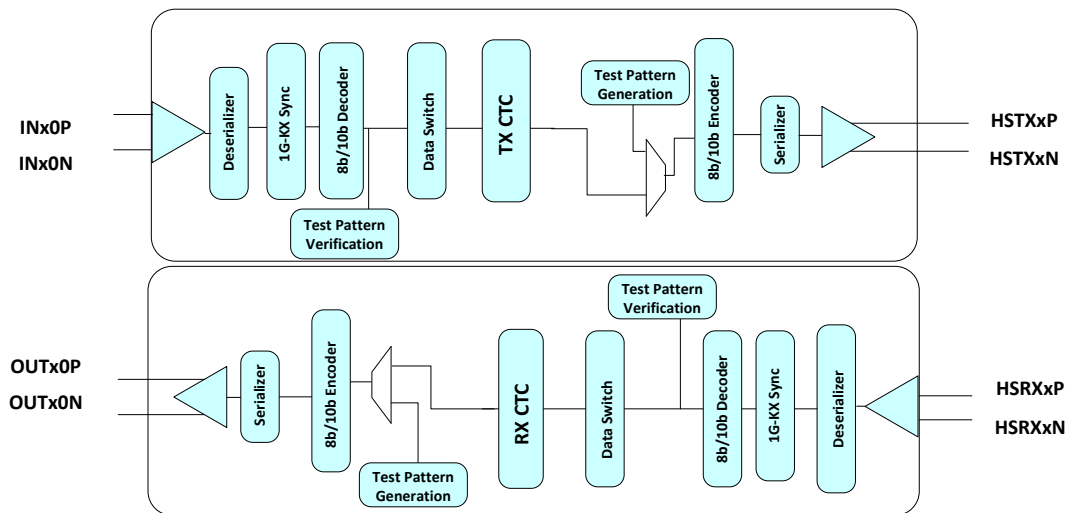
NOTE: TX Latency numbers represent no external skew between lanes. External lane skew will increase overall latency

RX, FEC bypassed, CTC depth 12: 838-1203 UI (81ns - 117ns)

Figure 3-5. 10GBASE-KR Mode Latency Per Block

## 4 1GBASE-KX MODE FUNCTIONAL DESCRIPTION

A simplified block diagram of the 1GBASE-KX data path is shown in [Figure 4-1](#).



**Figure 4-1. A Simplified One Channel Block Diagram of the 1GKX Data Path**

### 4.1 Channel Sync Block

This block is used to align the deserialized signals to the proper 10-bit word boundaries. The Channel Sync block generates a synchronization flag indicating incoming data is synchronized to the correct word boundary. This module implements the synchronization state machine found in Figure 36-9 of the IEEE 802.3-2008 Standard. A synchronization status signal, latched low, is available to indicate synchronization errors.

### 4.2 8b/10b Encoder and Decoder Blocks

As in the 10GBASE-KR operating mode, these blocks are used to convert between 10-bit (encoded) data and 8-bit data words. They can be optionally bypassed. A code invalid signal, latched low, is available to indicate 8b/10b encode and decode errors.

### 4.3 TX CTC

The transmit clock tolerance compensation (CTC) block acts as a FIFO with add and delete capabilities, adding and deleting 2 cycles each time to support  $\pm 200$ ppm during IFG (no errors) between the read and write clocks. This block implements a 12 deep asynchronous FIFO with a usable space 8 deep. It has two separate pointer tracking systems. One determines when to delete or insert and another determines when to reset. Inserts and deletes are only allowed during non-errored inter-frame gaps and occurs 2 cycles at a time. It has an auto reset feature once collision occurs. If a collision occurs, the indication is latched high until read by MDIO.

### 4.4 1GBASE-KX Line Rate, PLL Settings, and Reference Clock Selection

When the TLK10232 is configured to operate in the 1GBASE-KX mode, the available line rates, reference clock frequencies, and corresponding PLL multipliers are summarized in [Table 4-1](#).

**Table 4-1. Specific Line Rate and Reference Clock Selection for the 1GBASE-KX Mode**

| LOW SPEED SIDE      |                       |         |                    | HIGH SPEED SIDE                 |                       |         |                    |
|---------------------|-----------------------|---------|--------------------|---------------------------------|-----------------------|---------|--------------------|
| Line Rate (Mbps)    | SERDES PLL Multiplier | Rate    | REFCLKP/N (MHz)    | Line Rate (Mbps) <sup>(1)</sup> | SERDES PLL Multiplier | Rate    | REFCLKP/N (MHz)    |
| 3125 <sup>(2)</sup> | 10                    | Full    | 156.25             | 3125 <sup>(2)</sup>             | 10                    | Full    | 156.25             |
| 3125 <sup>(2)</sup> | 5                     | Full    | 312.5              | 3125 <sup>(2)</sup>             | 5                     | Full    | 312.5              |
| 1250                | 10                    | Half    | 125 <sup>(2)</sup> | 1250                            | 20                    | Quarter | 125 <sup>(2)</sup> |
| 1250                | 8                     | Half    | 156.25             | 1250                            | 16                    | Quarter | 156.25             |
| 1250                | 8                     | Quarter | 312.5              | 1250                            | 8                     | Quarter | 312.5              |

(1) High Speed Side SERDES runs at 2x effective data rate.

(2) Manual mode only, as auto negotiation does not support 125Mhz REFCLK or line rate of 3125Mbps. To disable automatic setting of PLL and rate modes, write 1'b1 to bit 13 of register 0x1E.001D.

#### 4.5 Test Pattern Generator

In 1G-KX mode, this block can be used to generate test patterns allowing the 1G-KX channel to be tested for compliance while in a system environment or for diagnostic purposes. Test patterns generated are high/low/mixed frequency and CRPAT long or short.

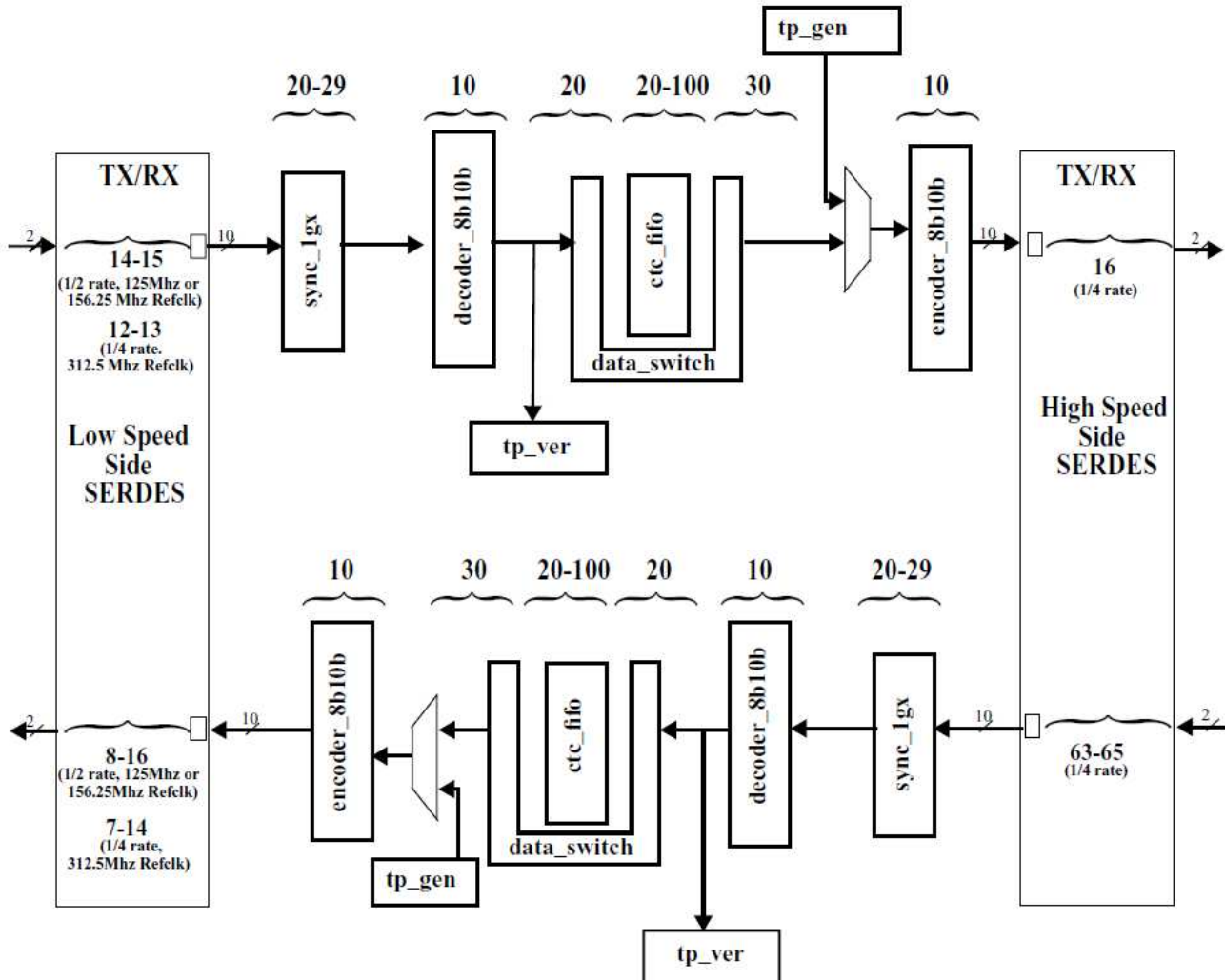
#### 4.6 Test Pattern Verifier

The 1G-KX test pattern verifier performs the verification and error reporting for the CRPAT Long and Short test patterns specified in Annex 36A of the IEEE 802.3-2008 standard. Errors are reported to MDIO registers.

#### 4.7 1GBASE-KX Mode Latency

The latency through the TLK10232 in 1G-KX mode is as shown in [Figure 4-2](#). Note that the latency ranges shown indicate static rather than dynamic latency variance, i.e., the range of possible latencies when the serial link is initially established. During normal operation, the latency through the device is fixed.

**TX Latency = 140 - 230 UI (typical 184), 125/156.25Mhz Refclk  
 = 138 - 228 UI (typical 182), 312.5Mhz Refclk**



**RX Latency = 181 - 280 UI (typical 230), 125/156.25Mhz Refclk  
 = 180 - 278 UI (typical 228), 312.5Mhz Refclk**

Figure 4-2. 1G-KX Mode Latency

## 5 GENERAL PURPOSE (10G) SERDES MODE FUNCTIONAL DESCRIPTION

A block diagram showing the transmit and receive data paths of the TLK10232 operating in General Purpose (10G) SerDes mode is shown in Figure 5-1.

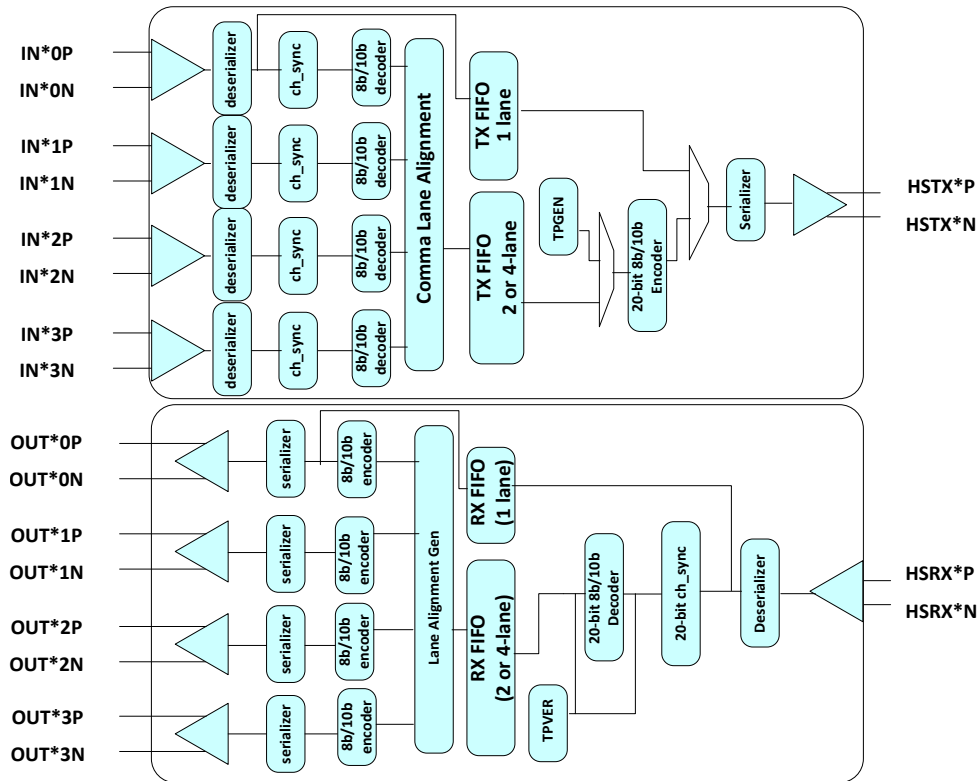


Figure 5-1. Block Diagram Showing General Purpose SerDes Mode

### 5.1 General Purpose SERDES Transmit Data Path

The TLK10232 General Purpose SERDES low speed to high speed (transmit) data path with the device configured to operate in the normal transceiver (mission) mode is shown in the upper half of Figure 5-1. In this mode, 8B/10B encoded serial data (IN\*P/N) in 2 or 4 lanes is received by the low speed side SERDES and deserialized into 10-bit parallel data for each lane. The data in each individual lane is then byte aligned (channel synchronized) and then 8B/10B decoded into 8-bit parallel data for each lane. The lane data is then lane aligned by the Lane Alignment Slave. 32 bits of lane aligned parallel data is input to a transmit FIFO which delivers it to an 8B/10B encoder, 16 data bits at a time. The resulting 20-bit 8B/10B encoded parallel data is sent to the high speed side SERDES for serialization and output through the HSTX\*P/N pins.

### 5.2 General Purpose SERDES Receive Data Path

With the device configured to operate in the normal transceiver (mission) mode, the high speed to low speed (receive) data path is shown in the lower half of Figure 5-1. 8B/10B encoded serial data (HSRX\*P/N) is received by the high speed side SERDES and deserialized into 20-bit parallel data. The data is then byte aligned, 8B/10B decoded into 16-bit parallel data, and then delivered to a receive FIFO. The receive FIFO in turn delivers 32-bit parallel data to the Lane Alignment Master which splits the data into the same number of lanes as configured on the transmit data path. The lane data is then 8B/10B encoded and the resulting 10-bit parallel data for each lane is input to the low speed side SERDES for serialization and output through the OUT\*P/N pins.

### 5.3 Channel Synchronization

As in the 10GBASE-KR mode, the channel synchronization block is used in the 10G General Purpose SERDES mode to align received serial data to a defined byte boundary. The channel synchronization block detects the comma pattern found in the K28.5 character, and follows the synchronization flowchart shown in [Figure 3-2](#).

### 5.4 8B/10B Encoder and Decoder

As in the 10GBASE-KR and 1GBASE-KX modes, the 8B/10B encoder and decoder blocks are used to convert between 10-bit (encoded) and 8-bit (unencoded) data words.

### 5.5 Lane Alignment Scheme for 8b/10b General Purpose Serdes Mode

Lower rate multi-lane serial signals per channel must be byte aligned and lane aligned such that high speed multiplexing (proper reconstruction of higher rate signal) is possible. For that reason, the TLK10232 implements a special lane alignment scheme on the low speed (LS) side for 8b/10b data that does not contain XAUI alignment characters.

During lane alignment, a proprietary pattern (or a custom comma compliant data stream) is sent by the LS transmitter to the LS receiver on each active lane. This pattern allows the LS receiver to both delineate byte boundaries within a lower speed lane and align bytes across the lanes (2 or 4) such that the original higher rate data ordering is restored.

Lane alignment completes successfully when the LS receiver asserts a “Link Status OK” signal monitored by the LS transmitter on the link partner device such as an FPGA. The TLK10232 sends out the “Link Status OK” signals through the LS\_OK\_OUT\_A/B output pins, and monitors the “Link Status OK” signals from the link partner device through the LS\_OK\_IN\_A/B input pins. If the link partner device does not need the TLK10232 Lane Alignment Master (LAM) to send proprietary lane alignment pattern, LS\_OK\_IN\_A/B can be tied high on the application board or set through MDIO register bits.

The lane alignment scheme is activated under any of the following conditions:

- Device/System power up (after configuration/provisioning)
- Loss of channel synchronization assertion on any enabled LS lane
- Loss of signal assertion on any enabled LS lane
- LS SERDES PLL Lock indication deassertion
- After device configuration change
- After software determined LS 8B/10B decoder error rate threshold exceeded
- After device reset is deasserted
- Any time the LS receiver deasserts “Link Status OK”.
- Presence of reoccurring higher level / protocol framing errors

All the above conditions are selectable through MDIO register provisioning.

The block diagram of the lane alignment scheme is shown in [Figure 5-2](#).

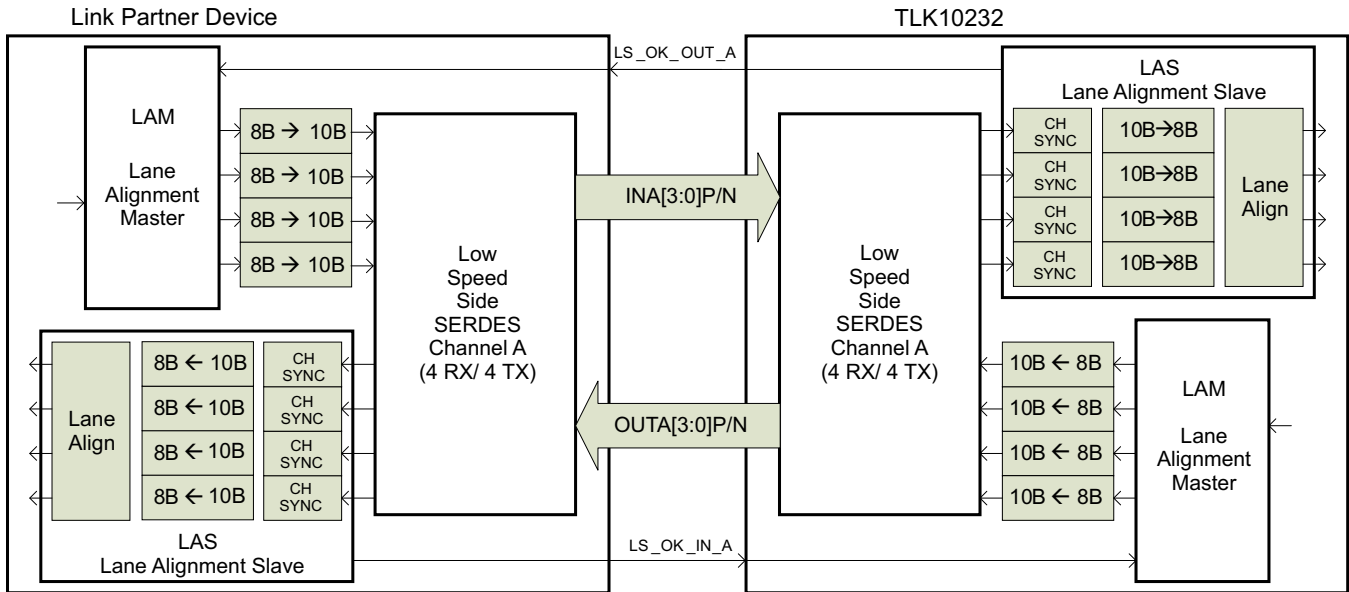


Figure 5-2. Block Diagram of the Lane Alignment Scheme

### 5.6 Lane Alignment Components

- Lane Alignment Master (LAM)
  - Responsible for generating proprietary LS lane alignment initialization pattern
  - Resides in the TLK10232 receive path (one instance per channel)
    - Responsible for bringing up LS receive link for the data sent from the TLK10232 to a link partner device
    - Monitors the LS\_OK\_IN pins for “Link Status OK” signals sent from the Lane Alignment Slave (LAS) of the link partner device
  - Resides in the link partner device (one instance per channel)
    - Responsible for bringing up LS transmit link for the data sent from the link partner device to the TLK10232
    - Monitors the “Link Status OK” signals sent from the LS\_OK\_OUT pins of the Lane Alignment Slave (LAS) of the TLK10232
- Lane Alignment Slave (LAS)
  - Responsible for monitoring the LS lane alignment initialization pattern
  - Performs channel synchronization per lane (2 or 4 lanes) through byte rotation
  - Performs lane alignment and realignment of bytes across lanes
  - Resides in the TLK10232 transmit path (one instance per channel)
    - Generates the “Link Status OK” signal for the LAM on the link partner device
  - Resides in the link partner device (one instance per channel)
    - Generates the “Link Status OK” signal for the LAM on the TLK10232 device.

Reference code from Texas Instruments is available for the LAM and LAS modules for easy integration into FPGAs.

### 5.7 Lane Alignment Operation

During lane alignment, the LAM sends a repeating pattern of 49 characters (control + data) simultaneously across all enabled LS lanes. These simultaneous streams are then encoded by 8B/10B encoders in parallel. The proprietary lane alignment pattern consists of the following characters:

/K28.5/ (CTL=1, Data=0xBC)

Repeat the following sequence of 12 characters four times:

```
/D30.5/ (CTL=0, Data=0xBE)
/D23.6/ (CTL=0, Data=0xD7)
/D3.1/ (CTL=0, Data=0x23)
/D7.2/ (CTL=0, Data=0x47)
/D11.3/ (CTL=0, Data=0x6B)
/D15.4/ (CTL=0, Data=0x8F)
/D19.5/ (CTL=0, Data=0xB3)
/D20.0/ (CTL=0, Data=0x14)
/D30.2/ (CTL=0, Data=0x5E)
/D27.7/ (CTL=0, Data=0xFB)
/D21.1/ (CTL=0, Data=0x35)
/D25.2/ (CTL=0, Data=0x59)
```

The above 49-character sequence is repeated until LS\_OK\_IN is asserted. Once LS\_OK\_IN is asserted, the LAM resumes transmitting traffic received from the high speed side SERDES immediately.

The TLK10232 performs lane alignment across the lanes similar in fashion to the IEEE 802.3-2008 (XAUI) specification. XAUI only operates across 4 lanes while LAS operates with 2 or 4 lanes. The lane alignment state machine is shown in [Figure 5-3](#). The TLK10232 uses the comma (K28.5) character for lane to lane alignment by default, but can be provisioned to use XAUI's /A/ character as well.

Lane alignment checking is not performed by the LAS after lane alignment is achieved. After LAM detects that the LS\_OK\_IN signal is asserted, normal system traffic is carried instead of the proprietary lane alignment pattern.

Channel synchronization is performed during lane alignment and normal system operation.



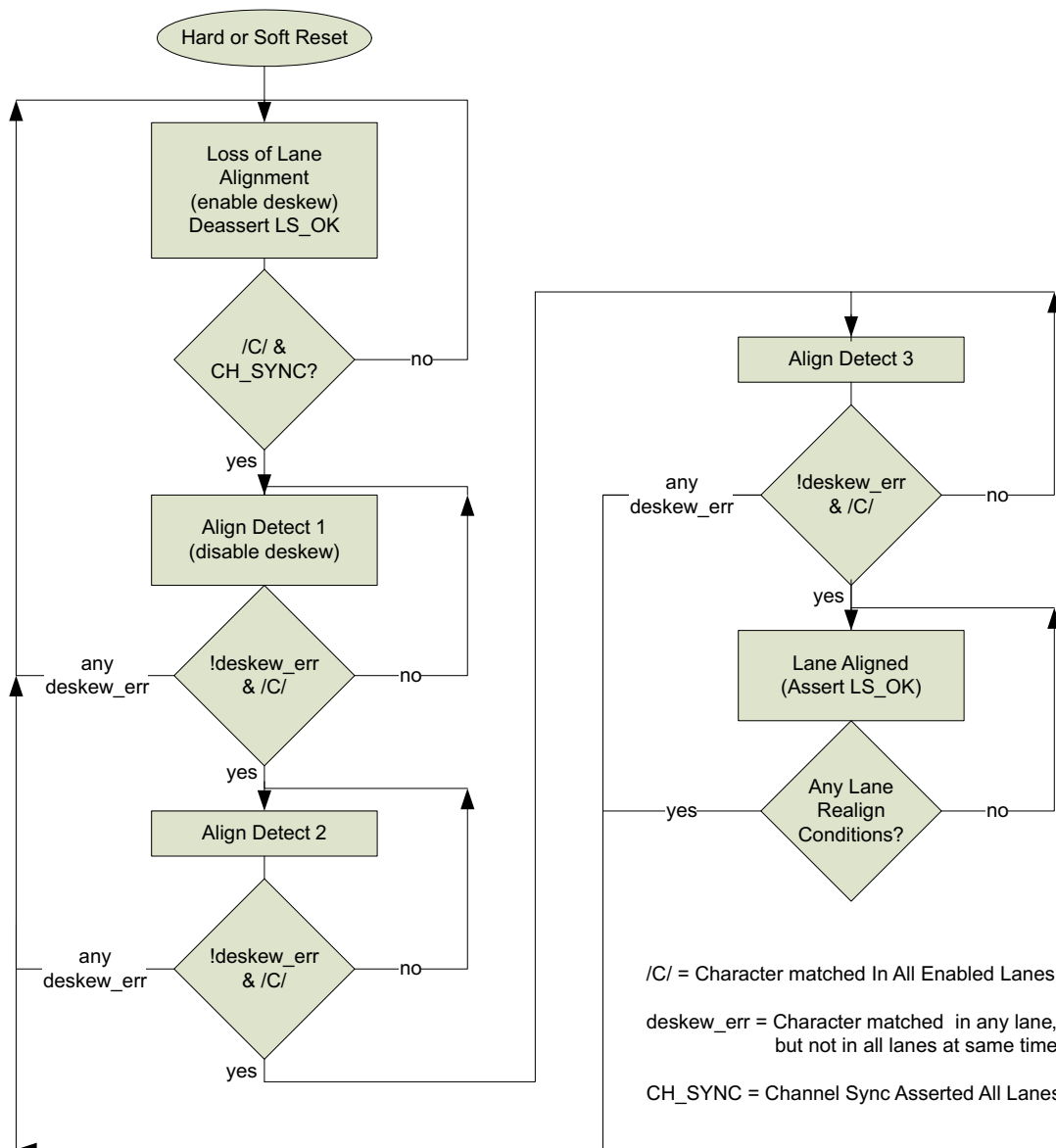


Figure 5-3. Lane Alignment State Machine

### 5.8 Line Rate, SERDES PLL Settings, and Reference Clock Selection for the General Purpose SERDES Mode

When the TLK10232 is set to operate in the General Purpose SERDES mode, the following tables show a summary of line rates and reference clock frequencies used for CPRI/OBSAI for 1:1, 2:1 and 4:1 operation modes.

**Table 5-1. Specific Line Rate Selection for the 1:1 General Purpose Operation Mode**

| LOW SPEED SIDE   |                       |      |                 | HIGH SPEED SIDE  |                       |         |                 |
|------------------|-----------------------|------|-----------------|------------------|-----------------------|---------|-----------------|
| Line Rate (Mbps) | SERDES PLL Multiplier | Rate | REFCLKP/N (MHz) | Line Rate (Mbps) | SERDES PLL Multiplier | Rate    | REFCLKP/N (MHz) |
| 4915.2           | 20                    | Full | 122.88          | 4915.2           | 20                    | Half    | 122.88          |
| 3840             | 12.5                  | Full | 153.6           | 3840             | 12.5                  | Half    | 153.6           |
| 3125             | 10                    | Full | 156.25          | 3125             | 10                    | Half    | 156.25          |
| 3125             | 5                     | Full | 312.5           | 3125             | 5                     | Half    | 312.5           |
| 3072             | 10                    | Full | 153.6           | 3072             | 10                    | Half    | 153.6           |
| 2457.6           | 8/10                  | Full | 153.6/122.88    | 2457.6           | 16/20                 | Quarter | 153.6/122.88    |
| 1920             | 12.5                  | Half | 153.6           | 1920             | 12.5                  | Quarter | 153.6           |
| 1536             | 10                    | Half | 153.6           | 1536             | 10                    | Quarter | 153.6           |
| 1228.8           | 8/10                  | Half | 153.6/122.88    | 1228.8           | 16/20                 | Eighth  | 153.6/122.88    |

**Table 5-2. Specific Line Rate and Reference Clock Selection for the 2:1 General Purpose Operation Mode**

| LOW SPEED SIDE   |                       |         |                 | HIGH SPEED SIDE  |                       |         |                 |
|------------------|-----------------------|---------|-----------------|------------------|-----------------------|---------|-----------------|
| Line Rate (Mbps) | SERDES PLL Multiplier | Rate    | REFCLKP/N (MHz) | Line Rate (Mbps) | SERDES PLL Multiplier | Rate    | REFCLKP/N (MHz) |
| 4915.2           | 20                    | Full    | 122.88          | 9830.4           | 20                    | Full    | 122.88          |
| 3840             | 12.5                  | Full    | 153.6           | 7680             | 12.5                  | Full    | 153.6           |
| 3072             | 10                    | Full    | 153.6           | 6144             | 10                    | Full    | 153.6           |
| 2457.6           | 8/10                  | Full    | 153.6/122.88    | 4915.2           | 16/20                 | Half    | 153.6/122.88    |
| 1920             | 12.5                  | Half    | 153.6           | 3840             | 12.5                  | Half    | 153.6           |
| 1536             | 10                    | Half    | 153.6           | 3072             | 10                    | Half    | 153.6           |
| 1228.8           | 8/10                  | Half    | 153.6/122.88    | 2457.6           | 16/20                 | Quarter | 153.6/122.88    |
| 768              | 10                    | Quarter | 153.6           | 1536             | 10                    | Quarter | 153.6           |
| 614.4            | 8/10                  | Quarter | 153.6/122.88    | 1228.8           | 16/20                 | Eighth  | 153.6/122.88    |

**Table 5-3. Specific Line Rate and Reference Clock Selection for the 4:1 General Purpose Operation Mode**

| LOW SPEED SIDE   |                       |         |                 | HIGH SPEED SIDE  |                       |         |                 |
|------------------|-----------------------|---------|-----------------|------------------|-----------------------|---------|-----------------|
| Line Rate (Mbps) | SERDES PLL Multiplier | Rate    | REFCLKP/N (MHz) | Line Rate (Mbps) | SERDES PLL Multiplier | Rate    | REFCLKP/N (MHz) |
| 2457.6           | 8/10                  | Full    | 153.6/122.88    | 9830.4           | 16/20                 | Full    | 153.6/122.88    |
| 1536             | 10                    | Half    | 153.6           | 6144             | 10                    | Full    | 153.6           |
| 1228.8           | 8/10                  | Half    | 153.6/122.88    | 4915.2           | 16/20                 | Half    | 153.6/122.88    |
| 768              | 10                    | Quarter | 153.6           | 3072             | 10                    | Half    | 153.6           |
| 614.4            | 8/10                  | Quarter | 153.6/122.88    | 2457.6           | 16/20                 | Quarter | 153.6/122.88    |

Table 5-1, Table 5-2, and Table 5-3 indicate two possible reference clock frequencies for CPRI/OBSAI applications: 153.6MHz and 122.88MHz, which can be used based on the application preference. The SERDES PLL Multiplier (MPY) has been given for each reference clock frequency respectively. For each channel, the low speed side and the high speed side SERDES use the same reference clock frequency. Note that Channel A and B are independent and their application rates and references clocks are separate.

For other line rates not shown in Table 5-1, Table 5-2, or Table 5-3, valid reference clock frequencies can be selected with the help of the information provided in Table 5-4 and Table 5-5 for the low speed and high speed side SERDES. The reference clock frequency has to be the same for the two SERDES and must be within the specified valid ranges for different PLL multipliers.

**Table 5-4. Line Rate and Reference Clock Frequency Ranges for the Low Speed Side SERDES (General Purpose Mode)**

| SERDES PLL Multiplier (MPY) | Reference Clock (MHz) |         | Full Rate (Gbps) |      | Half Rate (Gbps) |       | Quarter Rate (Gbps) |        |
|-----------------------------|-----------------------|---------|------------------|------|------------------|-------|---------------------|--------|
|                             | Min                   | Max     | Min              | Max  | Min              | Max   | Min                 | Max    |
| 4                           | 250                   | 425     | 2                | 3.4  | 1                | 1.7   | 0.5                 | 0.85   |
| 5                           | 200                   | 425     | 2                | 4.25 | 1                | 2.125 | 0.5                 | 1.0625 |
| 6                           | 166.667               | 416.667 | 2                | 5    | 1                | 2.5   | 0.5                 | 1.25   |
| 8                           | 125                   | 312.5   | 2                | 5    | 1                | 2.5   | 0.5                 | 1.25   |
| 10                          | 122.88                | 250     | 2.4576           | 5    | 1.2288           | 2.5   | 0.6144              | 1.25   |
| 12                          | 122.88                | 208.333 | 2.94912          | 5    | 1.47456          | 2.5   | 0.73728             | 1.25   |
| 12.5                        | 122.88                | 200     | 3.072            | 5    | 1.536            | 2.5   | 0.768               | 1.25   |
| 15                          | 122.88                | 166.667 | 3.6864           | 5    | 1.8432           | 2.5   | 0.9216              | 1.25   |
| 20                          | 122.88                | 125     | 4.9152           | 5    | 2.4576           | 2.5   | 1.2288              | 1.25   |

RateScale: Full Rate = 0.5, Half Rate = 1, Quarter Rate = 2

**Table 5-5. Line Rate and Reference Clock Frequency Ranges for the High Speed Side SERDES (General Purpose Mode)**

| SERDES PLL Multiplier (MPY) | Reference Clock (MHz) |         | Full Rate (Gbps) |     | Half Rate (Gbps) |      | Quarter Rate (Gbps) |       | Eighth Rate (Gbps) |        |
|-----------------------------|-----------------------|---------|------------------|-----|------------------|------|---------------------|-------|--------------------|--------|
|                             | Min                   | Max     | Min              | Max | Min              | Max  | Min                 | Max   | Min                | Max    |
| 4                           | 375                   | 425     | 6                | 6.8 | 3                | 3.4  | 1.5                 | 1.7   |                    |        |
| 5                           | 300                   | 425     | 6                | 8.5 | 3                | 4.25 | 1.5                 | 2.125 | 1.0                | 1.0625 |
| 6                           | 250                   | 416.667 | 6                | 10  | 3                | 5    | 1.5                 | 2.5   | 1.0                | 1.25   |
| 8                           | 187.5                 | 312.5   | 6                | 10  | 3                | 5    | 1.5                 | 2.5   | 1.0                | 1.25   |
| 10                          | 150                   | 250     | 6                | 10  | 3                | 5    | 1.5                 | 2.5   | 1.0                | 1.25   |
| 12                          | 125                   | 208.333 | 6                | 10  | 3                | 5    | 1.5                 | 2.5   | 1.0                | 1.25   |
| 12.5                        | 153.6                 | 200     | 7.68             | 10  | 3.84             | 5    | 1.92                | 2.5   | 1.0                | 1.25   |
| 15                          | 122.88                | 166.667 | 7.3728           | 10  | 3.6864           | 5    | 1.8432              | 2.5   | 1.0                | 1.25   |
| 16                          | 122.88                | 156.25  | 7.86432          | 10  | 3.932            | 5    | 1.966               | 2.5   | 1.0                | 1.25   |
| 20                          | 122.88                | 125     | 9.8304           | 10  | 4.9152           | 5    | 2.4576              | 2.5   | 1.2288             | 1.25   |

RateScale: Full Rate = 0.25, Half Rate = 0.5, Quarter Rate = 1, Eighth Rate = 2

For example, in the 2:1 operation mode, if the low speed side line rate is 1.987Gbps, the high-speed side line rate will be 3.974Gbps. The following steps can be taken to make a reference clock frequency selection:

1. Determine the appropriate SERDES rate modes that support the required line rates. Table 5-4 shows that the 1.987Gbps line rate on the low speed side is only supported in the half rate mode (RateScale = 1). Table 5-5 shows that the 3.974Gbps line rate on the high speed side is only supported in the half rate mode (RateScale = 1).
2. For each SERDES side, and for all available PLL multipliers (MPY), compute the corresponding reference clock frequencies using the formula:

$$\text{Reference Clock Frequency} = (\text{LineRate} \times \text{RateScale}) / \text{MPY}$$

The computed reference clock frequencies are shown in [Table 5-6](#) along with the valid minimum and maximum frequency values.

3. Mark all the common frequencies that appear on both SERDES sides. Note and discard all those that fall outside the allowed range. In this example, the common frequencies are highlighted in [Table 5-6](#). The highest and lowest computed reference clock frequencies must be discarded because they exceed the recommended range.
4. Select any of the remaining marked common reference clock frequencies. Higher reference clock frequencies are generally preferred. In this example, any of the following reference clock frequencies can be selected: 397.4MHz, 331.167MHz, 248.375MHz, 198.7MHz, 165.583MHz, 158.96MHz, and 132.467MHz

**Table 5-6. Reference Clock Frequency Selection Example**

| LOW SPEED SIDE SERDES |                                 |         |         | HIGH SPEED SIDE SERDES |                                 |        |         |
|-----------------------|---------------------------------|---------|---------|------------------------|---------------------------------|--------|---------|
| SERDES PLL MULTIPLIER | REFERENCE CLOCK FREQUENCY (MHz) |         |         | SERDES PLL MULTIPLIER  | REFERENCE CLOCK FREQUENCY (MHz) |        |         |
|                       | COMPUTED                        | MIN     | MAX     |                        | COMPUTED                        | MIN    | MAX     |
| 4                     | 496.750                         | 250     | 425     | 4                      | 496.750                         | 375    | 425     |
| 5                     | 397.400                         | 200     | 425     | 5                      | 397.400                         | 300    | 425     |
| 6                     | 331.167                         | 166.667 | 416.667 | 6                      | 331.167                         | 250    | 416.667 |
| 8                     | 248.375                         | 125     | 312.5   | 8                      | 248.375                         | 187.5  | 312.5   |
| 10                    | 198.700                         | 122.88  | 250     | 10                     | 198.700                         | 150    | 250     |
| 12                    | 165.583                         | 122.88  | 208.333 | 12                     | 165.583                         | 125    | 208.333 |
| 12.5                  | 158.960                         | 122.88  | 200     | 12.5                   | 158.960                         | 153.6  | 200     |
| 15                    | 132.467                         | 122.88  | 166.667 | 15                     | 132.467                         | 122.88 | 166.667 |
| 20                    | 99.350                          | 122.88  | 125     | 20                     | 99.350                          | 122.88 | 125     |

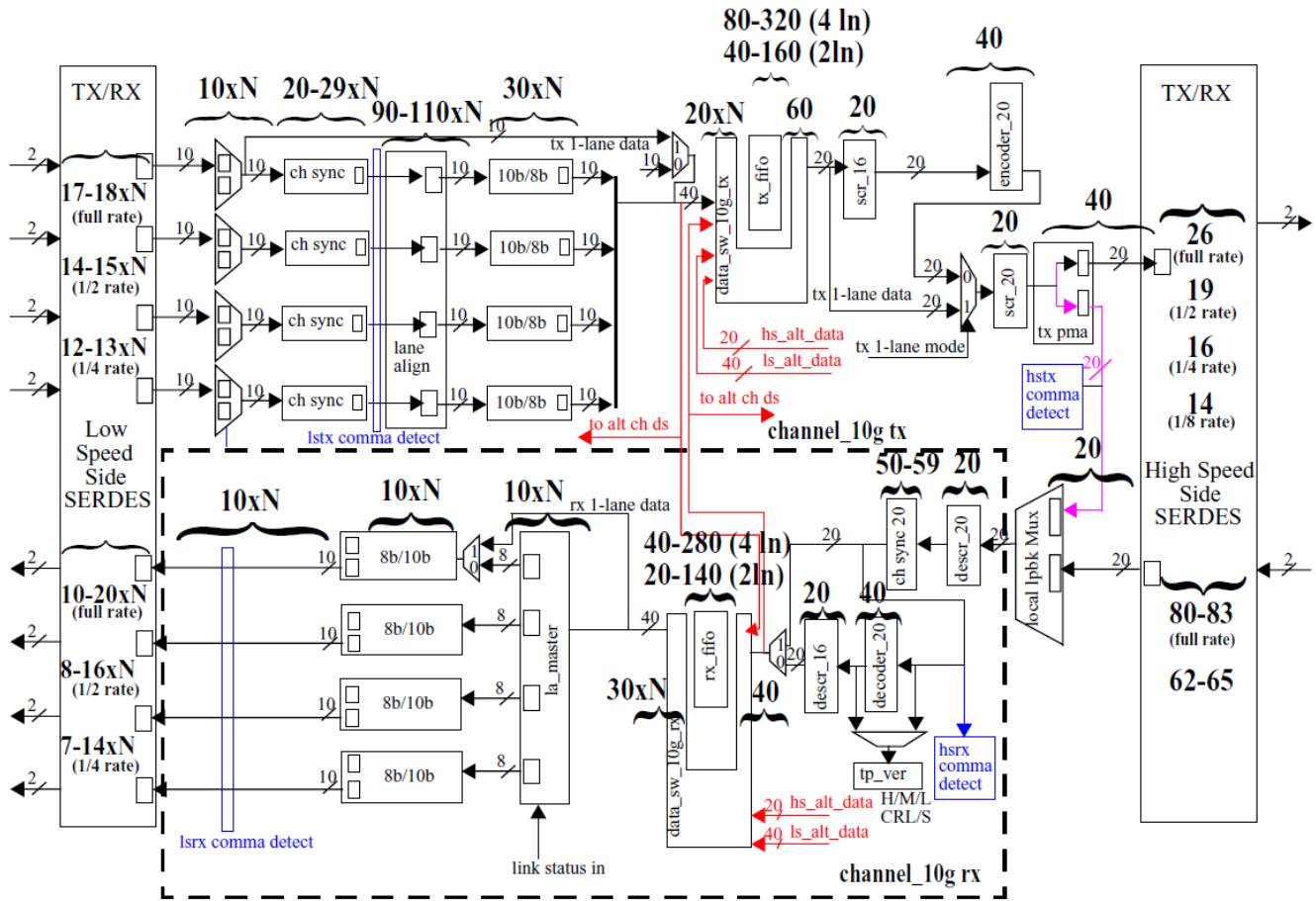
### 5.9 General Purpose SERDES Mode Test Pattern Support

The TLK10232 has the capability to generate and verify various test patterns for self-test and system diagnostic measurements. Most of the same test pattern support is available for 10G General Purpose Mode as for 10G-KR. (See Register 1E.000B for details).

### 5.10 General Purpose SERDES Mode Latency

The latency through the TLK10232 in General Purpose SERDES mode is as shown in [Figure 5-4](#). Note that the latency ranges shown indicate static rather than dynamic latency variance, i.e., the range of possible latencies when the serial link is initially established. During normal operation, the latency through the device is fixed.

**TX Full Rate Latency = 187-217x4 + 286-526 UI (4 ln: 1034-1394, 1059 typical)  
187-217x2 + 246-366 UI (2 ln: 620-800, 645 typical)**

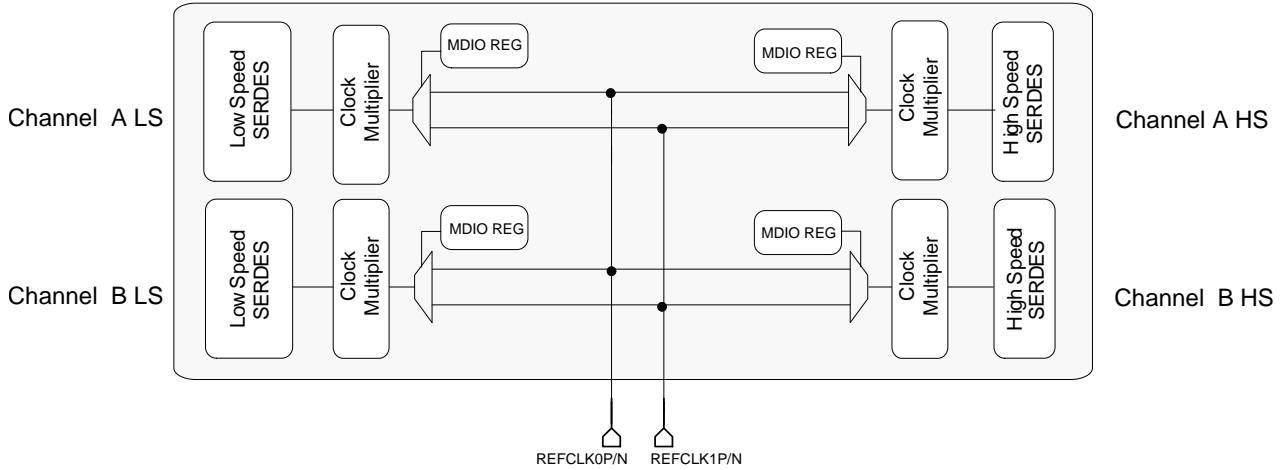


**RX Full Rate Latency = 70-80x4 + 310-562 UI (4 ln: 590-882, 637 typical)  
70-80x2 + 290-422 UI (2 ln: 430-582, 467 typical)**

Figure 5-4. General Purpose SERDES Mode Latency

## 6 CLOCKING ARCHITECTURE (All Modes)

A simplified clocking architecture for the TLK10232 is captured in [Figure 6-1](#). Each channel has an option of operating with a differential reference clock provided either on pins REFCLK0P/N or REFCLK1P/N. The choice is made either through MDIO or through REFCLK\_SEL pins. The reference clock frequencies for each channel can be chosen independently. For each channel, the low speed side SERDES, high speed side SERDES and the associated part of the digital core can operate from the same reference clock.



**Figure 6-1. Reference Clock Architecture**

The TLK10232 has two output clock ports - CLKOUTAP/N and CLKOUTBP/N. Both of these output ports can be configured to output the recovered byte clock of either channel's low speed or high speed sides. Output clocks can also be chosen to be synchronous with the transmit clock rate. Various divider values can be chosen using the MDIO interface. The maximum CLKOUT frequency is 500 MHz.

## 7 ADDITIONAL FEATURES

### 7.1 Integrated Smart Switch

The TLK10232 allows for adjustable routing of data within the device. Each output port may be configured to output data corresponding to any input port.

Figure 7-1 illustrates the different possible data path routings.

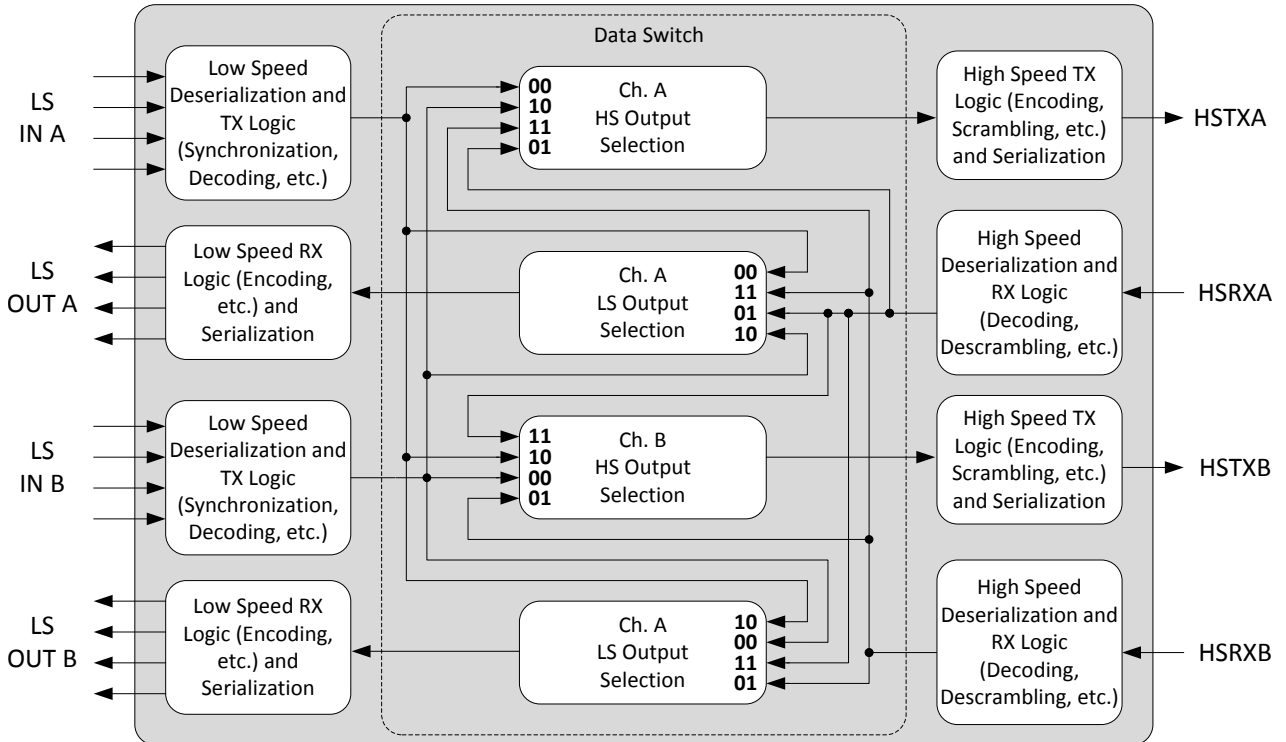


Figure 7-1. Signal Routings for Integrated Smart Switch

### 7.2 Intelligent Switching Modes

The TLK10232 supports various switching modes that allow for the user to choose when changes in data routing take effect. There are three options:

1. Wait for the end of the current packet, insert IDLEs, then switch to the new channel at the start of its next packet. This option allows the current packet to complete so that data is not lost.
2. Drop current packet and insert a programmable character (such as Local Fault), then switch to the new channel at the start of its next packet. This can provide a more immediate switch-over at the expense of the current packet's data.
3. Immediately switch lanes without packet monitoring.

For more information on selecting different intelligent switching modes, see MDIO register bits 0x1E.0017 through 0x1E.001B.

### 7.3 Serial Loopback Modes

The TLK10232 supports internal loopback of the serial output signals for self-test and system diagnostic purposes. Loopback mode can be enabled independently for each SERDES via MDIO register bits. When loopback mode is enabled for a particular SERDES, the serial output data will be internally routed to the SERDES's serial input port. The output data will remain available for monitoring on the output pins.

### 7.4 Latency Measurement Function (General Purpose SerDes Mode)

The TLK10232 includes a latency measurement function to support CPRI and OBSAI type applications. There are two start and two stop locations for the latency counter as shown in Figure 7-2 for Channel A. The start and stop locations are selectable through MDIO register bits. The elapsed time from a comma detected at an assigned counter start location of a particular channel to a comma detected at an assigned counter stop location of the same channel is measured and reported through the MDIO interface. The function operates on one channel at a time. The following three control characters (containing commas) are monitored:

1. K28.1 (control = 1, data = 0x3C)
2. K28.5 (control = 1, data = 0xBC)
3. K28.7 (control = 1, data = 0xFC).

The first comma found at the assigned counter start location will start up the latency counter. The first comma detected at the assigned counter stop location will stop the latency counter. The 20-bit latency counter result of this measurement is readable through the MDIO interface. The accuracy of the measurement is a function of the serial bit rate at which the channel being measured is operating. The register will return a value of 0xFFFFF if the duration between transmit and receive comma detection exceeds the depth of the counter. Only one measurement value is stored internally until the 20-bit results counter is read. The counter will return zero in cases where a transmit comma was never detected (indicating the results counter never began counting). In addition, the stopwatch counter can be configured to be started or stopped manually based on the state of the PRTAD0 pin (see MDIO register map for details).

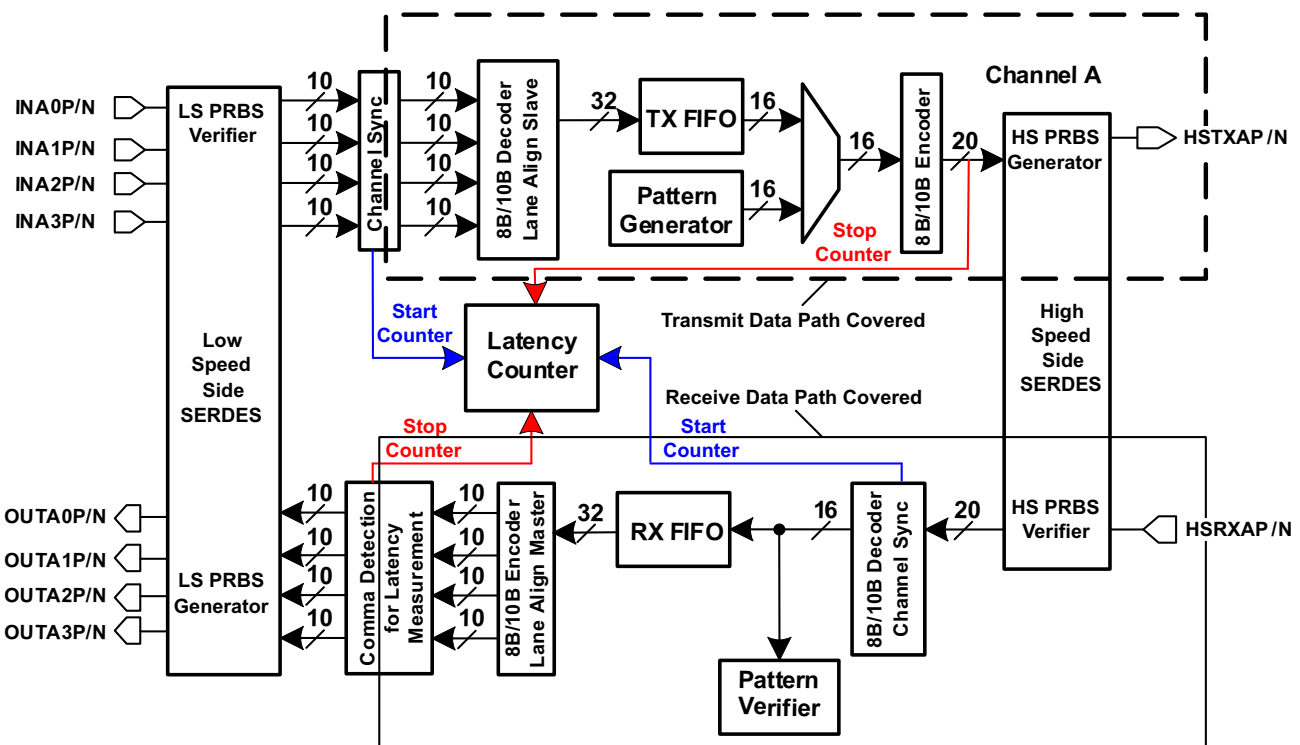


Figure 7-2. Location of TX and RX Comma Character Detection (Only Channel A Shown)

In high speed side SERDES full rate mode, the latency measurement function runs off of an internal clock which is equal to the frequency of the transmit serial bit rate divided by 8. In half rate mode, the latency measurement function runs off of an internal clock which is equal to the serial bit rate divided by 4. In quarter rate mode, the latency measurement function runs off of an internal clock which is equal to the serial bit rate divided by 2. In eighth rate mode, the latency measurement function runs off of a clock which is equal to the serial bit rate.



The latency measurement does not include the low speed side transmit SERDES contribution as well as part of the channel synchronization block. The latency introduced by those two is up to  $(18 + 10) \times N$  high speed side unit intervals (UIs), where  $N = 2, 4$  is the multiplex factor. The latency measurement also doesn't account for the low speed side receive SERDES contribution which is estimated to be up to  $20 \times N$  high speed side UIs.

The latency measurement accuracy in all cases is equal to plus or minus one latency measurement clock period. The measurement clock can be divided down if a longer duration measurement is required, in which case the accuracy of the measurement is accordingly reduced. The high speed latency measurement clock is divided by either 1, 2, 4, or 8 via register settings. The measurement clock used is always selected by the channel under test. The high speed latency measurement clock may only be used when operating at one of the serial rates specified in the CPRI/OBSAI specifications. It is also possible to run the latency measurement function off of the recovered byte clock for the channel under test (giving a latency measurement clock frequency equal to the serial bit rate divided by 20).

The accuracy for the standard based CPRI/OBSAI application rates is shown in [Table 7-1](#), and assumes the latency measurement clock is not divided down per user selection (division is required to measure a duration greater than 682us). For each division of 2 in the measurement clock, the accuracy is also reduced by a factor of two.

**Table 7-1. CPRI/OBSAI Latency Measurement Function Accuracy (Undivided Measurement Clock)**

| LINE RATE (Gbps) | RATE    | LATENCY CLOCK FREQUENCY (GHz) | ACCURACY ( $\pm$ ns) |
|------------------|---------|-------------------------------|----------------------|
| 1.2288           | Eighth  | 1.2288                        | 0.8138               |
| 1.536            | Quarter | 0.768                         | 1.302                |
| 2.4576           | Quarter | 1.2288                        | 0.8138               |
| 3.072            | Half    | 0.768                         | 1.302                |
| 3.84             | Half    | 0.96                          | 1.0417               |
| 4.9152           | Half    | 1.2288                        | 0.8138               |
| 6.144            | Full    | 0.768                         | 1.302                |
| 7.68             | Full    | 0.96                          | 1.0417               |
| 9.8304           | Full    | 1.2288                        | 0.8138               |

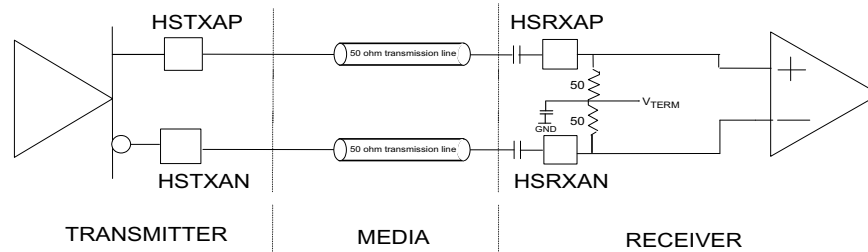
## 7.5 Power Down Mode

The TLK10232 can be put in power down either through device input pins or through MDIO control register 1E.0001.

- PDTRXA\_N: Active low, powers down channel A.
- PDTRXB\_N: Active low, powers down channel B.

### 7.5.1 High Speed CML Output

The high speed data output driver is implemented using Current Mode Logic (CML) with integrated pull up resistors. The transmit outputs must be AC coupled.



NOTE: Channel A HS Side is Shown

**Figure 7-3. Example of High Speed I/O AC Coupled Mode**

Current Mode Logic (CML) drivers often require external components. The disadvantage of the external component is a limited edge rate due to package and line parasitic. The CML driver on TLK10232 has on-chip 50Ω termination resistors terminated to VDDT, providing optimum performance for increased speed requirements. The transmitter output driver is highly configurable allowing output amplitude and de-emphasis to be tuned to a channel's individual requirements. Software programmability allows for very flexible output amplitude control. Only AC coupled output mode is supported.

When transmitting data across long lengths of PCB trace or cable, the high frequency content of the signal is attenuated due to dielectric losses and the skin effect of the media. This causes a “smearing” of the data eye when viewed on an oscilloscope. The net result is reduced timing margins for the receiver and clock recovery circuits. In order to provide equalization for the high frequency loss, 4-tap finite impulse response (FIR) transmit de-emphasis is implemented. A highly configurable output driver maximizes flexibility in the end system by allowing de-emphasis and output amplitude to be tuned to a channel's individual requirements. Output swing control is via MDIO.

### 7.5.2 High Speed Receiver

The high speed receiver is differential CML with internal termination resistors. The receiver requires AC coupling. The termination impedances of the receivers are configured as 100 Ω with the center tap weakly tied to 0.7×VDDT, and a capacitor is used to create an AC ground (see [Figure 7-3](#)).

TLK10232 serial receivers incorporate adaptive equalizers. This circuit compensates for channel insertion loss by amplifying the high frequency components of the signal, reducing inter-symbol interference. Equalization can be enabled or disabled per register settings. Both feed-forward equalization (FFE) and decision feedback equalization (DFE) are used to minimize the pre-cursor and post-cursor components (respectively) of intersymbol interference.

### 7.5.3 Loss of Signal Output Generation (LOS)

Loss of input signal detection is based on the voltage level of each serial input signal IN\*P/N, HSRX\*P/N. When LOS indication is enabled and a channel's differential serial receive input level is < 75mVpp, that channel's respective LOS indicator (LOSA or LOSB) will be asserted (high true). If the input signal is >150mVpp, the LOS indicator will be deasserted (low false). Outside of these ranges, the LOS indication is undefined. The LOS indicators can also directly be read through the MDIO interface.

The following additional critical status conditions can be combined with the loss of signal condition enabling additional real-time status signal visibility on the LOS\* outputs per channel:

1. Loss of Channel Synchronization Status – Logically OR'd with LOS condition(s) when enabled. Loss of channel synchronization can be optionally logically OR'd (disabled by default) with the internally generated LOS condition (per channel).
2. Loss of PLL Lock Status on LS and HS sides – Logically OR'd with LOS condition(s) when enabled. The internal PLL loss of lock status bit is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
3. Receive 8B/10B Decode Error (Invalid Code Word or Running Disparity Error) – Logically OR'd with LOS condition(s) when enabled. The occurrence of an 8B/10B decode error (invalid code word or disparity error) is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
4. AGCLOCK (Active Gain Control Currently Locked) – Inverted and Logically OR'd with LOS condition(s) when enabled. HS RX SERDES adaptive gain control unlocked indication is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
5. AZDONE (Auto Zero Calibration Done) - Inverted and Logically OR'd with LOS conditions(s) when enabled. HS RX SERDES auto-zero not done indication is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).

Refer to [Figure 7-4](#), which shows the detailed implementation of the LOSA signal along with the associated MDIO control registers for the General Purpose SERDES mode. More details about LOS settings including configurations related to the 10GBASE-KR mode can be found in the Programmers Reference section.

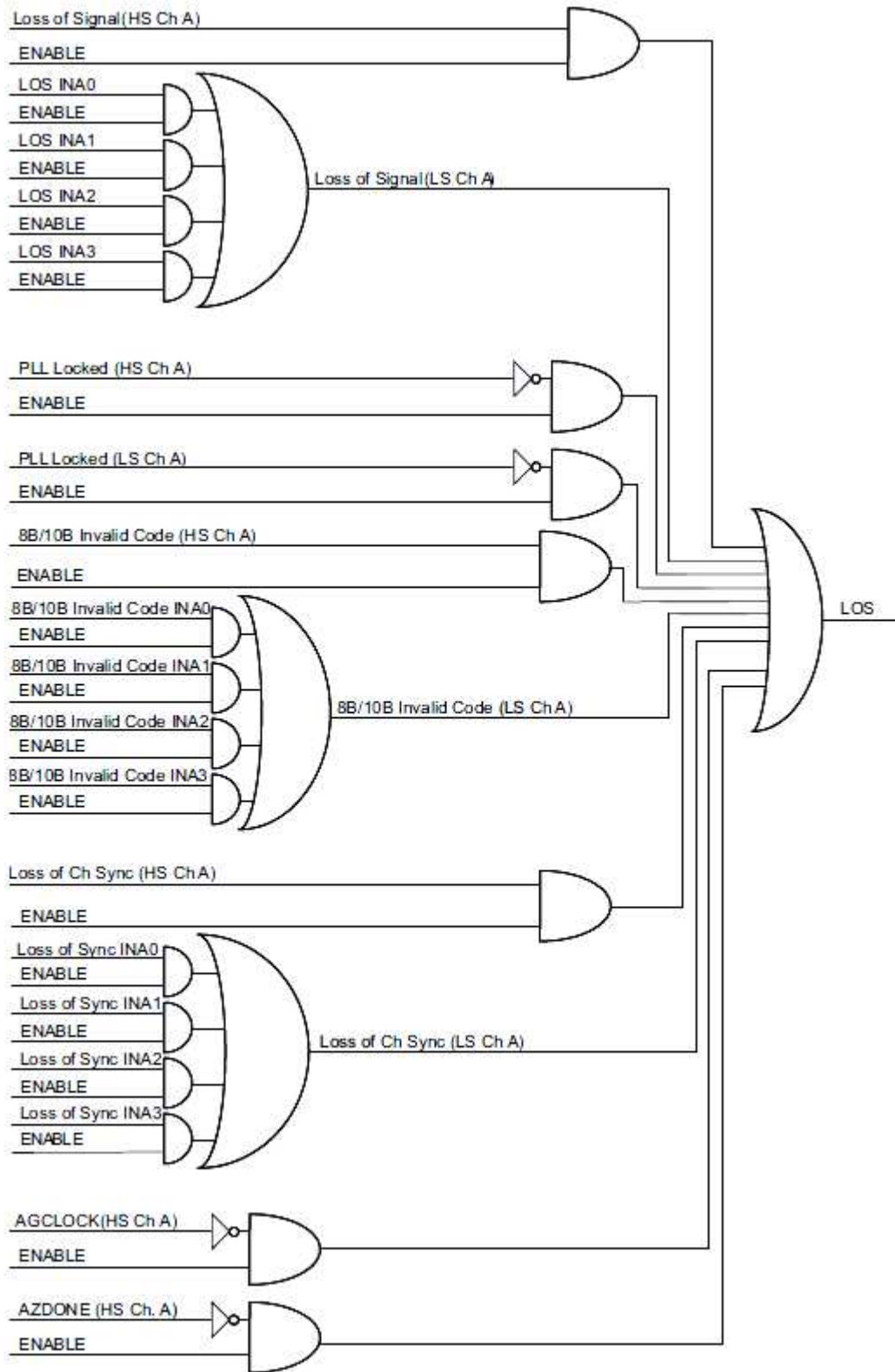


Figure 7-4. LOSA – Logic Circuit Implementation

## 7.6 MDIO Management Interface

The TLK10232 supports the Management Data Input/Output (MDIO) Interface as defined in Clauses 22 and 45 of the IEEE 802.3-2008 Ethernet specification. The MDIO allows register-based management and control of the serial links.

The MDIO Management Interface consists of a bi-directional data path (MDIO) and a clock reference (MDC). The device identification and port address are determined by control pins (see Table 2-1). Also, whether the device responds as a Clause 22 or Clause 45 device is also determined by control pin ST (see Table 2-1).

In Clause 45 (ST = 0) and Clause 22 (ST = 1), the top 4 control pins PRTAD[4:1] determine the device port address. In this mode, TLK10232 will respond if the PHY address field on the MDIO protocol (PA[4:1]) matches PRTAD[4:1] pin value. In both these modes the 2 individual channels in TLK10232 are classified as 2 different ports. So for any PRTAD[4:1] value there will be 2 ports per TLK10232. The LSB of PHY address field (PA[0]) will determine which channel/port within TLK10232 to respond.

If PA[0] = 1'b0, TLK10232 Channel A will respond.

If PA[0] = 1'b1, TLK10232 Channel B will respond.

In Clause 22 (ST = 1) mode, only 32 (5'b00000 to 5'b11111) register addresses can be accessed through standard protocol. Due to this limitation, an indirect addressing method (More description in Clause 22 Indirect Addressing section) is implemented to provide access to all device specific control/status registers that cannot be accessed through the standard Clause 22 register address space.

Write transactions which address an invalid register or device or a read only register will be ignored. Read transactions which address an invalid register or device will return a 0.

## 7.7 MDIO Protocol Timing

Timing for a Clause 45 address transaction is shown in Figure 7-5. The Clause 45 timing required to write to the internal registers is shown in Figure 7-6. The Clause 45 timing required to read from the internal registers is shown in Figure 7-7. The Clause 45 timing required to read from the internal registers and then increment the active address for the next transaction is shown in Figure 7-8. The Clause 22 timing required to read from the internal registers is shown in Figure 7-9. The Clause 22 timing required to write to the internal registers is shown in Figure 7-10.

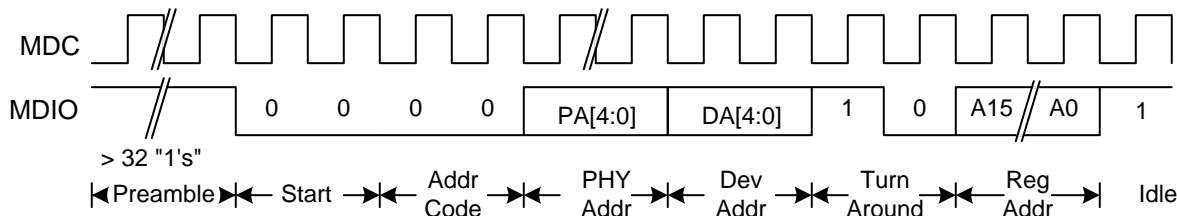


Figure 7-5. CL45 - Management Interface Extended Space Address Timing

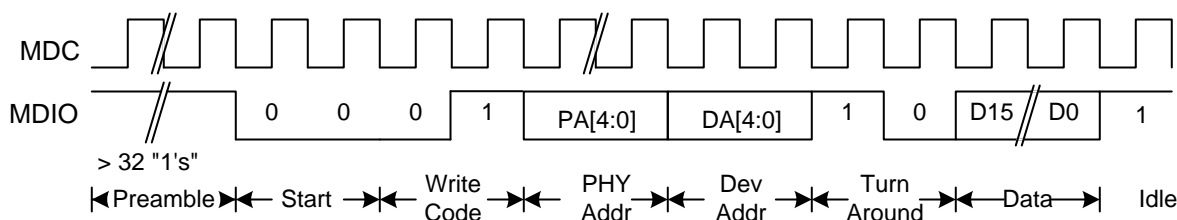


Figure 7-6. CL45 - Management Interface Extended Space Write Timing

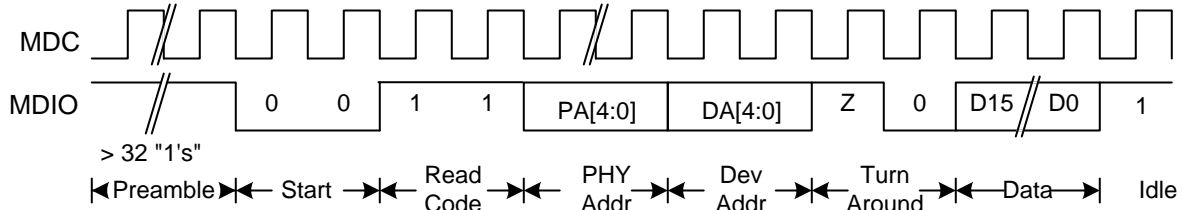


Figure 7-7. CL45 - Management Interface Extended Space Read Timing

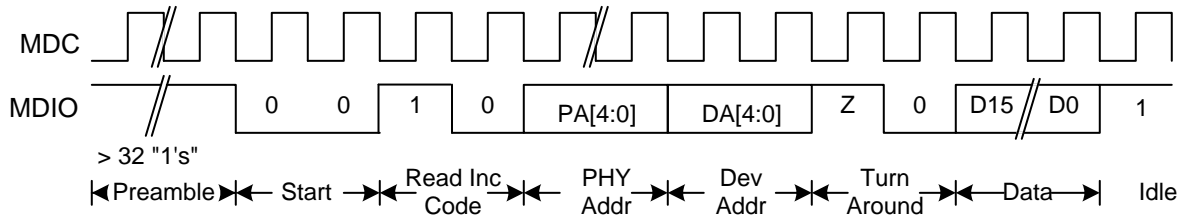


Figure 7-8. CL45 - Management Interface Extended Space Read And Increment Timing

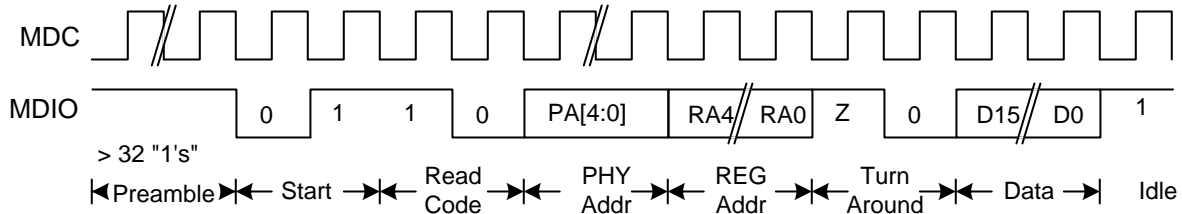


Figure 7-9. CL22 - Management Interface Read Timing

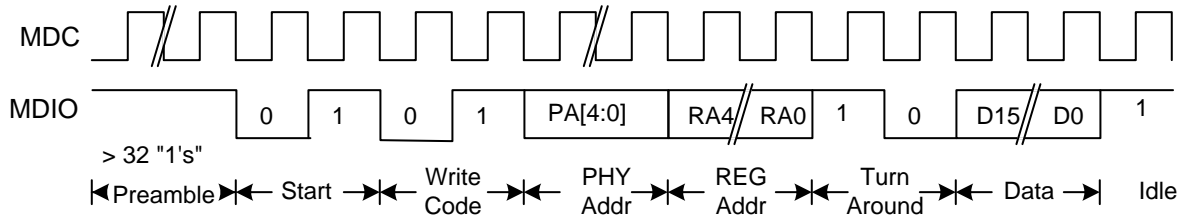
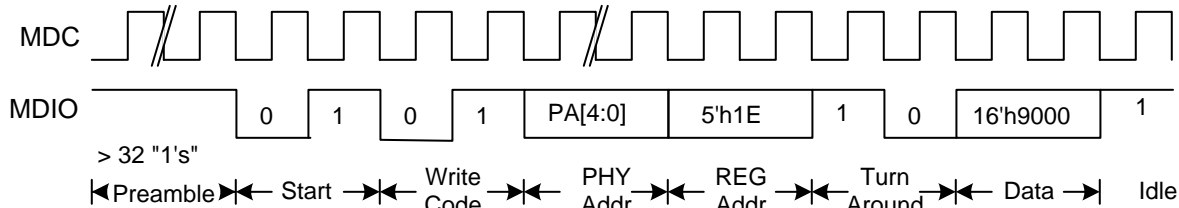


Figure 7-10. CL22 - Management Interface Write Timing

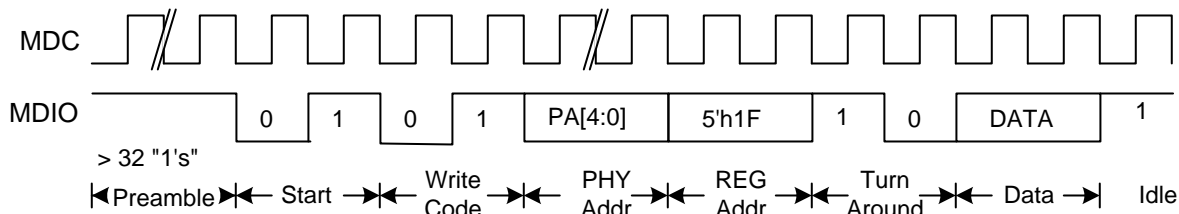
The IEEE 802.3 Clause 22/45 specification defines many of the registers, and additional registers have been implemented for expanded functionality.

### 7.8 Clause 22 Indirect Addressing

Due to Clause 22 register space limitations, an indirect addressing method is implemented so that the extended register space can be accessed through Clause 22. All the device specific control and status registers that cannot be accessed through Clause 22 direct addressing can be accessed through this indirect addressing method. To access this register space, an address control register (Reg 30, 5'h1E) should be written with the register address followed by a read/write transaction to address content register (Reg 31, 5'h1F) to access the contents of the address specified in address control register. Following timing diagrams illustrate an example write transaction to Register 16'h9000 using indirect addressing in Clause 22.

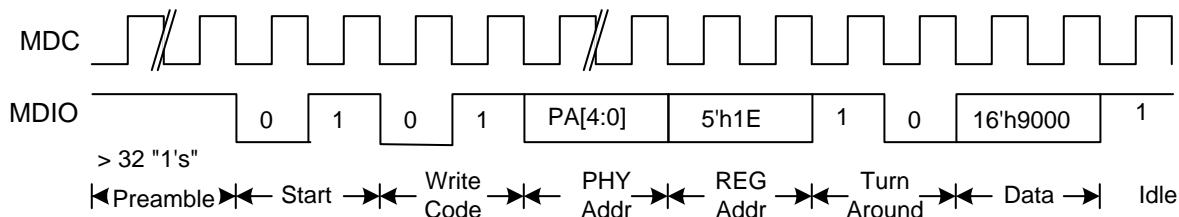


**Figure 7-11. CL22 – Indirect Address Method – Address Write**

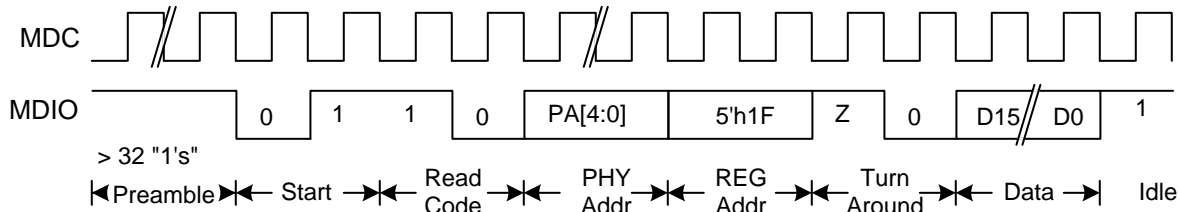


**Figure 7-12. CL22 - Indirect Address Method – Data Write**

Following timing diagrams illustrate an example read transaction to read contents of Register 16'h9000 using indirect addressing in Clause 22.



**Figure 7-13. CL22 - Indirect Address Method – Address Write**



**Figure 7-14. CL22 - Indirect Address Method – Data Read**

## 7.9 Programmers Reference

Channel identification is based on PHY (Port) address field. Channel A can be accessed by setting LSB of PHY address to 0. Channel B can be accessed by setting LSB of PHY address to 1.

## 7.10 Register Bit Definitions

### **RW: Read-Write**

User can write 0 or 1 to this register bit. Reading this register bit returns the same value that has been written.

### **RW/SC: Read-Write Self-Clearing**

User can write 0 or 1 to this register bit. Writing a "1" to this register creates a high pulse. Reading this register bit always returns 0.

### **RO: Read-Only**

This register can only be read. Writing to this register bit has no effect. Reading from this register bit returns its current value.

### **RO/LH: Read-Only Latched High**

This register can only be read. Writing to this register bit has no effect. Reading a "1" from this register bit indicates that either the condition is occurring or it has occurred since the last time it was read. Reading a "0" from this register bit indicates that the condition is not occurring presently, and it has not occurred since the last time the register was read. A latched high register, when read high, should be read again to distinguish if a condition occurred previously or is still occurring. If it occurred previously, the second read will read low. If it is still occurring, the second read will read high. Reading this register bit automatically resets its value to 0.

### **RO/LL: Read-Only Latched Low**

This register can only be read. Writing to this register bit has no effect. Reading a "0" from this register bit indicates that either the condition is occurring or it has occurred since the last time it was read. Reading a "1" from this register bit indicates that the condition is not occurring presently, and it has not occurred since the last time the register was read. A latched low register, when read low, should be read again to distinguish if a condition occurred previously or is still occurring. If it occurred previously, the second read will read high. If it is still occurring, the second read will read low. Reading this register bit automatically sets its value to 1.

### **COR: Clear-On-Read**

This register can only be read. Writing to this register bit has no effect. Reading from this register bit returns its current value, then resets its value to 0. Counter value freezes at Max.

Following code letters in Name field of each control/status register bit(s) indicate the mode that they are applicable/valid.

R = Indicates control/status bit(s) valid in 10GKR mode

X = Indicates control/status bit(s) valid in 1GKX mode

G = Indicates control/status bit(s) valid in 10G general purpose serdes mode



## 8 DEVICE REGISTERS

### 8.1 Vendor Specific Device Registers

Below registers can be accessed directly through Clause 22 and Clause 45. In Clause 45 mode, these registers can be accessed by setting device address field to 0x1E (DA[4:0] = 5'b11110). In Clause 22 mode, these registers can be accessed by setting 5 bit register address field to same value as 5 LSB bits of Register Address field specified for each register. For example, 16 bit register address 0x001C in clause 45 mode can be accessed by setting register address field to 5'h1C in clause 22 mode.

**Table 8-1. GLOBAL\_CONTROL\_1<sup>(1)</sup>**

| Device Address: 0x1E |                              | Register Address: 0x0000  | Default: 0x0610 |                         |
|----------------------|------------------------------|---|-----------------|-------------------------|
| Bit(s)               | Name                         | Description   |                 | Access                  |
| 15                   | GLOBAL_RESET (RXG)           | Global reset.<br>0 = Normal operation (Default 1'b0)<br>1 = Resets TX and RX data path including MDIO registers. Equivalent to asserting RESET_N.   |                 | RW<br>SC <sup>(2)</sup> |
| 14:12                | PRTAD0_PIN_EN_SEL[2:0] (RXG) | PRTAD0 pin selection control. Valid only when 1E.0000 bit 5 is 1. PRTAD0 is used for the assignment specified below.<br>000 = Channel A stopwatch (Default 3'b000)<br>001 = Channel B stopwatch<br>010 = Channel A Tx data switch<br>011 = Channel A Rx data switch<br>100 = Channel B Tx data switch<br>101 = Channel B Rx data switch<br>11x = Reserved   |                 | RW                      |
| 11                   | GLOBAL_WRITE (RXG)           | Global write enable.<br>0 = Control settings are specific to channel addressed (Default 1'b0)<br>1 = Control settings in channel specific registers are applied to all 4 channels regardless of channel addressed   |                 | RW                      |
| 10:7                 | RESERVED                     | For TI use only (Default 5'b1100)   |                 | RW                      |
| 6                    | RESERVED                     | For TI use only. Always reads 0.  |                 | RW                      |
| 5                    | PRTAD0_PIN_EN (RXG)          | PRTAD0 pin enable control.<br>0 = Input pin (PRTAD0) is used for the assignment specified in 1E.0000 bits 14:12 (Default 1'b0)<br>1 = Input pin (PRTAD0) is not used for the assignment specified in 1E.0000 bits 14:12   |                 | RW                      |
| 4:0                  | PRBS_PASS_OVERLAY[4:0] (RXG) | PRBS_PASS pin status selection. Applicable only when PRBS test pattern verification is enabled on HS side or LS side. PRBS_PASS pin reflects PRBS verification status on selected Channel HS/LS side. PRBS_PASS pin reflects PRBS verification status on selected Channel HS/LS side. LS Serdes lanes 1/2/3 are not applicable in 1GKX modes.<br>1xx00 = PRBS_PASS reflects combined status of Channel A/B HS serdes PRBS verification. If PRBS verification fails on any channel HS serdes, PRBS_PASS will be asserted low. (Default 5'b10000)<br>00000 = Status from Channel A HS Serdes side<br>00001 = Reserved<br>0001x = Reserved<br>00100 = Status from Channel A LS Serdes side Lane 0<br>00101 = Status from Channel A LS Serdes side Lane 1<br>00110 = Status from Channel A LS Serdes side Lane 2<br>00111 = Status from Channel A LS Serdes side Lane 3<br>01000 = Status from Channel B HS Serdes side<br>01001 = Reserved<br>0101x = Reserved<br>01100 = Status from Channel B LS Serdes side Lane 0<br>01101 = Status from Channel B LS Serdes side Lane 1<br>01110 = Status from Channel B LS Serdes side Lane 2<br>01111 = Status from Channel B LS Serdes side Lane 3 |                 | RW                      |

(1) This global register is channel independent.

(2) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

**Table 8-2. CHANNEL\_CONTROL\_1**

| Device Address: 0x1E |                          | Register Address:0x0001  | Default: 0x0B00 |        |
|----------------------|--------------------------|--|-----------------|--------|
| Bit(s)               | Name                     | Description  |                 | Access |
| 15                   | POWERDOWN (RXG)          | Setting this bit high powers down entire data path with exception that MDIO interface stays active.<br>0 = Normal operation (Default 1'b0)<br>1 = Power Down mode is enabled.  |                 | RW     |
| 14                   | LT_TRAINING_CONTROL (XG) | Link training control. Valid in 10G and 1GKX modes only.<br>0 = Link training disabled(Default 1'b0)<br>1 = Link training enable control dependent on LT_TRAINING_ENABLE (1E.0036 bit 1).  |                 | RW     |
| 13                   | 10G_RX_MODE_SEL (G)      | RX mode selection. Valid in 10G only.<br>0 = RX mode dependent upon RX_DEMUX_SEL(Default 1'b0)<br>1 = Enables 1 to 1 mode on receive channel.  |                 | RW     |
| 12                   | 10G_TX_MODE_SEL (G)      | TX mode selection Valid in 10G only.<br>0 = TX mode dependent upon TX_MUX_SEL (Default 1'b0)<br>1 = Enables 1 to 1 mode on transmit channel.   |                 | RW     |
| 11                   | SW_PCS_SEL (RX)          | Applicable in Clause 45 mode only. Valid only when MODE_SEL pin is 0, AN_ENABLE (07.0000 bit 12) is 0 and SW_DEV_MODE_SEL (1E.0001 bit 10) is 0.<br>1 = Set device to 10G-KR mode(Default 1'b1)<br>0 = Set device to 1G-KX mode  |                 | RW     |
| 10                   | SW_DEV_MODE_SEL (RXG)    | Valid only when MODE_SEL pin is 0<br>1 = Device set to 10G mode<br>0 = In clause 45 mode, device mode is set using Auto negotiation. In clause 22 mode, device set to 1G-KX mode(Default 1'b0)   |                 | RW     |
| 9                    | 10G_RX_DEMUX_SEL (G)     | RX De-Mux selection control for lane de-serialization on receive channel. Valid in 10G and when 10G_RX_MODE_SEL (1E.0001 bit 13) is LOW<br>0 = 1 to 2<br>1 = 1 to 4 (Default 1'b1)   |                 | RW     |
| 8                    | 10G_TX_MUX_SEL (G)       | TX Mux selection control for lane serialization on transmit channel. Valid in 10G and when 10G_TX_MODE_SEL (1E.0001 bit 12) is LOW<br>0 = 2 to 1<br>1 = 4 to 1 (Default 1'b1)  |                 | RW     |
| 7:2                  | RESERVED                 | For TI use only  |                 | RO     |
| 1                    | REFCLK_SW_SEL (RXG)      | Channel HS Reference clock selection.<br>0 = Selects REFCLK_0_P/N as clock reference to Channel x HS side serdes macro(Default 1'b0)<br>1 = Selects REFCLK_1_P/N as clock reference to Channel x HS side serdes macro  |                 | RW     |
| 0                    | LS_REFCLK_SEL (RXG)      | Channel LS Reference clock selection.<br>0 = LS side serdes macro reference clock is same as HS side serdes reference clock (E.g. If REFCLK_0_P/N is selected as HS side serdes macro reference clock, REFCLK_0_P/N is selected as LS side serdes macro reference clock and vice versa) (Default 1'b0)<br>1 = Alternate reference clock is selected as clock reference to Channel x LS side serdes macro (E.g. If REFCLK_0_P/N is selected as HS side serdes macro reference clock, REFCLK_1_P/N is selected as LS side serdes macro reference clock and vice versa) |                 | RW     |

**Table 8-3. HS\_SERDES\_CONTROL\_1**

| Device Address: 0x1E |                               | Register Address:0x0002   | Default: 0x831D |        |
|----------------------|-------------------------------|---|-----------------|--------|
| Bit(s)               | Name                          | Description   |                 | Access |
| 15:10                | RESERVED                      | For TI use only (Default 6'b100000)   |                 | RW     |
| 9:8                  | HS_LOOP_BANDWIDT H[1:0] (RXG) | HS Serdes PLL Loop Bandwidth settings<br>00 = Medium Bandwidth<br>01 = Low Bandwidth<br>10 = High Bandwidth<br>11 = Ultra High Bandwidth. (Default 2'b11) |                 | RW     |
| 7                    | RESERVED                      | For TI use only (Default 1'b0)  |                 | RW     |

**Table 8-3. HS\_SERDES\_CONTROL\_1 (continued)**

| Device Address: 0x1E |                        | Register Address: 0x0002   | Default: 0x831D |        |
|----------------------|------------------------|--|-----------------|--------|
| Bit(s)               | Name                   | Description  |                 | Access |
| 6                    | HS_VRANGE (RXG)        | HS Serdes PLL VCO range selection.<br>0 = VCO runs at higher end of frequency range (Default 1'b0)<br>1 = VCO runs at lower end of frequency range<br>This bit needs to be set HIGH if VCO frequency (REFCLK *HS_PLL_MULT) is below 2.5 Ghz. |                 | RW     |
| 5                    | RESERVED               | For TI use only (Default 1'b0)   |                 | RW     |
| 4                    | HS_ENPLL (RXG)         | HS Serdes PLL enable control. HS Serdes PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1E.0001 bit 15 is set HIGH.<br>0 = Disables PLL in HS serdes<br>1 = Enables PLL in HS serdes (Default 1'b1)        |                 | RW     |
| 3:0                  | HS_PLL_MULT[3:0] (RXG) | HS Serdes PLL multiplier setting (Default 4'b1101).<br>Refer : <a href="#">Table 8-4</a> HS PLL multiplier control   |                 | RW     |

**Table 8-4. HS PLL Multiplier Control**

| HS_PLL_MULT[3:0] |                       | HS_PLL_MULT[3:0] |                       |
|------------------|-----------------------|------------------|-----------------------|
| Value            | PLL Multiplier factor | Value            | PLL Multiplier factor |
| 0000             | Reserved              | 1000             | 12x                   |
| 0001             | Reserved              | 1001             | 12.5x                 |
| 0010             | 4x                    | 1010             | 15x                   |
| 0011             | 5x                    | 1011             | 16x                   |
| 0100             | 6x                    | 1100             | 16.5x                 |
| 0101             | 8x                    | 1101             | 20x                   |
| 0110             | 8.25x                 | 1110             | 25x                   |
| 0111             | 10x                   | 1111             | Reserved              |

**Table 8-5. HS\_SERDES\_CONTROL\_2**

| Device Address: 0x1E |                        | Register Address: 0x0003   | Default: 0xA848 |        |
|----------------------|------------------------|--|-----------------|--------|
| Bit(s)               | Name                   | Description  |                 | Access |
| 15:12                | HS_SWING[3:0] (RXG)    | Transmitter Output swing control for HS Serdes. (Default 4'b1010)<br>Refer <a href="#">Table 8-6</a> .   |                 | RW     |
| 11                   | HS_ENTX (RXG)          | HS Serdes transmitter enable control. HS Serdes transmitter is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1E.0001 bit 15 is set HIGH.<br>0 = Disables HS serdes transmitter<br>1 = Enables HS serdes transmitter (Default 1'b1)  |                 | RW     |
| 10                   | HS_EQHLD (RXG)         | HSRX Equalizer hold control.<br>0 = Normal operation (Default 1'b0)<br>1 = Holds equalizer and long tail correction in its current state   |                 | RW     |
| 9:8                  | HS_RATE_TX [1:0] (RXG) | HS Serdes TX rate settings.<br>00 = Full rate (Default 2'b00)<br>01 = Half rate<br>10 = Quarter rate<br>11 = Eighth rate   |                 | RW     |
| 7:6                  | HS_AGCCTRL[1:0] (RXG)  | Adaptive gain control loop.<br>00 = Attenuator will not change after lock has been achieved, even if AGC becomes unlocked<br>01 = Attenuator will not change when in lock state, but could change when AGC becomes unlocked (Default 2'b01)<br>10 = Force the attenuator off<br>11 = Force the attenuator on |                 | RW     |
| 5:4                  | HS_AZCAL[1:0] (RXG)    | Auto zero calibration.<br>00 = Auto zero calibration initiated when receiver is enabled (Default 2'b00)<br>01 = Auto zero calibration disabled<br>10 = Forced with automatic update.<br>11 = Forced without automatic update   |                 | RW     |

**Table 8-5. HS\_SERDES\_CONTROL\_2 (continued)**

| Device Address: 0x1E |                        | Register Address:0x0003  | Default:0xA848 |  |
|----------------------|------------------------|--|----------------|--|
| Bit(s)               | Name                   | Description  | Access         |  |
| 3                    | HS_ENRX (RXG)          | HS Serdes receiver enable control.<br>HS Serdes receiver is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1E.0001 bit 15 is set HIGH.<br>0 = Disables HS serdes receiver<br>1 = Enables HS serdes receiver (Default 1'b1)   | RW             |  |
| 2:0                  | HS_RATE_RX [2:0] (RXG) | HS Serdes RX rate settings. This setting is automatically controlled and value set through these register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set.<br>000 = Full rate (Default 3'b000)<br>101 = Half rate<br>110 = Quarter rate<br>111 = Eighth rate<br>001 = Reserved<br>01x = Reserved<br>100 = Reserved | RW             |  |

**Table 8-6. HSTX AC Mode Output Swing Control**

| HS_SWING[3:0] | AC MODE                    |
|---------------|----------------------------|
|               | TYPICAL AMPLITUDE (mVdfpp) |
| 0000          | 130                        |
| 0001          | 220                        |
| 0010          | 300                        |
| 0011          | 390                        |
| 0100          | 480                        |
| 0101          | 570                        |
| 0110          | 660                        |
| 0111          | 750                        |
| 1000          | 830                        |
| 1001          | 930                        |
| 1010          | 1020                       |
| 1011          | 1110                       |
| 1100          | 1180                       |
| 1101          | 1270                       |
| 1110          | 1340                       |
| 1111          | 1400                       |

**Table 8-7. HS\_SERDES\_CONTROL\_3**

| Device Address: 0x1E |                       | Register Address: 0x0004  | Default: 0x1500 |  |
|----------------------|-----------------------|---|-----------------|--|
| Bit(s)               | Name                  | Description   | Access          |  |
| 15                   | HS_ENTRACK (RXG)      | HSRX ADC Track mode.<br>0 = Normal operation (Default 1'b0)<br>1 = Forces ADC into track mode   | RW              |  |
| 14:12                | HS_EQPRE[2:0] (RXG)   | Serdes Rx precursor equalizer selection<br>000 = 1/9 cursor amplitude<br>001 = 3/9 cursor amplitude (Default 3'b001)<br>010 = 5/9 cursor amplitude<br>011 = 7/9 cursor amplitude<br>100 = 9/9 cursor amplitude<br>101 = 11/9 cursor amplitude<br>110 = 13/9 cursor amplitude<br>111 = Disable | RW              |  |
| 11:10                | HS_CDRMULT[1:0] (RXG) | Clock data recovery algorithm frequency multiplication selection (Default 2'b01)<br>00 = First order. Frequency offset tracking disabled<br>01 = Second order. 1x mode<br>10 = Second order. 2x mode<br>11 = Reserved   | RW              |  |
| 9:8                  | HS_CDRTHR[1:0] (RXG)  | Clock data recovery algorithm threshold selection (Default 2'b01)<br>00 = Four vote threshold<br>01 = Eight vote threshold<br>10 = Sixteen vote threshold<br>11 = Thirty two vote threshold   | RW              |  |
| 7                    | RESERVED              | For TI use only (Default 1'b0)  | RW              |  |
| 6                    | HS_PEAK_DISABLE (RXG) | HS Serdes PEAK_DISABLE control<br>0 = Normal operation (Default 1'b0)<br>1 = Disables high frequency peaking. Suitable for <6 Gbps operation  | RW              |  |
| 5                    | HS_H1CDRMODE (RXG)    | HS_Serdes H1CDRMODE control<br>0 = Normal operation (Default 1'b0)<br>1 = Enables CDR mode suitable for short channel operation.  | RW              |  |
| 4:0                  | HS_TWCRF[4:0] (RXG)   | Cursor Reduction Factor (Default 5'b00000). Refer to <a href="#">Table 8-8</a> .  | RW              |  |

**Table 8-8. HSTX Cursor Reduction Factor Weights**

| HS_TWCRF[4:0] |                      | HS_TWCRF[4:0] |                      |
|---------------|----------------------|---------------|----------------------|
| Value         | Cursor reduction (%) | Value         | Cursor reduction (%) |
| 00000         | 0                    | 10000         | 17                   |
| 00001         | 2.5                  | 10001         | 20                   |
| 00010         | 5.0                  | 10010         | 22                   |
| 00011         | 7.5                  | 10011         | 25                   |
| 00100         | 10.0                 | 10100         | 27                   |
| 00101         | 12                   | 10101         | 30                   |
| 00110         | 15                   | 10110         | 32                   |
| 00111         | Reserved             | 10111         | 35                   |
| 01000         |                      | 11000         | 37                   |
| 01001         |                      | 11001         | 40                   |
| 01010         |                      | 11010         | 42                   |
| 01011         |                      | 11011         | 45                   |
| 01100         |                      | 11100         | 47                   |
| 01101         |                      | 11101         | 50                   |
| 01110         |                      | 11110         | 52                   |
| 01111         |                      | 11111         | 55                   |

**Table 8-9. HS\_SERDES\_CONTROL\_4**

| Device Address: 0x1E |                       | Register Address:0x0005  | Default:0x2000 |
|----------------------|-----------------------|--|----------------|
| Bit(s)               | Name                  | Description  | Access         |
| 15                   | HS_RX_INVPAIR (RXG)   | Receiver polarity.<br>0 = Normal polarity. HSRXxP considered positive data. HSRXxN considered negative data (Default 1'b0)<br>1 = Inverted polarity. HSRXxP considered negative data. HSRXxN considered positive data          | RW             |
| 14                   | HS_TX_INVPAIR (RXG)   | Transmitter polarity.<br>0 = Normal polarity. HSTXxP considered positive data and HSTXxN considered negative data (Default 1'b0)<br>1 = Inverted polarity. HSTXxP considered negative data and HSTXxN considered positive data | RW             |
| 13                   | RESERVED              | For TI use only (Default 1'b1)   | RW             |
| 12:8                 | HS_TWPOST1[4:0] (RXG) | Adjacent post cursor1 Tap weight. Selects TAP settings for TX waveform. (Default 5'b00000 ) Refer <a href="#">Table 8-10</a> .   | RW             |
| 7:4                  | HS_TWPRES[3:0] (RXG)  | Precursor Tap weight. Selects TAP settings for TX waveform. (Default 4'b0000) Refer <a href="#">Table 8-12</a> .   | RW             |
| 3:0                  | HS_TWPOST2[3:0] (RXG) | Adjacent post cursor2 Tap weight. Selects TAP settings for TX waveform. (Default 4'b0000) Refer <a href="#">Table 8-11</a> .   | RW             |

**Table 8-10. HSTX Post-Cursor1 Transmit Tap Weights**

| HS_TWPOST1[4:0] |                | HS_TWPOST1[4:0] |                |
|-----------------|----------------|-----------------|----------------|
| Value           | Tap weight (%) | Value           | Tap weight (%) |
| 00000           | 0              | 10000           | 0              |
| 00001           | +2.5           | 10001           | -2.5           |
| 00010           | +5.0           | 10010           | -5.0           |
| 00011           | +7.5           | 10011           | -7.5           |
| 00100           | +10.0          | 10100           | -10.0          |
| 00101           | +12.5          | 10101           | -12.5          |
| 00110           | +15.0          | 10110           | -15.0          |
| 00111           | +17.5          | 10111           | -17.5          |
| 01000           | +20.0          | 11000           | -20.0          |
| 01001           | +22.5          | 11001           | -22.5          |
| 01010           | +25.0          | 11010           | -25.0          |
| 01011           | +27.5          | 11011           | -27.5          |
| 01100           | +30.0          | 11100           | -30.0          |
| 01101           | +32.5          | 11101           | -32.5          |
| 01110           | +35.0          | 11110           | -35.0          |
| 01111           | +37.5          | 11111           | -37.5          |

**Table 8-11. HSTX Post-Cursor2 Transmit Tap Weights**

| HS_TWPOST2[3:0] |                | HS_TWPOST2[3:0] |                |
|-----------------|----------------|-----------------|----------------|
| Value           | Tap weight (%) | Value           | Tap weight (%) |
| 0000            | 0              | 1000            | 0              |
| 0001            | +2.5           | 1001            | -2.5           |
| 0010            | +5.0           | 1010            | -5.0           |
| 0011            | +7.5           | 1011            | -7.5           |
| 0100            | +10.0          | 1100            | -10.0          |
| 0101            | +12.5          | 1101            | -12.5          |
| 0110            | +15.0          | 1110            | -15.0          |

**Table 8-11. HSTX Post-Cursor2 Transmit Tap Weights (continued)**

| HS_TWPOST2[3:0] |                | HS_TWPOST2[3:0] |                |
|-----------------|----------------|-----------------|----------------|
| Value           | Tap weight (%) | Value           | Tap weight (%) |
| 0111            | +17.5          | 1111            | -17.5          |

**Table 8-12. HSTX Pre-Cursor Transmit Tap Weights**

| HS_TWPRE[3:0] |                | HS_TWPRE[3:0] |                |
|---------------|----------------|---------------|----------------|
| Value         | Tap weight (%) | Value         | Tap weight (%) |
| 0000          | 0              | 1000          | 0              |
| 0001          | +2.5           | 1001          | -2.5           |
| 0010          | +5.0           | 1010          | -5.0           |
| 0011          | +7.5           | 1011          | -7.5           |
| 0100          | +10.0          | 1100          | -10.0          |
| 0101          | +12.5          | 1101          | -12.5          |
| 0110          | +15.0          | 1110          | -15.0          |
| 0111          | +17.5          | 1111          | -17.5          |

**Table 8-13. LS\_SERDES\_CONTROL\_1**

| Device Address: 0x1E |                                 | Register Address: 0x0006  | Default: 0xF115 |
|----------------------|---------------------------------|---|-----------------|
| Bit(s)               | Name                            | Description   | Access          |
| 15:12                | LS_LN_CFG_EN[3:0]<br>(RXG)      | Configuration control for LS Serdes Lane settings (Default 4'b1111)<br>[3] corresponds to LN3, [2] corresponds to LN2<br>[1] corresponds to LN1, [0] corresponds to LN0<br>0 = Writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 control registers do not affect respective LS Serdes lane<br>1 = Writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 control registers affect respective LS Serdes lane<br>For example, if subsequent writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 registers need to affect the settings in Lanes 0 and 1, LS_LN_CFG_EN[3:0] should be set to 4'b0011<br>Read values in LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 reflect the settings value for Lane selected through LS_LN_CFG_EN[3:0].<br>To read Lane 0 settings, LS_LN_CFG_EN[3:0] should be set to 4'b0001<br>To read Lane 1 settings, LS_LN_CFG_EN[3:0] should be set to 4'b0010<br>To read Lane 2 settings, LS_LN_CFG_EN[3:0] should be set to 4'b0100<br>To read Lane 3 settings, LS_LN_CFG_EN[3:0] should be set to 4'b1000<br>Read values of LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 registers are not valid for any other LS_LN_CFG_EN[3:0] combination | RW              |
| 11:10                | RESERVED                        | For TI use only (Default 2'b00)   | RW              |
| 9:8                  | LS_LOOP_BANDWIDTH[1:0]<br>(RXG) | LS Serdes PLL Loop Bandwidth settings<br>00 = Reserved<br>01 = Applicable when external JC_PLL is NOT used (Default 2'b01)<br>10 = Applicable when external JC_PLL is used<br>11 = Reserved   | RW              |
| 7:5                  | RESERVED                        | For TI use only (Default 3'b000)  | RW              |
| 4                    | LS_ENPLL<br>(RXG)               | LS Serdes PLL enable control. LS Serdes PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1E.0001 bit 15 is set HIGH.<br>0 = Disables PLL in LS serdes<br>1 = Enables PLL in LS serdes (Default 1'b1)   | RW              |
| 3:0                  | LS_MPY[3:0]<br>(RXG)            | LS Serdes PLL multiplier setting (Default 4'b0101).<br>Refer 10GKR supported rates for valid PLL Multiplier values.<br>Refer to <a href="#">Table 8-14</a> .  | RW              |

**Table 8-14. LS PLL Multiplier Control**

| LS_MPY[3:0] |                       | LS_MPY[3:0] |                       |
|-------------|-----------------------|-------------|-----------------------|
| Value       | PLL Multiplier factor | Value       | PLL Multiplier factor |
| 0000        | 4x                    | 1000        | 15x                   |
| 0001        | 5x                    | 1001        | 20x                   |
| 0010        | 6x                    | 1010        | 25x                   |
| 0011        | Reserved              | 1011        | Reserved              |
| 0100        | 8x                    | 1100        | Reserved              |
| 0101        | 10x                   | 1101        | 50x                   |
| 0110        | 12x                   | 1110        | 65x                   |
| 0111        | 12.5x                 | 1111        | Reserved              |

**Table 8-15. LS\_SERDES\_CONTROL\_2**

| Device Address: 0x1E |                        | Register Address:0x0007  | Default:0xDC04 |        |
|----------------------|------------------------|--|----------------|--------|
| Bit(s)               | Name                   | Description  |                | Access |
| 15                   | RESERVED               | For TI use only.   |                | RW     |
| 14:12                | LS_SWING[2:0] (RXG)    | Output swing control on LS Serdes side. (Default 3'b101)<br>Refer to <a href="#">Table 8-16</a> .  |                | RW     |
| 11                   | LS_LOS (RXG)           | LS Serdes LOS detector control<br>0 = Disable Loss of signal detection on LS serdes lane inputs<br>1 = Enable Loss of signal detection on LS serdes lane inputs (Default 1'b1)   |                | RW     |
| 10                   | LS_TX_ENRX (RXG)       | LS Serdes enable control on the transmit channel. LS Serdes per lane on transmitter channel is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1E.0001 bit 15 is set HIGH. Lanes 3 and 2 are automatically disabled when in 2In 10G mode on transmit channel. Lanes 3, 2 and 1 are automatically disabled when in 1In 10G mode or 1G-KX mode on transmit channel.<br>0 = Disables LS serdes lane<br>1 = Enables LS serdes lane (Default 1'b1) |                | RW     |
| 9:8                  | LS_TX_RATE [1:0] (RXG) | LS Serdes lane rate settings on transmit channel.<br>00 = Full rate (Default 2'b00)<br>01 = Half rate<br>10 = Quarter rate<br>11 = Reserved  |                | RW     |
| 7:4                  | LS_DE[3:0] (RXG)       | LS Serdes De-emphasis settings. (Default 4'b0000)<br>Refer to <a href="#">Table 8-17</a> .   |                | RW     |
| 3                    | RESERVED               | For TI use only.   |                | RW     |
| 2                    | LS_RX_ENTX (RXG)       | LS Serdes lane enable control on receive channel. LS Serdes per lane on receiver channel is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1E.0001 bit 15 is set HIGH. Lanes 3 and 2 are automatically disabled when in 2In 10G mode on receive channel. Lanes 3, 2 and 1 are automatically disabled when in 1In 10G or 1G-KX mode on receive channel.<br>0 = Disables LS serdes lane<br>1 = Enables LS serdes lane (Default 1'b1)           |                | RW     |
| 1:0                  | LS_RX_RATE [1:0] (RXG) | LS Serdes lane rate settings on receive channel.<br>00 = Full rate (Default 2'b00)<br>01 = Half rate<br>10 = Quarter rate<br>11 = Reserved   |                | RW     |

**Table 8-16. LSRX Output AC Mode Output Swing Control**

| LS_SWING[2:0] | AC MODE                    |
|---------------|----------------------------|
|               | TYPICAL AMPLITUDE (mVdfpp) |
| 000           | 190                        |
| 001           | 380                        |
| 010           | 560                        |



**Table 8-16. LSRX Output AC Mode Output Swing Control (continued)**

| LS_SWING[2:0] | AC MODE                    |
|---------------|----------------------------|
|               | TYPICAL AMPLITUDE (mVdfpp) |
| 011           | 710                        |
| 100           | 850                        |
| 101           | 950                        |
| 110           | 1010                       |
| 111           | 1050                       |

**Table 8-17. LSRX Output De-emphasis**

| LS_DE[3:0] |                     |       | LS_DE[3:0] |                     |        |
|------------|---------------------|-------|------------|---------------------|--------|
| Value      | Amplitude reduction |       | Value      | Amplitude reduction |        |
|            | (%)                 | dB    |            | (%)                 | dB     |
| 0000       | 0                   | 0     | 1000       | 38.08               | -4.16  |
| 0001       | 4.76                | -0.42 | 1001       | 42.85               | -4.86  |
| 0010       | 9.52                | -0.87 | 1010       | 47.61               | -5.61  |
| 0011       | 14.28               | -1.34 | 1011       | 52.38               | -6.44  |
| 0100       | 19.04               | -1.83 | 1100       | 57.14               | -7.35  |
| 0101       | 23.8                | -2.36 | 1101       | 61.9                | -8.38  |
| 0110       | 28.56               | -2.92 | 1110       | 66.66               | -9.54  |
| 0111       | 33.32               | -3.52 | 1111       | 71.42               | -10.87 |

**Table 8-18. LS\_SERDES\_CONTROL\_3**

| Device Address: 0x1E |                            | Register Address: 0x0008   | Default: 0x000D |
|----------------------|----------------------------|--|-----------------|
| Bit(s)               | Name                       | Description  | Access          |
| 15                   | LS_RX_INVPA<br>IR<br>(RXG) | LS Serdes lane outputs polarity on the receive channel. (x = Channel A or B, y = Lane 0 or 1 or 2 or 3)<br>0 = Normal polarity. OUTxyP considered positive data. OUTxyN considered negative data (Default 1'b0)<br>1 = Inverted polarity. OUTxyP considered negative data. OUTxyN considered positive data   | RW              |
| 14                   | LS_TX_INVPA<br>IR<br>(RXG) | LS Serdes lane inputs polarity on the transmit channel. (x = Channel A or B, y = Lane 0 or 1 or 2 or 3)<br>0 = Normal polarity. INxyP considered positive data and INxyN considered negative data (Default 1'b0)<br>1 = Inverted polarity. INxyP considered negative data and INxyN considered positive data | RW              |
| 13:12                | RESERVED                   | For TI use only (Default 2'b00)  | RW              |
| 11:8                 | LS_EQ[3:0]<br>(RXG)        | LS Serdes Equalization control (Default 4'b0000). <a href="#">Table 8-19</a>   | RW              |
| 7:0                  | RESERVED                   | For TI use only (Default 8'b00001101)  | RW              |

**Table 8-19. LS\_EQ Serdes Equalization**

| LS_EQ[3:0] |               |           | LS_EQ[3:0] |               |           |
|------------|---------------|-----------|------------|---------------|-----------|
| Value      | Low Freq Gain | Zero Freq | Value      | Low Freq Gain | Zero Freq |
| 0000       | Maximum       |           | 1000       | Adaptive      | 365 MHz   |
| 0001       | Adaptive      |           | 1001       |               | 275 MHz   |
| 0010       | Reserved      |           | 1010       |               | 195 MHz   |
| 0011       |               |           | 1011       |               | 140 MHz   |
| 0100       |               |           | 1100       |               | 105 MHz   |
| 0101       |               |           | 1101       |               | 75 MHz    |
| 0110       |               |           | 1110       |               | 55 MHz    |
| 0111       |               |           | 1111       |               | 50 MHz    |

**Table 8-20. HS\_OVERLAY\_CONTROL**

| Device Address: 0x1E<br>Default:0x0380 |                                      | Register Address:0x0009  |        |  |
|--|--------------------------------------|--|--------|--|
| Bit(s)                                 | Name                                 | Description  | Access |  |
| 15:14                                  | LS_OK_OUT_GATE[1:0]<br>(G)           | LS_OK_OUT gating control<br>X0 = Gating disabled (Default 2'b00)<br>01 = Gating enabled. LS_OK_OUT gated to LOW<br>11 = Gating enabled. LS_OK_OUT gated to HIGH  | RW     |  |
| 13:12                                  | LS_OK_IN_GATE[1:0]<br>(G)            | LS_OK_IN gating control<br>X0 = Gating disabled (Default 2'b00)<br>01 = Gating enabled. LS_OK_IN gated to LOW<br>11 = Gating enabled. LS_OK_IN gated to HIGH   | RW     |  |
| 11:8                                   | RESERVED                             | For TI use only. (Default 4'b0011)   | RW     |  |
| 7                                      | HS_LOS_MASK<br>(G)                   | 0 = HS Serdes LOS status is used to generate HS channel synchronization status. If HS Serdes indicates LOS, channel synchronization indicates synchronization is not achieved<br>1 = HS Serdes LOS status is not used to generate HS channel synchronization status (Default 1'b1) | RW     |  |
| 6                                      | RESERVED                             | For TI use only. Always reads 0.   | RW     |  |
| 5                                      | HS_CH_SYNC_OVERLAY<br>(RXG)          | 0 = LOSx pin does not reflect receive channel loss of block lock (Default 1'b0)<br>1 = Allows channel loss of block lock to be reflected on LOSx pin   | RW     |  |
| 4                                      | HS_INVALID_CODE_OVE<br>RLAY<br>(RXG) | 0 = LOSx pin does not reflect receive channel invalid code word error (Default 1'b0)<br>1 = Allows invalid code word error to be reflected on LOSx pin   | RW     |  |
| 3                                      | HS_AGCLOCK_OVERLAY<br>(RXG)          | 0 = LOSx pin does not reflect HS Serdes AGC unlock status (Default 1'b0)<br>1 = Allows HS Serdes AGC unlock status to be reflected on LOSx pin   | RW     |  |
| 2                                      | HS_AZDONE_OVERLAY<br>(RXG)           | 0 = LOSx pin does not reflect HS Serdes auto zero calibration not done status (Default 1'b0)<br>1 = Allows auto zero calibration not done status to be reflected on LOSx pin   | RW     |  |
| 1                                      | HS_PLL_LOCK_OVERLAY<br>(RXG)         | 0 = LOSx pin does not reflect loss of HS Serdes PLL lock status (Default 1'b0)<br>1 = Allows HS Serdes loss of PLL lock status to be reflected on LOSx pin   | RW     |  |
| 0                                      | HS_LOS_OVERLAY<br>(RXG)              | 0 = LOSx pin does not reflect HS Serdes Loss of signal condition (Default 1'b0)<br>1 = Allows HS Serdes Loss of signal condition to be reflected on LOSx pin   | RW     |  |

**Table 8-21. LS\_OVERLAY\_CONTROL**

| Device Address: 0x1E |                              | Register Address:0x000A  |        | Default:0x4000 |  |
|----------------------|------------------------------|--|--------|----------------|--|
| Bit(s)               | Name                         | Description  | Access |                |  |
| 15:13                | RESERVED                     | For TI use only (Default 3'b010)   | RW     |                |  |
| 12                   | LS_PLL_LOCK_OVERLAY<br>(RXG) | 0 = LOSx pin does not reflect loss of LS SERDES PLL lock status (Default 1'b0)<br>1 = Allows LS SERDES loss of PLL lock status to be reflected on LOSx pin | RW     |                |  |

**Table 8-21. LS\_OVERLAY\_CONTROL (continued)**

| Device Address: 0x1E |  | Register Address:0x000A  | Default:0x4000 |        |
|----------------------|--|--|----------------|--------|
| Bit(s)               | Name                                     | Description  |                | Access |
| 11:8                 | LS_CH_SYNC_OVERLAY_LN[3:0]<br>(RXG)      | [3] Corresponds to Lane 3, [2] Corresponds to Lane 2<br>[1] Corresponds to Lane 1, [0] Corresponds to Lane 0<br>0 = LOSx pin does not reflect LS Serdes lane loss of synchronization condition (Default 1'b0)<br>1 = Allows LS serdes lane loss of synchronization condition to be reflected on LOSx pin |                | RW     |
| 7:4                  | LS_INVALID_CODE_OVERLAY_LN[3:0]<br>(RXG) | [3] Corresponds to Lane 3, [2] Corresponds to Lane 2<br>[1] Corresponds to Lane 1, [0] Corresponds to Lane 0<br>0 = LOSx pin does not reflect LS Serdes lane invalid code condition (Default 1'b0)<br>1 = Allows LS serdes lane invalid code condition to be reflected on LOSx pin                       |                | RW     |
| 3:0                  | LS_LOS_OVERLAY_LN[3:0]<br>(RXG)          | [3] Corresponds to Lane 3, [2] Corresponds to Lane 2<br>[1] Corresponds to Lane 1, [0] Corresponds to Lane 0<br>0 = LOSx pin does not reflect LS Serdes lane Loss of signal condition (Default 1'b0)<br>1 = Allows LS serdes lane Loss of signal condition to be reflected on LOSx pin                   |                | RW     |

**Table 8-22. LOOPBACK\_TP\_CONTROL**

| Device Address: 0x1E |                                | Register Address:0x000B   | Default:0x0D10 |        |
|----------------------|--------------------------------|---|----------------|--------|
| Bit(s)               | Name                           | Description   |                | Access |
| 15:14                | RESERVED                       | For TI use only. (Default 2'b00)  |                | RW     |
| 13                   | HS_TP_GEN_EN<br>(RXG)          | 0 = Normal operation (Default 1'b0)<br>1 = Activates test pattern generation selected by bits 1E.000B bits 10:8   |                | RW     |
| 12                   | HS_TP_VERIFY_EN<br>(RXG)       | 0 = Normal operation (Default 1'b0)<br>1 = Activates test pattern verification selected by bits 1E.000B bits 10:8   |                | RW     |
| 11                   | LS_TEST_PATT_SEL[2]<br>(RXG)   | See selection in 1E.000B bits 5:4   |                | RW     |
| 10:8                 | HS_TEST_PATT_SEL[2:0]<br>(RXG) | Test Pattern Selection. Refer Refer to TLK10232 Bringup Procedure (a separate document) for more information.<br>H/L/M/CRPAT valid in 1GKX/10G modes<br>000 = High Frequency Test Pattern<br>001 = Low Frequency Test Pattern<br>010 = Mixed Frequency Test Pattern<br>011 = CRPAT Long<br>100 = CRPAT Short<br>PRBS pattern valid in 1GKX/10G/10GKR modes.<br>101 = $2^7 - 1$ PRBS pattern (Default 3'b101)<br>110 = $2^{23} - 1$ PRBS pattern<br>111 = $2^{31} - 1$ PRBS pattern<br>Errors can be checked by reading HS_ERROR_COUNT register. For KR standard pattern generation and verification, please refer to Register 03.002A |                | RW     |
| 7                    | LS_TP_GEN_EN<br>(RXG)          | 0 = Normal operation (Default 1'b0)<br>1 = Activates test pattern generation selected by bits {1E.000B bit 11, 1E.000B bits 5:4} on the LS side   |                | RW     |
| 6                    | LS_TP_VERIFY_EN<br>(RXG)       | 0 = Normal operation (Default 1'b0)<br>1 = Activates test pattern verification selected by bits {1E.000B bit 11, 1E.000B bits 5:4} on the LS side   |                | RW     |
| 5:4                  | LS_TEST_PATT_SEL[1:0]<br>(RXG) | LS Test Pattern Selection LS_TEST_PATT_SEL[2:0].<br>LS_TEST_PATT_SEL[2] is 1E.000B bit 11<br>000 = High Frequency Test Pattern<br>001 = Low Frequency Test Pattern<br>010 = Mixed Frequency Test Pattern<br>011 = CRPAT Long (In 1GKX mode only)<br>100 = CRPAT Short (In 1GKX mode only)<br>101 = $2^7 - 1$ PRBS pattern (Default 3'b101)<br>110 = $2^{23} - 1$ PRBS pattern<br>111 = $2^{31} - 1$ PRBS pattern<br>For XAUI standard test pattern generation and verification in KR mode, please refer register 01.8002 and 01.8003  |                | RW     |

**Table 8-22. LOOPBACK\_TP\_CONTROL (continued)**

| Device Address: 0x1E |                          | Register Address:0x000B   | Default:0x0D10 |        |
|----------------------|--------------------------|---|----------------|--------|
| Bit(s)               | Name                     | Description   |                | Access |
| 3                    | DEEP_REMOTE_LPBK (RXG)   | 0 = Normal functional mode (Default 1'b0)<br>1 = Enable deep remote loopback mode   |                | RW     |
| 2                    | RESERVED                 | For TI use only (Default 1'b0)  |                | RW     |
| 1                    | RESERVED                 | For TI use only (Default 1'b0)  |                | RW     |
| 0                    | SHALLOW_LOCAL_LPBK (RXG) | 0 = Normal functional mode (Default 1'b0)<br>1 = Enable shallow local loopback mode |                | RW     |

**Table 8-23. LS\_CONFIG\_CONTROL**

| Device Address: 0x1E |                         | Register Address:0x000C   | Default:0x0330 |        |
|----------------------|-------------------------|---|----------------|--------|
| Bit(s)               | Name                    | Description   |                | Access |
| 15:14                | RESERVED                | For TI use only (Default 2'b00)   |                | RW     |
| 13:12                | LS_STATUS_CFG[1:0] (RG) | Selects selected lane status to be reflected in LS_STATUS_1 register<br>1E.0015 bit 14<br>00 = Lane 0 (Default 2'b00)<br>01 = Lane 1<br>10 = Lane 2<br>11 = Lane 3        |                | RW     |
| 11:10                | RESERVED                | For TI use only. Always reads 0.  |                | RW     |
| 9:8                  | RESERVED                | For TI use only. (Default 2'b11)  |                | RW     |
| 7:6                  | RESERVED                | For TI use only.  |                | RO     |
| 5                    | LS_LOS_MASK (G)         | 0 = LS Serdes LOS status of enabled lanes is used to generate link status<br>1 = LS Serdes LOS status of enabled lanes is not used to generate link status (Default 1'b1) |                | RW     |
| 4                    | LS_PLL_LOCK_MASK (G)    | 0 = LS Serdes PLL Lock status is used to generate link status<br>1 = LS Serdes PLL Lock status is not used to generate link status (Default 1'b1)                         |                | RW     |
| 3                    | RESERVED                | For TI use only. Always reads 0.  |                | RW     |
| 2                    | FORCE_LM_REALIGN (G)    | 0 = Normal operation (Default 1'b0)<br>1 = Force lane realignment in Link status monitor  |                | RW/SC  |
| 1:0                  | RESERVED                | For TI use only   |                | RO     |

**Table 8-24. CLK\_CONTROL<sup>(1)</sup>**

| Device Address: 0x1E |                        | Register Address:0x000D  | Default: 0x2F80 |        |
|----------------------|------------------------|--|-----------------|--------|
| Bit(s)               | Name                   | Description  |                 | Access |
| 15:14                | RESERVED               | For TI use only. Always reads 0.   |                 | RW     |
| 13                   | CLKOUT_EN (RXG)        | Output clock enable.<br>0 = Holds CLKOUTx_P/N output to a fixed value.<br>1 = Allows CLKOUTx_P/N output to toggle normally. (Default 1'b1) |                 | RW     |
| 12                   | CLKOUT_POWERDOWN (RXG) | 0 = Normal operation (Default 1'b0)<br>1 = Enable CLKOUTx_P/N Power Down.  |                 | RW     |
| 11:8                 | RESERVED               | For TI use only. (Default 4'b1111)   |                 | RW     |

(1) This register is channel independent.

**Table 8-24. CLK\_CONTROL<sup>(1)</sup> (continued)**

| Device Address: 0x1E |                          | Register Address: 0x000D   | Default: 0x2F80 |        |
|----------------------|--------------------------|--|-----------------|--------|
| Bit(s)               | Name                     | Description  |                 | Access |
| 7:4                  | CLKOUT_DIV[3:0]<br>(RXG) | CLKOUT Output clock divide setting. This value is used to divide selected clock (Selected using CLKOUT_SEL) before giving it out onto respective channel CLKOUTx_P/N.<br>0000 = Divide by 1<br>0001 = RESERVED<br>0010 = RESERVED<br>0011 = RESERVED<br>0100 = Divide by 2<br>0101 = RESERVED<br>0110 = RESERVED<br>0111 = RESERVED<br>1000 = Divide by 4 (Default 4'b1000)<br>1001 = Divide by 8<br>1010 = Divide by 16<br>1011 = RESERVED<br>1100 = Divide by 5<br>1101 = Divide by 10<br>1110 = Divide by 20<br>1111 = Divide by 25   |                 | RW     |
| 3:0                  | CLKOUT_SEL[3:0]<br>(RXG) | CLKOUT Output clock select. Selects Recovered clock sent out on CLKOUTx_P/N pins (Default 4'b0000)<br>00x0 = Selects Ch A HS recovered byte clock as output clock<br>00x1 = Selects Ch A HS transmit byte clock as output clock<br>010x = Selects Ch A HSRX VCO divide by 4 clock as output clock<br>0110 = Selects Ch A LS recovered byte clock as output clock<br>0111 = Selects Ch A LS transmit byte clock as output clock<br>10x0 = Selects Ch B HS recovered byte clock as output clock<br>10x1 = Selects Ch B HS transmit byte clock as output clock<br>110x = Selects Ch B HSRX VCO divide by 4 clock as output clock<br>1110 = Selects Ch B LS recovered byte clock as output clock<br>1111 = Selects Ch B LS transmit byte clock as output clock |                 | RW     |

**Table 8-25. RESET\_CONTROL**

| Device Address: 0x1E |                         | Register Address: 0x000E  | Default: 0x0000 |                         |
|----------------------|-------------------------|---|-----------------|-------------------------|
| Bit(s)               | Name                    | Description   |                 | Access                  |
| 15:8                 | RESERVED                | For TI use only. Always reads 0.  |                 | RW                      |
| 7:4                  | RESERVED                | For TI use only. (Default 4'b0000)  |                 | RW                      |
| 3                    | DATAPATH_RESET<br>(RXG) | Channel datapath reset control. Required once the desired functional mode is configured.<br>0 = Normal operation. (Default 1'b0)<br>1 = Resets channel logic excluding MDIO registers. (Resets both Tx and Rx datapath) |                 | RW<br>SC <sup>(1)</sup> |
| 2                    | TXFIFO_RESET<br>(G)     | Transmit FIFO reset control. Applicable in 10G mode only. Not required in 10GKR mode as 10GKR FIFO is self centering.<br>0 = Normal operation. (Default 1'b0)<br>1 = Resets transmit datapath FIFO.                     |                 |                         |
| 1                    | RXFIFO_RESET<br>(G)     | Receive FIFO reset control. Applicable in 10G mode only. Not required in 10GKR mode as 10GKR FIFO is self centering.<br>0 = Normal operation. (Default 1'b0)<br>1 = Resets receive datapath FIFO.                       |                 |                         |
| 0                    | RESERVED                | For TI use only. (Default 1'b0)   |                 | RW                      |

(1) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

**Table 8-26. CHANNEL\_STATUS\_1**

| Device Address: 0x1E |                         | Register Address:0x000F  | Default:0x0000 |  |
|----------------------|-------------------------|--|----------------|--|
| Bit(s)               | Name                    | Description  | Access         |  |
| 15                   | HS_TP_STATUS (RXG)      | Test Pattern status for High/Low/Mixed/CRPAT test patterns. Valid in 10G/1GKX modes.<br>1 = Alignment has achieved and correct pattern has been received. Any bit errors are reflected in HS_ERROR_COUNTER register (0x10)<br>0 = Alignment has not been determined      | RO             |  |
| 14                   | LS_ALIGN_STATUS (RXG)   | Lane alignment status<br>1 = Lane alignment is achieved on the LS side<br>0 = Lane alignment is not achieved on the LS side  | RO/LL          |  |
| 13                   | HS_LOS (RXG)            | Loss of Signal Indicator.<br>When high, indicates that a loss of signal condition is detected on HS serial receive inputs  | RO/LH          |  |
| 12                   | HS_AZ_DONE (RXG)        | Auto zero complete indicator.<br>When high, indicates auto zero calibration is complete  | RO/LL          |  |
| 11                   | HS_AGC_LOCKED (RXG)     | Adaptive gain control loop lock indicator.<br>When high, indicates AGC loop is in locked state   | RO/LL          |  |
| 10                   | HS_CHANNEL_SYNC (RXG)   | Channel synchronization status indicator.<br>When high, indicates channel synchronization has achieved   | RO/LL          |  |
| 9                    | RESERVED                | For TI use only.   | RO/LH          |  |
| 8                    | HS_DECODE_INVALID (RXG) | Valid when decoder is enabled and during CRPAT test pattern verification. When high, indicates decoder received an invalid code word, or a 8b/10b disparity error. In functional mode, number of DECODE_INVALID errors are reflected in HS_ERROR_COUNTER register (0x10) | RO/LH          |  |
| 7                    | TX_FIFO_UNDERFLOW (RG)  | Not applicable in 1GKX mode. When high, indicates underflow has occurred in the transmit datapath (CTC) FIFO.  | RO/LH          |  |
| 6                    | TX_FIFO_OVERFLOW (RXG)  | When high, in 10GKR and 10G modes indicates overflow has occurred in the transmit datapath (CTC) FIFO.   | RO/LH          |  |
| 5                    | RX_FIFO_UNDERFLOW (RG)  | Not applicable in 1GKX mode. When high, indicates underflow has occurred in the receive datapath (CTC) FIFO.   | RO/LH          |  |
| 4                    | RX_FIFO_OVERFLOW (RXG)  | In 10GKR and 10G modes, high indicates overflow has occurred in the receive datapath (CTC) FIFO. In 1G-KX mode, high indicates a FIFO error.   | RO/LH          |  |
| 3                    | RX_LS_OK (G)            | Receive link status indicator from system side. Applicable in 10G mode only<br>When high, indicates receive link status is achieved on the system side .   | RO/LL          |  |
| 2                    | TX_LS_OK (G)            | Link status indicator from Lane alignment/Link training slave inside TLK10232.<br>When high, indicates 10G Link align achieved sync and alignment .  | RO/LL          |  |
| 1                    | LS_PLL_LOCK (RXG)       | LS Serdes PLL lock indicator<br>When high, indicates LS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N  | RO/LL          |  |
| 0                    | HS_PLL_LOCK (RXG)       | HS Serdes PLL lock indicator<br>When high, indicates HS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N  | RO/LL          |  |

**Table 8-27. HS\_ERROR\_COUNTER**

| Device Address: 0x1E |                          | Register Address:0x0010   | Default:0xFFFFD |  |
|----------------------|--------------------------|---|-----------------|--|
| Bit(s)               | Name                     | Description   | Access          |  |
| 15:0                 | HS_ERR_COUNT[15:0] (RXG) | In functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder. In 10GKR mode, reading this register also clears value in 03.0021 bits 7:0.<br>In 10GKR mode, default value for this register is 16'h0000.<br>In HS test pattern verification mode , this counter reflects error count for the test pattern selected through 1E.000B bits 10:8<br>When PRBS_EN pin is set, this counter reflects error count for selected PRBS pattern.<br>Counter value cleared to 16'h0000 when read. | COR             |  |

**Table 8-28. LS\_LN0\_ERROR\_COUNTER**

| Device Address: 0x1E |                                 | Register Address:0x0011  | Default:0xFFFFD |
|----------------------|---------------------------------|--|-----------------|
| Bit(s)               | Name                            | Description  | Access          |
| 15:0                 | LS_LN0_ERR_COUNT[15:0]<br>(RXG) | Lane 0 Error counter<br>In 10GKR/1GKX functional modes, this counter reflects number of invalid code words (includes disparity errors) received by decoder<br>In 10G functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder in lane alignment slave.<br>In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 1E.000B bits 5:4<br>Counter value cleared to 16'h0000 when read. | COR             |

**Table 8-29. LS\_LN1\_ERROR\_COUNTER**

| Device Address: 0x1E |                                | Register Address:0x0012  | Default:0xFFFFD |
|----------------------|--------------------------------|--|-----------------|
| Bit(s)               | Name                           | Description  | Access          |
| 15:0                 | LS_LN1_ERR_COUNT[15:0]<br>(RG) | Lane 1 Error counter<br>In 10GKR/1GKX functional modes, this counter reflects number of invalid code words (includes disparity errors) received by decoder<br>In 10G functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder in lane alignment slave.<br>In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 1E.000B bits 5:4<br>Counter value cleared to 16'h0000 when read. | COR             |

**Table 8-30. LS\_LN2\_ERROR\_COUNTER**

| Device Address: 0x1E |                                | Register Address:0x0013  | Default:0xFFFFD |
|----------------------|--------------------------------|--|-----------------|
| Bit(s)               | Name                           | Description  | Access          |
| 15:0                 | LS_LN2_ERR_COUNT[15:0]<br>(RG) | Lane 2 Error counter<br>In 10GKR/1GKX functional modes, this counter reflects number of invalid code words (includes disparity errors) received by decoder<br>In 10G functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder in lane alignment slave.<br>In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 1E.000B bits 5:4<br>Counter value cleared to 16'h0000 when read. | COR             |

**Table 8-31. LS\_LN3\_ERROR\_COUNTER**

| Device Address: 0x1E |                                | Register Address:0x0014  | Default:0xFFFFD |
|----------------------|--------------------------------|--|-----------------|
| Bit(s)               | Name                           | Description  | Access          |
| 15:0                 | LS_LN3_ERR_COUNT[15:0]<br>(RG) | Lane 3 Error counter<br>In 10GKR/1GKX functional modes, this counter reflects number of invalid code words (includes disparity errors) received by decoder<br>In 10G functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder in lane alignment slave.<br>In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 1E.000B bits 5:4<br>Counter value cleared to 16'h0000 when read. | COR             |

**Table 8-32. LS\_STATUS\_1**

| Device Address: 0x1E |                            | Register Address:0x0015  | Default:0x0000 |
|----------------------|----------------------------|--|----------------|
| Bit(s)               | Name                       | Description  | Access         |
| 15:12                | RESERVED                   | For TI use only.   | RO             |
| 11                   | LS_INVALID_DECODE<br>(RXG) | LS Invalid decode error for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 1E.000C). Error count for each lane can also be monitored through respective LS_LNx_ERR_COUNT registers | RO/LH          |

**Table 8-32. LS\_STATUS\_1 (continued)**

| Device Address: 0x1E |                              | Register Address:0x0015   | Default:0x0000 |
|----------------------|------------------------------|---|----------------|
| Bit(s)               | Name                         | Description   | Access         |
| 10                   | LS_LOS<br>(RXG)              | Loss of Signal Indicator.<br>When high, indicates that a loss of signal condition is detected on LS serial receive inputs for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 1E.000C) | RO/LH          |
| 9                    | LS_LN_ALIGN_FIFO_ERR<br>(RG) | LS Lane alignment FIFO error status<br>1 = Lane alignment FIFO on LS side has error<br>0 = Lane alignment FIFO on LS side has no error  | RO/LH          |
| 8                    | LS_CH_SYNC_STATUS<br>(RXG)   | LS Channel sync status for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 1E.000C)  | RO/LL          |
| 7:4                  | RESERVED                     | For TI use only.  | RO             |
| 3:0                  | LS_CHSYNC_ROT[3:0]<br>(RXG)  | Channel synchronization pointer on LS side. Required for latency measurement function. See Latency Measurement function section for more details.   | RO             |

**Table 8-33. HS\_STATUS\_1**

| Device Address: 0x1E |                                 | Register Address:0x0016  | Default:0x0000 |
|----------------------|---------------------------------|--|----------------|
| Bit(s)               | Name                            | Description  | Access         |
| 15:7                 | RESERVED                        | For TI use only.   | RO             |
| 6:4                  | HS_KR_CH_SYNC_ROT[6:4]<br>(RXG) | Channel synchronization pointer on HS side in 10GKR mode. Required for latency measurement function. See Latency Measurement function section for more details.<br>In 10GKR mode, [6:4] reflects 3 MSB's of 7 bit HS sync rotation. In 1GKX and 10G modes, indicates channel synchronization state on HS side. | RO             |
| 3:0                  | HS_KR_CH_SYNC_ROT[3:0]<br>(RXG) | Channel synchronization pointer on HS side. Required for latency measurement function. See Latency Measurement function section for more details.<br>In 10GKR mode, reflects 4 LSB's of 7 bit HS sync rotation.<br>In 10G and 1GKX modes, reflects 4 bit HS sync rotation.                                     | RO             |

**Table 8-34. DST\_CONTROL\_1**

| Device Address: 0x1E |                                | Register Address:0x0017   | Default:0x2000 |
|----------------------|--------------------------------|---|----------------|
| Bit(s)               | Name                           | Description   | Access         |
| 15:13                | RESERVED                       | For TI use only (Default 3'b001)  | RW             |
| 12                   | DST_PIN_SW_EN<br>(RXG)         | 1 = Enable pin switch feature using top level pin. Ignore MDIO software switch. Requires setting PRTAD0_PIN_EN to high and setting PRTAD0_PIN_EN_SEL to control applicable channel Tx data switch.<br>0 = Disable pin switch feature. Only MDIO software switch is used (Default 1'b0)              | RW             |
| 11:10                | DST_PIN_SW_SRC_1[1:0]<br>(RXG) | Applicable when top level pin (PRTAD0) is assigned to control transmit dataswitch source input and if PRTAD0 is HIGH.<br>00 = Select same channel LS input(Default 2'b00)<br>01 = Select same channel HS input<br>10 = Select alternate channel LS input<br>11 = Select alternate channel HS output | RW             |
| 9:8                  | DST_PIN_SW_SRC_0[1:0]<br>(RXG) | Applicable when top level pin (PRTAD0) is assigned to control transmit dataswitch source input and if PRTAD0 is LOW.<br>00 = Select same channel LS input(Default 2'b00)<br>01 = Select same channel HS input<br>10 = Select alternate channel LS input<br>11 = Select alternate channel HS output  | RW             |
| 7                    | DST_OFF_SEL<br>(RX)            | Applicable only in KR & KX modes. Selects data pattern to trigger OFF condition (Default 1'b0)<br>KR Mode:<br>1 = Local Fault (0x0100009c)<br>0 = IDLE (0x07 on all lanes)<br>KX Mode:<br>1 = Match DST_OFF_CHAR specified in 1E.802AB<br>0 = IDLE (Either /11/ or /12/)                            | RW             |



**Table 8-34. DST\_CONTROL\_1 (continued)**

| Device Address: 0x1E |                    | Register Address: 0x0017   | Default: 0x2000 |        |
|----------------------|--------------------|--|-----------------|--------|
| Bit(s)               | Name               | Description  |                 | Access |
| 6                    | DST_ON_SEL (RX)    | Applicable only in KR & KX modes. Selects data pattern to trigger ON condition (Default 1'b0)<br>KR Mode:<br>1 = Local Fault (0x0100009c)<br>0 = IDLE (0x07 on all lanes)<br>KX Mode:<br>1 = Match DST_ON_CHAR specified in 1E.802A<br>0 = IDLE (Either /I1/ or /I2/)    |                 | RW     |
| 5                    | DST_STUFF_SEL (RX) | Applicable only in KR & KX modes. Selects data pattern to stuff the output during data switching (Default 1'b0)<br>KR Mode:<br>1 = Local Fault (0x0100009c)<br>0 = IDLE (0x07 on all lanes)<br>KX Mode:<br>1 = /V/ Error propagation (K30.7)<br>0 = /I2/ (/K28.5/D16.2/) |                 | RW     |
| 4:0                  | RESERVED           | For TI use only (Default 5'b00000)   |                 | RW     |

**Table 8-35. DST\_CONTROL\_2**

| Device Address: 0x1E |                             | Register Address: 0x0018   | Default: 0x0C20 |        |
|----------------------|-----------------------------|--|-----------------|--------|
| Bit(s)               | Name                        | Description  |                 | Access |
| 15:14                | DST_DATA_SRC_SEL[1:0] (RXG) | Data selection for transmit data switch source input. Applicable when DST_PIN_SW_EN is LOW.<br>00 = Select same channel LS input (Default 2'b00)<br>01 = Select same channel HS input<br>10 = Select alternate channel LS input<br>11 = Select alternate channel HS output   |                 | RW     |
| 13:12                | DST_DATA_SW_MODE[1:0] (RXG) | Selects condition to trigger data switch for the selected ON/OFF condition. (Default 2'b00)<br>OFF condition:<br>00 = Wait for OFF trigger<br>01 = Any data<br>10 = Any data<br>11 = Wait for OFF trigger<br>ON condition:<br>00 = Wait for ON trigger<br>01 = Wait for ON trigger<br>10 = Any data<br>11 = Any data |                 | RW     |
| 11:8                 | RESERVED                    | For TI use only (Default 4'b1100)  |                 | RW     |
| 7:0                  | DST_MASK_CYCLES[7:0] (RXG)  | Duration of clock cycles that the data-switch output data is masked with the data pattern selected through DST_STUFF_SEL. (Default 8'b0010_0000)   |                 | RW     |

**Table 8-36. DSR\_CONTROL\_1**

| Device Address: 0x1E |                             | Register Address: 0x0019  | Default: 0x2500 |        |
|----------------------|-----------------------------|---|-----------------|--------|
| Bit(s)               | Name                        | Description   |                 | Access |
| 15:13                | RESERVED                    | For TI use only (Default 3'b001)  |                 | RW     |
| 12                   | DSR_PIN_SW_EN (RXG)         | 1 = Enable pin switch feature using top level pin. Ignore MDIO software switch. Requires setting PRTAD0_PIN_EN to high and setting PRTAD0_PIN_EN_SEL to control applicable channel Rx data switch.<br>0 = Disable pin switch feature. Only MDIO software switch is used (Default 1'b0)              |                 | RW     |
| 11:10                | DSR_PIN_SW_SRC_1[1:0] (RXG) | Applicable when top level pin (PRTAD0) is assigned to control receive dataswitch source input and if PRTAD0 is HIGH.<br>00 = Select same channel LS input<br>01 = Select same channel HS input (Default 2'b01)<br>10 = Select alternate channel LS input<br>11 = Select alternate channel HS output |                 | RW     |

**Table 8-36. DSR\_CONTROL\_1 (continued)**

| Device Address: 0x1E |                                | Register Address:0x0019   | Default:0x2500 |        |
|----------------------|--------------------------------|---|----------------|--------|
| Bit(s)               | Name                           | Description   |                | Access |
| 9:8                  | DSR_PIN_SW_SRC_0[1:0]<br>(RXG) | Applicable when top level pin (PRTAD0) is assigned to control receive dataswitch source input and if PRTAD0 is LOW.<br>00 = Select same channel LS input<br>01 = Select same channel HS input(Default 2'b01)<br>10 = Select alternate channel LS input<br>11 = Select alternate channel HS output |                | RW     |
| 7                    | DSR_OFF_SEL<br>(RX)            | Applicable only in KR & KX modes. Selects data pattern to trigger OFF condition (Default 1'b0)<br>KR Mode:<br>1 = Local Fault (0x0100009c)<br>0 = IDLE (0x07 on all lanes)<br>KX Mode:<br>1 = Match DSR_OFF_CHAR specified in 1E.802E<br>0 = IDLE (Either /I1/ or /I2/)                           |                | RW     |
| 6                    | DSR_ON_SEL<br>(RX)             | Applicable only in KR & KX modes. Selects data pattern to trigger ON condition (Default 1'b0)<br>KR Mode:<br>1 = Local Fault (0x0100009c)<br>0 = IDLE (0x07 on all lanes)<br>KX Mode:<br>1 = Match DSR_ON_CHAR specified in 1E.802D<br>0 = IDLE (Either /I1/ or /I2/)                             |                | RW     |
| 5                    | DSR_STUFF_SEL<br>(RX)          | Applicable only in KR & KX modes. Selects data pattern to stuff the output during data switching (Default 1'b0)<br>KR Mode:<br>1 = Local Fault (0x0100009c)<br>0 = IDLE (0x07 on all lanes)<br>KX Mode:<br>1 = /V/ Error propagation (K30.7)<br>0 = /I2/ (/K28.5/D16.2/)                          |                | RW     |
| 4:0                  | RESERVED                       | For TI use only (Default 5'b00000)  |                | RW     |

**Table 8-37. DSR\_CONTROL\_2**

| Device Address: 0x1E |                                | Register Address:0x001A  | Default:0x4C20 |        |
|----------------------|--------------------------------|--|----------------|--------|
| Bit(s)               | Name                           | Description  |                | Access |
| 15:14                | DSR_DATA_SRC_SEL[1:0]<br>(RXG) | Data selection for receive data switch source input. Applicable when DST_PIN_SW_EN is LOW.<br>00 = Select same channel LS input<br>01 = Select same channel HS input(Default 2'b01)<br>10 = Select alternate channel LS input<br>11 = Select alternate channel HS output   |                | RW     |
| 13:12                | DSR_DATA_SW_MODE[1:0]<br>(RXG) | Selects condition to trigger data switch for the selected ON/OFF condition. (Default 2'b00)<br>OFF condition:<br>00 = Wait for OFF trigger<br>01 = Any data<br>10 = Any data<br>11 = Wait for OFF trigger<br>ON condition:<br>00 = Wait for ON trigger<br>01 = Wait for ON trigger<br>10 = Any data<br>11 = Any data |                | RW     |
| 11:8                 | RESERVED                       | For TI use only (Default 4'b1100)  |                | RW     |
| 7:0                  | DSR_MASK_CYCLES[7:0]<br>(RXG)  | Duration of clock cycles that the data-switch output data is masked with the data pattern selected through DST_STUFF_SEL. (Default 8'b0010_0000)   |                | RW     |

**Table 8-38. DATA\_SWITCH\_STATUS**

| Device Address: 0x1E |                         | Register Address: 0x001B   | Default: 0x1020 |  |
|----------------------|-------------------------|--|-----------------|--|
| Bit(s)               | Name                    | Description  | Access          |  |
| 15:12                | DST_EN[3:0]<br>(RXG)    | Source input data selection status on transmit side.<br>0001 = Same channel LS data<br>0010 = Same channel HS data<br>0100 = Alternate channel LS data<br>1000 = Alternate channel HS data | RO              |  |
| 11                   | DST_SW_PENDING<br>(RXG) | When HIGH, indicates data switching event is pending to be completed in the transmit side based on selected data source input  | RO              |  |
| 10                   | DST_SW_DONE<br>(RXG)    | When HIGH, indicates data switching event has occurred in the transmit side based on selected data source input  | RO/LH           |  |
| 9                    | DST_ON<br>(RXG)         | ON condition indicator from transmit data switch. When HIGH, indicates an ON condition has occurred in transmit data switch  | RO/LH           |  |
| 8                    | DST_OFF<br>(RXG)        | OFF condition indicator from transmit data switch. When HIGH, indicates an OFF condition has occurred in transmit data switch.   | RO/LH           |  |
| 7:4                  | DSR_EN[3:0]<br>(RXG)    | Source input data selection status on receive side.<br>0001 = Same channel LS data<br>0010 = Same channel HS data<br>0100 = Alternate channel LS data<br>1000 = Alternate channel HS data  | RO              |  |
| 3                    | DSR_SW_PENDING<br>(RXG) | When HIGH, indicates data switching event is pending to be completed in the receive side based on selected data source input   | RO              |  |
| 2                    | DSR_SW_DONE<br>(RXG)    | When HIGH, indicates data switching event has occurred in the receive side based on selected data source input   | RO/LH           |  |
| 1                    | DSR_ON<br>(RXG)         | ON condition indicator from receive data switch. When HIGH, indicates an ON condition has occurred in receive data switch.   | RO/LH           |  |
| 0                    | DSR_OFF<br>(RXG)        | OFF condition indicator from receive data switch. When HIGH, indicates an OFF condition has occurred in receive data switch.   | RO/LH           |  |

**Table 8-39. LS\_CH\_CONTROL\_1**

| Device Address: 0x1E |                                 | Register Address:0x001C  | Default: 0x0000 |  |
|----------------------|---------------------------------|--|-----------------|--|
| Bit(s)               | Name                            | Description  | Access          |  |
| 15:7                 | RESERVED                        | For TI use only. Always reads 0.   | RW              |  |
| 6                    | RESERVED                        | For TI use only. (Default 1'b0)  | RW/SC           |  |
| 5:2                  | RESERVED                        | For TI use only. (Default 4'b0000)   | RW              |  |
| 1:0                  | LS_CH_SYNC_HYS_SEL[1:0]<br>(RG) | LS Channel synchronization hysteresis selection for selected lane. Lane can be selected in LS_SERDES_CONTROL_1.<br>00 = The channel synchronization, when in the synchronization state, performs the Ethernet standard specified hysteresis to return to the LOS state (Default 2'b00)<br>01 = A single 8b/10b invalid decode error or disparity error causes the channel synchronization state machine to immediately transition from sync to LOS<br>10 = Two adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to LOS<br>11 = Three adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to LOS | RW              |  |

**Table 8-40. HS\_CH\_CONTROL\_1**

| Device Address: 0x1E |                                    | Register Address:0x001D  | Default: 0x0000 |  |
|----------------------|------------------------------------|--|-----------------|--|
| Bit(s)               | Name                               | Description  | Access          |  |
| 15:14                | RESERVED                           | For TI use only (Default 2'b00)  | RW              |  |
| 13                   | REFCLK_FREQ_SEL_1<br>(RX)          | Input REFCLK frequency selection MSB. When set, HS_PLL_MULT, LS_MPY and HS/LS TX/RX RATE settings can be set through related control bits specified in registers 1E.0002, 1E.0003, 1E.0006<br>0 = HS_PLL_MULT, LS_MPY and HS/LS TX/RX RATE are set automatically based on input REFCLK frequency as specified in REFCLK_FREQ_SEL_0(1E.001D bit 12) (Default 1'b0)<br>1 = Set this value if HS_PLL_MULT, LS_MPY and HS/LS TX/RX RATE values are NOT to be set automatically.  | RW              |  |
| 12                   | REFCLK_FREQ_SEL_0<br>(RXG)         | Input REFCLK frequency selection LSB. Applicable when REFCLK_FREQ_SEL_1(1E.001D bit 13) is set to 0.<br>0 = Set this value if REFCLK frequency is 156.25 MHz (Default 1'b0)<br>1 = Set this value if REFCLK frequency is 312.5 MHz   | RW              |  |
| 11                   | RX_CTC_BYPASS<br>(RX)              | 0 = Normal operation. (Default 1'b0)<br>1 = Disables RX CTC operation.   | RW              |  |
| 10                   | TX_CTC_BYPASS<br>(RX)              | 0 = Normal operation. (Default 1'b0)<br>1 = Disables TX CTC operation.   | RW              |  |
| 7:4                  | RESERVED                           | For TI use only (Default 4'b0000)  | RW              |  |
| 3                    | HS_ENC_BYPASS<br>(RXG)             | 0 = Normal operation. (Default 1'b0)<br>1 = Disables 8B/10B encoder on HS side.  | RW              |  |
| 2                    | HS_DEC_BYPASS<br>(RXG)             | 0 = Normal operation. (Default 1'b0)<br>1 = Disables 8B/10B decoder on HS side.  | RW              |  |
| 1:0                  | HS_CH_SYNC_HYSTERSIS[1:0]<br>(RXG) | Channel synchronization hysteresis control on the HS receive channel.<br>00 = The channel synchronization, when in the synchronization state, performs the Ethernet standard specified hysteresis to return to the unsynchronized state (Default 2'b00)<br>01 = A single 8b/10b invalid decode error or disparity error causes the channel synchronization state machine to immediately transition from sync to unsync<br>10 = Two adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to unsync<br>11 = Three adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to unsync | RW              |  |

**Table 8-41. EXT\_ADDRESS\_CONTROL**

| Device Address: 0x1E |                                | Register Address: 0x001E   | Default: 0x0000 |  |
|----------------------|--------------------------------|--|-----------------|--|
| Bit(s)               | Name                           | Description  | Access          |  |
| 15:0                 | EXT_ADDR_CONTROL[15:0]<br>(XG) | Applicable in Clause 22 mode only. This register should be written with the extended register address to be written/read. Contents of address written in this register can be accessed from Reg 1E.0x001F (Default 16'h0000) | RW              |  |

**Table 8-42. EXT\_ADDRESS\_DATA**

| Device Address: 0x1E |                             | Register Address: 0x001F  | Default: 0x0000 |  |
|----------------------|-----------------------------|---|-----------------|--|
| Bit(s)               | Name                        | Description   | Access          |  |
| 15:0                 | EXT_ADDR_DATA[15:0]<br>(XG) | Applicable in Clause 22 mode only. This register contains the data associated with the register address written in Register 1E.0x001E | RW              |  |

The registers below can be accessed directly through Clause 45 or indirectly through Clause 22. Contains mode specific control/status registers and implemented per channel basis.

**Table 8-43. VS\_10G\_LN\_ALIGN\_ACODE\_P**

| Device Address: 0x1E |                              | Register Address: 0x8003                                   | Default: 0x0283 |  |
|----------------------|------------------------------|--|-----------------|--|
| Bit(s)               | Name                         | Description  | Access          |  |
| 15:10                | RESERVED                     | For TI use only. Always reads 0.                           | RW              |  |
| 9:0                  | LN_ALIGN_ACODE_P[9:0]<br>(G) | 10 bit Alignment character to be matched (Default 10'h283) | RW              |  |

**Table 8-44. VS\_10G\_LN\_ALIGN\_ACODE\_N**

| Device Address: 0x1E |                              | Register Address: 0x8004                                   | Default: 0x017C |  |
|----------------------|------------------------------|--|-----------------|--|
| Bit(s)               | Name                         | Description  | Access          |  |
| 15:10                | RESERVED                     | For TI use only. Always reads 0.                           | RW              |  |
| 9:0                  | LN_ALIGN_ACODE_N[9:0]<br>(G) | 10 bit Alignment character to be matched (Default 10'h17C) | RW              |  |

**Table 8-45. MC\_AUTO\_CONTROL**

| Device Address: 0x1E |                                    | Register Address: 0x8021  | Default: 0x000F |  |
|----------------------|------------------------------------|---|-----------------|--|
| Bit(s)               | Name                               | Description   | Access          |  |
| 15:7                 | RESERVED                           | For TI use only. Always reads 0.  | RW              |  |
| 6                    | HS_PLL_LOCK_CHECK_DISABLE<br>(RXG) | 1 = Disable auto HS pll lock status check.<br>0 = Enable auto HS pll lock status check (Default 1'b0)   | RW              |  |
| 5                    | HS_LOS_CHECK_DISABLE<br>(RXG)      | 1 = Disable auto HS los status check<br>0 = Enable auto HS los sync status check (Default 1'b0)   | RW              |  |
| 4                    | SYNC_STATUS_CHECK_DISABLE<br>(RXG) | This bit needs to be set to 1 for PRBS testing.<br>1 = Disable auto sync status check.<br>0 = Enable auto sync status check (Default 1'b0)  | RW              |  |
| 3                    | CLKOUT_EN_AUTO_DISABLE<br>(RXG)    | This bit controls the signal which flat lines CLKOUT and applicable only when CLKOUT is selected to have HS Recovered byte clock<br>1 = CLKOUT clock flat lined if HS LOS is detected (Default 1'b1)<br>0 = CLKOUT clock not flat lined if HS LOS is detected | RW              |  |
| 2:0                  | RESERVED                           | For TI use only (Default 3'b111)  | RW              |  |

**Table 8-46. DST\_ON\_CHAR\_CONTROL**

| Device Address: 0x1E |                          | Register Address:0x802A  | Default: 0x02FD |
|----------------------|--------------------------|--|-----------------|
| Bit(s)               | Name                     | Description  | Access          |
| 15:10                | RESERVED                 | For TI use only. Always reads 0.   | RW              |
| 9:0                  | DST_ON_CHAR[9:0]<br>(XG) | Applicable only in 1GKX and 10G modes. 10 bit data pattern to trigger ON condition if matched on transmit side (Default 10'h2FD) | RW              |

**Table 8-47. DST\_OFF\_CHAR\_CONTROL**

| Device Address: 0x1E |                           | Register Address:0x802B   | Default: 0x02FD |
|----------------------|---------------------------|---|-----------------|
| Bit(s)               | Name                      | Description   | Access          |
| 15:10                | RESERVED                  | For TI use only. Always reads 0.  | RW              |
| 9:0                  | DST_OFF_CHAR[9:0]<br>(XG) | Applicable only in 1GKX and 10G modes. 10 bit data pattern to trigger OFF condition if matched on transmit side (Default 10'h2FD) | RW              |

**Table 8-48. DST\_STUFF\_CHAR\_CONTROL**

| Device Address: 0x1E |                            | Register Address:0x802C  | Default: 0x0207 |
|----------------------|----------------------------|--|-----------------|
| Bit(s)               | Name                       | Description  | Access          |
| 15:10                | RESERVED                   | For TI use only. Always reads 0.   | RW              |
| 9:0                  | DST_STUFF_CHAR[9:0]<br>(G) | Applicable only in 10G mode. 10 bit data pattern to stuff the output of data switch on transmit side (Default 10'h207) | RW              |

**Table 8-49. DSR\_ON\_CHAR\_CONTROL**

| Device Address: 0x1E |                          | Register Address:0x802D   | Default: 0x02FD |
|----------------------|--------------------------|---|-----------------|
| Bit(s)               | Name                     | Description   | Access          |
| 15:10                | RESERVED                 | For TI use only. Always reads 0.  | RW              |
| 9:0                  | DSR_ON_CHAR[9:0]<br>(XG) | Applicable only in 1GKX and 10G modes. 10 bit data pattern to trigger ON condition if matched on receive side (Default 10'h2FD) | RW              |

**Table 8-50. DSR\_OFF\_CHAR\_CONTROL**

| Device Address: 0x1E |                           | Register Address:0x802E  | Default: 0x02FD |
|----------------------|---------------------------|--|-----------------|
| Bit(s)               | Name                      | Description  | Access          |
| 15:10                | RESERVED                  | For TI use only. Always reads 0.   | RW              |
| 9:0                  | DSR_OFF_CHAR[9:0]<br>(XG) | Applicable only in 1GKX and 10G modes. 10 bit data pattern to trigger OFF condition if matched on receive side (Default 10'h2FD) | RW              |

**Table 8-51. DSR\_STUFF\_CHAR\_CONTROL**

| Device Address: 0x1E |                            | Register Address:0x802F   | Default: 0x0207 |
|----------------------|----------------------------|---|-----------------|
| Bit(s)               | Name                       | Description   | Access          |
| 15:10                | RESERVED                   | For TI use only. Always reads 0.  |                 |
| 9:0                  | DSR_STUFF_CHAR[9:0]<br>(G) | Applicable only in 10G mode. 10 bit data pattern to stuff the output of data switch on receive side (Default 10'h207) | RW              |

**Table 8-52. LATENCY\_MEASURE\_CONTROL**

| Device Address: 0x1E |                                      | Register Address:0x8040  | Default: 0x0000 |
|----------------------|--------------------------------------|--|-----------------|
| Bit(s)               | Name                                 | Description  | Access          |
| 15:8                 | RESERVED                             | For TI use only. Always reads 0.   | RW              |
| 7:6                  | LATENCY_MEAS_STOP_SEL[1: 0]<br>(RXG) | Latency measurement stop point selection<br>00 = Selects LS RX as stop point (Default 2'b00)<br>01 = Selects HS TX as stop point<br>1x = Selects external pin (PRTAD0) as stop point | RW              |

**Table 8-52. LATENCY\_MEASURE\_CONTROL (continued)**

| Device Address: 0x1E |                                       | Register Address:0x8040  | Default: 0x0000 |        |
|----------------------|---------------------------------------|--|-----------------|--------|
| Bit(s)               | Name                                  | Description  |                 | Access |
| 5:4                  | LATENCY_MEAS_CLK_DIV[1:0]<br>(RXG)    | Latency measurement clock divide control. Valid only when bit 1E.8040 bit 2 is 0. Divides clock to needed resolution. Higher the divide value, lesser the latency measurement resolution. Divider value should be chosen such that the divided clock doesn't result in clock slower than the high speed byte clock.<br>00 = Divide by 1 (Default 2'b00) (Most Accurate Measurement)<br>01 = Divide by 2<br>10 = Divide by 4<br>11 = Divide by 8 (Longest Measurement Capability) |                 | RW     |
| 3:2                  | LATENCY_MEAS_START_SEL[ 1:0]<br>(RXG) | Latency measurement start point selection<br>00 = Selects LS TX as start point (Default 2'b00)<br>01 = Selects HS RX as start point<br>1x = Selects external pin (PRTAD0) as start point   |                 | RW     |
| 1                    | LATENCY_MEAS_EN<br>(RXG)              | Latency measurement enable<br>0 = Disable Latency measurement (Default 'b0)<br>1 = Enable Latency measurement  |                 | RW     |
| 0                    | LATENCY_MEAS_CLK_SELECT<br>(RXG)      | Latency measurement clock selection.<br>0 = Selects VCO clock as per Latency measurement table. Bits 1E.8040 bits 5:4 can be used to divide this clock to achieve needed resolution. (Default 1'b0)<br>1 = Selects respective channel recovered byte clock   |                 | RW     |

**Table 8-53. LATENCY\_COUNTER\_2**

| Device Address: 0x1E |  | Register Address:0x8041   | Default: 0x0000 |        |
|----------------------|--|---|-----------------|--------|
| Bit(s)               | Name                                   | Description   |                 | Access |
| 15:12                | LATENCY_MEAS_START_COMMA[3:0]<br>(RXG) | Latency measurement start comma location status. "1" indicates start comma location found. If LS TX is selected as start point (1E.8040 bit 7 = 0), [3:0] indicates status for lane3, lane2, lane1, lane0. If HS RX is selected as start point (1E.8040 bit 7 = 1), [0] indicates status for data[9:0], [1] indicates status for data[19:10]. [3:2] is unused.<br>Reading this register will clear Latency stopwatch status specified in LATENCY_COUNTER_1 & LATENCY_COUNTER_2 registers. Below sequence of reads needs to be performed for accurate and repeat stopwatch measurements. See Latency measurement procedure more information.<br>READ 0x8041<br>READ 0x8042 |                 | RO/LH  |
| 11:8                 | LATENCY_MEAS_STOP_COMMA[3:0]<br>(RXG)  | Latency measurement stop comma location status. "1" indicates stop comma location found. If LS RX is selected as stop point (1E.8040 bit 6 = 0), [3:0] indicates status for lane3, lane2, lane1, lane0. If HS TX is selected as stop point (1E.8040 bit 6 = 1), [0] indicates status for data[9:0], [1] indicates status for data[19:10]. [3:2] is unused.  |                 | RO/LH  |
| 4                    | LATENCY_MEAS_READY<br>(RXG)            | Latency measurement ready indicator<br>0 = Indicates latency measurement not complete.<br>1 = Indicates latency measurement is complete and value in latency measurement counter (LATENCY_MEAS_COUNT[19:0]) is ready to be read.  |                 | RO/LH  |
| 3:0                  | LATENCY_MEAS_COUNT[19:16]<br>(RXG)     | Bits[19:16] of 20 bit wide latency measurement counter. Latency measurement counter value represents the latency in number of clock cycles. Each clock cycle is half of the period of the measurement clock as determined by register 1E.8040 bits 5:4 and 1E.8040 bit 0. This counter will return 20'h00000 if it's read before rx comma is received. If latency is more than 20'hFFFFFF clock cycles then this counter returns 20'hFFFFFF.  |                 | RO     |

**Table 8-54. LATENCY\_COUNTER\_1**

| Device Address: 0x1E |                                   | Register Address:0x8042  | Default: 0x0000 |                    |
|----------------------|-----------------------------------|--|-----------------|--------------------|
| Bit(s)               | Name                              | Description  |                 | Access             |
| 15:0                 | LATENCY_MEAS_COUNT[15:0]<br>(RXG) | Bits[15:0] of 20 bit wide latency measurement counter. Below sequence of reads needs to be performed for accurate and repeat stopwatch measurements.<br>READ 0x8041<br>READ 0x8042 |                 | COR <sup>(1)</sup> |

(1) Latency measurement counter value resets to 20'h00000 when this register is read. Start and Stop Comma (1E.8041 bits 15:12 & 1E.8041 bits 11:8) and count valid (1E.8041 bit 4) bits are also cleared when this register is read

**Table 8-55. TRIGGER\_LOAD\_CONTROL**

| Device Address: 0x1E |                               | Register Address:0x8100  | Default: 0x0000 |        |
|----------------------|-------------------------------|--|-----------------|--------|
| Bit(s)               | Name                          | Description  |                 | Access |
| 15:11                | RESERVED                      | For TI use only. Always reads 0.   |                 | RW     |
| 10:3                 | RESERVED                      | For TI use only. (Default 8'b00000000)   |                 | RW     |
| 2                    | DEFAULT_TX_LOAD_TRIGGER (RXG) | Valid only when DEFAULT_TX_TRIGGER_EN is HIGH<br>1 = Trigger loading default HS TX setting values<br>0 = Normal operation (Default 1'b0)<br>This bit needs to be written HIGH and then LOW to load the HS Tx default values. Applicable when link training is enabled. |                 | RW     |
| 1:0                  | RESERVED                      | For TI use only. (Default 2'b00)   |                 | RW     |

**Table 8-56. TRIGGER\_EN\_CONTROL**

| Device Address: 0x1E |                             | Register Address:0x8101  | Default: 0x0000 |        |
|----------------------|-----------------------------|--|-----------------|--------|
| Bit(s)               | Name                        | Description  |                 | Access |
| 15:11                | RESERVED                    | For TI use only. Always reads 0.   |                 | RW     |
| 10:3                 | RESERVED                    | For TI use only. (Default 8'b00000000)   |                 | RW     |
| 2                    | DEFAULT_TX_TRIGGER_EN (RXG) | 1 = Enable loading of Tx default values through DEFAULT_TX_LOAD_TRIGGER<br>0 = Normal operation (Default 1'b0) |                 | RW     |
| 1:0                  | RESERVED                    | For TI use only. (Default 2'b00)   |                 | RW     |

## 8.2 PMA/PMD Registers

The registers below can be accessed only in Clause 45 mode and with device address field set to 0x01 (DA[4:0] = 5'b00001).

NOTE: Link training registers can also be accessed in Clause 22 mode using indirect address method and in Clause 45 mode with device address field set to 0x1E (DA[4:0] = 5'b11110). Link training registers are also applicable in 10G and 1GKX modes.

**Table 8-57. PMA\_CONTROL\_1**

| Device Address: 0x01 |                | Register Address:0x0000  | Default: 0x0000 |        |
|----------------------|----------------|--|-----------------|--------|
| Bit(s)               | Name           | Description  |                 | Access |
| 15                   | RESET (RX)     | 1 = Global reset. Resets datapath and MDIO registers of all channels. Equivalent to asserting RESET_N.<br>0 = Normal operation (Default 1'b0)                                    |                 | RW/SC  |
| 14:12                | RESERVED       | For TI use only. Always reads 0.   |                 | RW     |
| 11                   | POWERDOWN (RX) | 1 = Enable power down mode<br>0 = Normal operation (Default 1'b0)  |                 | RW     |
| 10:1                 | RESERVED       | For TI use only. Always reads 0.   |                 | RW     |
| 0                    | LOOPBACK (RX)  | 1 = Enables loopback on HS side. LS data traverses through entire Tx datapath excluding HS serdes and will be available at LS output side<br>0 = Normal operation (Default 1'b0) |                 | RW     |

**Table 8-58. PMA\_STATUS\_1**

| Device Address: 0x01 |              | Register Address:0x0001  | Default: 0x0002 |        |
|----------------------|--------------|--|-----------------|--------|
| Bit(s)               | Name         | Description  |                 | Access |
| 7                    | FAULT (RX)   | 1 = Fault condition detected on either Tx or Rx side<br>0 = No fault condition detected<br>This bit is cleared after Register 01.0008 is read and no fault condition occurs after 01.0008 is read. |                 | RO     |
| 2                    | RX_LINK (RX) | 1 = Receive link is up<br>0 = Receive link is down   |                 | RO/LL  |



**Table 8-58. PMA\_STATUS\_1 (continued)**

| Device Address: 0x01 |                        | Register Address: 0x0001  | Default: 0x0002 |  |
|----------------------|------------------------|---|-----------------|--|
| Bit(s)               | Name                   | Description   | Access          |  |
| 1                    | LOW_POWER_ABILITY (RX) | Always reads 1.<br>1 = Supports low power mode<br>0 = Does not support low power mode | RO              |  |

**Table 8-59. PMA\_DEV\_IDENTIFIER\_1**

| Device Address: 0x01 |                            | Register Address: 0x0002   | Default: 0x4000 |  |
|----------------------|----------------------------|--|-----------------|--|
| Bit(s)               | Name                       | Description  | Access          |  |
| 15:0                 | DEV_IDENTIFIER[31:16] (RX) | 16 MSB of 32 bit unique device identifier. See <a href="#">Table 8-61</a> for identifier code details. | RO              |  |

**Table 8-60. PMA\_DEV\_IDENTIFIER\_2**

| Device Address: 0x01 |                           | Register Address: 0x0003  | Default: 0x5100 |  |
|----------------------|---------------------------|---|-----------------|--|
| Bit(s)               | Name                      | Description   | Access          |  |
| 15:0                 | DEV_IDENTIFIER[15:0] (RX) | 16 LSB of 32 bit unique device identifier. See <a href="#">Table 8-61</a> for identifier code details | RO              |  |

**Table 8-61. UNIQUE DEVICE IDENTIFIER <sup>(1)</sup>**

| Register address   | Value                   | Description                               |
|--------------------|-------------------------|---|
| 01.0002 bits 15:0  | 16'b0100_0000_0000_0000 | OUI[3-18]                                 |
| 01.0003 bits 15:10 | 6'b010100               | OUI[19-24]                                |
| 01.0003 bits 9:4   | 6'b010000               | 6-bit Manufacturer device model number    |
| 01.0003 bits 3:0   | 4'b0000                 | 4-bit Manufacturer device revision number |

- (1) The identifier code is composed of bits 3-24 of 25-bit organizationally unique identifier (OUI) assigned to Texas Instruments by IEEE. The 6-bit Manufacturer device model number is unique to TLK10232. The 4-bit Manufacturer device revision number denotes the current revision of TLK10232.

**Table 8-62. PMA\_SPEED\_ABILITY**

| Device Address: 0x01 |                | Register Address: 0x0004  | Default: 0x0011 |  |
|----------------------|----------------|---|-----------------|--|
| Bit(s)               | Name           | Description   | Access          |  |
| 4                    | SPEED_1G (RX)  | Always reads 1.<br>1 = Capable of operating at 1000 Mb/s<br>0 = Not capable of operating at 1000 Mb/s | RO              |  |
| 0                    | SPEED_10G (RX) | Always reads 1.<br>1 = Capable of operating at 10 Gb/s<br>0 = Not capable of operating at 10 Gb/s     | RO              |  |

**Table 8-63. PMA\_DEV\_PACKAGE\_1**

| Device Address: 0x01 |                      | Register Address: 0x0005  | Default: 0x000B |  |
|----------------------|----------------------|---|-----------------|--|
| Bit(s)               | Name                 | Description   | Access          |  |
| 3                    | PCS_PRESENT (RX)     | Always reads 1.<br>1 = PCS present in the package<br>0 = PCS not present in the package                                 | RO              |  |
| 1                    | PMA_PMD_PRESENT (RX) | Always reads 1.<br>1 = PMA/PMD present in the package<br>0 = PMA/PMD not present in the package                         | RO              |  |
| 0                    | CL22_PRESENT (RX)    | Always reads 1.<br>1 = Clause 22 registers present in the package<br>0 = Clause 22 registers not present in the package | RO              |  |

**Table 8-64. PMA\_DEV\_PACKAGE\_2**

| Device Address: 0x01 |                      | Register Address: 0x0006  | Default: 0x4000 |  |
|----------------------|----------------------|---|-----------------|--|
| Bit(s)               | Name                 | Description   | Access          |  |
| 15                   | VS_DEV2_PRESENT (RX) | Always reads 0.<br>1 = Vendor specific device 2 present in the package<br>0 = Vendor specific device 2 not present in the package | RO              |  |
| 14                   | VS_DEV1_PRESENT (RX) | Always reads 1.<br>1 = Vendor specific device 1 present in the package<br>0 = Vendor specific device 1 not present in the package | RO              |  |

**Table 8-65. PMA\_STATUS\_2**

| Device Address: 0x01 |                         | Register Address: 0x0008   | Default: 0xB000 |  |
|----------------------|-------------------------|--|-----------------|--|
| Bit(s)               | Name                    | Description  | Access          |  |
| 15:14                | DEV_PRESENT (RX)        | Always reads 2'b10<br>0x = No device responding at this address<br>10 = Device responding at this address<br>11 = No device responding at this address | RO              |  |
| 13                   | TX_FAULT_ABILITY (RX)   | Always reads 1'b1.<br>1 = Able to detect fault condition on Tx path<br>0 = Not able to detect fault condition on Tx path                               | RO              |  |
| 12                   | RX_FAULT_ABILITY (RX)   | Always reads 1'b1.<br>1 = Able to detect fault condition on Rx path<br>0 = Not able to detect fault condition on Rx path                               | RO              |  |
| 11                   | TX_FAULT (RX)           | 1 = Fault condition detected on transmit path<br>0 = No fault condition detected on transmit path  | RO/LH           |  |
| 10                   | RX_FAULT (RX)           | 1 = Fault condition detected on receive path<br>0 = No fault condition detected on receive path  | RO/LH           |  |
| 8                    | TX_DISABLE_ABILITY (RX) | Always reads 1'b0.<br>1 = Able to perform transmit disable function<br>0 = Not able to perform transmit disable function                               | RO              |  |

**Table 8-66. PMA\_RX\_SIGNAL\_DET\_STATUS**

| Device Address: 0x01 |                    | Register Address: 0x000A   | Default: 0x0000 |  |
|----------------------|--------------------|--|-----------------|--|
| Bit(s)               | Name               | Description  | Access          |  |
| 0                    | RX_SIGNAL_DET (RX) | 1 = Signal detected on serial Rx pins<br>0 = Signal not detected on serial Rx pins | RO              |  |

**Table 8-67. PMA\_EXTENDED\_ABILITY**

| Device Address: 0x01 |                 | Register Address: 0x000B  | Default: 0x0050 |  |
|----------------------|-----------------|---|-----------------|--|
| Bit(s)               | Name            | Description   | Access          |  |
| 6                    | KX_ABILITY (RX) | Always reads 1'b11 = Able to perform 1000BASE-KX<br>0 = Not able to perform 1000BASE-KX | RO              |  |
| 4                    | KR_ABILITY (RX) | Always reads 1'b11 = Able to perform 10GBASE-KR<br>0 = Not able to perform 10GBASE-KR   | RO              |  |

**Table 8-68. LT\_TRAIN\_CONTROL**

| Device Address: 0x01 |                           | Register Address: 0x0096  | Default: 0x0002 |  |
|----------------------|---------------------------|---|-----------------|--|
| Bit(s)               | Name                      | Description   | Access          |  |
| 15:2                 | RESERVED                  | For TI use only. Always reads 0.  | RW              |  |
| 1                    | LT_TRAINING_ENABLE (RXG)  | 1 = Enable start-up protocol as per 10GBASE-KR standard(Default 1'b1)<br>0 = Disable start-up protocol<br>This bit should be set to HIGH for autotrain mode to function correctly | RW              |  |
| 0                    | LT_RESTART_TRAINING (RXG) | 1 = Reset link/auto train<br>0 = Normal operation (Default 1'b0)  | RW/SC           |  |

**Table 8-69. LT\_TRAIN\_STATUS**

| Device Address: 0x01      Register Address: 0x0097      Default: 0x0000 |                            |  |        |
|---|----------------------------|--|--------|
| Bit(s)  | Name                       | Description  | Access |
| 3   | LT_TRAINING_FAIL<br>(RXG)  | 1 = Training failure has been detected<br>0 = Training failure has not been detected   | RO     |
| 2   | LT_START_PROTOCOL<br>(RXG) | 1 = Start up protocol in progress<br>0 = Start up protocol complete                    | RO     |
| 1   | LT_FRAME_LOCK<br>(RXG)     | 1 = Training frame delineation detected<br>0 = Training frame delineation not detected | RO     |
| 0   | LT_RX_STATUS<br>(RXG)      | 1 = Receiver trained and ready to receive data<br>0 = Receiver training in progress    | RO     |

**Table 8-70. LT\_LINK\_PARTNER\_CONTROL**

| Device Address: 0x01      Register Address: 0x0098      Default: 0x0000 |                           |  |        |
|---|---------------------------|--|--------|
| Bit(s)  | Name                      | Description  | Access |
| 13  | LT_LP_PRESET<br>(RXG)     | 1 = KR preset coefficients<br>0 = Normal operation   | RO     |
| 12  | LT_LP_INITIALIZE<br>(RXG) | 1 = Initialize KR coefficients<br>0 = Normal operation   | RO     |
| 9   | LT_LP_COEFF_SWG<br>(RXG)  | Swing update<br>11 = Reserved<br>01 = Increment<br>10 = Decrement<br>00 = Hold                             | RO     |
| 7   | LT_LP_COEFF_PS2<br>(RXG)  | Post2 tap control update<br>11 = Reserved<br>01 = Increment<br>10 = Decrement<br>00 = Hold                 | RO     |
| 5   | LT_LP_COEFF_P1<br>(RXG)   | Coefficient K(+1) update<br>11 = Reserved<br>01 = Increment<br>10 = Decrement<br>00 = Hold                 | RO     |
| 3   | LT_LP_COEFF_0<br>(RXG)    | Coefficient K(0) update<br>11 = Reserved<br>01 = Increment<br>10 = Decrement<br>00 = Hold                  | RO     |
| 1   | LT_LP_COEFF_M1<br>(RXG)   | Coefficient K(-1) update<br>11 = Reserved<br>01 = Increment<br>10 = Decrement<br>00 = Hold (Default 2'b00) | RO     |

**Table 8-71. LT\_LINK\_PARTNER\_STATUS**

| Device Address: 0x01      Register Address: 0x0099      Default: 0x0000 |                               |   |        |
|---|-------------------------------|---|--------|
| Bit(s)  | Name                          | Description   | Access |
| 15  | LT_LP_RX_READY<br>(RXG)       | 1 = LP receiver has determined that training is complete and prepared to receive data<br>0 = LP receiver is requesting that training continue | RO     |
| 9:8   | LT_LP_COEFF_SWG_STAT<br>(RXG) | Swing update<br>11 = Maximum<br>01 = Updated<br>10 = Minimum<br>00 = Not updated  | RO     |
| 7:6   | LT_LP_COEFF_PS2_STAT<br>(RXG) | Post2 tap control update<br>11 = Maximum<br>01 = Updated<br>10 = Minimum<br>00 = Not updated  | RO     |

**Table 8-71. LT\_LINK\_PARTNER\_STATUS (continued)**

| Device Address: 0x01 |                              | Register Address: 0x0099   |        | Default: 0x0000 |  |
|----------------------|------------------------------|--|--------|-----------------|--|
| Bit(s)               | Name                         | Description  | Access |                 |  |
| 5:4                  | LT_LP_COEFF_P1_STAT<br>(RXG) | Coefficient K(+1) update<br>11 = Maximum<br>01 = Updated<br>10 = Minimum<br>00 = Not updated | RO     |                 |  |
| 3:2                  | LT_LP_COEFF_0_STAT<br>(RXG)  | Coefficient K(0) update<br>11 = Maximum<br>01 = Updated<br>10 = Minimum<br>00 = Not updated  | RO     |                 |  |
| 1:0                  | LT_LP_COEFF_M1_STAT<br>(RXG) | Coefficient K(-1) update<br>11 = Maximum<br>01 = Updated<br>10 = Minimum<br>00 = Not updated | RO     |                 |  |

**Table 8-72. LT\_LOCAL\_DEVICE\_CONTROL**

| Device Address: 0x01 |                           | Register Address: 0x009A   |        | Default: 0x0000 |  |
|----------------------|---------------------------|--|--------|-----------------|--|
| Bit(s)               | Name                      | Description  | Access |                 |  |
| 15                   | RESERVED                  | For TI use only. Always reads 0.   | RO     |                 |  |
| 13                   | LT_LD_PRESET<br>(RXG)     | 1 = KR preset coefficients<br>0 = Normal operation (Default 1'b0)  | RO     |                 |  |
| 12                   | LT_LD_INITIALIZE<br>(RXG) | 1 = Initialize KR coefficients<br>0 = Normal operation (Default 1'b0)                                      | RO     |                 |  |
| 9:8                  | LT_LD_COEFF_SWG<br>(RXG)  | Swing update<br>11 = Reserved<br>01 = Increment<br>10 = Decrement<br>00 = Hold (Default 2'b00)             | RO     |                 |  |
| 7:6                  | LT_LD_COEFF_PS2<br>(RXG)  | Post2 tap control update<br>11 = Reserved<br>01 = Increment<br>10 = Decrement<br>00 = Hold (Default 2'b00) | RO     |                 |  |
| 5:4                  | LT_LD_COEFF_P1<br>(RXG)   | Coefficient K(+1) update<br>11 = Reserved<br>01 = Increment<br>10 = Decrement<br>00 = Hold (Default 2'b00) | RO     |                 |  |
| 3:2                  | LT_LD_COEFF_0<br>(RXG)    | Coefficient K(0) update<br>11 = Reserved<br>01 = Increment<br>10 = Decrement<br>00 = Hold (Default 2'b00)  | RO     |                 |  |
| 1:0                  | LT_LD_COEFF_M1<br>(RXG)   | Coefficient K(-1) update<br>11 = Reserved<br>01 = Increment<br>10 = Decrement<br>00 = Hold (Default 2'b00) | RO     |                 |  |

**Table 8-73. LT\_LOCAL\_DEVICE\_STATUS**

| Device Address: 0x01 |                         | Register Address: 0x009B  |        | Default: 0x0000 |  |
|----------------------|-------------------------|---|--------|-----------------|--|
| Bit(s)               | Name                    | Description   | Access |                 |  |
| 15                   | LT_LD_RX_READY<br>(RXG) | 1 = LD receiver has determined that training is complete and prepared to receive data<br>0 = LD receiver is requesting that training continue | RO     |                 |  |

**Table 8-73. LT\_LOCAL\_DEVICE\_STATUS (continued)**

| Device Address: 0x01 |                           | Register Address: 0x009B   |        | Default: 0x0000 |  |
|----------------------|---------------------------|--|--------|-----------------|--|
| Bit(s)               | Name                      | Description  | Access |                 |  |
| 4                    | LT_LD_COEFF_P1_STAT (RXG) | Coefficient K(+1) update<br>11 = Maximum<br>01 = Updated<br>10 = Minimum<br>00 = Not updated | RO     |                 |  |
| 3:2                  | LT_LD_COEFF_0_STAT (RXG)  | Coefficient K(0) update<br>11 = Maximum<br>01 = Updated<br>10 = Minimum<br>00 = Not updated  | RO     |                 |  |
| 1:0                  | LT_LD_COEFF_M1_STAT (RXG) | Coefficient K(-1) update<br>11 = Maximum<br>01 = Updated<br>10 = Minimum<br>00 = Not updated | RO     |                 |  |

**Table 8-74. KX\_STATUS**

| Device Address: 0x01 |                         | Register Address: 0x00A1  |        | Default: 0x3000 |  |
|----------------------|-------------------------|---|--------|-----------------|--|
| Bit(s)               | Name                    | Description   | Access |                 |  |
| 13                   | KX_TX_FAULT_ABILITY (X) | Always reads 1.<br>1 = Able to detect fault condition on transmit path<br>0 = Not able to detect fault condition on transmit path | RO     |                 |  |
| 12                   | KX_RX_FAULT_ABILITY (X) | Always reads 1.<br>1 = Able to detect fault condition on receive path<br>0 = Not able to detect fault condition on receive path   | RO     |                 |  |
| 11                   | KX_TX_FAULT (X)         | 1 = Fault condition detected on transmit path<br>0 = No fault condition detected on transmit path                                 | RO/LH  |                 |  |
| 10                   | KX_RX_FAULT (X)         | 1 = Fault condition detected on receive path<br>0 = No fault condition detected on receive path                                   | RO/LH  |                 |  |
| 0                    | KX_RX_SIGNAL_DETECT (X) | 1 = Signal detected<br>0 = Signal not detected  | RO     |                 |  |

**Table 8-75. KR\_FEC\_ABILITY**

| Device Address: 0x01 |                        | Register Address: 0x00AA   |        | Default: 0x0003 |  |
|----------------------|------------------------|--|--------|-----------------|--|
| Bit(s)               | Name                   | Description  | Access |                 |  |
| 1                    | KR_FEC_ERR_ABILITY (R) | Always reads 1.<br>1 = Device supports 10GBASE-R FEC error indication to PCS<br>0 = Device does not support 10GBASE-R FEC function error indication tx PCS | RO     |                 |  |
| 0                    | KR_FEC_ABILITY (R)     | Always reads 1.<br>1 = Device supports 10GBASE-R FEC function<br>0 = Device does not support 10GBASE-R FEC function  |        |                 |  |

**Table 8-76. KR\_FEC\_CONTROL**

| Device Address: 0x01 |                       | Register Address: 0x00AB   |        | Default: 0x0000 |  |
|----------------------|-----------------------|--|--------|-----------------|--|
| Bit(s)               | Name                  | Description  | Access |                 |  |
| 15:2                 | RESERVED              | For TI use only. Always reads 0.   | RW     |                 |  |
| 1                    | KR_FEC_ERR_IND_EN (R) | 1 = Enable FEC decoder to indicate errors to PCS<br>0 = Disable FEC decoder error indication to PCS (Default 1'b0) | RW     |                 |  |
| 0                    | KR_FEC_EN (R)         | 1 = Enable 10GBASE-R FEC function<br>0 = Disable 10GBASE-R FEC function (Default 1'b0)                             | RW     |                 |  |

**Table 8-77. KR\_FEC\_C\_COUNT\_1<sup>(1)</sup>**

| Device Address: 0x01      Register Address: 0x00AC      Default: 0x0000 |                             |   |        |
|---|-----------------------------|---|--------|
| Bit(s)  | Name                        | Description                                   | Access |
| 15:0  | KR_FEC_C_COUNT[15:0]<br>(R) | Lower 16 bits of FEC corrected blocks counter | COR    |

(1) To get correct 32 bit counter value of KR\_FEC\_C\_COUNT, Register 01.00AC should be read first followed by Register 01.00AD

**Table 8-78. KR\_FEC\_C\_COUNT\_2**

| Device Address: 0x01      Register Address: 0x00AD      Default: 0x0000 |                              |   |        |
|---|------------------------------|---|--------|
| Bit(s)  | Name                         | Description                                   | Access |
| 15:0  | KR_FEC_C_COUNT[31:16]<br>(R) | Upper 16 bits of FEC corrected blocks counter | COR    |

**Table 8-79. KR\_FEC\_UC\_COUNT\_1<sup>(1)</sup>**

| Device Address: 0x01      Register Address: 0x00AE      Default: 0x0000 |                              |   |        |
|---|------------------------------|---|--------|
| Bit(s)  | Name                         | Description                                     | Access |
| 15:0  | KR_FEC_UC_COUNT[15:0]<br>(R) | Lower 16 bits of FEC Uncorrected blocks counter | COR    |

(1) To get correct 32 bit counter value of KR\_FEC\_UC\_COUNT, Register 01.00AE should be read first followed by Register 01.00AF

**Table 8-80. KR\_FEC\_UC\_COUNT\_2**

| Device Address: 0x01      Register Address: 0x00AF      Default: 0x0000 |                               |   |        |
|---|-------------------------------|---|--------|
| Bit(s)  | Name                          | Description                                     | Access |
| 15:0  | KR_FEC_UC_COUNT[31:16]<br>(R) | Lower 16 bits of FEC Uncorrected blocks counter | COR    |

**Table 8-81. KR\_VS\_FIFO\_CONTROL\_1**

| Device Address: 0x01      Register Address: 0x8001      Default: 0xCC4C |                            |   |         |      |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
|---|----------------------------|---|---------|------|----|----|------|----|------|------|------|----|----|----------|-----|------|--|----|-----|-----|-----|--|----|-----|-----|-----|--|----|
| Bit(s)  | Name                       | Description   | Access  |      |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 15  | RESERVED                   | For TI use only (Default 1'b1)  | RW      |      |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 14:12   | RX_FIFO_DEPTH[2:0]<br>(R)  | Rx CTC FIFO depth selection<br>1xx = 32 deep (Default 3'b100)<br>011 = 24 deep<br>010 = 16 deep<br>001 = 12 deep<br>000 = 8 deep (No CTC function)  | RW      |      |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 11:10   | RX_CTC_WMK_SEL[1:0]<br>(R) | Water mark selection for receive CTC<br>Works in conjunction with RX_FIFO_DEPTH_SEL setting (Default 2'b11)<br><table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Depth-&gt;</th> <th>32</th> <th>24</th> <th>26</th> <th>12/8</th> </tr> </thead> <tbody> <tr> <td>11</td> <td>High</td> <td>High</td> <td>High</td> <td>NA</td> </tr> <tr> <td>10</td> <td>Mid-high</td> <td>Mid</td> <td>High</td> <td></td> </tr> <tr> <td>01</td> <td>Mid</td> <td>Low</td> <td>Low</td> <td></td> </tr> <tr> <td>00</td> <td>Low</td> <td>Low</td> <td>Low</td> <td></td> </tr> </tbody> </table> | Depth-> | 32   | 24 | 26 | 12/8 | 11 | High | High | High | NA | 10 | Mid-high | Mid | High |  | 01 | Mid | Low | Low |  | 00 | Low | Low | Low |  | RW |
| Depth->   | 32                         | 24  | 26      | 12/8 |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 11  | High                       | High  | High    | NA   |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 10  | Mid-high                   | Mid   | High    |      |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 01  | Mid                        | Low   | Low     |      |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 00  | Low                        | Low   | Low     |      |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 9   | RX_Q_CNT_IPG<br>(R)        | 0 = Normal operation. (Default 1'b0)<br>1 = Sequence columns are counted as IPG.  | RW      |      |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 8   | RX_CTC_Q_DROP_EN<br>(R)    | 0 = Normal operation. (Default 1'b0)<br>1 = Enable Q column drop in RX CTC.   | RW      |      |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 7   | XMIT_IDLE<br>(R)           | 1 = Transmit idle pattern onto LS side<br>0 = Normal operation (Default 1'b0)   | RW      |      |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |

**Table 8-81. KR\_VS\_FIFO\_CONTROL\_1 (continued)**

| Device Address: 0x01 |                            | Register Address: 0x8001  |      | Default: 0xCC4C |         |    |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
|----------------------|----------------------------|---|------|-----------------|---------|----|----|----|------|----|------|------|------|----|----|----------|-----|------|--|----|-----|-----|-----|--|----|-----|-----|-----|--|----|
| Bit(s)               | Name                       | Description   |      |                 | Access  |    |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 6:4                  | TX_FIFO_DEPTH[2:0]<br>(R)  | Tx CTC FIFO depth selection<br>1xx = 32 deep (Default 3'b100)011 = 24 deep<br>010 = 16 deep001 = 12 deep<br>000 = 8 deep (No CTC function)  |      |                 | RW      |    |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 3:2                  | TX_CTC_WMK_SEL[1:0]<br>(R) | Water mark selection for receive CTC<br>Works in conjunction with TX_FIFO_DEPTH_SEL setting (Default 2'b11)<br><table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Depth-&gt;</th> <th>32</th> <th>24</th> <th>26</th> <th>12/8</th> </tr> </thead> <tbody> <tr> <td>11</td> <td>High</td> <td>High</td> <td>High</td> <td>NA</td> </tr> <tr> <td>10</td> <td>Mid-high</td> <td>Mid</td> <td>High</td> <td></td> </tr> <tr> <td>01</td> <td>Mid</td> <td>Low</td> <td>Low</td> <td></td> </tr> <tr> <td>00</td> <td>Low</td> <td>Low</td> <td>Low</td> <td></td> </tr> </tbody> </table> |      |                 | Depth-> | 32 | 24 | 26 | 12/8 | 11 | High | High | High | NA | 10 | Mid-high | Mid | High |  | 01 | Mid | Low | Low |  | 00 | Low | Low | Low |  | RW |
| Depth->              | 32                         | 24  | 26   | 12/8            |         |    |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 11                   | High                       | High  | High | NA              |         |    |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 10                   | Mid-high                   | Mid   | High |                 |         |    |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 01                   | Mid                        | Low   | Low  |                 |         |    |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 00                   | Low                        | Low   | Low  |                 |         |    |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 1                    | TX_Q_CNT_IPG<br>(R)        | 0 = Normal operation. (Default 1'b0)<br>1 = Sequence columns are counted as IPG.  |      |                 | RW      |    |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |
| 0                    | TX_CTC_Q_DROP_EN<br>(R)    | 0 = Normal operation. (Default 1'b0)<br>1 = Enable Q column drop in TX CTC.   |      |                 | RW      |    |    |    |      |    |      |      |      |    |    |          |     |      |  |    |     |     |     |  |    |     |     |     |  |    |

**Table 8-82. KR\_VS\_TP\_GEN\_CONTROL**

| Device Address: 0x01 |                                 | Register Address: 0x8002  |  | Default: 0x0000 |        |
|----------------------|---------------------------------|---|--|-----------------|--------|
| Bit(s)               | Name                            | Description   |  |                 | Access |
| 15:6                 | RESERVED                        | For TI use only. Always reads 0.  |  |                 | RW     |
| 5:4                  | RX_TPG_HLM_TEST_SEL[1:0]<br>(R) | XAUI based test pattern selection on LS side. See Test pattern procedures for more information.<br>00 = High Frequency test pattern(Default 2'b00)<br>01 = Low Frequency test pattern<br>10 = Mixed Frequency test pattern<br>11 = Normal operation |  |                 | RW     |
| 3                    | RX_TPG_CRPAT_TEST_EN<br>(R)     | XAUI based test pattern selection on LS side. See Test pattern procedures for more information.<br>0 = Normal operation. (Default 1'b0)<br>1 = Enables CRPAT test pattern generation  |  |                 | RW     |
| 2                    | RX_TPG_CJPAT_TEST_EN<br>(R)     | XAUI based test pattern selection on LS side. See Test pattern procedures for more information.<br>0 = Normal operation. (Default 1'b0)<br>1 = Enables CJPAT test pattern generation  |  |                 | RW     |
| 1                    | RX_TPG_10GFC_TEST_EN<br>(R)     | XAUI based test pattern selection on LS side. See Test pattern procedures for more information.<br>0 = Normal operation. (Default 1'b0)<br>1 = Enables 10 GFC CJPAT test pattern generation   |  |                 | RW     |
| 0                    | RX_TPG_HLM_TEST_EN<br>(R)       | XAUI based test pattern selection on LS side. See Test pattern procedures for more information.<br>0 = Normal operation. (Default 1'b0)<br>1 = Enables H/L/M test pattern generation  |  |                 | RW     |

**Table 8-83. KR\_VS\_TP\_VER\_CONTROL**

| Device Address: 0x01 |                                 | Register Address: 0x8003  |  | Default: 0x0000 |        |
|----------------------|---------------------------------|---|--|-----------------|--------|
| Bit(s)               | Name                            | Description   |  |                 | Access |
| 15:14                | RESERVED                        | For TI use only. Always reads 0.  |  |                 | RW     |
| 13:12                | TX_TPV_HLM_TEST_SEL[1:0]<br>(R) | XAUI based test pattern selection on LS side. See Test pattern procedures for more information.<br>00 = High Frequency test pattern(Default 2'b00)<br>01 = Low Frequency test pattern<br>10 = Mixed Frequency test pattern<br>11 = Normal operation |  |                 | RW     |

**Table 8-83. KR\_VS\_TP\_VER\_CONTROL (continued)**

| Device Address: 0x01 |                          | Register Address: 0x8003  | Default: 0x0000 |        |
|----------------------|--------------------------|---|-----------------|--------|
| Bit(s)               | Name                     | Description   |                 | Access |
| 11                   | TX_TPV_CRPAT_TEST_EN (R) | XAUI based test pattern selection on LS side. See Test pattern procedures for more information.<br>0 = Normal operation. (Default 1'b0)<br>1 = Enables CRPAT test pattern verification        |                 | RW     |
| 10                   | TX_TPV_CJPAT_TEST_EN (R) | XAUI based test pattern selection on LS side. See Test pattern procedures for more information.<br>0 = Normal operation. (Default 1'b0)<br>1 = Enables CJPAT test pattern verification        |                 | RW     |
| 9                    | TX_TPV_10GFC_TEST_EN (R) | XAUI based test pattern selection on LS side. See Test pattern procedures for more information.<br>0 = Normal operation. (Default 1'b0)<br>1 = Enables 10 GFC CJPAT test pattern verification |                 | RW     |
| 8                    | TX_TPV_HLM_TEST_EN (R)   | XAUI based test pattern selection on LS side. See Test pattern procedures for more information.<br>0 = Normal operation. (Default 1'b0)<br>1 = Enables HL/M test pattern verification         |                 | RW     |
| 7:0                  | RESERVED                 | For TI use only(Default 8'b00000000)  |                 | RW     |

**Table 8-84. KR\_VS\_CTC\_ERR\_CODE\_LN0**

| Device Address: 0x01 |                         | Register Address: 0x8005   | Default: 0xCE00 |        |
|----------------------|-------------------------|--|-----------------|--------|
| Bit(s)               | Name                    | Description  |                 | Access |
| 15:7                 | KR_CTC_ERR_CODE_LN0 (R) | Applicable in 10G-KR mode only. XGMII code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 0 corresponds to 8'h9C with the control bit being 1'b1. The default values for lanes 0~3 correspond to   LF |                 | RW     |
| 6:0                  | RESERVED                | For TI use only. Always reads 0.   |                 | RW     |

**Table 8-85. KR\_VS\_CTC\_ERR\_CODE\_LN1**

| Device Address: 0x01 |                         | Register Address: 0x8006   | Default: 0x0000 |        |
|----------------------|-------------------------|--|-----------------|--------|
| Bit(s)               | Name                    | Description  |                 | Access |
| 15:7                 | KR_CTC_ERR_CODE_LN1 (R) | Applicable in 10G-KR mode only. XGMII code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 1 corresponds to 8'h00 with the control bit being 1'b0. The default values for lanes 0~3 correspond to   LF |                 | RW     |
| 6:0                  | RESERVED                | For TI use only. Always reads 0.   |                 | RW     |

**Table 8-86. KR\_VS\_CTC\_ERR\_CODE\_LN2**

| Device Address: 0x01 |                         | Register Address: 0x8007   | Default: 0x0000 |        |
|----------------------|-------------------------|--|-----------------|--------|
| Bit(s)               | Name                    | Description  |                 | Access |
| 15:7                 | KR_CTC_ERR_CODE_LN2 (R) | Applicable in 10G-KR mode only. XGMII code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 2 corresponds to 8'h00 with the control bit being 1'b0. The default values for lanes 0~3 correspond to   LF |                 | RW     |
| 6:0                  | RESERVED                | For TI use only. Always reads 0.   |                 | RW     |



**Table 8-87. KR\_VS\_CTC\_ERR\_CODE\_LN3**

| Device Address: 0x01 |                         | Register Address: 0x8008   |        | Default: 0x0080 |  |
|----------------------|-------------------------|--|--------|-----------------|--|
| Bit(s)               | Name                    | Description  | Access |                 |  |
| 15:7                 | KR_CTC_ERR_CODE_LN3 (R) | Applicable in 10G-KR mode only. XGMII code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 3 corresponds to 8'h01 with the control bit being 1'b0. The default values for lanes 0~3 correspond to   LF | RW     |                 |  |
| 6:0                  | RESERVED                | For TI use only. Always reads 0.   | RW     |                 |  |

**Table 8-88. KR\_VS\_LN0\_EOP\_ERROR\_COUNTER**

| Device Address: 0x01 |                          | Register Address: 0x8010  |        | Default: 0xFFFF |  |
|----------------------|--------------------------|---|--------|-----------------|--|
| Bit(s)               | Name                     | Description   | Access |                 |  |
| 15:0                 | KR_LN0_EOP_ERR_COUNT (R) | Lane 0 End of packet Error counter. End of packet error is detected when Terminate character is in lane 0 and one or both of the following holds: <ul style="list-style-type: none"> <li>• Terminate character is not followed by /K/ characters in lanes 1, 2 and 3</li> <li>• The column following the terminate column is neither   K   nor   A  .</li> </ul> Counter value cleared to 16'h0000 when read. | COR    |                 |  |

**Table 8-89. KR\_VS\_LN1\_EOP\_ERROR\_COUNTER**

| Device Address: 0x01 |                          | Register Address: 0x8011   |        | Default: 0xFFFF |  |
|----------------------|--------------------------|--|--------|-----------------|--|
| Bit(s)               | Name                     | Description  | Access |                 |  |
| 15:0                 | KR_LN1_EOP_ERR_COUNT (R) | Lane 1 End of packet Error counter. End of packet error is detected when Terminate character is in lane 1 and one or both of the following holds: <ul style="list-style-type: none"> <li>• Terminate character is not followed by /K/ characters in lanes 2 and 3</li> <li>• The column following the terminate column is neither   K   nor   A  .</li> </ul> Counter value cleared to 16'h0000 when read. | COR    |                 |  |

**Table 8-90. KR\_VS\_LN2\_EOP\_ERROR\_COUNTER**

| Device Address: 0x01 |                          | Register Address: 0x8012  |        | Default: 0xFFFF |  |
|----------------------|--------------------------|---|--------|-----------------|--|
| Bit(s)               | Name                     | Description   | Access |                 |  |
| 15:0                 | KR_LN2_EOP_ERR_COUNT (R) | Lane 2 End of packet Error counter. End of packet error is detected when Terminate character is in lane 2 and one or both of the following holds: <ul style="list-style-type: none"> <li>• Terminate character is not followed by /K/ characters in lane 3</li> <li>• The column following the terminate column is neither   K   nor   A  .</li> </ul> Counter value cleared to 16'h0000 when read. | COR    |                 |  |

**Table 8-91. KR\_VS\_LN3\_EOP\_ERROR\_COUNTER**

| Device Address: 0x01 |                          | Register Address: 0x8013   |        | Default: 0xFFFF |  |
|----------------------|--------------------------|--|--------|-----------------|--|
| Bit(s)               | Name                     | Description  | Access |                 |  |
| 15:0                 | KR_LN3_EOP_ERR_COUNT (R) | Lane 3 End of packet Error counter. End of packet error is detected when Terminate character is in lane 3 and the column following the terminate column is neither   K   nor   A  . Counter value cleared to 16'h0000 when read. | COR    |                 |  |

**Table 8-92. KR\_VS\_TX\_CTC\_DROP\_COUNT**

| Device Address: 0x01 |                       | Register Address: 0x8014                              |        | Default: 0xFFFFD |  |
|----------------------|-----------------------|---|--------|------------------|--|
| Bit(s)               | Name                  | Description   | Access |                  |  |
| 15:0                 | TX_CTC_DROP_COUNT (R) | Counter for number of idle drops in the transmit CTC. | COR    |                  |  |

**Table 8-93. KR\_VS\_TX\_CTC\_INSERT\_COUNT**

| Device Address: 0x01 |                      | Register Address: 0x8015                                |        | Default: 0xFFFFD |  |
|----------------------|----------------------|---|--------|------------------|--|
| Bit(s)               | Name                 | Description   | Access |                  |  |
| 15:0                 | TX_CTC_INS_COUNT (R) | Counter for number of idle inserts in the transmit CTC. | COR    |                  |  |

**Table 8-94. KR\_VS\_RX\_CTC\_DROP\_COUNT**

| Device Address: 0x01 |                       | Register Address: 0x8016                             |        | Default: 0xFFFFD |  |
|----------------------|-----------------------|--|--------|------------------|--|
| Bit(s)               | Name                  | Description  | Access |                  |  |
| 15:0                 | RX_CTC_DROP_COUNT (R) | Counter for number of idle drops in the receive CTC. | COR    |                  |  |

**Table 8-95. KR\_VS\_RX\_CTC\_INSERT\_COUNT**

| Device Address: 0x01 |                      | Register Address: 0x8017                               |        | Default: 0xFFFFD |  |
|----------------------|----------------------|--|--------|------------------|--|
| Bit(s)               | Name                 | Description  | Access |                  |  |
| 15:0                 | RX_CTC_INS_COUNT (R) | Counter for number of idle inserts in the receive CTC. | COR    |                  |  |

**Table 8-96. KR\_VS\_STATUS\_1**

| Device Address: 0x01 |                       | Register Address: 0x8018   |        | Default: 0x0000 |  |
|----------------------|-----------------------|--|--------|-----------------|--|
| Bit(s)               | Name                  | Description  | Access |                 |  |
| 15                   | TX_TPV_TP_SYNC (R)    | 0 = Test pattern sync is not achieved on on Tx side<br>1 = Test pattern sync is achieved on on Tx side | RO     |                 |  |
| 11                   | RESERVED              | For TI use only  |        |                 |  |
| 5                    | INVALID_S_COL_ERR (R) | 1 = Indicates invalid start (S) column error detected  | RO/LH  |                 |  |
| 4                    | INVALID_T_COL_ERR (R) | 1 = Indicates invalid terminate (T) column error detected  |        |                 |  |
| 3                    | INVALID_XGMII_LN3 (R) | 1 = Indicates invalid XGMII character detected in Lane 3   |        |                 |  |
| 2                    | INVALID_XGMII_LN2 (R) | 1 = Indicates invalid XGMII character detected in Lane 2   |        |                 |  |
| 1                    | INVALID_XGMII_LN1 (R) | 1 = Indicates invalid XGMII character detected in Lane 1   |        |                 |  |
| 0                    | INVALID_XGMII_LN0 (R) | 1 = Indicates invalid XGMII character detected in Lane 0   |        |                 |  |

**Table 8-97. KR\_VS\_TX\_CRCJ\_ERR\_COUNT\_1**

| Device Address: 0x01 |                                   | Register Address: 0x8019   |        | Default: 0xFFFFF |  |
|----------------------|-----------------------------------|--|--------|------------------|--|
| Bit(s)               | Name                              | Description  | Access |                  |  |
| 15:0                 | TX_TPV_CR_CJ_ERR_COUNT[31:16] (R) | Error Counter for CR/CJ test pattern verification on Tx side. MSBs [31:16] | COR    |                  |  |

**Table 8-98. KR\_VS\_TX\_CRCJ\_ERR\_COUNT\_2**

| Device Address: 0x01      Register Address: 0x801A      Default: 0xFFFFD |                                     |  |        |
|--|-------------------------------------|--|--------|
| Bit(s)   | Name                                | Description  | Access |
| 15:0   | TX_TPV_CR_CJ_ERR_COUNT[15:0]<br>(R) | Error Counter for CR/CJ test pattern verification on Tx side LSBs [15:0] | COR    |

**Table 8-99. KR\_VS\_TX\_LN0\_HLM\_ERR\_COUNT**

| Device Address: 0x01      Register Address: 0x801B      Default: 0xFFFFD |                                   |  |        |
|--|-----------------------------------|--|--------|
| Bit(s)   | Name                              | Description  | Access |
| 15:0   | TX_TPV_LN0_ERR_COUNT[15:0]<br>(R) | Error Counter for H/L/M test pattern verification on Lane 0 of Tx side | COR    |

**Table 8-100. KR\_VS\_TX\_LN1\_HLM\_ERR\_COUNT**

| Device Address: 0x01      Register Address: 0x801C      Default: 0xFFFFD |                                   |  |        |
|--|-----------------------------------|--|--------|
| Bit(s)   | Name                              | Description  | Access |
| 15:0   | TX_TPV_LN1_ERR_COUNT[15:0]<br>(R) | Error Counter for H/L/M test pattern verification on Lane 1 of Tx side | COR    |

**Table 8-101. KR\_VS\_TX\_LN2\_HLM\_ERR\_COUNT**

| Device Address: 0x01      Register Address: 0x801D      Default: 0xFFFFD |                                   |  |        |
|--|-----------------------------------|--|--------|
| Bit(s)   | Name                              | Description  | Access |
| 15:0   | TX_TPV_LN2_ERR_COUNT[15:0]<br>(R) | Error Counter for H/L/M test pattern verification on Lane 2 of Tx side | COR    |

**Table 8-102. KR\_VS\_TX\_LN3\_HLM\_ERR\_COUNT**

| Device Address: 0x01      Register Address: 0x801E      Default: 0xFFFFD |                                   |  |        |
|--|-----------------------------------|--|--------|
| Bit(s)   | Name                              | Description  | Access |
| 15:0   | TX_TPV_LN3_ERR_COUNT[15:0]<br>(R) | Error Counter for H/L/M test pattern verification on Lane 3 of Tx side | COR    |

**Table 8-103. LT\_VS\_CONTROL\_2**

| Device Address: 0x01      Register Address: 0x9001      Default: 0x0000 |                              |  |        |
|---|------------------------------|--|--------|
| Bit(s)  | Name                         | Description  | Access |
| 15:14   | RESERVED                     | For T1 use only (Default 2'b00)  | RW     |
| 13:12   | RESERVED                     | For T1 use only (Default 2'b00)  | RW/SC  |
| 11:9  | AP_SEARCH_MODE[2:0]<br>(RXG) | 000 = Auto search, autotrain disabled (Default 3'b000)<br>001 = Full region search, autotrain disabled<br>010 = Auto search, autotrain enabled<br>011 = Full region search, autotrain enabled<br>1xx = Manual search | RW     |
| 8:0   | RESERVED                     | For T1 use only (Default 9'b000000000)   | RW     |

### 8.3 PCS Registers

The registers below can be accessed only in Clause 45 mode and with device address field set to 0x03 (DEVADD [4:0] = 5'b00011). Valid only when device is in 10GBASE-KR mode.

**Table 8-104. PCS\_CONTROL**

| Device Address: 0x03 |                     | Register Address: 0x0000  | Default: 0x0000 |  |
|----------------------|---------------------|---|-----------------|--|
| Bit(s)               | Name                | Description   | Access          |  |
| 15                   | PCS_RESET<br>(R)    | 1 = Resets datapath and MDIO registers of all channels. Equivalent to asserting RESET_N.<br>0 = Normal operation (Default 1'b0) | RW/SC           |  |
| 14                   | PCS_LOOPBACK<br>(R) | 1 = Enables PCS loopback<br>0 = Normal operation (Default 1'b0)<br>Requires Auto Negotiation and Link Training to be disabled.  | RW              |  |
| 13:12                | RESERVED            | For TI use only. Always reads 0.  | RW              |  |
| 11                   | PCS_LP_MODE<br>(R)  | 1 = Enable power down mode<br>0 = Normal operation (Default 1'b0)   | RW              |  |
| 10:0                 | RESERVED            | For TI use only. Always reads 0.  | RW              |  |

**Table 8-105. PCS\_STATUS\_1**

| Device Address: 0x03 |                       | Register Address: 0x0001  | Default: 0x0002 |  |
|----------------------|-----------------------|---|-----------------|--|
| Bit(s)               | Name                  | Description   | Access          |  |
| 7                    | PCS_FAULT<br>(R)      | 1 = Fault condition detected on either PCS TX or PCS RX<br>0 = No fault condition detected<br>This bit is cleared after Register 03.0008 is read and no fault condition occurs after 03.0008 is read. | RO              |  |
| 2                    | PCS_RX_LINK<br>(R)    | 1 = PCS receive link is up<br>0 = PCS receive link is down  | RO/LL           |  |
| 1                    | PCS_LP_ABILITY<br>(R) | Always reads 1.<br>1 = Supports low power mode<br>0 = Does not support low power mode   | RO              |  |

**Table 8-106. PCS\_STATUS\_2**

| Device Address: 0x03 |                             | Register Address: 0x0008  | Default: 0x8001 |  |
|----------------------|-----------------------------|---|-----------------|--|
| Bit(s)               | Name                        | Description   | Access          |  |
| 15:14                | DEV_PRESENT<br>(R)          | Always reads 2'b10.<br>0x = No device responding at this address<br>10 = Device responding at this address<br>11 = No device responding at this address | RO              |  |
| 11                   | PCS_TX_FAULT<br>(R)         | 1 = Fault condition detected on transmit path<br>0 = No fault condition detected on transmit path   | RO/LH           |  |
| 10                   | PCS_RX_FAULT<br>(R)         | 1 = Fault condition detected on receive path<br>0 = No fault condition detected on receive path   | RO/LH           |  |
| 0                    | PCS_10GBASER_CAPABLE<br>(R) | Always reads 1.<br>1 = PCS is able to support 10GBASE-R PCS type<br>0 = PCS not able to support 10GBASE-R PCS type                                      | RO              |  |

**Table 8-107. KR\_PCS\_STATUS\_1**

| Device Address: 0x03 |                           | Register Address: 0x0020  | Default: 0x0004 |  |
|----------------------|---------------------------|---|-----------------|--|
| Bit(s)               | Name                      | Description   | Access          |  |
| 12                   | PCS_RX_LINK_STATUS<br>(R) | 1 = 10GBASE-R PCS receive link up<br>0 = 10GBASE-R PCS receive link down  | RO              |  |
| 2                    | PCS_PRBS31_ABILITY<br>(R) | Always reads 1.<br>1 = PCS is able to support PRBS31 pattern testing<br>0 = PCS is not able to support PRBS31 testing | RO              |  |

**Table 8-107. KR\_PCS\_STATUS\_1 (continued)**

| Device Address: 0x03 |                       | Register Address: 0x0020   |        | Default: 0x0004 |  |
|----------------------|-----------------------|--|--------|-----------------|--|
| Bit(s)               | Name                  | Description  | Access |                 |  |
| 1                    | PCS_HI_BER<br>(R)     | 1 = High BER condition detected<br>0 = High BER condition not detected   | RO     |                 |  |
| 0                    | PCS_BLOCK_LOCK<br>(R) | 1 = PCS locked to receive blocks<br>0 = PCS not locked to receive blocks | RO     |                 |  |

**Table 8-108. KR\_PCS\_STATUS\_2**

| Device Address: 0x03 |                                 | Register Address: 0x0021  |        | Default: 0x0000 |  |
|----------------------|---------------------------------|---|--------|-----------------|--|
| Bit(s)               | Name                            | Description   | Access |                 |  |
| 15                   | PCS_BLOCK_LOCK_LL<br>(R)        | 1 = PCS locked to receive blocks<br>0 = PCS not locked to receive blocks  | RO/LL  |                 |  |
| 14                   | PCS_HI_BER_LH<br>(R)            | 1 = High BER condition detected<br>0 = High BER condition not detected  | RO/LH  |                 |  |
| 13:8                 | PCS_BER_COUNT[5:0]<br>(R)       | Value indicating number of times BER state machine enters BER_BAD_SH state  | COR    |                 |  |
| 7:0                  | PCS_ERR_BLOCK_COUNT[7:0]<br>(R) | Value indicating number of times RX decode state machine enters RX_E state. Same value is also reflected in 1E.0010 and reading either register clears the counter value. | COR    |                 |  |

**Table 8-109. PCS\_TP\_SEED\_A0**

| Device Address: 0x03 |                            | Register Address: 0x0022      |        | Default: 0x0000 |  |
|----------------------|----------------------------|-------------------------------|--------|-----------------|--|
| Bit(s)               | Name                       | Description                   | Access |                 |  |
| 15:0                 | PCS_TP_SEED_A[15:0]<br>(R) | Test pattern seed A bits 15-0 | RW     |                 |  |

**Table 8-110. PCS\_TP\_SEED\_A1**

| Device Address: 0x03 |                             | Register Address: 0x0023       |        | Default: 0x0000 |  |
|----------------------|-----------------------------|--------------------------------|--------|-----------------|--|
| Bit(s)               | Name                        | Description                    | Access |                 |  |
| 15:0                 | PCS_TP_SEED_A[31:16]<br>(R) | Test pattern seed A bits 31-16 | RW     |                 |  |

**Table 8-111. PCS\_TP\_SEED\_A2**

| Device Address: 0x03 |                             | Register Address: 0x0024       |        | Default: 0x0000 |  |
|----------------------|-----------------------------|--------------------------------|--------|-----------------|--|
| Bit(s)               | Name                        | Description                    | Access |                 |  |
| 15:0                 | PCS_TP_SEED_A[47:32]<br>(R) | Test pattern seed A bits 47-32 | RW     |                 |  |

**Table 8-112. PCS\_TP\_SEED\_A3**

| Device Address: 0x03 |                             | Register Address: 0x0025         |        | Default: 0x0000 |  |
|----------------------|-----------------------------|----------------------------------|--------|-----------------|--|
| Bit(s)               | Name                        | Description                      | Access |                 |  |
| 15:10                | RESERVED                    | For TI use only. Always reads 0. | RW     |                 |  |
| 9:0                  | PCS_TP_SEED_A[57:48]<br>(R) | Test pattern seed A bits 57-48   | RW     |                 |  |

**Table 8-113. PCS\_TP\_SEED\_B0**

| Device Address: 0x03 |                            | Register Address: 0x0026      |        | Default: 0x0000 |  |
|----------------------|----------------------------|-------------------------------|--------|-----------------|--|
| Bit(s)               | Name                       | Description                   | Access |                 |  |
| 15:0                 | PCS_TP_SEED_B[15:0]<br>(R) | Test pattern seed B bits 15-0 | RW     |                 |  |

**Table 8-114. PCS\_TP\_SEED\_B1**

| Device Address: 0x03 |                             | Register Address: 0x0027       | Default: 0x0000 |
|----------------------|-----------------------------|--------------------------------|-----------------|
| Bit(s)               | Name                        | Description                    | Access          |
| 15:0                 | PCS_TP_SEED_B[31:16]<br>(R) | Test pattern seed B bits 31-16 | RW              |

**Table 8-115. PCS\_TP\_SEED\_B2**

| Device Address: 0x03 |                             | Register Address: 0x0028       | Default: 0x0000 |
|----------------------|-----------------------------|--------------------------------|-----------------|
| Bit(s)               | Name                        | Description                    | Access          |
| 15:0                 | PCS_TP_SEED_B[47:32]<br>(R) | Test pattern seed B bits 47-32 | RW              |

**Table 8-116. PCS\_TP\_SEED\_B3**

| Device Address: 0x03 |                             | Register Address: 0x0029         | Default: 0x0000 |
|----------------------|-----------------------------|----------------------------------|-----------------|
| Bit(s)               | Name                        | Description                      | Access          |
| 15:10                | RESERVED                    | For TI use only. Always reads 0. | RW              |
| 9:0                  | PCS_TP_SEED_B[57:48]<br>(R) | Test pattern seed B bits 57-48   | RW              |

**Table 8-117. PCS\_TP\_CONTROL**

| Device Address: 0x03 |                            | Register Address: 0x002A   | Default: 0x0000 |
|----------------------|----------------------------|--|-----------------|
| Bit(s)               | Name                       | Description  | Access          |
| 15:6                 | RESERVED                   | For TI use only. Always reads 0.   | RW              |
| 5                    | PCS_PRBS31_RX_TP_EN<br>(R) | 1 = Enable PRBS31 test pattern verification on receive path<br>0 = Normal operation (Default 1'b0) | RW              |
| 4                    | PCS_PRBS31_TX_TP_EN<br>(R) | 1 = Enable PRBS31 test pattern generation on transmit path<br>0 = Normal operation (Default 1'b0)  | RW              |
| 3                    | PCS_TX_TP_EN<br>(R)        | 1 = Enable transmit test pattern generation<br>0 = Normal operation (Default 1'b0)                 | RW              |
| 2                    | PCS_RX_TP_EN<br>(R)        | 1 = Enable receive test pattern verification<br>0 = Normal operation (Default 1'b0)                | RW              |
| 1                    | PCS_TP_SEL<br>(R)          | 1 = Square wave test pattern<br>0 = Pseudo random test pattern (Default 1'b0)                      | RW              |
| 0                    | PCS_DP_SEL<br>(R)          | 1 = 0'S data pattern<br>0 = LF data pattern (Default 1'b0)   | RW              |

**Table 8-118. PCS\_TP\_ERR\_COUNT**

| Device Address: 0x03 |                               | Register Address: 0x002B   | Default: 0x0000 |
|----------------------|-------------------------------|--|-----------------|
| Bit(s)               | Name                          | Description  | Access          |
| 15:0                 | PCS_TP_ERR_COUNT[15:0]<br>(R) | Test pattern error counter. This counter reflects number of errors occurred during the test pattern mode selected through PCS_TP_CONTROL. In PRBS31 test pattern verification mode, counter value indicates the number of received bytes that have 1 or more bit errors. | COR             |

**Table 8-119. PCS\_VS\_CONTROL**

| Device Address: 0x03 |                     | Register Address: 0x8000  | Default: 0x00B0 |
|----------------------|---------------------|---|-----------------|
| Bit(s)               | Name                | Description   | Access          |
| 15:8                 | RESERVED            | For TI use only. Always reads 0.  | RW              |
| 7:4                  | PCS_SQWAVE_N<br>(R) | Sets number of repeating 0's followed by repeating 1's during square wave test pattern generation mode (Default 4'1011) | RW              |
| 3                    | RESERVED            | For TI use only (Default 1'b0)  | RW              |

**Table 8-119. PCS\_VS\_CONTROL (continued)**

| Device Address: 0x03 |                          | Register Address: 0x8000   | Default: 0x00B0 |        |
|----------------------|--------------------------|--|-----------------|--------|
| Bit(s)               | Name                     | Description  |                 | Access |
| 2                    | PCS_RX_DEC_CTRL_CHAR (R) | PCS RX Decode control character selection. Determines what control characters are passed<br>0 = A/K/R control characters are changed to Idles. Reserved characters passed through (Default 1'b0)<br>1 = A/K/R control characters are passed through as is RW |                 | RW     |
| 1                    | PCS_DESCR_DISABLE (R)    | De-scrambler control in 10GKR RX PCS<br>1 = Disable descrambler<br>0 = Enable descrambler (Default 1'b0)   |                 | RW     |
| 0                    | PCS_SCR_DISABLE (R)      | Scrambler control in 10GKR TX PCS<br>1 = Disable scrambler<br>0 = Enable scrambler (Default 1'b0)  |                 | RW     |

**Table 8-120. PCS\_VS\_STATUS**

| Device Address: 0x03 |                       | Register Address: 0x8010  | Default: 0x00FD |        |
|----------------------|-----------------------|---|-----------------|--------|
| Bit(s)               | Name                  | Description   |                 | Access |
| 13                   | UNCORR_ERR_STATUS (R) | 1 = Uncorrectable block error found   |                 | RO/LH  |
| 12                   | CORR_ERR_STATUS (R)   | 1 = Correctable block error found   |                 | RO/LH  |
| 8                    | PCS_TP_ERR (R)        | PCS test pattern verification status PCS_SCR_DISABLE<br>1 = Error occurred during pseudo random test pattern verification<br>Number of errors can be checked by reading PCS_TP_ERR_COUNT (03.002B) register |                 | RO/LH  |
| 7:0                  | RESERVED              | For TI use only.  |                 | COR    |

## 8.4 Auto-Negotiation Registers

The registers below can be accessed only in Clause 45 mode and with device address field set to 0x07 (DA[4:0] = 5'b00111)

**Table 8-121. AN\_CONTROL**

| Device Address: 0x07 |                 | Register Address: 0x0000  | Default: 0x3000 |                      |
|----------------------|-----------------|---|-----------------|----------------------|
| Bit(s)               | Name            | Description   |                 | Access               |
| 15                   | AN_RESET (RX)   | 1 = Resets Auto Negotiation<br>0 = Normal operation (Default 1'b0)  |                 | RW/SC                |
| 14                   | RESERVED        | For TI use only. Always reads 0.  |                 | RW                   |
| 13                   | RESERVED        | For TI use only (Default 1'b1)  |                 | RW                   |
| 12                   | AN_ENABLE (RX)  | 1 = Enable Auto Negotiation (Default 1'b1)<br>0 = Disable Auto Negotiation  |                 | RW                   |
| 11:10                | RESERVED        | For TI use only. Always reads 0.  |                 | RW                   |
| 9                    | AN_RESTART (RX) | 1 = Restart Auto Negotiation<br>0 = Normal operation (Default 1'b0)<br>If set, a read of this register is required to clear AN_RESTART bit. |                 | RW/SC <sup>(1)</sup> |
| 8:0                  | RESERVED        | For TI use only. Always reads 0.  |                 | RW                   |

(1) If set, a read of register 07.0000 is required to clear AN\_RESTART bit.

**Table 8-122. AN\_STATUS**

| Device Address: 0x07 |                       | Register Address: 0x0001   | Default: 0x0088 |        |
|----------------------|-----------------------|--|-----------------|--------|
| Bit(s)               | Name                  | Description  |                 | Access |
| 9                    | AN_PAR_DET_FAULT (RX) | 1 = Fault has been detected via parallel detection function<br>0 = Fault has not been detected via parallel detection function |                 | RO/LH  |
| 7                    | AN_EXP_NP_STATUS (RX) | 1 = Extended next page is used<br>0 = Extended next page is not allowed  |                 | RO     |

**Table 8-122. AN\_STATUS (continued)**

| Device Address: 0x07 |                       | Register Address: 0x0001   | Default: 0x0088 |        |
|----------------------|-----------------------|--|-----------------|--------|
| Bit(s)               | Name                  | Description  |                 | Access |
| 6                    | AN_PAGE_RCVD<br>(RX)  | 1 = A page has been received<br>0 = A page has not been received   |                 | RO/LH  |
| 5                    | AN_COMPLETE<br>(RX)   | 1 = Auto Negotiation process is completed<br>0 = Auto Negotiation process not completed                              |                 | RO     |
| 4                    | REMOTE_FAULT<br>(RX)  | 1 = Remote fault detected by AN<br>0 = Remote fault not detected by AN   |                 | RO/LH  |
| 3                    | AN_ABILITY<br>(RX)    | Always reads 1.<br>1 = Device is able to perform Auto Negotiation<br>0 = Device not able to perform Auto Negotiation |                 | RO     |
| 2                    | LINK_STATUS<br>(RX)   | 1 = Link is up<br>0 = Link is down   |                 | RO/LL  |
| 0                    | AN_LP_ABILITY<br>(RX) | 1 = LP is able to perform Auto Negotiation<br>0 = LP not able to perform Auto Negotiation                            |                 | RO     |

**Table 8-123. AN\_DEV\_PACKAGE**

| Device Address: 0x07 |                    | Register Address: 0x0005   | Default: 0x0080 |        |
|----------------------|--------------------|--|-----------------|--------|
| Bit(s)               | Name               | Description  |                 | Access |
| 7                    | AN_PRESENT<br>(RX) | Always reads 1<br>1 = Auto Negotiation present in the package<br>0 = Auto Negotiation not present in the package |                 | RO     |

**Table 8-124. AN\_ADVERTISEMENT\_1**

| Device Address: 0x07 |                            | Register Address: 0x0010   | Default: 0x1001 |        |
|----------------------|----------------------------|--|-----------------|--------|
| Bit(s)               | Name                       | Description  |                 | Access |
| 15                   | AN_NEXT_PAGE<br>(RX)       | NP bit (D15) in base link codeword<br>1 = Next page available<br>0 = Next page not available (Default 1'b0)  |                 | RW     |
| 14                   | AN_ACKNOWLEDGE<br>(RX)     | Acknowledge bit (D14) in base link codeword. Always reads 0.   |                 | RO     |
| 13                   | AN_REMOTE_FAULT<br>(RX)    | RF bit (D13) in base link codeword<br>1 = Sets RF bit to 1<br>0 = Normal operation (Default 1'b0)  |                 | RW     |
| 12:10                | AN_CAPABILITY[2:0]<br>(RX) | Value to be set in D12:D10 bits of the base link codeword. Consists of abilities like PAUSE, ASM_DIR (Default 3'b100)  |                 | RW     |
| 9:5                  | AN_ECHO_NONCE[4:0]<br>(RX) | Value to be set in D9:D5 bits of the base link codeword. Consists of Echo nonce value. Transmitted in base page only until local device and link Partner have exchanged unique Nonce values, at which time transmitted Echoed Nonce will change to Link Partner's Nonce value. Read value always reflects the value written, not the actual Echoed Nonce. (Default 5'b00000) |                 | RW     |
| 4:0                  | AN_SELECTOR[4:0]<br>(RX)   | Value to be set in D4:D0 bits of the base link codeword. Consists of selector field value (Default 5'b00001)   |                 | RW     |

**Table 8-125. AN\_ADVERTISEMENT\_2**

| Device Address: 0x07 |                          | Register Address: 0x0011  | Default: 0x0080 |        |
|----------------------|--------------------------|---|-----------------|--------|
| Bit(s)               | Name                     | Description   |                 | Access |
| 15:8                 | AN_ABILITY[10:3]<br>(RX) | Value to be set in D31:D24 bits of the base link codeword. Consists of technology ability field bits [10:3] (Default 9'b000000000)                                  |                 | RW     |
| 7                    | AN_ABILITY[2]<br>(RX)    | Value to be set in D23 bits of the base link codeword. Consists of technology ability field bits [2]. When set, indicates device supports 10GBASE-KR (Default 1'b1) |                 | RW     |
| 6                    | AN_ABILITY[1]<br>(RX)    | Value to be set in D22 bits of the base link codeword. Consists of technology ability field bits [1]. Always set to 0 (Default 1'b0)                                |                 | RW     |



**Table 8-125. AN\_ADVERTISEMENT\_2 (continued)**

| Device Address: 0x07 |                                   | Register Address: 0x0011  | Default: 0x0080 |        |
|----------------------|-----------------------------------|---|-----------------|--------|
| Bit(s)               | Name                              | Description   |                 | Access |
| 5                    | AN_ABILITY[0]<br>(RX)             | Value to be set in D21 bits of the base link codeword. Consists of technology ability field bit [0]. When set, indicates device supports 1000BASE-KX (Default 1'b0)               |                 | RW     |
| 4:0                  | AN_TRANS_NONCE_FIELD[4:0]<br>(RX) | Not used. Transmitted Nonce field is generated by hardware random number generator. Read value always reflects value written, not the actual Transmitted Nonce (Default 5'b00000) |                 | RW     |

**Table 8-126. AN\_ADVERTISEMENT\_3**

| Device Address: 0x07 |                           | Register Address: 0x0012   | Default: 0x4000 |        |
|----------------------|---------------------------|--|-----------------|--------|
| Bit(s)               | Name                      | Description  |                 | Access |
| 15                   | AN_FEC_REQUESTED<br>(RX)  | Value to be set in D47 bits of the base link codeword. When set, indicates a request to enable FEC on the link (Default 1'b0)              |                 | RW     |
| 14                   | AN_FEC_ABILITY<br>(RX)    | Value to be set in D46 bits of the base link codeword. When set, indicates 10GBASE-KR has FEC ability (Default 1'b1)                       |                 |        |
| 13:0                 | AN_ABILITY[24:11]<br>(RX) | Value to be set in D45:D32 bits of the base link codeword. Consists of technology ability field bits [24:11] (Default 14'b000000000000000) |                 |        |

**Table 8-127. AN\_LP\_ADVERTISEMENT\_1<sup>(1)</sup>**

| Device Address: 0x07 |                             | Register Address: 0x0013   | Default: 0x0001 |        |
|----------------------|-----------------------------|--|-----------------|--------|
| Bit(s)               | Name                        | Description  |                 | Access |
| 15                   | AN_LP_NEXT_PAGE<br>(RX)     | NP bit (D15) in link partner base page<br>1 = Next page available in link partner<br>0 = Next page not available in link partner     |                 | RO     |
| 14                   | AN_LP_ACKNOWLEDGE<br>(RX)   | Acknowledge bit (D14) in link partner base page.   |                 | RO     |
| 13                   | AN_LP_REMOTE_FAULT<br>(RX)  | RF bit (D13) in link partner base page<br>1 = Remote fault detected in link partner<br>0 = Remote fault not detected in link partner |                 | RO     |
| 12:10                | AN_LP_CAPABILITY<br>(RX)    | D12:D10 bits of the link partner base page. Consists of abilities like PAUSE, ASM_DIR  |                 | RO     |
| 9:5                  | AN_LP_ECHO_NONCE<br>(RX)    | D9:D5 bits of the link partner base page. Consists of Echo nonce value   |                 | RO     |
| 4:0                  | AN_LP_SELECTOR[4:0]<br>(RX) | D4:D0 bits of the link partner base page. Consists of selector field value Always reads 5'b00001                                     |                 | RO     |

(1) To get accurate AN\_LP\_ADVERTISEMENT read value, Register 07.0013 should be read first before reading 07.0014 and 07.0015

**Table 8-128. AN\_LP\_ADVERTISEMENT\_2**

| Device Address: 0x07 |                                 | Register Address: 0x0014   | Default: 0x0000 |        |
|----------------------|---------------------------------|--|-----------------|--------|
| Bit(s)               | Name                            | Description  |                 | Access |
| 15:8                 | AN_LP_ABILITY[10:3]<br>(RX)     | D31:D24 bits of the link partner base page. Consists of technology ability field bits [10:3]   |                 | RO     |
| 7                    | AN_LP_ABILITY[2]<br>(RX)        | D23 bits of the link partner base page. Consists of technology ability field bits [2]. When high, indicates link partner supports 10GBASE-KR |                 |        |
| 6                    | AN_LP_ABILITY[1]<br>(RX)        | D22 bits of the link partner base page. Consists of technology ability field bits [1].   |                 |        |
| 5                    | AN_LP_ABILITY[0]<br>(RX)        | D21 bits of the link partner base page. Consists of technology ability field bit [0]. When high, indicates link partner supports 1000BASE-KX |                 |        |
| 4:0                  | AN_LP_TRANS_NONCE_FIELD<br>(RX) | D20:D16 bits of the link partner base page. Consists of transmitted nonce value  |                 |        |

**Table 8-129. AN\_LP\_ADVERTISEMENT\_3**

| Device Address: 0x07 |                           | Register Address: 0x0015  |        | Default: 0x0000 |  |
|----------------------|---------------------------|---|--------|-----------------|--|
| Bit(s)               | Name                      | Description   | Access |                 |  |
| 15                   | AN_LP_FEC_REQUESTED (RX)  | D47 bits of the link partner base page. When high, indicates link partner request to enable FEC on the link | RO     |                 |  |
| 14                   | AN_LP_FEC_ABILITY (RX)    | D46 bits of the link partner base page. When high, indicates link partner has FEC ability                   |        |                 |  |
| 13:0                 | AN_LP_ABILITY[24:11] (RX) | D45:D32 bits of the link partner base page. Consists of link partner technology ability field bits [24:11]  |        |                 |  |

**Table 8-130. AN\_XNP\_TRANSMIT\_1**

| Device Address: 0x07 |                       | Register Address: 0x0016  |        | Default: 0x2000 |  |
|----------------------|-----------------------|---|--------|-----------------|--|
| Bit(s)               | Name                  | Description   | Access |                 |  |
| 15                   | AN_XNP_NEXT_PAGE (RX) | NP bit (D15) in next page code word<br>1 = Next page available<br>0 = Next page not available (Default 1'b0)  | RW     |                 |  |
| 14                   | RESERVED              | Always reads 0.   | RO     |                 |  |
| 13                   | AN_MP (RX)            | Message page bit (D13) in next page code word<br>1 = Sets MP bit to 1 indicating next page is a message page (Default 1'b1)<br>0 = Sets MP bit to 0 indicating next page is unformatted next page | RW     |                 |  |
| 12                   | AN_ACKNOWLEDGE_2 (RX) | Value to be set in D12 bit of the next page code word. When set, indicates device is able to act on the information defined in the message (Default 1'b0)   | RW     |                 |  |
| 11                   | AN_TOGGLE (RX)        | Not used. Toggle value is generated by hardware. Read value always reflects value written, not the actual Toggle field (Default 1'b0)   | RW     |                 |  |
| 10:0                 | AN_CODE_FIELD (RX)    | Value to be set in D10:D0 bits of the next page code word. Consists of Message/Unformatted code field value (Default 11'b000000000000)  | RW     |                 |  |

**Table 8-131. AN\_XNP\_TRANSMIT\_2**

| Device Address: 0x07 |                    | Register Address: 0x0017  |        | Default: 0x0000 |  |
|----------------------|--------------------|---|--------|-----------------|--|
| Bit(s)               | Name               | Description   | Access |                 |  |
| 15:0                 | AN_MSG_CODE_1 (RX) | Value to be set in D31:D16 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000) | RW     |                 |  |

**Table 8-132. AN\_XNP\_TRANSMIT\_3**

| Device Address: 0x07 |                    | Register Address: 0x0018  |        | Default: 0x0000 |  |
|----------------------|--------------------|---|--------|-----------------|--|
| Bit(s)               | Name               | Description   | Access |                 |  |
| 15:0                 | AN_MSG_CODE_2 (RX) | Value to be set in D47:D32 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000) | RW     |                 |  |

**Table 8-133. AN\_LP\_XNP\_ABILITY\_1<sup>(1)</sup>**

| Device Address: 0x07 |                            | Register Address: 0x0019  |        | Default: 0x0000 |  |
|----------------------|----------------------------|---|--------|-----------------|--|
| Bit(s)               | Name                       | Description   | Access |                 |  |
| 15                   | AN_LP_XNP_NEXT_PAGE (RX)   | NP bit (D15) in next page code word<br>1 = Next page available<br>0 = Next page not available (Default 1'b0)  | RO     |                 |  |
| 14                   | AN_LP_XNP_ACKNOWLEDGE (RX) | Value in D14 bit of the next page code word. When set, indicates device is able to act on the information defined in the message (Default 1'b0)   | RO     |                 |  |
| 13                   | AN_LP_MP (RX)              | Message page bit (D13) in next page code word<br>1 = Sets MP bit to 1 indicating next page is a message page<br>0 = Sets MP bit to 0 indicating next page is unformatted next page (Default 1'b0) | RO     |                 |  |
| 12                   | AN_LP_ACKNOWLEDGE_2 (RX)   | Value in D12 bit of the next page code word. When set, indicates device is able to act on the information defined in the message (Default 1'b0)   | RO     |                 |  |

(1) To get accurate AN\_LP\_XNP\_ABILITY read value, Register 07.0019 should be read first before reading 07.001A and 07.001B

**Table 8-133. AN\_LP\_XNP\_ABILITY\_1<sup>(1)</sup> (continued)**

| Device Address: 0x07 |                          | Register Address: 0x0019   | Default: 0x0000 |        |
|----------------------|--------------------------|--|-----------------|--------|
| Bit(s)               | Name                     | Description  |                 | Access |
| 11                   | AN_LP_TOGGLE<br>(RX)     | Value of D11 bit of the next page code word. Consists of Toggle field value(Default 1'b0)                                    |                 | RO     |
| 10:0                 | AN_LP_CODE_FIELD<br>(RX) | Value in D10:D0 bits of the next page code word. Consists of Message/Unformatted code field value (Default 11'b000000000000) |                 | RO     |

**Table 8-134. AN\_LP\_XNP\_ABILITY\_2**

| Device Address: 0x07 |                          | Register Address: 0x001A  | Default: 0x0000 |        |
|----------------------|--------------------------|---|-----------------|--------|
| Bit(s)               | Name                     | Description   |                 | Access |
| 15:0                 | AN_LP_MSG_CODE_1<br>(RX) | Value to be set in D31:D16 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000) |                 | RO     |

**Table 8-135. AN\_LP\_XNP\_ABILITY\_3**

| Device Address: 0x07 |                          | Register Address: 0x001B  | Default: 0x0000 |        |
|----------------------|--------------------------|---|-----------------|--------|
| Bit(s)               | Name                     | Description   |                 | Access |
| 15:0                 | AN_LP_MSG_CODE_2<br>(RX) | Value to be set in D47:D32 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000) |                 | RO     |

**Table 8-136. AN\_BP\_STATUS**

| Device Address: 0x07 |                          | Register Address: 0x0030  | Default: 0x0001 |        |
|----------------------|--------------------------|---|-----------------|--------|
| Bit(s)               | Name                     | Description   |                 | Access |
| 4                    | AN_10G_KR_FEC<br>(RX)    | 1 = PMA/PMD is negotiated to perform 10GBASE-KR FEC                     |                 | RO     |
| 3                    | AN_10G_KR<br>(RX)        | 1 = PMA/PMD is negotiated to perform 10GBASE-KR                         |                 |        |
| 1                    | AN_1G_KX<br>(RX)         | 1 = PMA/PMD is negotiated to perform 1000BASE-KX                        |                 |        |
| 0                    | AN_BP_AN_ABILITY<br>(RX) | Always reads 1.<br>1 = Indicates 1000BASE-KX, 10GBASE-KR is implemented |                 |        |

**Table 8-137. TI\_Reserved Control and Status Registers**

| Register Name       | Register Address | Default Value | Access |  | Register Name       | Register Address | Default Value | Access |
|---------------------|------------------|---------------|--------|--|---------------------|------------------|---------------|--------|
| TI_RESERVED_CONTROL | 1E.8000          | 0x04C0        | RW     |  | TI_RESERVED_STATUS  | 1E.A014          | 0x0000        | RO     |
| TI_RESERVED_CONTROL | 1E.8001          | 0x0207        | RW     |  | TI_RESERVED_STATUS  | 1E.A015          | 0x0000        | RO     |
| TI_RESERVED_CONTROL | 1E.8002          | 0x02FE        | RW     |  | TI_RESERVED_STATUS  | 1E.A016          | 0x0000        | RO     |
| TI_RESERVED_CONTROL | 1E.8005          | 0x0000        | RW     |  | TI_RESERVED_STATUS  | 1E.A017          | 0x0000        | RO     |
| TI_RESERVED_CONTROL | 1E.8006          | 0x0000        | RW     |  | TI_RESERVED_STATUS  | 1E.A018          | 0x0000        | RO     |
| TI_RESERVED_CONTROL | 1E.8007          | 0x8000        | RW     |  | TI_RESERVED_CONTROL | 1E.A116          | 0x0000        | RW     |
| TI_RESERVED_CONTROL | 1E.8008          | 0x0000        | RW     |  | TI_RESERVED_CONTROL | 1E.A117          | 0x0000        | RW     |
| TI_RESERVED_CONTROL | 1E.8009          | 0xFC00        | RW     |  | TI_RESERVED_STATUS  | 1E.A118          | 0x0000        | RO     |
| TI_RESERVED_CONTROL | 1E.800A          | 0xBC3C        | RW     |  | TI_RESERVED_STATUS  | 1E.A119          | 0x0000        | RO     |
| TI_RESERVED_CONTROL | 1E.800B          | 0x0000        | RW     |  | TI_RESERVED_CONTROL | 01.8000          | 0x4800        | RW     |
| TI_RESERVED_CONTROL | 1E.800C          | 0x0000        | RW     |  | TI_RESERVED_STATUS  | 01.801F          | 0xFFFFD       | COR    |
| TI_RESERVED_CONTROL | 1E.800D          | 0x01FC        | RW     |  | TI_RESERVED_STATUS  | 01.8020          | 0xFFFFD       | COR    |
| TI_RESERVED_CONTROL | 1E.800E          | 0x0000        | RW     |  | TI_RESERVED_STATUS  | 01.8021          | 0xFFFFD       | COR    |
| TI_RESERVED_CONTROL | 1E.800F          | 0x00C0        | RW     |  | TI_RESERVED_STATUS  | 01.8022          | 0xFFFFD       | COR    |
| TI_RESERVED_CONTROL | 1E.8011          | 0x7F00        | RW     |  | TI_RESERVED_STATUS  | 01.8023          | 0xFFFFF       | COR    |
| TI_RESERVED_STATUS  | 1E.8012          | 0xFFFFD       | COR    |  | TI_RESERVED_STATUS  | 01.8024          | 0xFFFFD       | COR    |

**Table 8-137. TI\_Reserved Control and Status Registers (continued)**

| Register Name       | Register Address | Default Value | Access | Register Name       | Register Address | Default Value | Access |
|---------------------|------------------|---------------|--------|---------------------|------------------|---------------|--------|
| TI_RESERVED_STATUS  | 1E.8013          | 0xFFFFD       | COR    | TI_RESERVED_CONTROL | 01.9000          | 0x0249        | RW     |
| TI_RESERVED_STATUS  | 1E.8014          | 0x0000        | RO/LH  | TI_RESERVED_CONTROL | 01.9002          | 0x1335        | RW     |
| TI_RESERVED_STATUS  | 1E.8015          | 0x0000        | RO     | TI_RESERVED_CONTROL | 01.9003          | 0x5E29        | RW     |
| TI_RESERVED_CONTROL | 1E.8019          | 0xFC00        | RW     | TI_RESERVED_CONTROL | 01.9004          | 0x007F        | RW     |
| TI_RESERVED_CONTROL | 1E.801A          | 0xBC3C        | RW     | TI_RESERVED_CONTROL | 01.9005          | 0x1C00        | RW     |
| TI_RESERVED_CONTROL | 1E.801C          | 0x0000        | RW     | TI_RESERVED_CONTROL | 01.9006          | 0x0000        | RW     |
| TI_RESERVED_CONTROL | 1E.801D          | 0x01FC        | RW     | TI_RESERVED_CONTROL | 01.9007          | 0x5120        | RW     |
| TI_RESERVED_CONTROL | 1E.801E          | 0x0000        | RW     | TI_RESERVED_CONTROL | 01.9008          | 0xC018        | RW     |
| TI_RESERVED_CONTROL | 1E.801F          | 0x00C0        | RW     | TI_RESERVED_CONTROL | 01.9009          | 0xE667        | RW     |
| TI_RESERVED_CONTROL | 1E.8020          | 0x0200        | RW     | TI_RESERVED_CONTROL | 01.900A          | 0x5E8F        | RW     |
| TI_RESERVED_CONTROL | 1E.8022          | 0x0000        | RW     | TI_RESERVED_CONTROL | 01.900B          | 0xAFAF        | RW     |
| TI_RESERVED_CONTROL | 1E.8023          | 0x0000        | RW     | TI_RESERVED_CONTROL | 01.900C          | 0x0800        | RW     |
| TI_RESERVED_CONTROL | 1E.8024          | 0x0000        | RW     | TI_RESERVED_CONTROL | 01.900D          | 0x461A        | RW     |
| TI_RESERVED_CONTROL | 1E.8025          | 0xF000        | RW     | TI_RESERVED_CONTROL | 01.900E          | 0x1723        | RW     |
| TI_RESERVED_STATUS  | 1E.8030          | 0x0000        | RO     | TI_RESERVED_CONTROL | 01.900F          | 0x7003        | RW     |
| TI_RESERVED_STATUS  | 1E.8031          | 0x0000        | RO     | TI_RESERVED_CONTROL | 01.9010          | 0x0851        | RW     |
| TI_RESERVED_STATUS  | 1E.8032          | 0x0000        | RO     | TI_RESERVED_CONTROL | 01.9011          | 0x1EFF        | RW     |
| TI_RESERVED_STATUS  | 1E.8033          | 0x0000        | RO     | TI_RESERVED_STATUS  | 01.9020          | 0x0000        | RO     |
| TI_RESERVED_STATUS  | 1E.8034          | 0x0000        | RO     | TI_RESERVED_STATUS  | 01.9021          | 0xFFFFD       | COR    |
| TI_RESERVED_STATUS  | 1E.8035          | 0x0000        | RO     | TI_RESERVED_STATUS  | 01.9022          | 0x0000        | RO     |
| TI_RESERVED_CONTROL | 1E.8050          | 0x0000        | RW     | TI_RESERVED_STATUS  | 01.9023          | 0x0000        | RO     |
| TI_RESERVED_CONTROL | 1E.8102          | 0xF280        | RW     | TI_RESERVED_STATUS  | 01.9024          | 0x0000        | RO     |
| TI_RESERVED_CONTROL | 1E.A000          | 0x0000        | RW     | TI_RESERVED_STATUS  | 01.9025          | 0x0000        | RO     |
| TI_RESERVED_STATUS  | 1E.A010          | 0x0000        | RO     | TI_RESERVED_STATUS  | 01.9026          | 0x0000        | RO     |
| TI_RESERVED_STATUS  | 1E.A011          | 0x0000        | RO     | TI_RESERVED_STATUS  | 01.9027          | 0x0000        | RO     |
| TI_RESERVED_STATUS  | 1E.A012          | 0x0000        | RO     | TI_RESERVED_STATUS  | 01.9028          | 0x0000        | RO     |
| TI_RESERVED_STATUS  | 1E.A013          | 0x0000        | RO     | TI_RESERVED_STATUS  | 01.9029          | 0x0000        | RO     |

## 9 ELECTRICAL CHARACTERISTICS

### 9.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)(2)</sup>

|   |   | VALUE |              | UNIT |
|---|---|-------|--------------|------|
|   |   | MIN   | MAX          |      |
| Supply voltage                                      | DVDD, VDDA_LS/HS, VDDT_LS/HS, VPP, VDDD | -0.3  | 1.4          | V    |
|   | VDDRA/B_LS/HS, VDDO[1:0]                | -0.3  | 2.2          | V    |
| Input Voltage, V <sub>I</sub> , (LVCMOS/CML/Analog) |   | -0.3  | Supply + 0.3 | V    |
| Storage temperature                                 |   | -65   | 150          | °C   |
| Operating Junction Temperature                      |   |       | 105          | °C   |
| Electrostatic Discharge:                            | HBM                                     |       | 1            | kV   |
|   | CDM                                     |       | 500          | V    |
| Characterized free-air operating temperature range  |   | -40   | 85           | °C   |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground (VSS).

### 9.2 Recommended Operating Conditions

| PARAMETER   |   | TEST CONDITIONS  | MIN   | NOM  | MAX   | UNIT |
|---|---|--|-------|------|-------|------|
| Digital / analog supply voltages                    | VDDD, VDDA_LS/HS, DVDD, VDDT_LS/HS, VPP |  | 0.95  | 1.00 | 1.05  | V    |
| SERDES PLL regulator voltage                        | VDDRA_LS/HS, VDDRB_LS/HS                | 1.5V Nominal   | 1.425 | 1.5  | 1.575 | V    |
|   |   | 1.8V Nominal   | 1.71  | 1.8  | 1.89  |      |
| LVCMOS I/O supply voltage                           | VDDO[1:0]                               | 1.5V Nominal   | 1.425 | 1.5  | 1.575 | V    |
|   |   | 1.8V Nominal   | 1.71  | 1.8  | 1.89  |      |
| I <sub>DD</sub> Supply current                      | VDDD                                    | 10.3 Gbps  |       |      | 650   | mA   |
|   | VDDA_LS/HS                              |  |       |      | 650   |      |
|   | DVDD + VPP                              |  |       |      | 700   |      |
|   | VDDT_LS/HS                              |  |       |      | 600   |      |
|   | VDDRA/B_LS                              |  |       |      | 70    |      |
|   | VDDRA/B_HS                              |  |       |      | 70    |      |
|   | VDDO[1:0]                               |  |       |      | 10    |      |
| P <sub>D</sub> Power dissipation                    |   | Nominal  |       | 1.6  |       | W    |
|   |   | Worst case supply voltage, temperature, and process. 10GBASE-KR, Both channels active, default swing and Clkout settings |       |      | 2.3   |      |
| I <sub>SD</sub> Shutdown current                    | VDDD                                    | PD* Asserted   |       |      | 300   | mA   |
|   | VDDA                                    |  |       |      | 85    |      |
|   | DVDD + VPP                              |  |       |      | 250   |      |
|   | VDDT                                    |  |       |      | 65    |      |
|   | VDDRA_HS/LS + VDDRB_HS/LS               |  |       |      | 7     |      |
|   | VDDO                                    |  |       |      | 5     |      |
| J <sub>R</sub> REFCLK0P/N, REFCLK1P/N Random Jitter |   | 12kHz to 20MHz   |       |      | 1     | ps   |

### 9.3 High Speed Side Serial Transmitter Characteristics

| PARAMETER                       | TEST CONDITIONS   | MIN  | NOM  | MAX  | UNIT             |                  |
|---------------------------------|---|--|------|--|------------------|------------------|
| V <sub>OD(p-p)</sub>            | TX Output differential peak-to-peak voltage swing, transmitter enabled                | SWING = 0000   | 50   | 130  | 220              | mV <sub>pp</sub> |
|                                 |   | SWING = 0001   | 110  | 220  | 320              |                  |
|                                 |   | SWING = 0010   | 180  | 300  | 430              |                  |
|                                 |   | SWING = 0011   | 250  | 390  | 540              |                  |
|                                 |   | SWING = 0100   | 320  | 480  | 650              |                  |
|                                 |   | SWING = 0101   | 390  | 570  | 770              |                  |
|                                 |   | SWING = 0110   | 460  | 660  | 880              |                  |
|                                 |   | SWING = 0111   | 530  | 750  | 1000             |                  |
|                                 |   | SWING = 1000   | 590  | 830  | 1100             |                  |
|                                 |   | SWING = 1001   | 660  | 930  | 1220             |                  |
|                                 |   | SWING = 1010   | 740  | 1020   | 1320             |                  |
|                                 |   | SWING = 1011   | 820  | 1110   | 1430             |                  |
|                                 |   | SWING = 1100   | 890  | 1180   | 1520             |                  |
|                                 |   | SWING = 1101   | 970  | 1270   | 1610             |                  |
|                                 |   | SWING = 1110   | 1060 | 1340   | 1680             |                  |
|                                 | SWING = 1111  | 1090   | 1400 | 1740   |                  |                  |
|                                 | Transmitter disabled  |  |      | 30   |                  |                  |
| V <sub>pre/post</sub>           | TX Output pre/post cursor emphasis voltage  | See register bits TWPOST1, TWPOST2, and TWPRE for de-emphasis settings. See <a href="#">Figure 9-2</a> |      | -17.5/<br>-37.5%                               | +17.5/<br>+37.5% |                  |
| V <sub>CMT</sub>                | TX Output common mode voltage   | 100-Ω differential termination. DC-coupled.  |      | V <sub>DDT</sub> - 0.25 * V <sub>OD(p-p)</sub> |                  | mV               |
| t <sub>skew</sub>               | Intra-pair output skew  | Serial Rate = 9.8304 Gbps  |      | 0.045  |                  | UI               |
| T <sub>r</sub> , T <sub>f</sub> | Differential output signal rise, fall time (20% to 80%), Differential Load = 100Ω     | 24   |      |  |                  | ps               |
| J <sub>T1</sub>                 | Serial output total jitter (CPRI LV/LV-II/LV-III, OBSAI and 10GBASE-KR Rates)         | Serial Rate ≤ 3.072Gbps  |      | 0.35   |                  | UI <sub>pp</sub> |
|                                 |   | Serial Rate > 3.072Gbps  |      | 0.28   |                  |                  |
| J <sub>D1</sub>                 | Serial output deterministic jitter (CPRI LV/LV-II/LV-III, OBSAI and 10GBASE-KR Rates) | Serial Rate ≤ 3.072Gbps  |      | 0.17   |                  | UI <sub>pp</sub> |
|                                 |   | Serial Rate > 3.072Gbps  |      | 0.15   |                  |                  |
| J <sub>R1</sub>                 | Serial output random jitter (CPRI LV/LV-II/LV-III, OBSAI and 10GBASE-KR Rates)        | Serial Rate > 3.072Gbps  |      | 0.15   |                  | UI <sub>pp</sub> |
| J <sub>T2</sub>                 | Serial output total jitter (CPRI E.12.HV)   | Serial Rate = 1.2288Gbps   |      | 0.279  |                  | UI <sub>pp</sub> |
| J <sub>D2</sub>                 | Serial output deterministic jitter (CPRI E.12.HV)                                     |  |      | 0.14   |                  |                  |
| SDD22                           | Differential output return loss   | 50 MHz < f < 2.5 GHz   |      | 9  |                  | dB               |
|                                 |   | 2.5 GHz < f < 7.5 GHz  |      | See <sup>(1)</sup>                             |                  |                  |
| SCC22                           | Common-mode output return loss  | 50 MHz < f < 2.5 GHz   |      | 6  |                  | dB               |
|                                 |   | 2.5 GHz < f < 7.5 GHz  |      | See <sup>(2)</sup>                             |                  |                  |
| T <sub>(LATENCY)</sub>          | Transmit path latency   | 10GBASE-KR mode  |      | see <a href="#">Figure 3-5</a>                 |                  |                  |
|                                 |   | 1GBASE-KX mode   |      | see <a href="#">Figure 4-2</a>                 |                  |                  |
|                                 |   | General Purpose mode   |      | see <a href="#">Figure 5-4</a>                 |                  |                  |

(1) Differential input return loss, SDD22 = 9 – 12 log<sub>10</sub>(f / 2500MHz)) dB  
 (2) Common-mode output return loss, SDD22 = 6 – 12 log<sub>10</sub>(f / 2500MHz)) dB

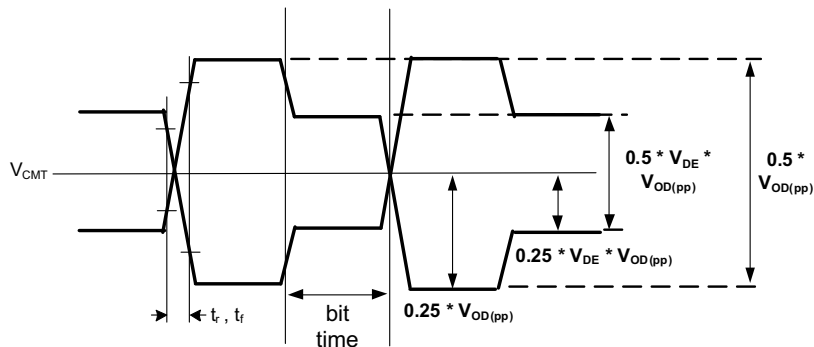
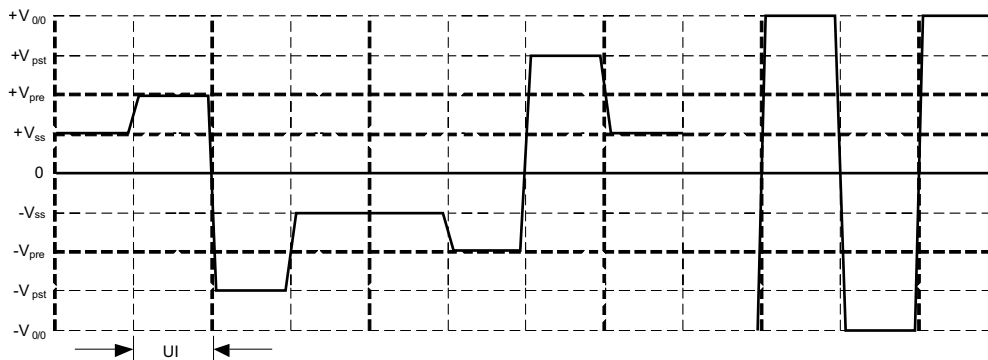


Figure 9-1. Transmit Output Waveform Parameter Definitions



$h_{-1}$  = TWPRE (0%  $\geq$  -17.5% for typical application) setting  
 $h_1$  = TWPOST1 (0%  $\geq$  -37.5% for typical application) setting  
 $h_0 = 1 - |h_1| - |h_{-1}|$   
 $V_{0,0}$  = Output Amplitude with TWPRE = 0%, TWPOST = 0%.  
 $V_{ss}$  = Steady State Output Voltage =  $V_{0,0} * |h_1 + h_0 + h_{-1}|$   
 $V_{pre}$  = PreCursor Output Voltage =  $V_{0,0} * |-h_1 - h_0 + h_{-1}|$   
 $V_{pst}$  = PostCursor Output Voltage =  $V_{0,0} * |-h_1 + h_0 + h_{-1}|$

Figure 9-2. Pre/Post Cursor Swing Definitions

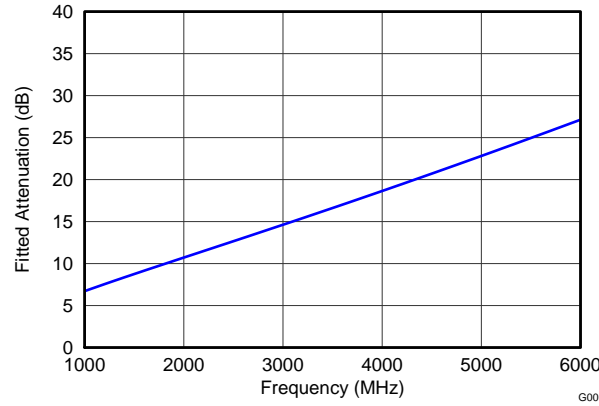
### 9.4 High Speed Side Serial Receiver Characteristics

| PARAMETER           |   | TEST CONDITIONS                      | MIN | NOM                | MAX   | UNIT             |
|---------------------|---|--------------------------------------|-----|--------------------|-------|------------------|
| V <sub>ID</sub>     | RX Input differential voltage,  RXP – RXN   | Full Rate, AC Coupled                | 50  |                    | 600   | mV               |
|                     |   | Half/Quarter/Eighth Rate, AC Coupled | 50  |                    | 800   |                  |
| V <sub>ID(pp)</sub> | RX Input differential peak-to-peak voltage swing, 2× RXP – RXN  | Full Rate, AC Coupled                | 100 |                    | 1200  | mV <sub>pp</sub> |
|                     |   | Half/Quarter/Eighth Rate, AC Coupled | 100 |                    | 1600  |                  |
| C <sub>1</sub>      | RX Input capacitance  |                                      |     |                    | 2     | pF               |
| J <sub>TOL</sub>    | 10GBASE-KR Jitter tolerance, test channel with mTC =1 (see Figure 9-3 for attenuation curve), PRBS31 test pattern at 10.3125 Gbps | Applied sinusoidal jitter            |     |                    | 0.115 | UI <sub>pp</sub> |
|                     |   | Applied random jitter                |     |                    | 0.130 |                  |
|                     |   | Applied duty cycle distortion        |     |                    | 0.035 |                  |
|                     |   | Broadband noise amplitude (RMS)      |     |                    | 5.2   |                  |
| SDD11               | Differential input return loss  | 50 MHz < f < 2.5 GHz                 |     | 9                  |       | dB               |
|                     |   | 2.5 GHz < f < 7.5 GHz                |     | See <sup>(1)</sup> |       |                  |
| t <sub>skew</sub>   | Intra-pair input skew   |                                      |     |                    | 0.23  | UI               |

(1) Differential input return loss, SDD11 = 9 – 12 log<sub>10</sub>(f / 2.5GHz) dB

**High Speed Side Serial Receiver Characteristics (continued)**

| PARAMETER                            | TEST CONDITIONS      | MIN            | NOM | MAX | UNIT |
|--------------------------------------|----------------------|----------------|-----|-----|------|
| $t_{(LATENCY)}$ Receive path latency | 10GBASE-KR mode      | see Figure 3-5 |     |     |      |
|                                      | 1GBASE-KX mode       | see Figure 4-2 |     |     |      |
|                                      | General Purpose mode | see Figure 5-4 |     |     |      |



**Figure 9-3. 10GBASE-KR Fitted Channel Attenuation Limit**

**9.5 Low Speed Side Serial Transmitter Characteristics**

| PARAMETER   | TEST CONDITIONS                                     | MIN                           | NOM  | MAX  | UNIT |
|---|---|-------------------------------|------|------|------|
| $V_{OD(pp)}$ Transmitter output differential peak-to-peak voltage swing | SWING = 000   | 110                           | 190  | 280  | mVpp |
|   | SWING = 001   | 280                           | 380  | 490  |      |
|   | SWING = 010   | 420                           | 560  | 700  |      |
|   | SWING = 011   | 560                           | 710  | 870  |      |
|   | SWING = 100   | 690                           | 850  | 1020 |      |
|   | SWING = 101   | 760                           | 950  | 1150 |      |
|   | SWING = 110   | 800                           | 1010 | 1230 |      |
|   | SWING = 111   | 830                           | 1050 | 1270 |      |
| DE Transmitter output de-emphasis voltage swing reduction               | DE = 0000   | 0                             |      |      | dB   |
|   | DE = 0001   | 0.42                          |      |      |      |
|   | DE = 0010   | 0.87                          |      |      |      |
|   | DE = 0011   | 1.34                          |      |      |      |
|   | DE = 0100   | 1.83                          |      |      |      |
|   | DE = 0101   | 2.36                          |      |      |      |
|   | DE = 0110   | 2.92                          |      |      |      |
|   | DE = 0111   | 3.52                          |      |      |      |
|   | DE = 1000   | 4.16                          |      |      |      |
|   | DE = 1001   | 4.86                          |      |      |      |
|   | DE = 1010   | 5.61                          |      |      |      |
|   | DE = 1011   | 6.44                          |      |      |      |
|   | DE = 1100   | 7.35                          |      |      |      |
|   | DE = 1101   | 8.38                          |      |      |      |
| DE = 1110   | 9.54  |                               |      |      |      |
| DE = 1111   | 10.87   |                               |      |      |      |
| $V_{CMT}$ Transmitter output common mode voltage                        | 100- $\Omega$ differential termination. DC-coupled. | $V_{DDT} - 0.5 * V_{OD(p-p)}$ |      |      | mV   |
| $t_{skew}$ Intra-pair output skew                                       |   | 0.045                         |      |      | UI   |



**Low Speed Side Serial Transmitter Characteristics (continued)**

| PARAMETER  | TEST CONDITIONS  | MIN | NOM | MAX  | UNIT |
|------------|--|-----|-----|------|------|
| $t_R, t_F$ | Differential output signal rise, fall time (20% to 80%) Differential Load = 100Ω | 30  |     |      | ps   |
| $J_T$      | Serial output total jitter   |     |     | 0.35 | UI   |
| $J_D$      | Serial output deterministic jitter   |     |     | 0.17 | UI   |
| $t_{skew}$ | Lane-to-lane output skew   |     |     | 50   | ps   |

**9.6 Low Speed Side Serial Receiver Characteristics**

| PARAMETER       | TEST CONDITIONS   | MIN                              | NOM | MAX  | UNIT        |
|-----------------|---|----------------------------------|-----|------|-------------|
| $V_{ID}$        | Receiver input differential voltage,  INP – INN                               | Full Rate, AC Coupled            | 50  | 600  | mV          |
|                 |   | Half/Quarter Rate, AC Coupled    | 50  | 800  |             |
| $V_{ID(pp)}$    | Receiver input differential peak-to-peak voltage swing $2 \times  INP – INN $ | Full Rate, AC Coupled            | 100 | 1200 | $mV_{dfpp}$ |
|                 |   | Half/Quarter Rate, AC Coupled    | 100 | 1600 |             |
| $C_I$           | Receiver input capacitance  |                                  |     | 2    | pF          |
| $J_{TOL}$       | Jitter tolerance, total jitter at serial input (DJ + RJ) (BER $10^{-15}$ )    | Zero crossing, Half/Quarter Rate |     | 0.66 | $UI_{p-p}$  |
|                 |   | Zero crossing, Full Rate         |     | 0.65 |             |
| $J_{DR}$        | Serial input deterministic jitter (BER $10^{-15}$ )                           | Zero crossing, Half/Quarter Rate |     | 0.50 | $UI_{p-p}$  |
|                 |   | Zero crossing, Full Rate         |     | 0.35 |             |
| $t_{skew}$      | Intra-pair input skew   |                                  |     | 0.23 | UI          |
| $t_{lane-skew}$ | Lane-to-lane input skew   |                                  |     | 30   | UI          |

**9.7 Reference Clock Characteristics (REFCLK0P/N, REFCLK1P/N)**

| PARAMETER         | TEST CONDITIONS              | MIN                                      | NOM  | MAX  | UNIT      |
|-------------------|------------------------------|--|------|------|-----------|
| F                 | Frequency                    | 122.88                                   |      | 425  | MHz       |
| $F_{HS_{offset}}$ | Accuracy                     | Relative to Nominal HS Serial Data Rate  | -100 | 100  | ppm       |
|                   |                              | Relative to Incoming HS Serial Data Rate | -200 | 200  |           |
| DC                | Duty cycle                   | High Time                                | 45%  | 50%  | 55%       |
| $V_{ID}$          | Differential input voltage   | 250                                      |      | 2000 | $mV_{pp}$ |
| $C_{IN}$          | Input capacitance            |  |      | 1    | pF        |
| $R_{IN}$          | Differential input impedance |  | 100  |      | Ω         |
| $T_{RISE}$        | Rise/fall time               | 10% to 90%                               | 50   | 350  | ps        |

**9.8 Differential Output Clock Characteristics (CLKOUTA/BP/N)**

| PARAMETER  | TEST CONDITIONS             | MIN  | NOM  | MAX  | UNIT        |
|------------|-----------------------------|--|------|------|-------------|
| $V_{OD}$   | Differential output voltage | Peak to peak                                       | 1000 | 2000 | $mV_{dfpp}$ |
| $T_{RISE}$ | Output rise time            | 10% to 90%, 2pF lumped capacitive load, AC-Coupled |      | 350  | ps          |
| $R_{TERM}$ | Output termination          | CLKOUTxP/N to DVDD                                 | 50   |      | Ω           |
| F          | Output frequency            |  | 0    | 500  | MHz         |

**9.9 LVCMOS Electrical Characteristics (VDDO):**

| PARAMETER | TEST CONDITIONS           | MIN                                    | NOM                   | MAX       | UNIT |
|-----------|---------------------------|--|-----------------------|-----------|------|
| $V_{OH}$  | High-level output voltage | $I_{OH} = 2$ mA, Driver Enabled (1.8V) | $V_{DDO} - 0.45$      | $V_{DDO}$ | V    |
|           |                           | $I_{OH} = 2$ mA, Driver Enabled (1.5V) | $0.75 \times V_{DDO}$ | $V_{DDO}$ |      |

**LVC MOS Electrical Characteristics (VDDO): (continued)**

| PARAMETER                         |                                      | TEST CONDITIONS                                | MIN         | NOM | MAX         | UNIT |
|-----------------------------------|--------------------------------------|--|-------------|-----|-------------|------|
| V <sub>OL</sub>                   | Low-level output voltage             | I <sub>OL</sub> = -2 mA, Driver Enabled (1.8V) | 0           |     | 0.45        | V    |
|                                   |                                      | I <sub>OL</sub> = -2 mA, Driver Enabled (1.5V) | 0           |     | 0.25 × VDDO |      |
| V <sub>IH</sub>                   | High-level input voltage             |  | 0.65 × VDDO |     | VDDO + 0.3  | V    |
| V <sub>IL</sub>                   | Low-level input voltage              |  | -0.3        |     | 0.35 × VDDO | V    |
| I <sub>IH</sub> , I <sub>IL</sub> | Receiver only                        | Low/High Input Current                         |             |     | ±170        | μA   |
| I <sub>OZ</sub>                   | Driver only                          | Driver Disabled                                |             |     | ±25         | μA   |
|                                   | Driver/Receiver With Pullup/Pulldown | Driver disabled With Pull Up/Down Enabled      |             |     | ±195        |      |
| C <sub>IN</sub>                   | Input capacitance                    |  |             |     | 3           | pF   |

**9.10 MDIO Timing Requirements**

over recommended operating conditions (unless otherwise noted)

| PARAMETER           |                       | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---------------------|-----------------------|-----------------|-----|-----|-----|------|
| t <sub>period</sub> | MDC period            | See Figure 9-4  | 100 |     |     | ns   |
| t <sub>setup</sub>  | MDIO setup to ↑ MDC   |                 | 10  |     |     | ns   |
| t <sub>hold</sub>   | MDIO hold to ↑ MDC    |                 | 10  |     |     | ns   |
| T <sub>valid</sub>  | MDIO valid from MDC ↑ |                 | 0   |     | 40  | ns   |

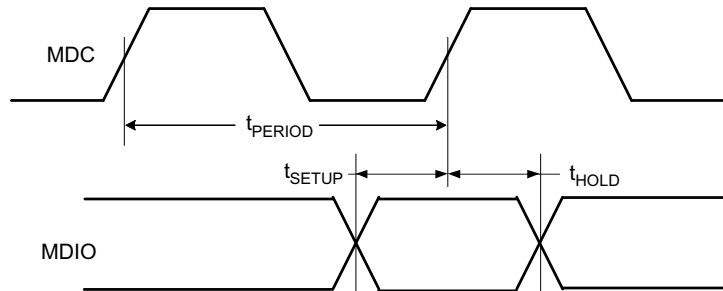


Figure 9-4. MDIO Read/Write Timing

**9.11 JTAG Timing Requirements**

over recommended operating conditions (unless otherwise noted)

| PARAMETER           |                                | TEST CONDITIONS | MIN   | NOM | MAX | UNIT |
|---------------------|--------------------------------|-----------------|-------|-----|-----|------|
| T <sub>PERIOD</sub> | TCK period                     | See Figure 9-5  | 66.67 |     |     | ns   |
| T <sub>SETUP</sub>  | TDI/TMS/TRST_N setup to ↑ TCK  |                 | 3     |     |     |      |
| T <sub>HOLD</sub>   | TDI/TMS/TRST_N hold from ↑ TCK |                 | 5     |     |     |      |
| T <sub>VALID</sub>  | TDO delay from TCK Falling     |                 | 0     |     | 10  | ns   |

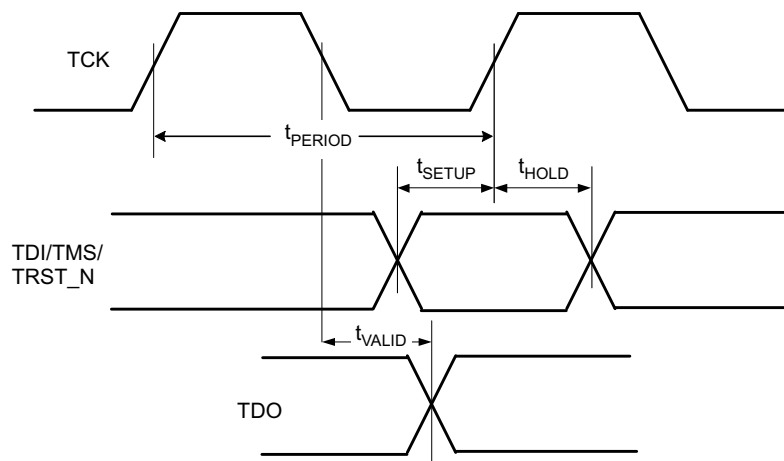


Figure 9-5. JTAG Timing

### 9.12 Power Sequencing Guidelines

The TLK10232 allows either the core or I/O power supply to be powered up for an indefinite period of time while the other supply is not powered up, if all of the following conditions are met:

1. All maximum ratings and recommending operating conditions are followed
2. Bus contention while 1.5/1.8V power is applied (>0V) must be limited to 100 hours over the projected lifetime of the device.
3. Junction temperature is less than 105°C during device operation. Note: Voltage stress up to the absolute maximum voltage values for up to 100 hours of lifetime operation at a TJ of 105°C or lower will minimally impact reliability.

The TLK10232 LVCMOS I/O are not failsafe (i.e. cannot be driven with the I/O power disabled). TLK10232 inputs should not be driven high until their associated power supply is active.

## 10 MECHANICAL AND THERMAL DATA

### 10.1 Package Thermal Dissipation Ratings

Table 10-1 details the thermal characteristics of the TLK10232 package.

**Table 10-1. Package Thermal Characteristics**

| JEDEC STANDARD BOARD                            |          |       |
|---|----------|-------|
| PARAMETER                                       |          | VALUE |
| $\Theta_{JA}$                                   | Theta-JA | 25.5  |
| $\Psi_{JT}$                                     | Psi-JT   | 1.8   |
| $\Psi_{JB}$                                     | Psi-JB   | 13.7  |
| CUSTOM TYPICAL APPLICATION BOARD <sup>(1)</sup> |          |       |
| $\Theta_{JA}$                                   | Theta-JA | 24.5  |
| $\Psi_{JT}$                                     | Psi-JT   | 0.9   |
| $\Psi_{JB}$                                     | Psi-JB   | 11    |

(1) Custom Typical Application Board Characteristics:

- 10x15 inches
- 12 layer
  - 8 power/ground layers – 95% copper (1oz)
  - 4 signal layers – 20% copper (1oz)

$$\Psi_{JB} = (T_J - T_B) / (\text{Total Device Power Dissipation})$$

$T_J$  = Device Junction Temperature  
 $T_B$  = Temperature of PCB 1 mm from device edge.

$$\Psi_{JT} = (T_J - T_C) / (\text{Total Device Power Dissipation})$$

$T_J$  = Device Junction Temperature  
 $T_C$  = Hottest temperature on the case of the package.

**Table 10-2. ORDERING INFORMATION**

| Generic Part Number | Orderable Part Number |
|---------------------|-----------------------|
| TLK10232            | TLK10232CTR           |

## 11 APPENDIX A: PROVISIONABLE XAUI CLOCK TOLERANCE COMPENSATION

The XAUI interface is defined to allow for separate clock domains on each side of the link. Though the reference clocks for two devices on a XAUI/KR link have the same specified frequencies, there are slight differences that, if not compensated for, will lead to over or under run of the FIFOs on the receive/transmit data paths.

The XAUI CTC block performs the clock domain transition and rate compensation by utilizing a FIFO that is 32 deep and 40-bits wide. The usable FIFO size in the RX and TX directions is dependent upon the RX\_FIFO\_DEPTH and TX\_FIFO\_DEPTH MDIO fields, respectively. The word format is illustrated in Figure 11-1.

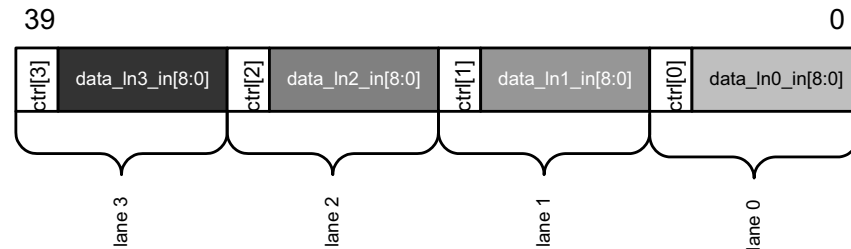


Figure 11-1. XAUI CTC FIFO Word Format

The XAUI CTC performs one of the following operations to compensate the clock rate difference:

1. Delete Idle column from the data stream
2. Delete Sequence column from the data stream (enabled via MDIO)
3. Insert Idle column to the data stream.

The following rules apply for insertion/removal:

- Idle insertion/deletion occurs in groups of 4 idle characters (i.e., in columns)
- Idle characters are added following Idle or Sequence ordered\_set
- Idle characters are not added while data is being received
- When deleting Idle characters, minimum IPG of 5 characters is maintained. /T/ characters are counted towards IPG.
- The first Idle column after /T/ is never deleted
- Sequence ordered\_sets are deleted only when two consecutive Sequence columns are received. In this case, only one of the two Sequence columns will be deleted.

**Insertion:** When the FIFO fill level is **at or below LOW watermark (insertion is triggered)**, the XAUI CTC needs to insert an IDLE column. It does so by skipping a read from the FIFO and inserting IDLE column to the data stream. It continues the insertion until the FIFO fill level is above the mid point. This occurs on the read side of the FIFO.

**Removal:** When the FIFO fill level is **at or above HIGH watermark (deletion is triggered)**, the XAUI CTC needs to remove an IDLE column. It does so by skipping a write to the FIFO and discarding the IDLE column or Sequence ordered\_set. It continues the deletion until the FIFO fill level is below the mid point. This occurs on the write side of the FIFO.

On the write side of the XAUI CTC FIFO a 40-bit write is performed at every cycle of the 312.5 MHz clock except during removal when it discards the IDLE or sequence ordered\_set. On the read side of the XAUI CTC FIFO a 40-bit read is performed at every cycle of the 312.5 MHz clock except during insertion when it generates IDLE columns to the output while not reading the FIFO at all.

In IEEE 802.3-2008 the XAUI clock rate tolerance is given as 3.125 GHz ± 100 ppm, the XGMII clock rate tolerance is given as 156.25 MHz ± 0.02% (which is equivalent to 200ppm), and the Jumbo packet size is 9600 bytes which is equivalent to 2400 cycles of 312.5 MHz clock. The average inter-frame gap is 12 bytes (3 columns), which implies that there is one opportunity to insert/delete a column in between every packet on average. This gives one column deletion/insertion in every 2400 columns which results in a 400 ppm tolerance capability. If the IPG increases, then more clock rate variance or larger packet size can be supported. Note that the maximum frequency tolerance is limited by the frequency accuracy requirement of the reference clock.

The number of words in the FIFO (fifo\_depth[2:0]) and the HIGH/LOW watermark levels (wmk\_sel[1:0]) are set through MDIO register 01.8001, and determine the allowable difference between the write clock and the read clock as well as the maximum packet size that can be processed without FIFO collision. At these watermarks the drop and insert start respectively and must happen before it hits overflow/underflow condition. Although the FIFO is supposed to never overflow/underflow given the average IPG, if it ever happens the overflow/underflow indications signal the error to the MDIO interface and the FIFO is reset. Note that the overflow/underflow status indications are latched high and cleared when read.

Table 11-1 shows XAUI CTC FIFO configuration and capabilities:

**Table 11-1. XAUI CTC FIFO Configurations**

| fifo_depth[2:0] | FIFO Depth | wmk_sel[1:0]       | LOW Watermark | HIGH Watermark | Max Latency (Cycles) | Nom Latency (Cycles) | Min Latency (Cycles) | Max pkt size (400ppm)                      | Max pkt size (200ppm) | Max pkt size (100ppm) | Max pkt size (50ppm) | Min #of removable columns in IPG to support the max pkt size |         |
|-----------------|------------|--------------------|---------------|----------------|----------------------|----------------------|----------------------|--|-----------------------|-----------------------|----------------------|--|---------|
| 1xx             | 32         | 11                 | 15            | 18             | 28                   | 16                   | 4                    | 100KB                                      | 200KB                 | 400KB                 | 800KB                | 10   | default |
|                 |            | 10                 | 13            | 20             | 28                   | 16                   | 4                    | 80KB                                       | 160KB                 | 320KB                 | 640KB                | 8  |         |
|                 |            | 01                 | 10            | 23             | 28                   | 16                   | 4                    | 50KB                                       | 100KB                 | 200KB                 | 400KB                | 5  |         |
|                 |            | 00                 | 6             | 27             | 28                   | 16                   | 4                    | 10KB                                       | 20KB                  | 40KB                  | 80KB                 | 1  |         |
| 011             | 24         | 11                 | 11            | 14             | 20                   | 12                   | 4                    | 60KB                                       | 120KB                 | 240KB                 | 480KB                | 6  |         |
|                 |            | 10                 | 9             | 16             | 20                   | 12                   | 4                    | 40KB                                       | 80KB                  | 160KB                 | 320KB                | 4  |         |
|                 |            | 0x                 | 6             | 19             | 20                   | 12                   | 4                    | 10KB                                       | 20KB                  | 40KB                  | 80KB                 | 1  |         |
| 010             | 16         | 1x                 | 7             | 10             | 13                   | 8                    | 3                    | 30KB                                       | 60KB                  | 120KB                 | 240KB                | 3  |         |
|                 |            | 0x                 | 5             | 12             | 13                   | 8                    | 3                    | 10KB                                       | 20KB                  | 40KB                  | 80KB                 | 1  |         |
| 001             | 12         | xx                 | 5             | 8              | 9                    | 6                    | 3                    | 10KB                                       | 20KB                  | 40KB                  | 80KB                 | 1  |         |
| 000             | 8          | Plain FIFO, No CTC |               |                | 7                    | 4                    | 1                    | No limit on pkt size (needs 0 ppm to work) |                       |                       |                      |  |         |

**Note:** To support the max packet sizes as shown in Table 11-1, it is assumed that there are enough IDLE columns in IPG for deletion. Below is one example:

Configure the FIFO to be 32-deep (fifo\_depth[2:0] = 3'b1xx) and set the LOW/HIGH Watermarks to 10/23 (wmk\_sel[1:0] = 2'b01). If the write clock is faster than the read clock by 200ppm, to support the max packet size of 100KB, a minimum of 5 removable columns in IPG is required (either IDLE columns or Sequence ordered\_sets). If there are only 4 removable columns in IPG, the max packet size supported is dropped to 80KB. If there are only 3 removable columns in IPG, the max packet size supported is dropped to 60KB, and so on. As a rule of thumb, one removable column in IPG corresponds to 10KB at 400ppm, 20KB at 200ppm, 40KB at 100ppm, and 80KB at 50ppm

The following figures illustrate XAUI CTC FIFO configuration and capabilities. The green region (the middle of the FIFO fill level) indicates that the FIFO is operating stably without insertion or deletion. The more green bars in the figure, the more clock wander it can tolerate. The more yellow bars in the figure, the bigger packet size it can support.

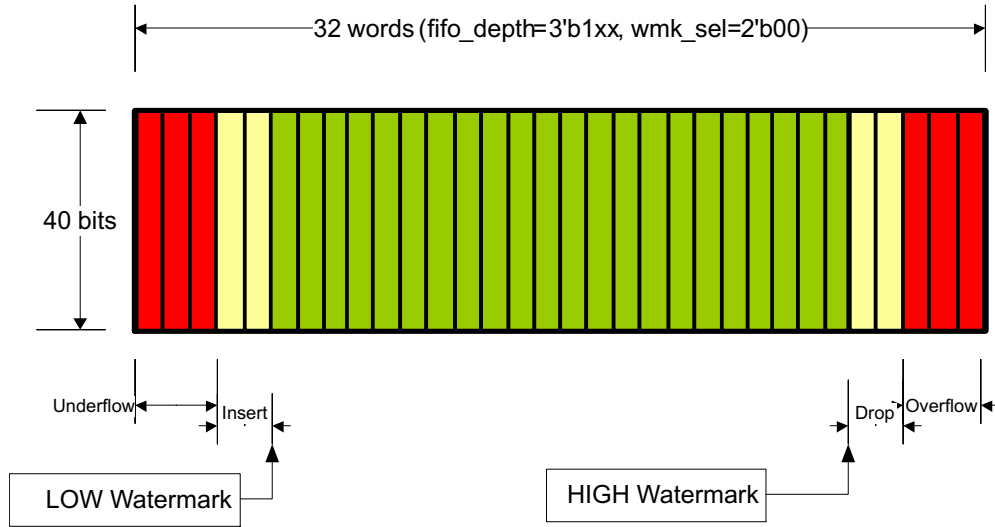


Figure 11-2. Organization of the XAUI CTC FIFO (32-Deep, Low Watermark)

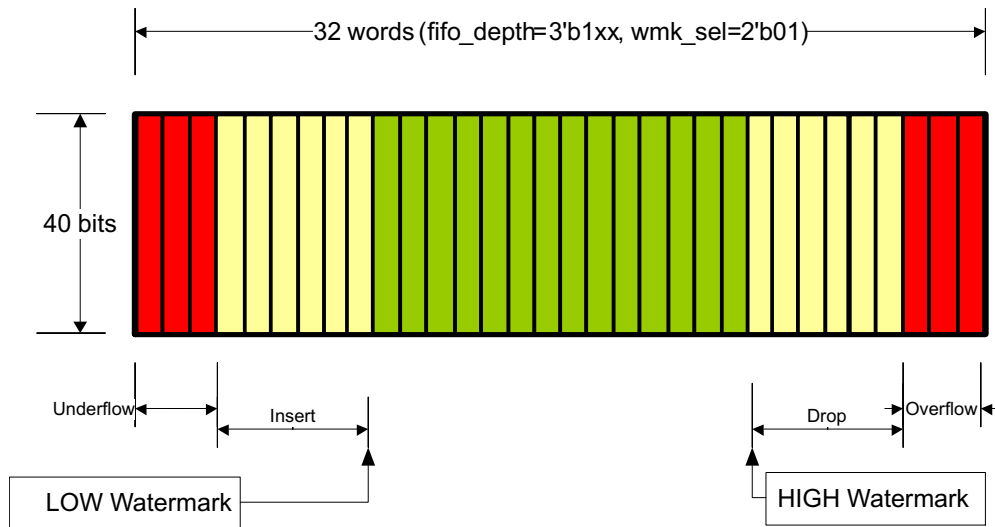
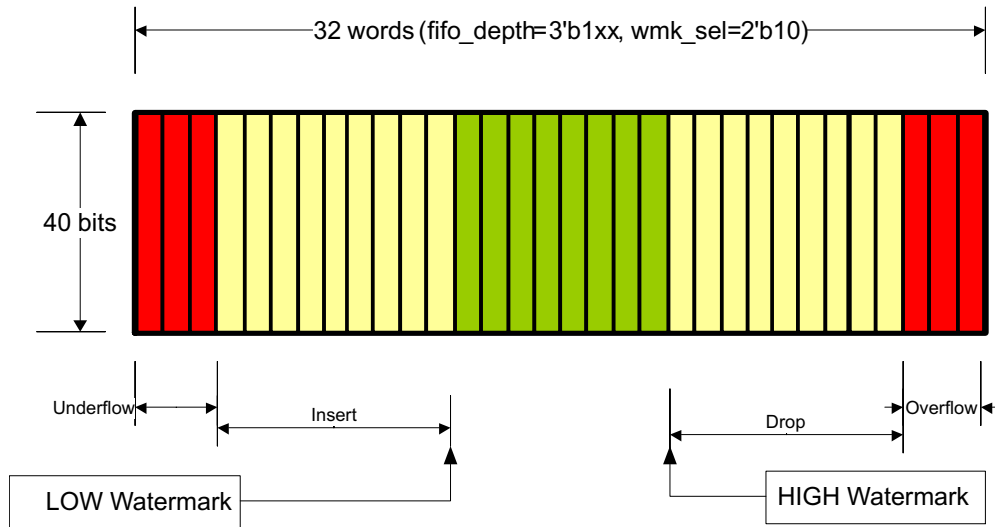
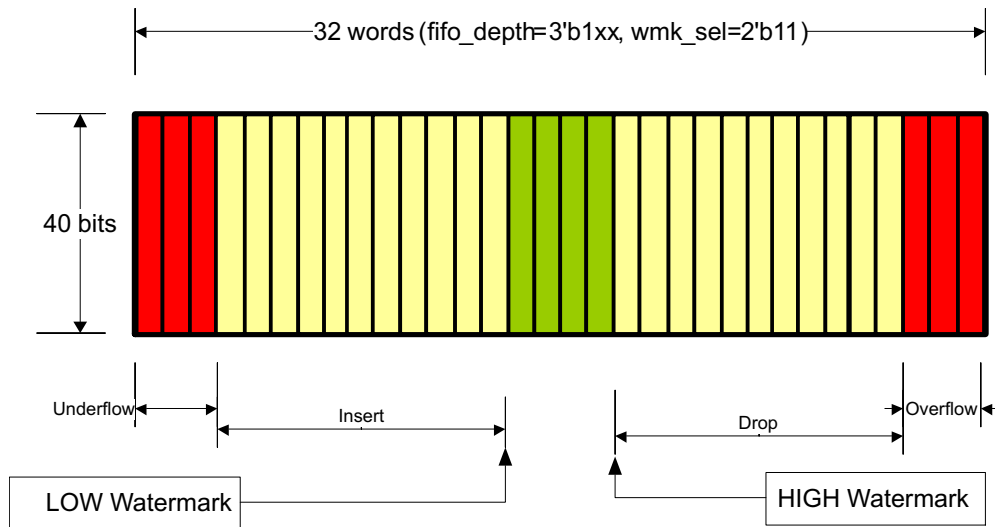


Figure 11-3. Organization of the XAUI CTC FIFO (32-Deep, Mid Watermark)



**Figure 11-4. Organization of the XAUI CTC FIFO (32-Deep, Mid-High Watermark)**



**Figure 11-5. Organization of the XAUI CTC FIFO (32-Deep, High Watermark)**



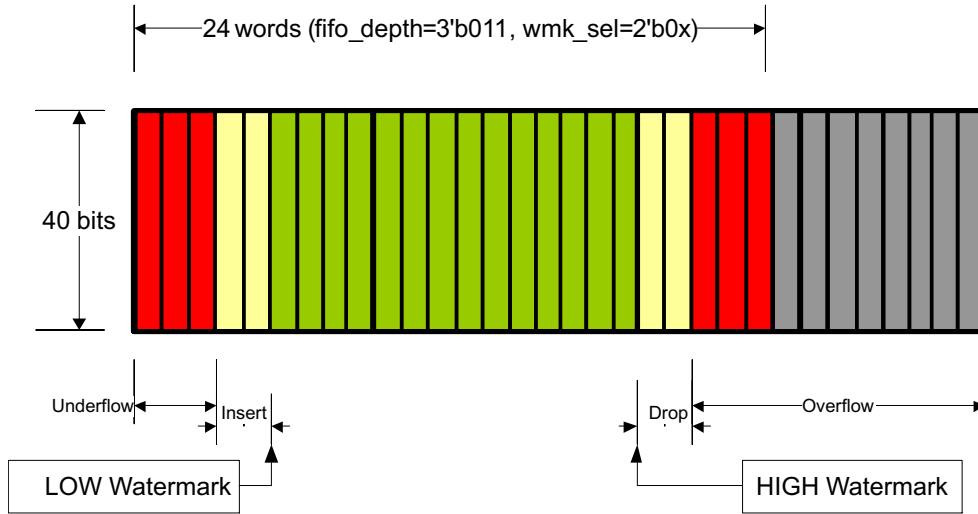


Figure 11-6. Organization of the XAUI CTC FIFO (24-Deep, Low Watermark)

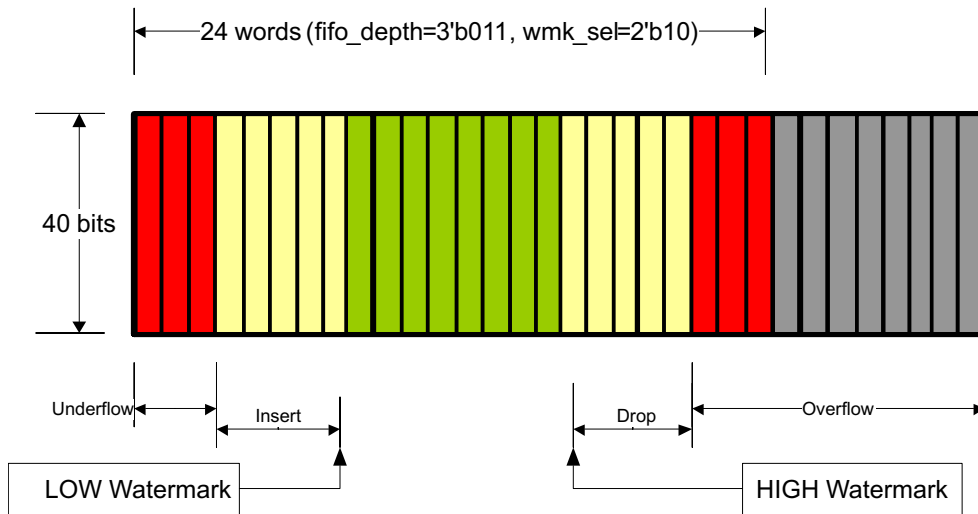


Figure 11-7. Organization of the XAUI CTC FIFO (24-Deep, Mid Watermark)

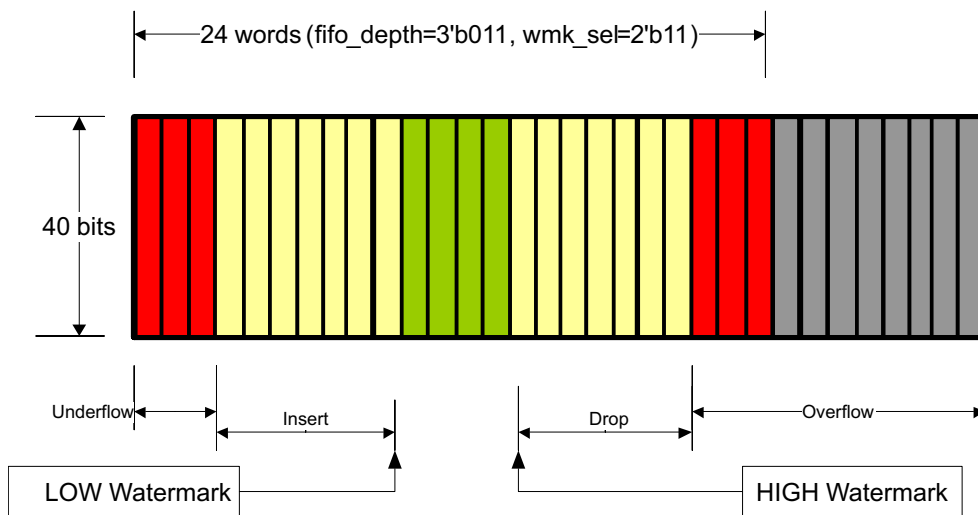


Figure 11-8. Organization of the XAUI CTC FIFO (24-Deep, High Watermark)

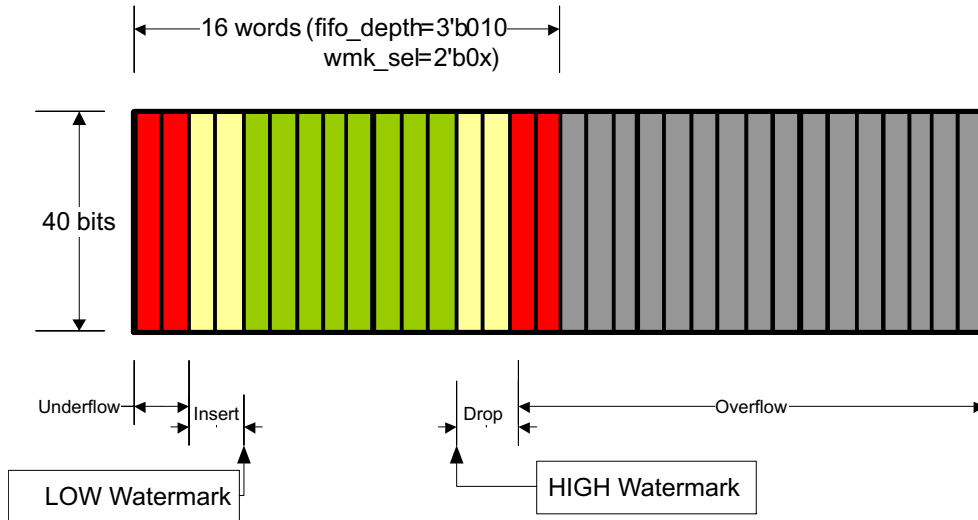


Figure 11-9. Organization of the XAUI CTC FIFO (16-Deep, Low Watermark)

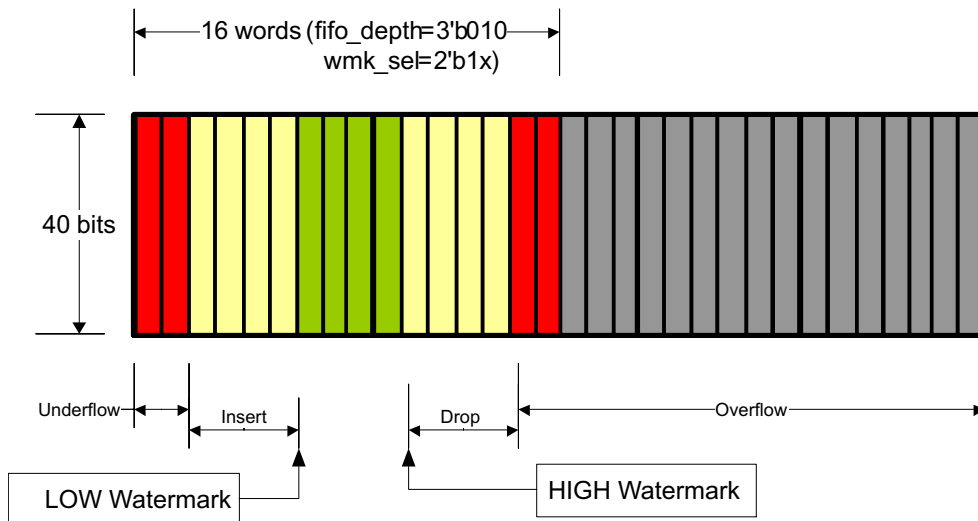


Figure 11-10. Organization of the XAUI CTC FIFO (16-Deep, High Watermark)

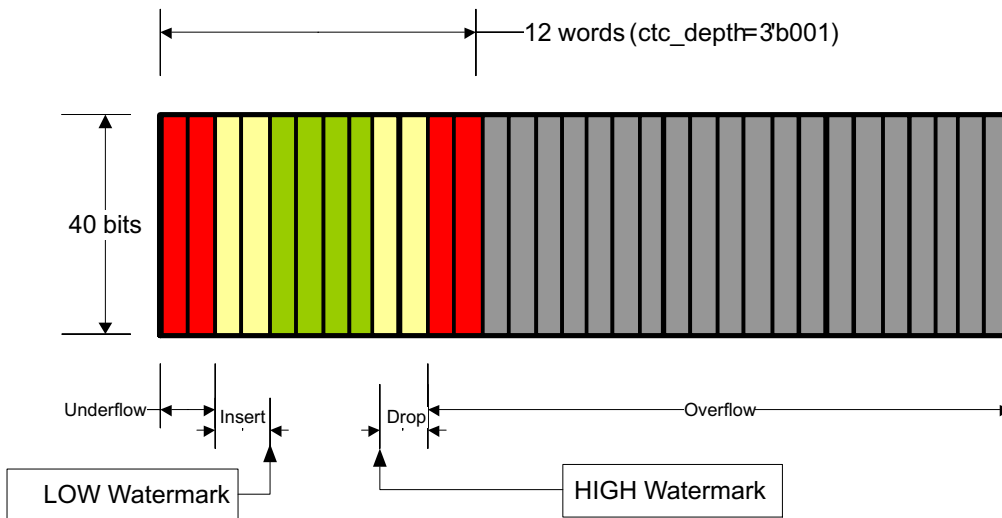


Figure 11-11. Organization of the XAUI CTC FIFO (12-Deep)

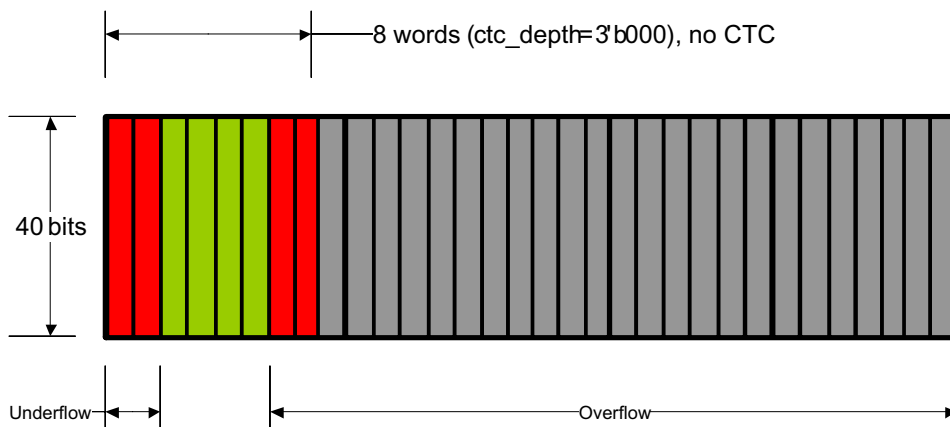


Figure 11-12. Organization of the XAUI CTC FIFO (8-Deep)

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| TLK10232CTR      | ACTIVE        | FCBGA        | CTR             | 144  | 119         | RoHS & Green    | SNAGCU                               | Level-4-260C-72 HR   | -40 to 85    | TLK10232                | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

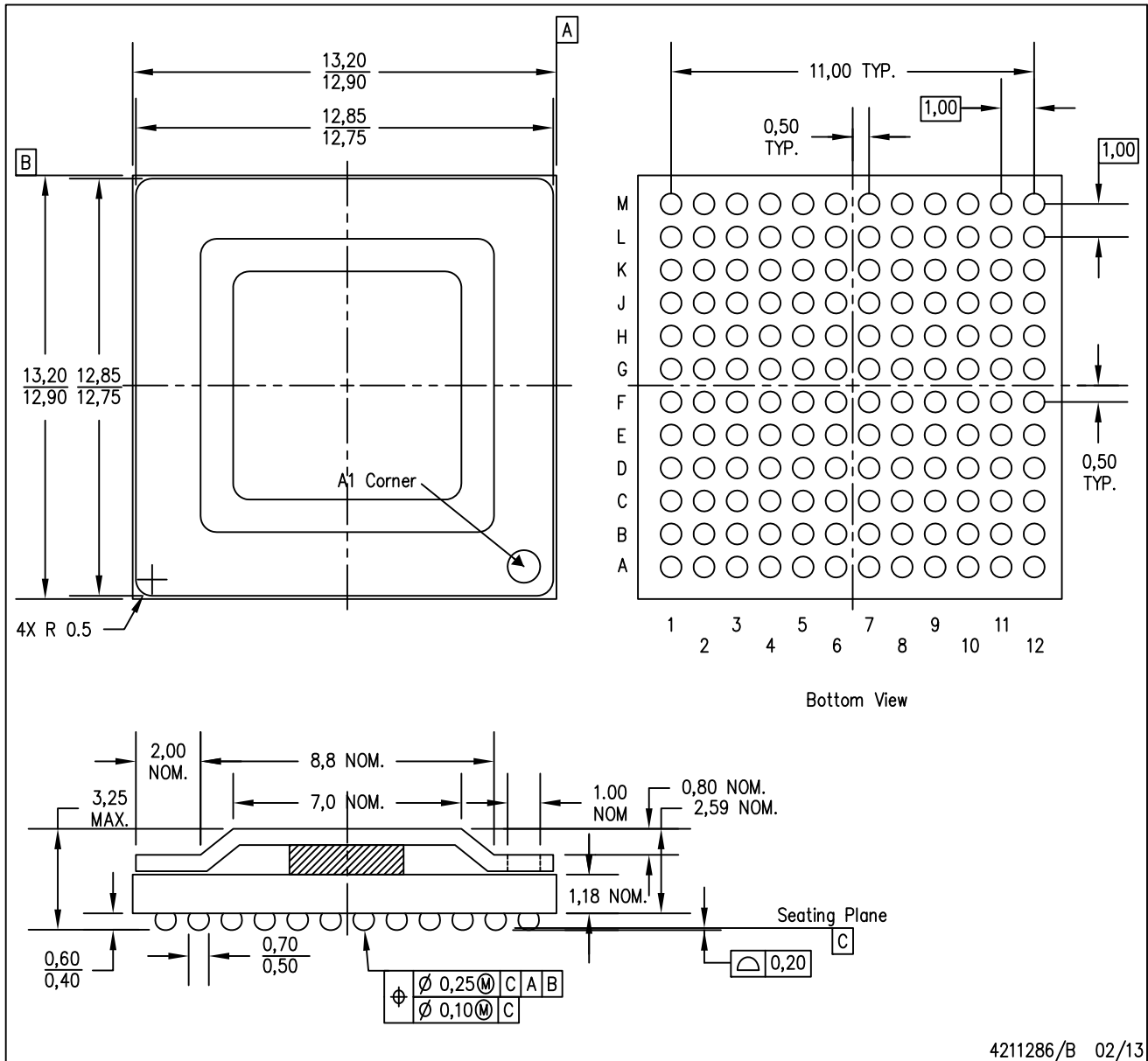
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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CTR (S-PBGA-N144)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Flip chip application only.
  - D. Pb-free die bump and solder ball.

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