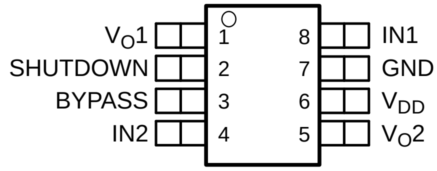
300-mW STEREO AUDIO POWER AMPLIFIER

- **300-mW Stereo Output**
- **PC Power Supply Compatibility 5-V and 3.3-V Specified Operation**
- **Shutdown Control**
- **Internal Midrail Generation**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
- **Functional Equivalent of the LM4880**

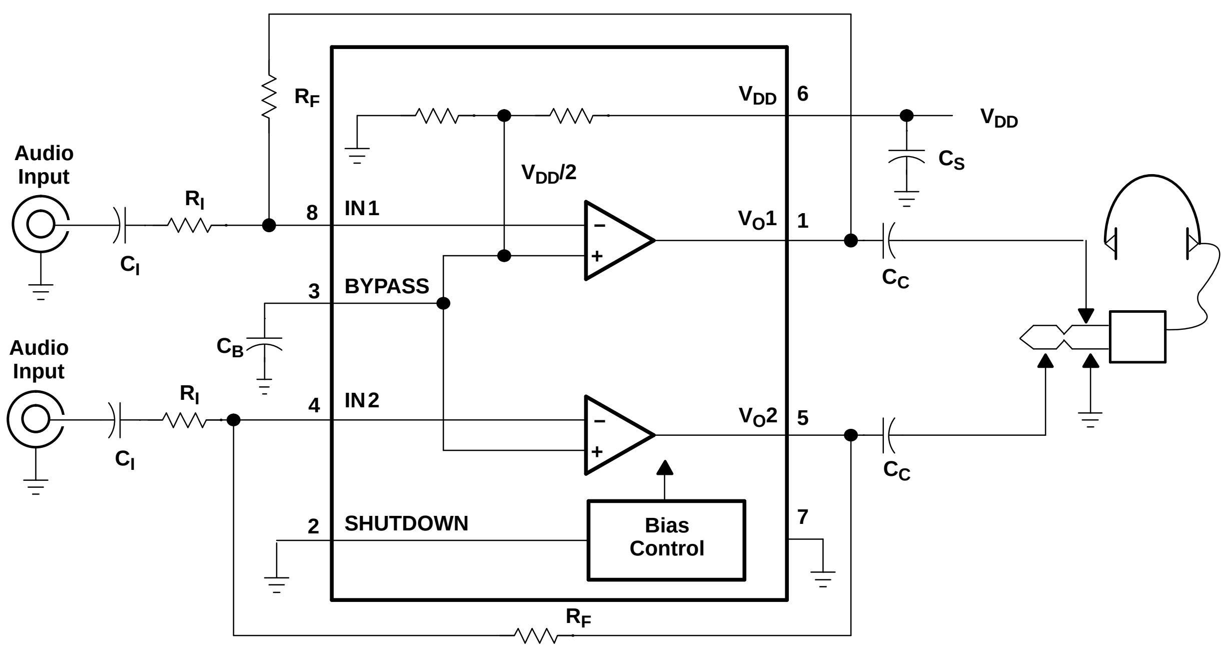
D PACKAGE
(TOP VIEW)



DESCRIPTION

The TPA302 is a stereo audio power amplifier capable of delivering 250 mW of continuous average power into an 8-Ω load at less than 0.06% THD+N from a 5-V power supply or up to 300 mW at 1% THD+N. The TPA302 has high current outputs for driving small unpowered speakers at 8 Ω or headphones at 32 Ω. For headphone applications driving 32-Ω loads, the TPA302 delivers 60 mW of continuous average power at less than 0.06% THD+N. The amplifier features a shutdown function for power-sensitive applications as well as internal thermal and short-circuit protection. The amplifier is available in an 8-pin SOIC (D) package that reduces board space and facilitates automated assembly.

TYPICAL APPLICATION CIRCUIT



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	SMALL OUTLINE (1) (D)
–40°C to 85°C	TPA302D

(1) The D packages are available taped and reeled. To order a taped and reeled part, add the suffix R (e.g., TPA302DR)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		UNIT
V_{DD}	Supply voltage	6 V
V_I	Input voltage	–0.3 V to V_{DD} + 0.3 V
	Continuous total power dissipation	Internally limited (see Dissipation Rating Table)
T_J	Operating junction temperature range	–40°C to 150° C
T_{stg}	Storage temperature range	–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	731 mW	5.8 mW/°C	460 mW	380 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2.7	5.5	V
T_A	Operating free-air temperature	–40	85	°C

DC ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{DD}	Supply current			2.25	5	mA
V_{IO}	Input offset voltage			5	20	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V		55		dB
$I_{DD(SD)}$	Quiescent current in shutdown			0.6	20	µA

AC OPERATING CHARACTERISTICS

V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
P_O	Output power	Gain = –1, f = 1 kHz	THD < 0.08%		100		mW
			THD < 1%		125		
			THD < 0.08%, R_L = 32 Ω		25		
			THD < 1%, R_L = 32 Ω		35		
B_{OM}	Maximum output power bandwidth	Gain = 10,	1% THD		20		kHz
B_1	Unity gain bandwidth	Open loop			1.5		MHz
	Channel separation	f = 1 kHz			75		dB
	Supply ripple rejection ratio	f = 1 kHz			45		dB
V_n	Noise output voltage	Gain = –1			10		µVrms

DC ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

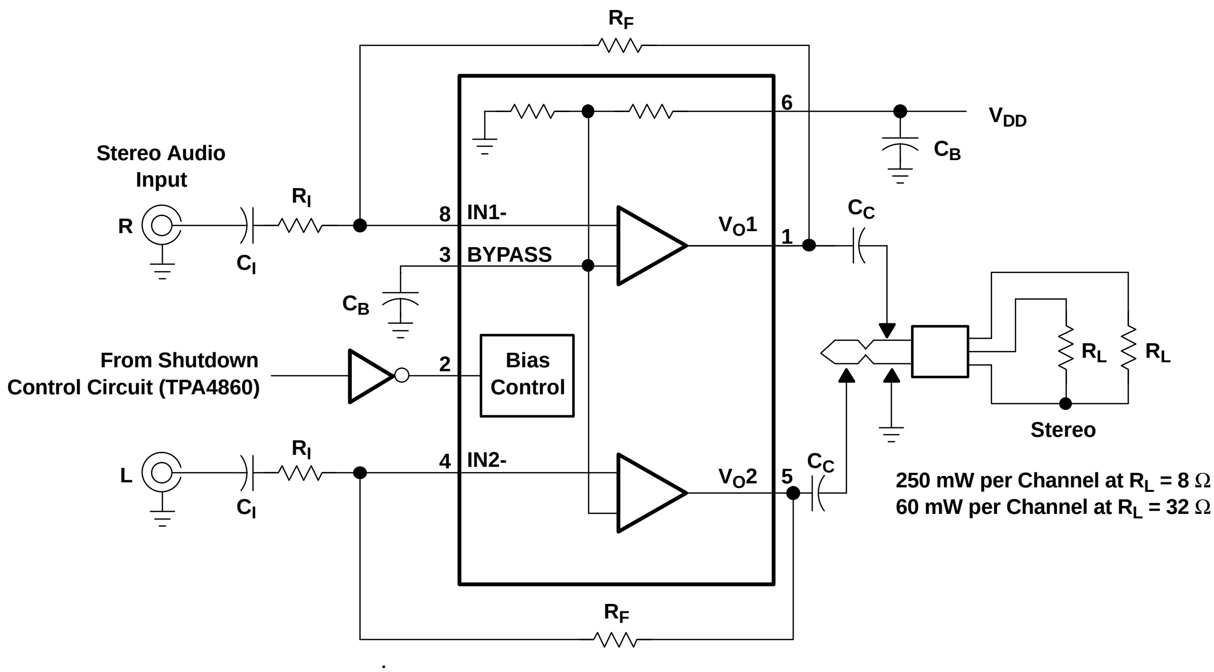
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{DD}	Supply current			4	10	mA
V_{OO}	Output offset voltage			5	20	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		65		dB
$I_{DD(SD)}$	Quiescent current in shutdown			0.6		µA

AC OPERATING CHARACTERISTICS

V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
P_O	Output power	Gain = –1, f = 1 kHz	THD < 0.06%		250		mW
			THD < 1%		300		
			THD < 0.06%, R_L = 32 Ω		60		
			THD < 1%, R_L = 32 Ω		80		
B_{OM}	Maximum output power bandwidth	Gain = 10,	1% THD		20		kHz
B_1	Unity gain bandwidth	Open loop			1.5		MHz
	Channel separation	f = 1 kHz			75		dB
	Supply ripple rejection ratio	f = 1 kHz			45		dB
V_n	Noise output voltage	Gain = -1			10		µVrms

TYPICAL APPLICATION



TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Frequency	1-3, 7-9, 13-15, 19-21
		vs Output power	4-6, 10-12 16-18, 22-24
I_{DD}	Supply current	vs Supply voltage	25
		vs Free-air temperature	26
V_n	Output noise voltage	vs Frequency	27, 28
	Maximum package power dissipation	vs Free-air temperature	29
	Power dissipation	vs Output power	30, 31
P_{Omax}	Maximum output power	vs Free-air temperature	32, 33
P_O	Output power	vs Load resistance	34
		vs Supply voltage	35
	Open-loop response		36
	Closed-loop response		37
	Crosstalk	vs Frequency	38, 39
	Supply ripple rejection ratio	vs Frequency	40, 41

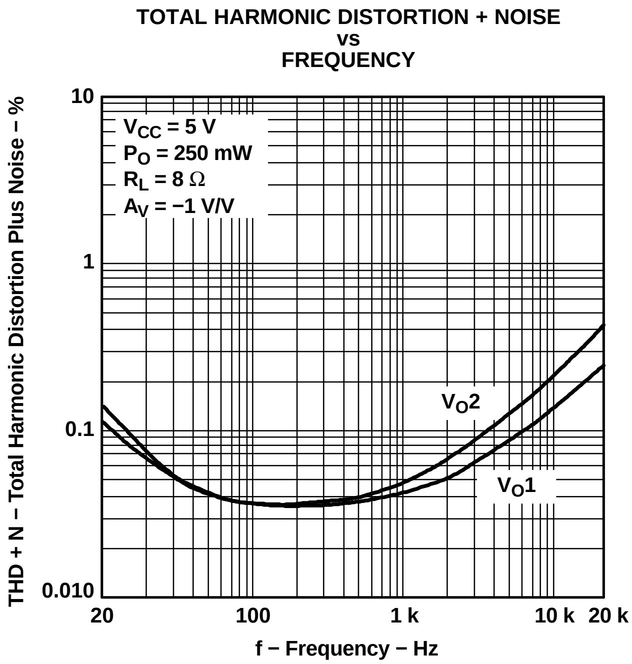


Figure 1.

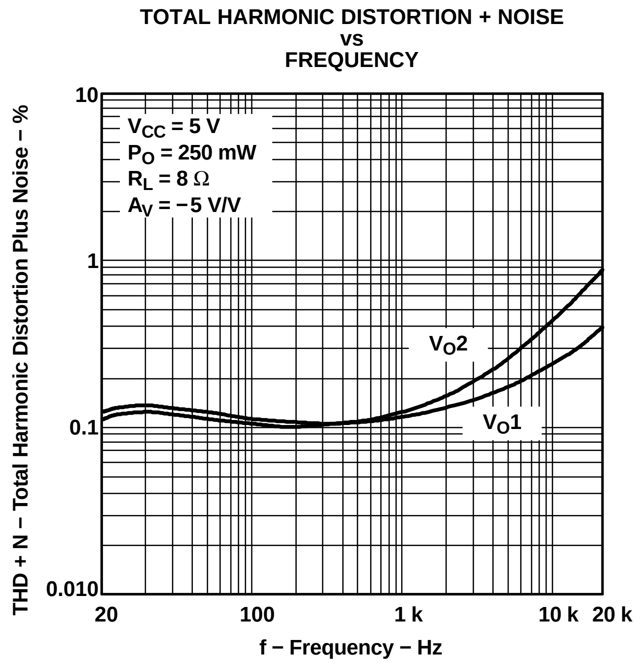


Figure 2.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

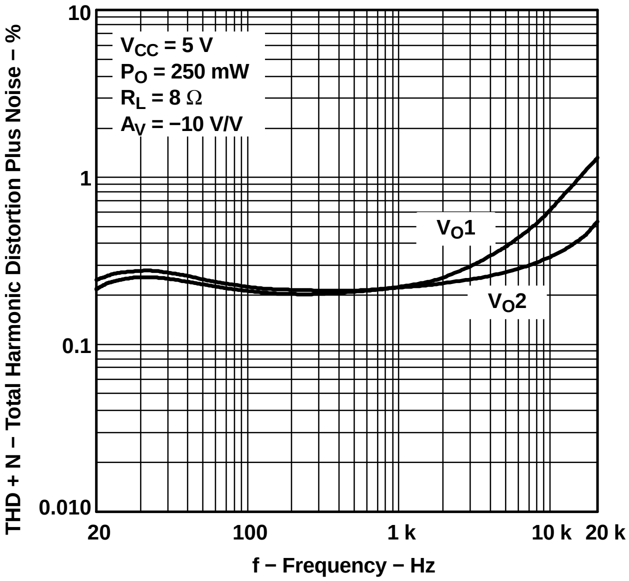


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

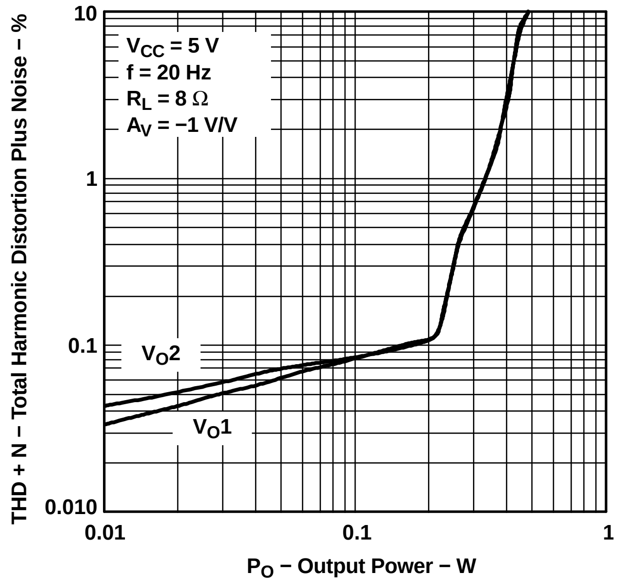


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

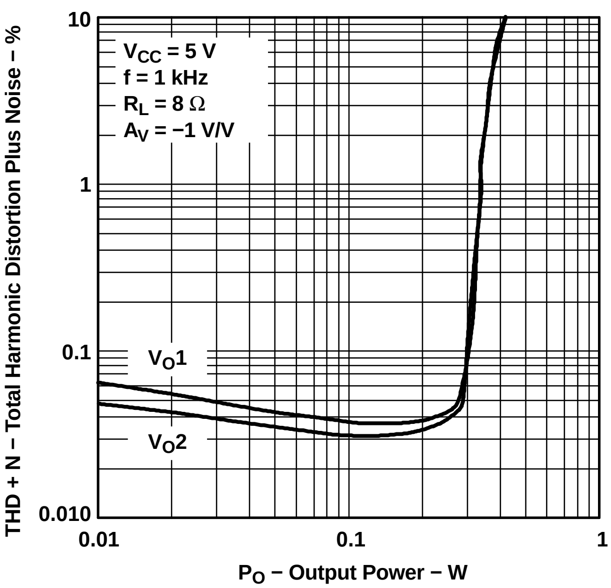


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

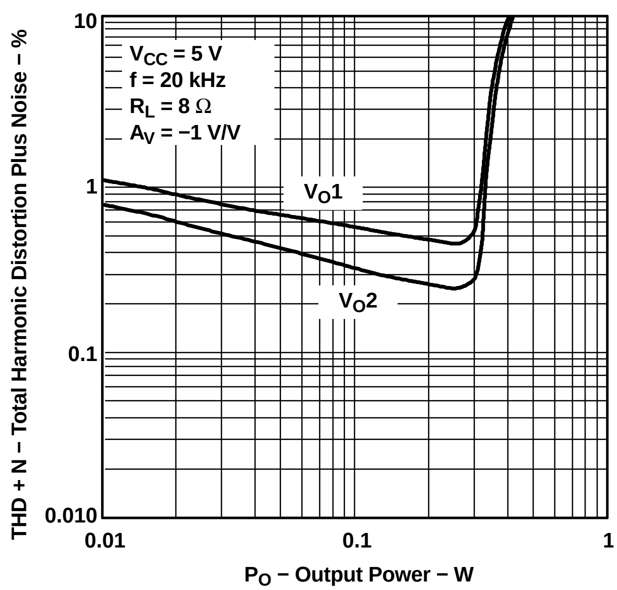


Figure 6.

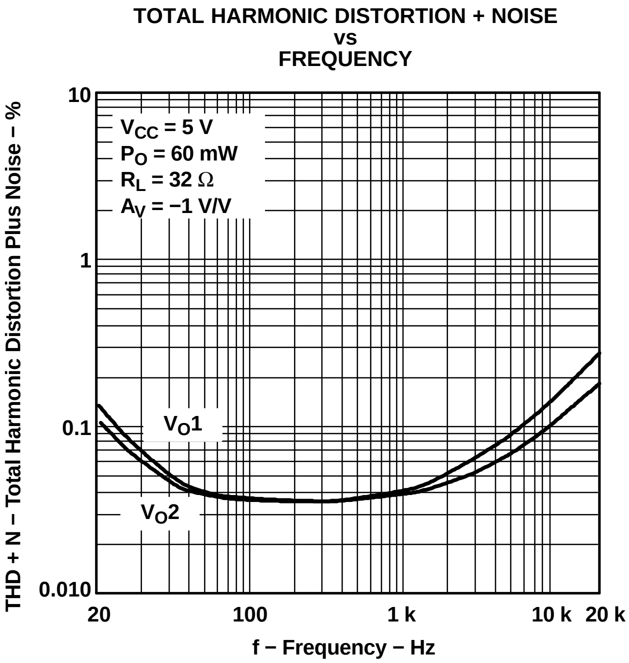


Figure 7.

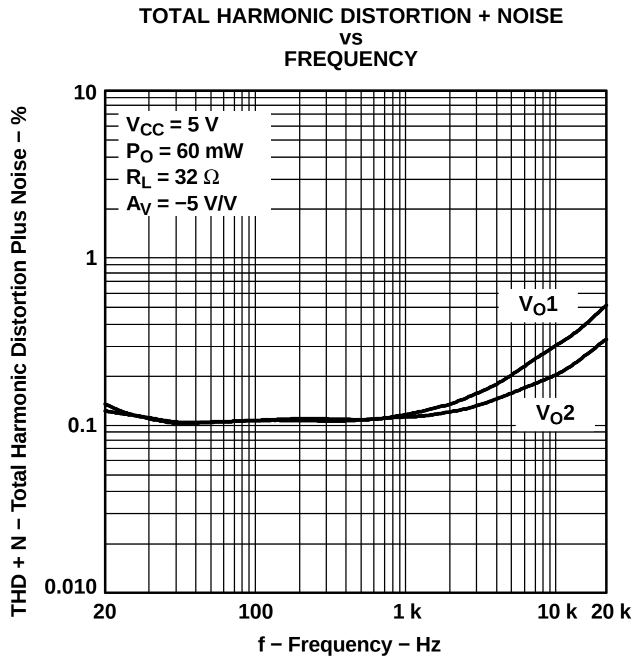


Figure 8.

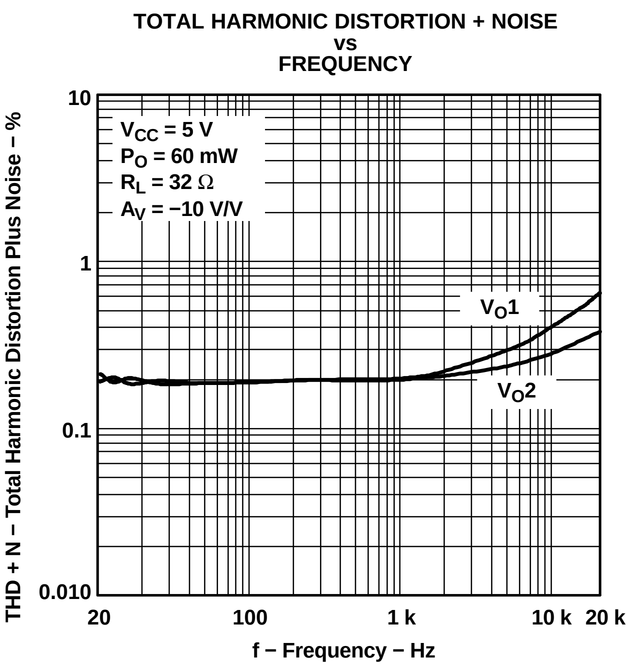


Figure 9.

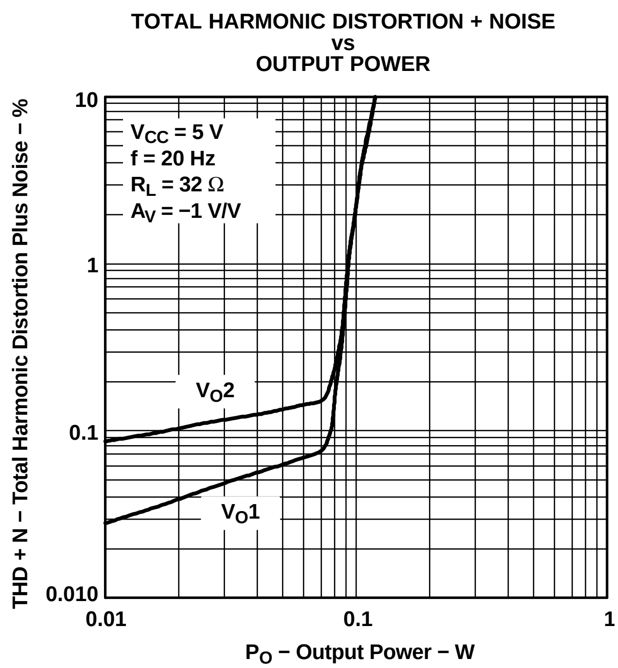


Figure 10.

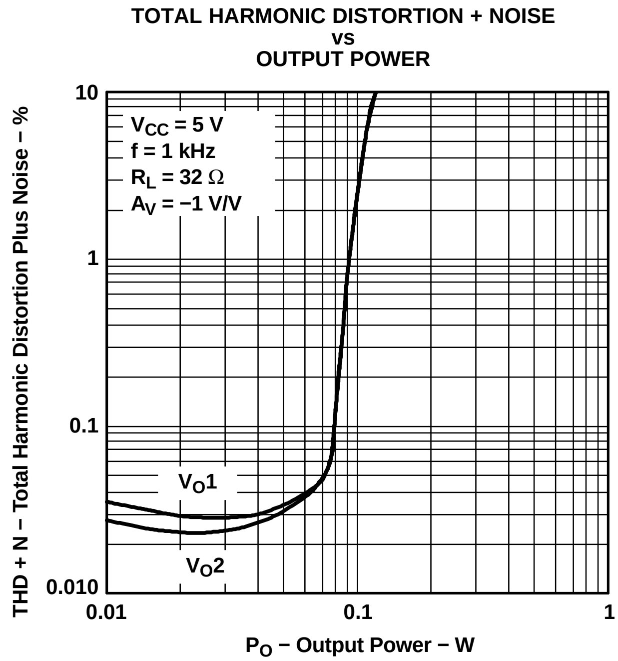


Figure 11.

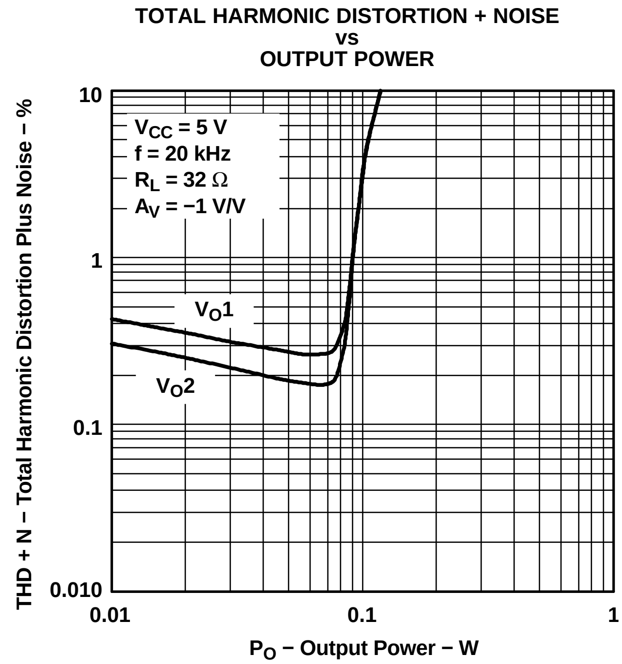


Figure 12.

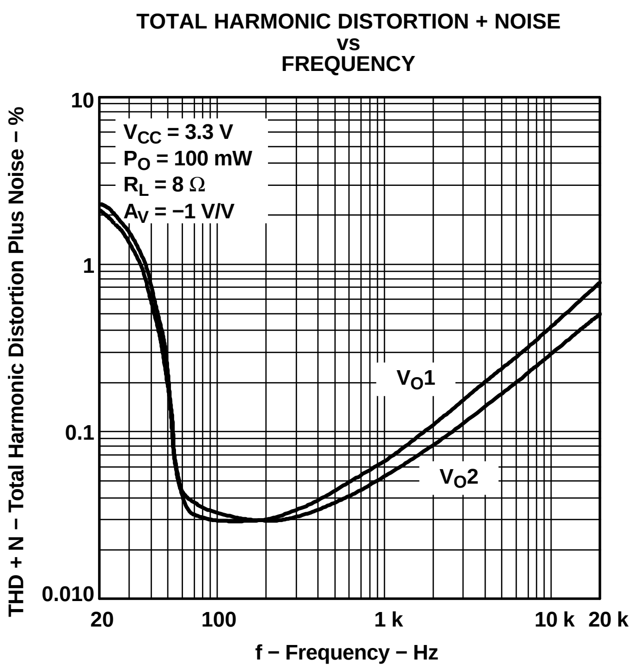


Figure 13.

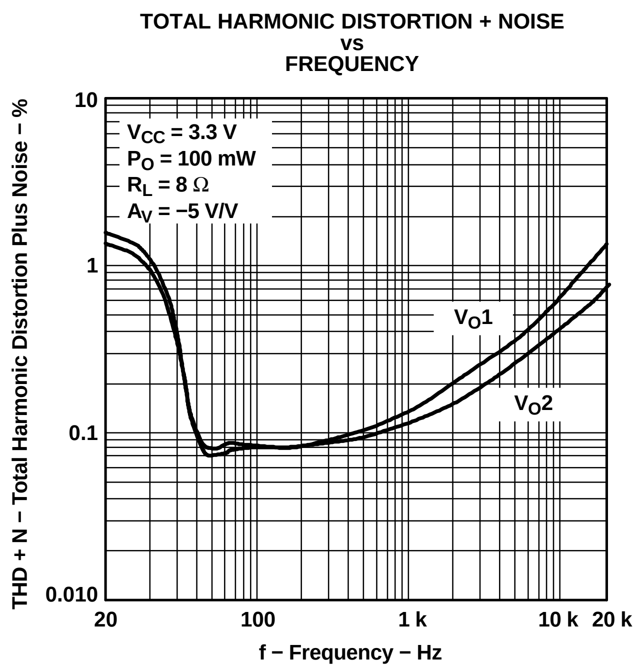


Figure 14.

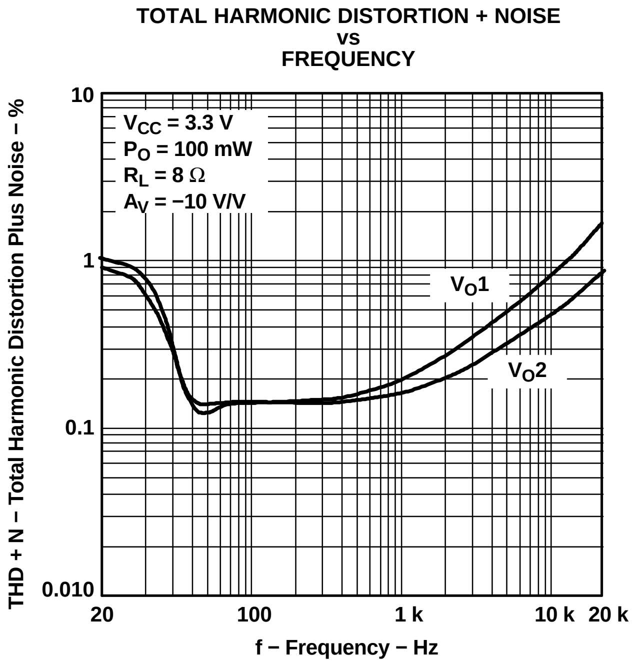


Figure 15.

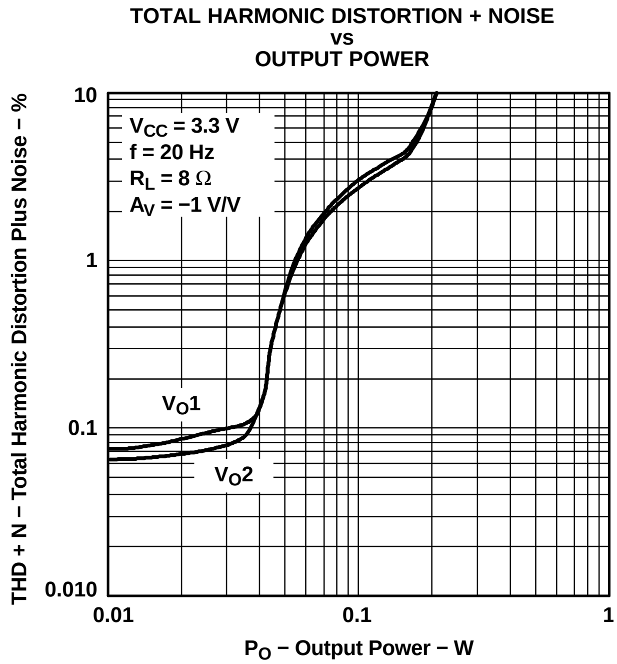


Figure 16.

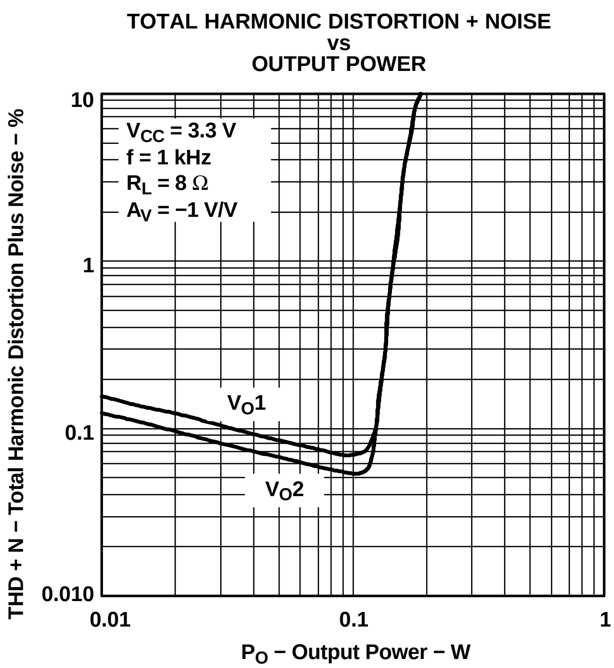


Figure 17.

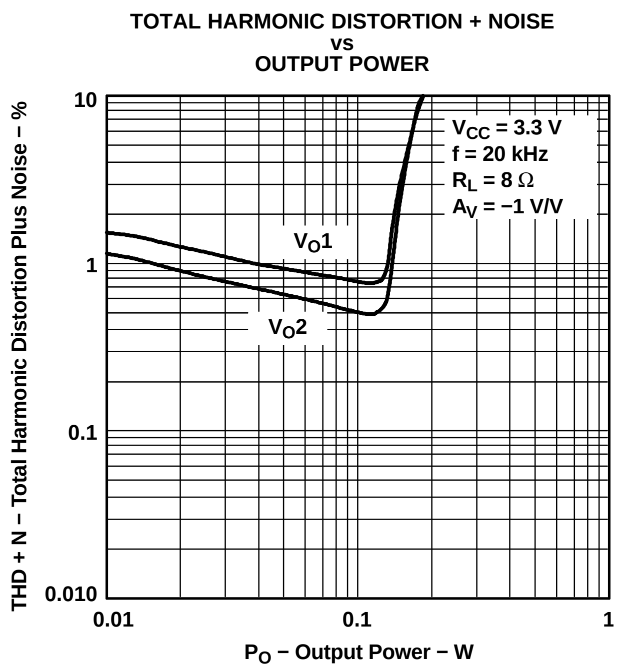


Figure 18.

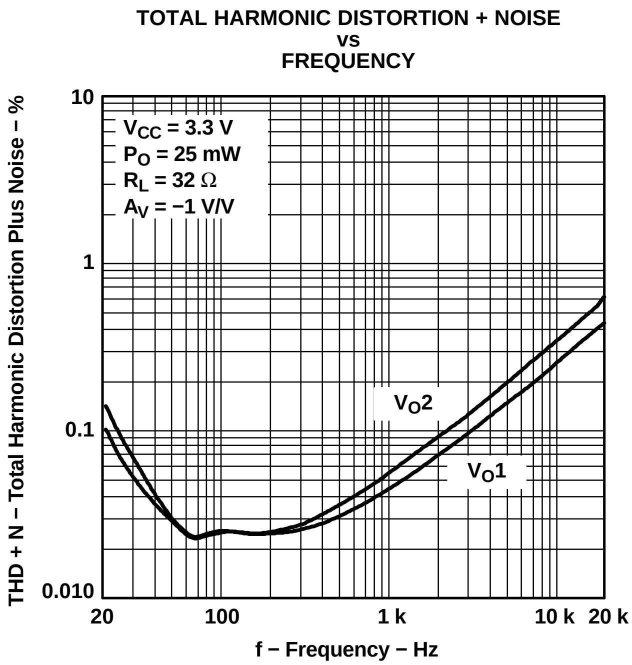


Figure 19.

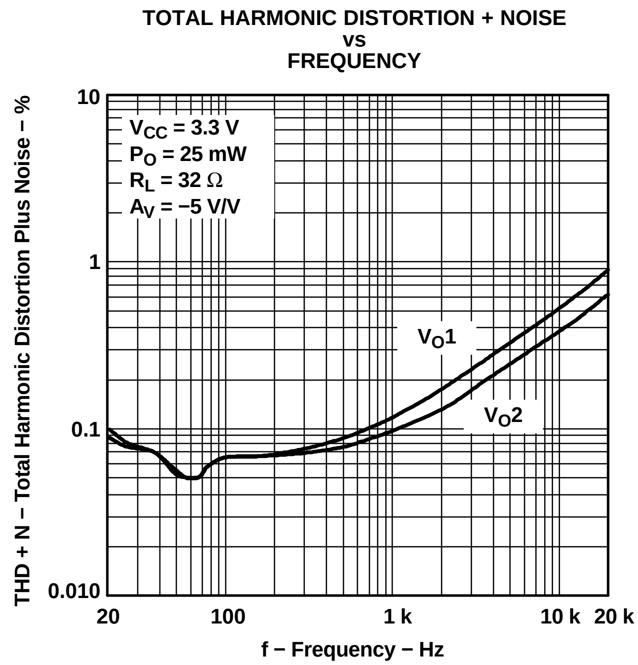


Figure 20.

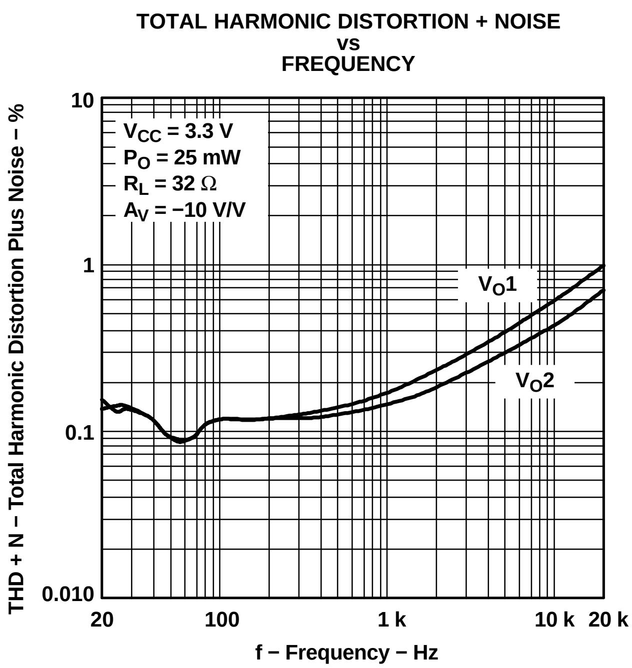


Figure 21.

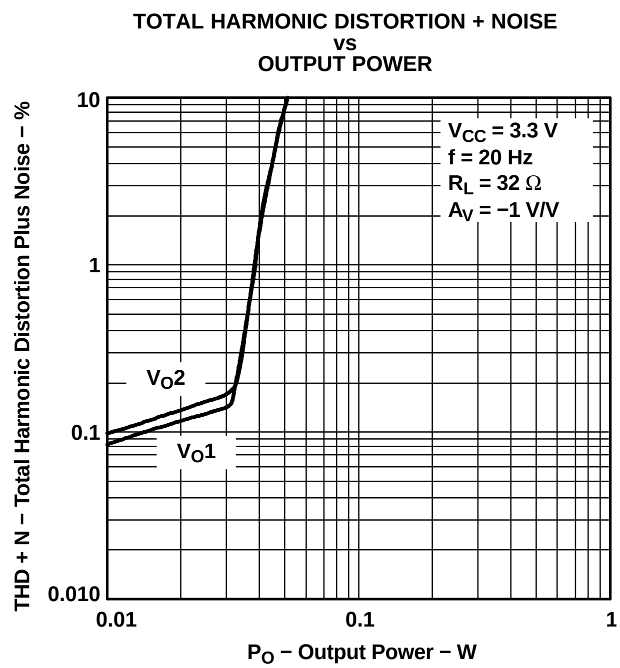


Figure 22.

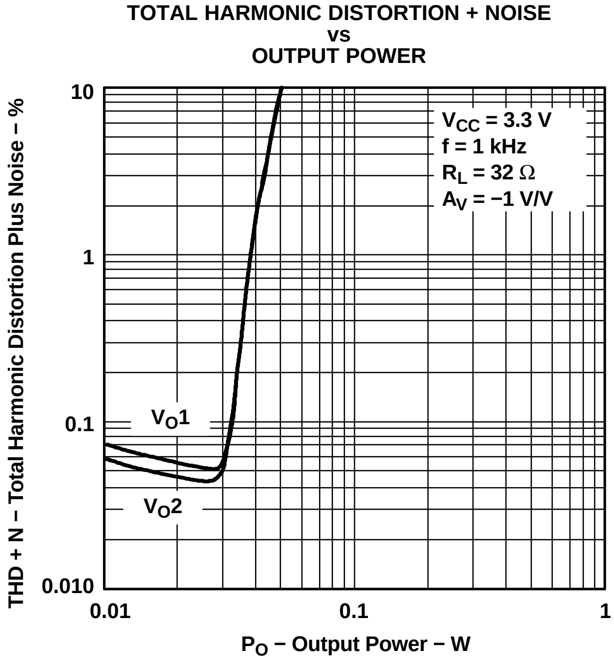


Figure 23.

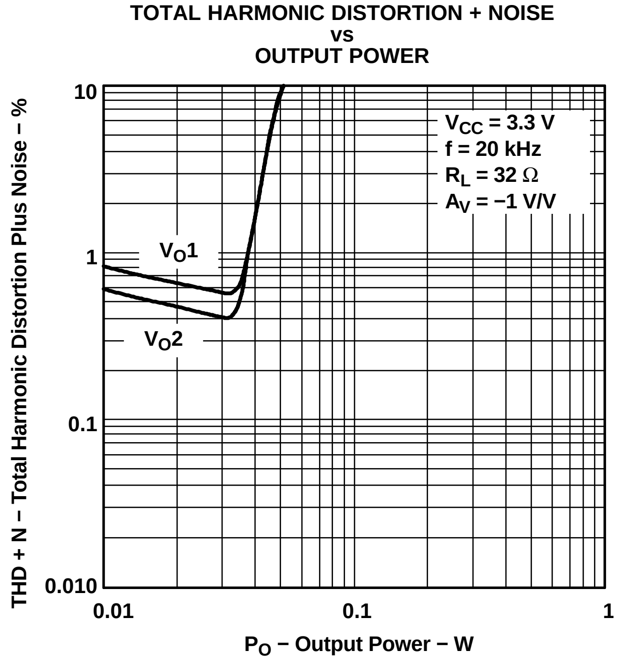


Figure 24.

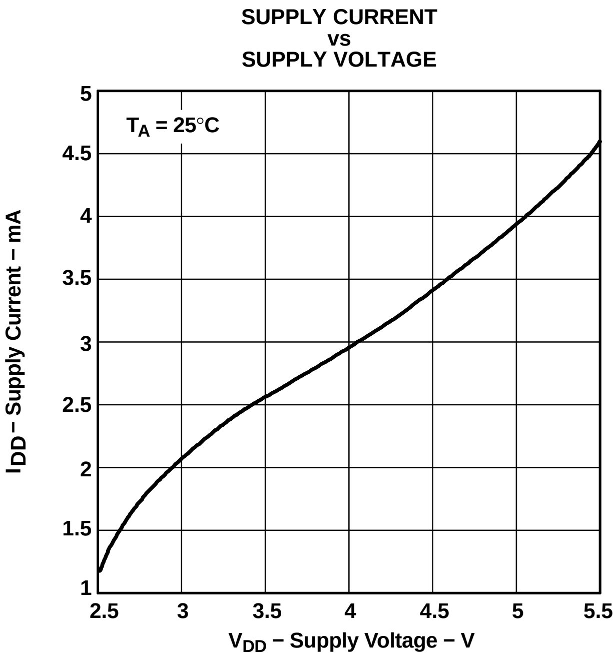


Figure 25.

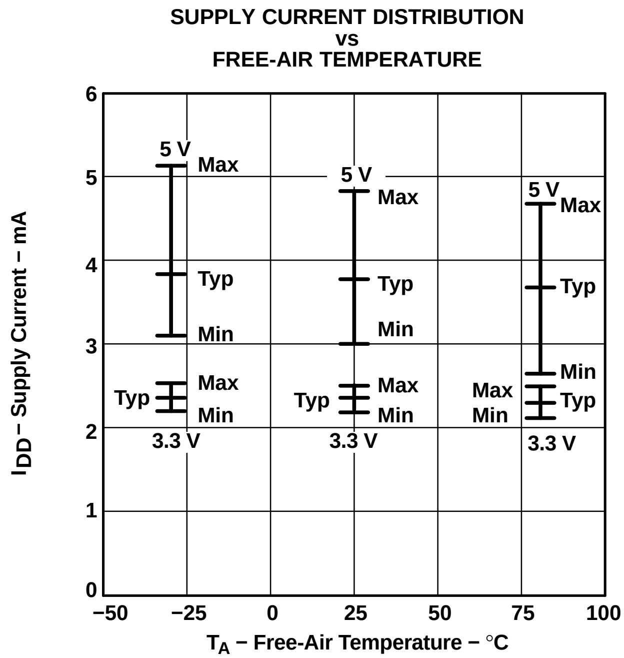


Figure 26.

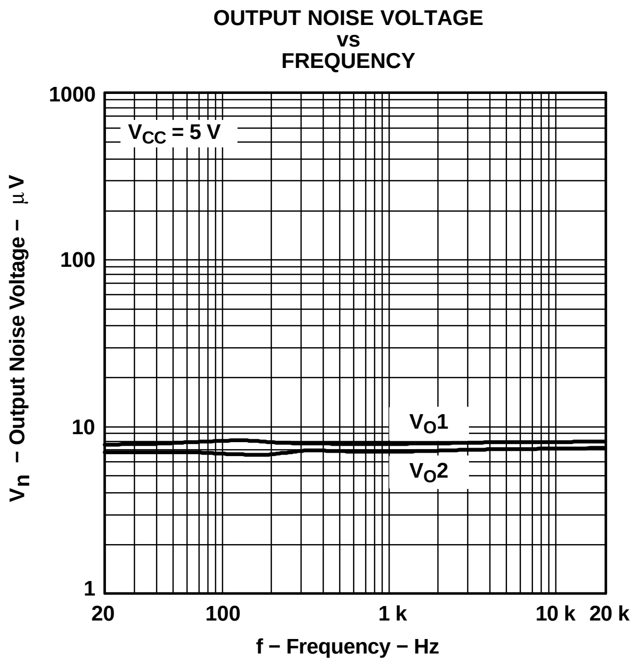


Figure 27.

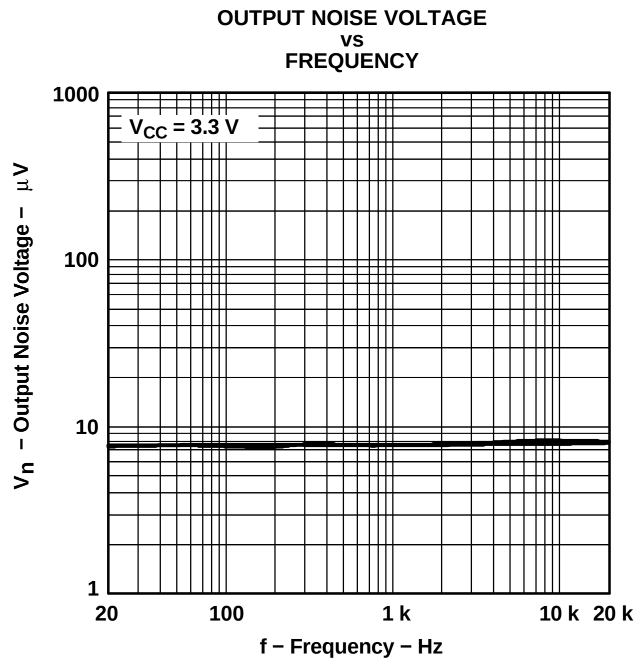


Figure 28.

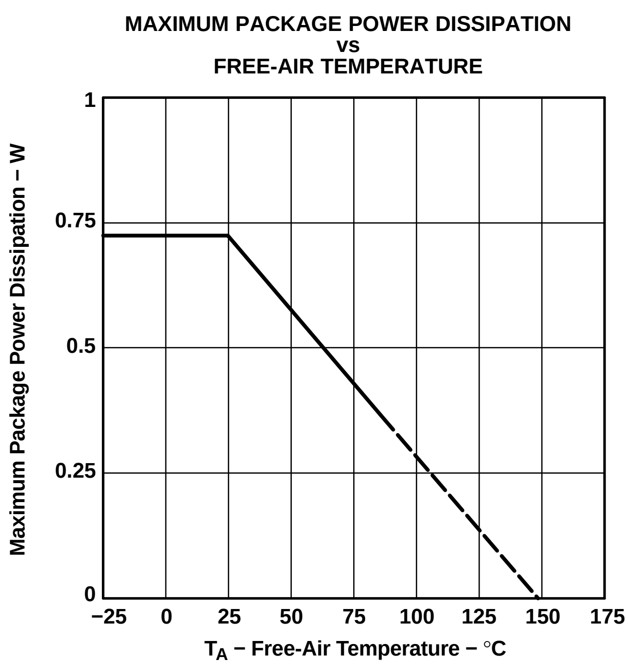


Figure 29.

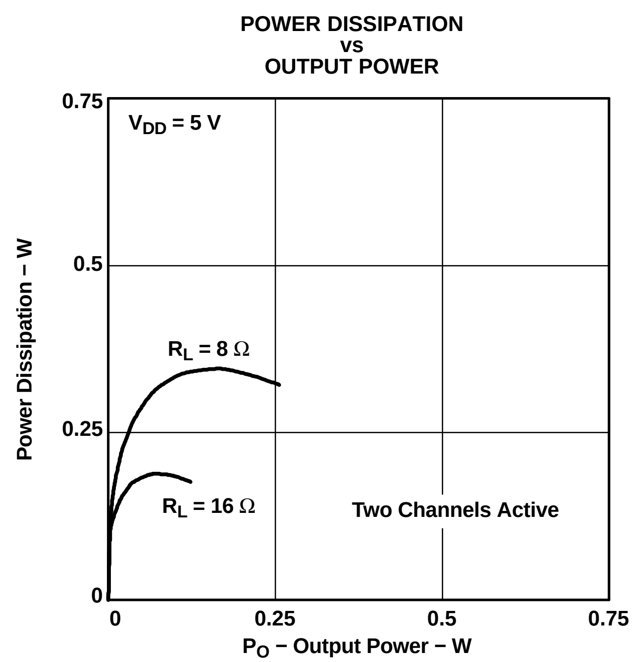


Figure 30.

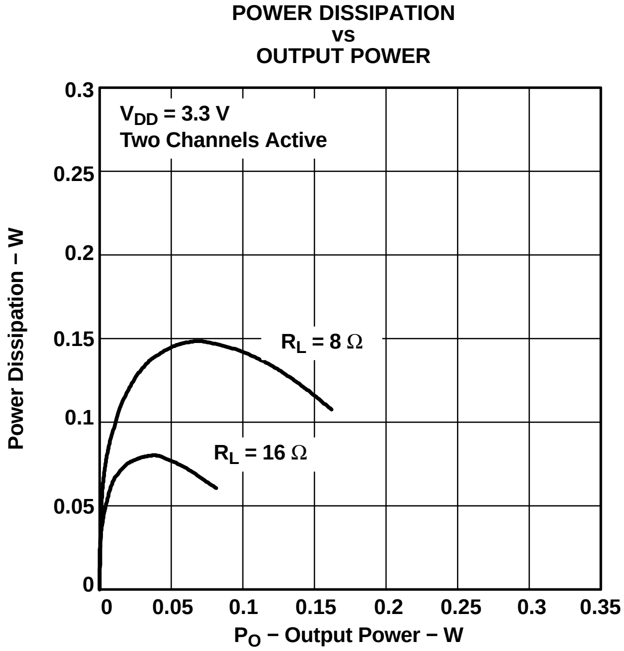


Figure 31.

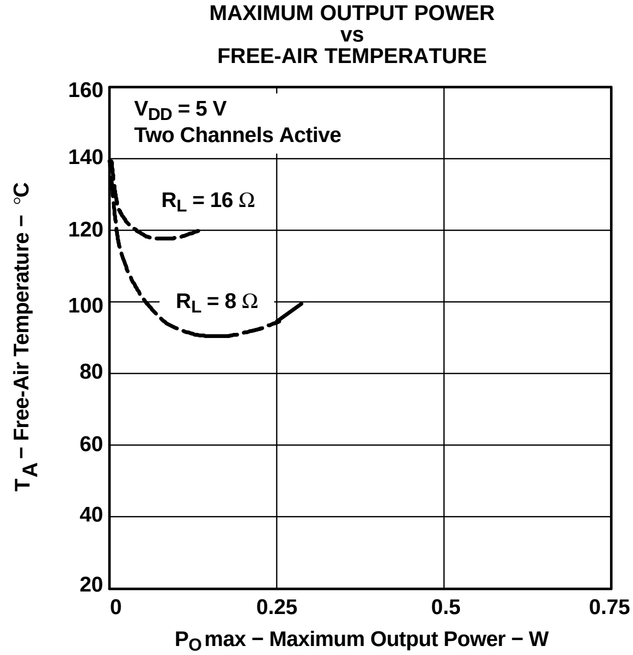


Figure 32.

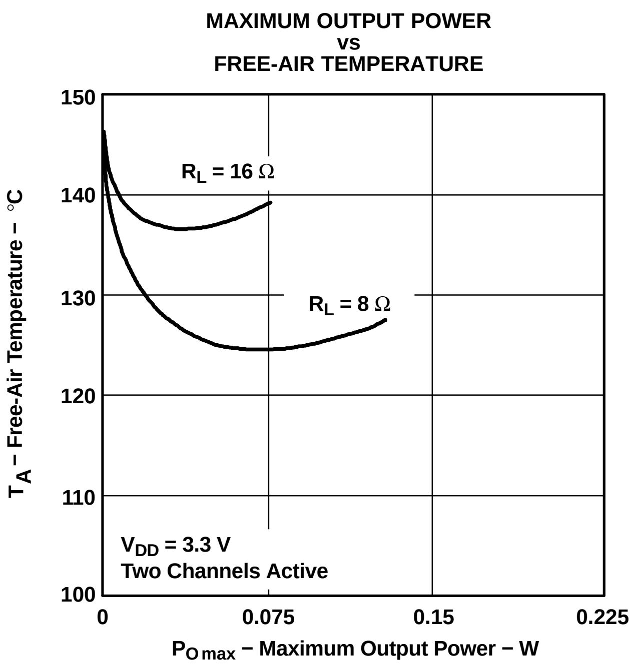


Figure 33.

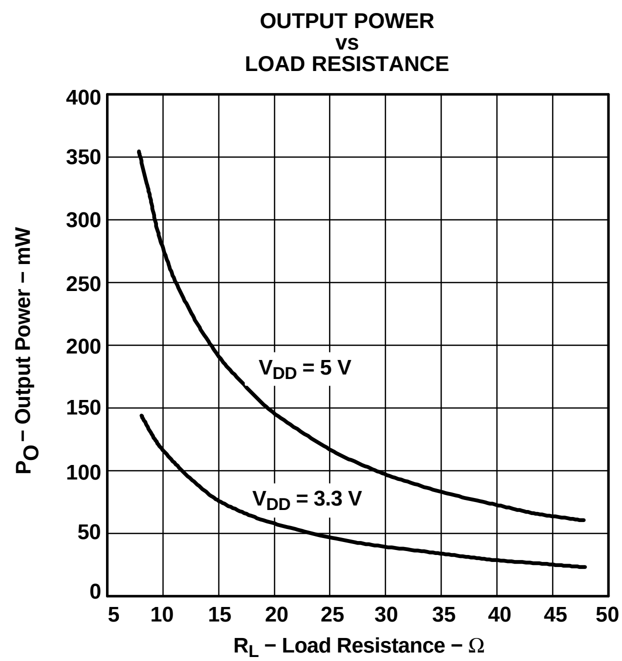


Figure 34.

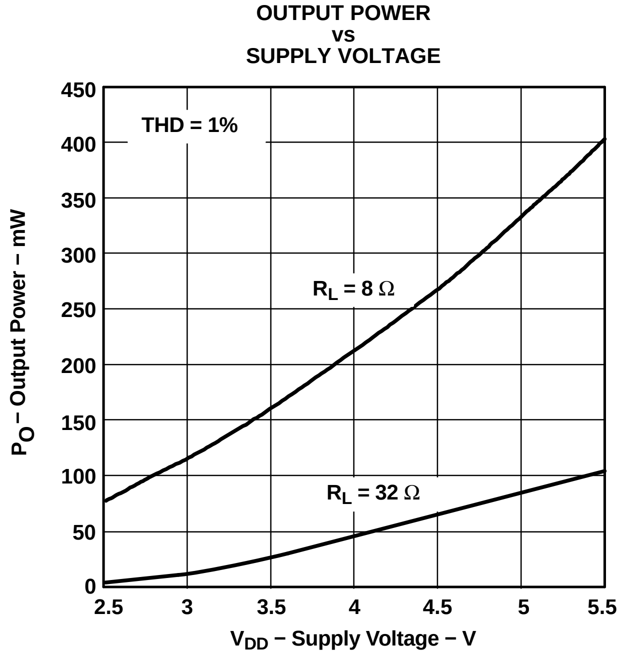


Figure 35.

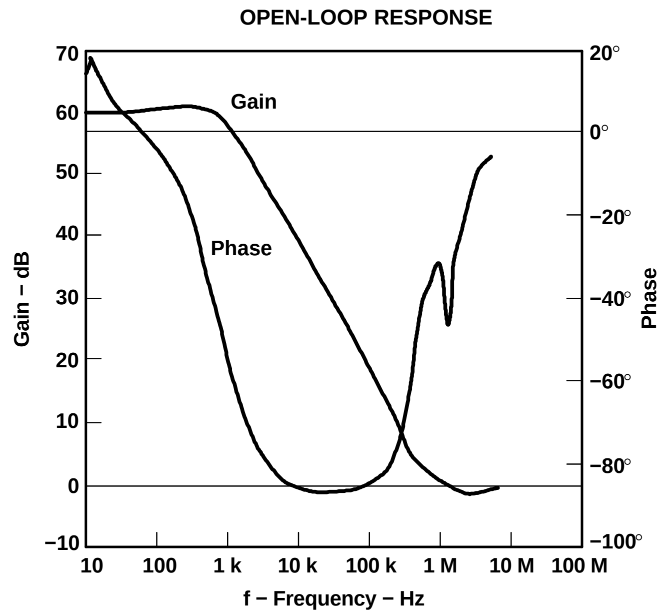


Figure 36.

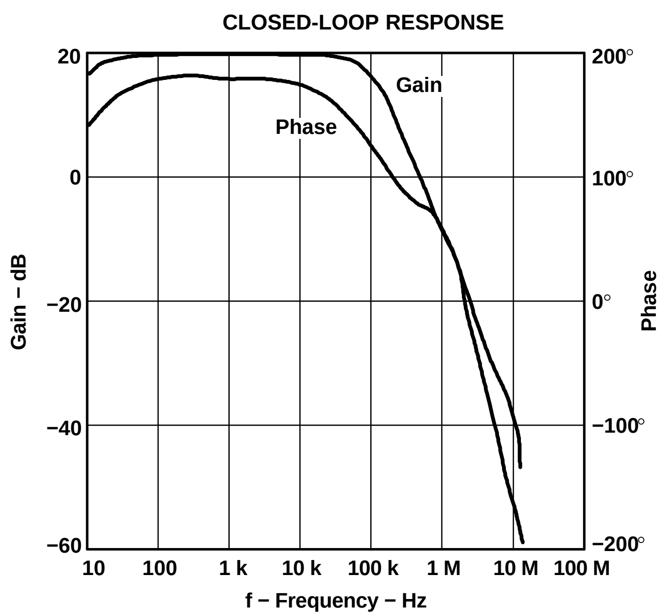


Figure 37.

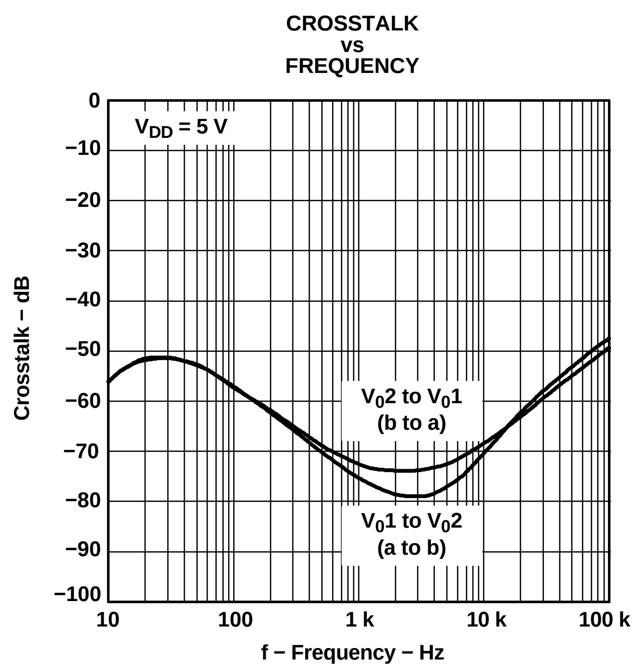


Figure 38.

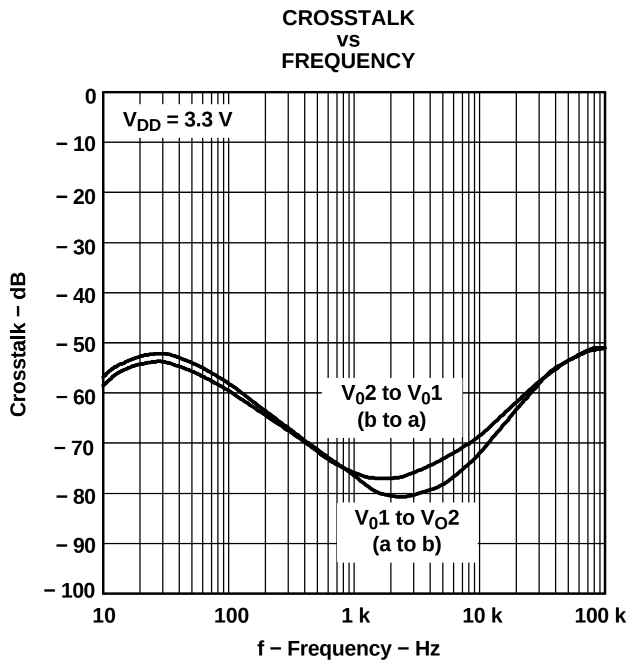


Figure 39.

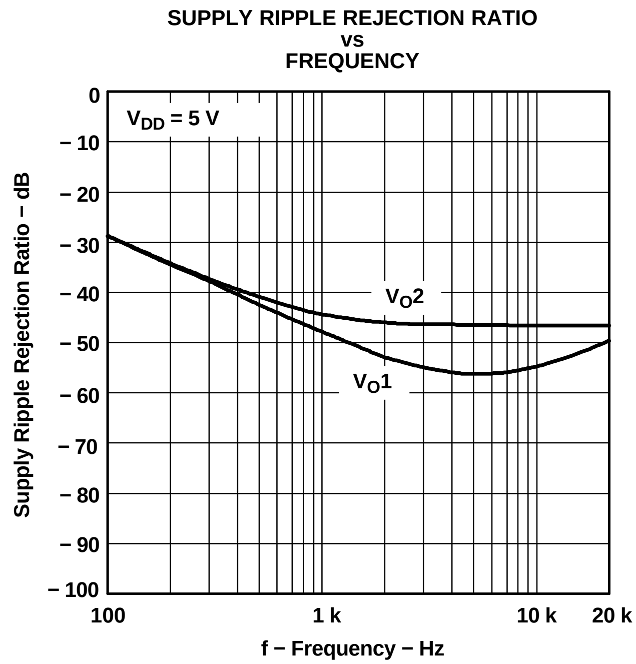


Figure 40.

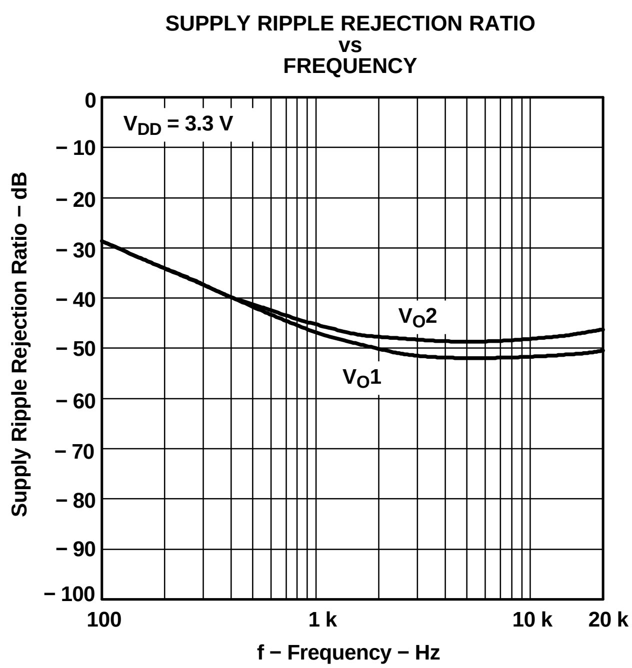
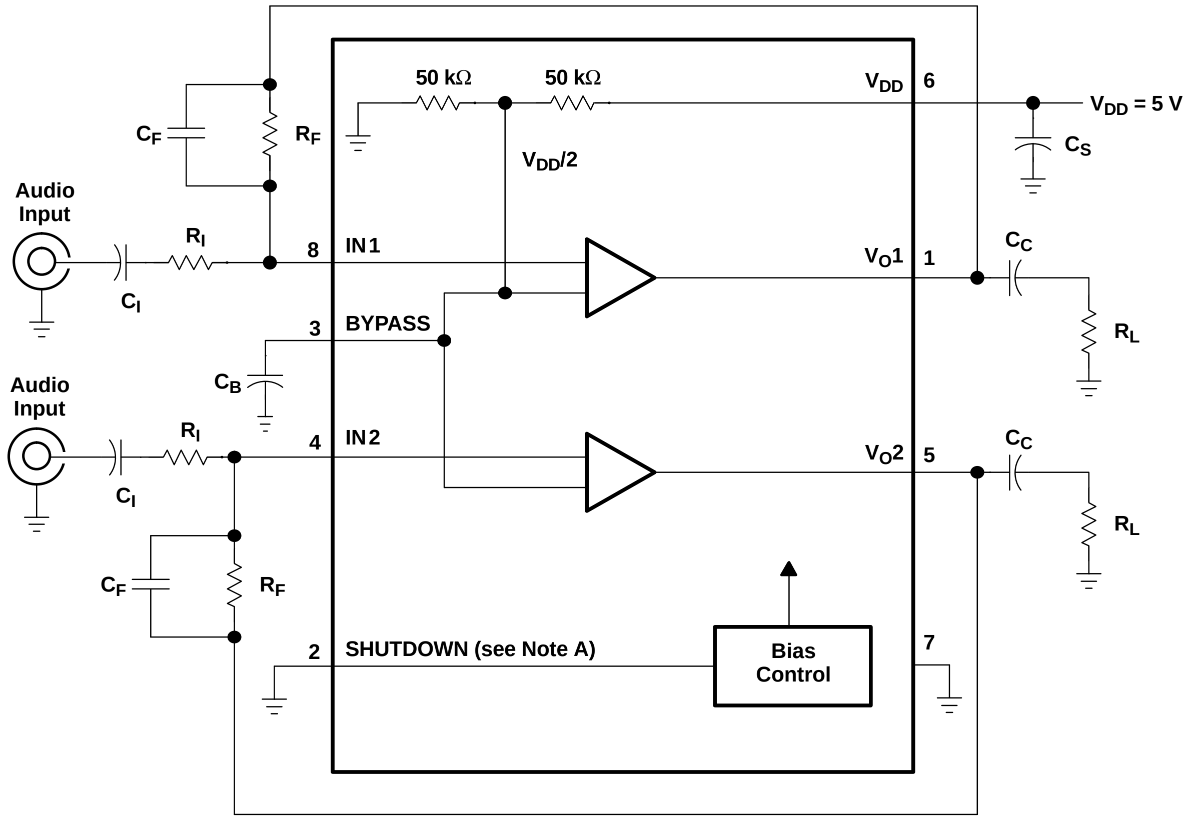


Figure 41.

APPLICATION INFORMATION

SELECTION OF COMPONENTS

Figure 42 is a schematic diagram of a typical application circuit.



NOTE A: SHUTDOWN must be held low for normal operation and asserted high for shutdown mode.

Figure 42. TPA302 Typical Notebook Computer Application Circuit

Gain Setting Resistors, R_F and R_I

The gain for the TPA302 is set by resistors R_F and R_I according to Equation 1.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \tag{1}$$

Given that the TPA302 is an MOS amplifier, the input impedance is high; consequently, input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together, it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in Equation 2.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{2}$$

As an example, consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The gain of the amplifier would be –5 and the effective impedance at the inverting terminal would be 8.3 kΩ, which is within the recommended range.

APPLICATION INFORMATION (continued)

For high-performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. In effect, this creates a low-pass filter network with the cutoff frequency defined in Equation 3.

$$f_{c(lowpass)} = \frac{1}{2\pi R_F C_F} \tag{3}$$

For example, if R_F is 100 kΩ and C_F is 5 pF, then $f_{c(lowpass)}$ is 318 kHz, which is well outside of the audio range.

Input Capacitor, C_I

In the typical application, input capacitor C_I is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in Equation 4.

$$f_{c(highpass)} = \frac{1}{2\pi R_I C_I} \tag{4}$$

The value of C_I is important to consider as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 4 is reconfigured as Equation 5.

$$C_I = \frac{1}{2\pi R_I f_{c(highpass)}} \tag{5}$$

In this example, C_I is 0.4 µF; so, one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (>10). For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

Power Supply Decoupling, C_S

The TPA302 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the power amplifier is recommended.

Midrail Bypass Capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During startup or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it cannot be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 25-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in Equation 6 should be maintained.

$$\frac{1}{\left(C_B \times 25\ k\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \tag{6}$$

As an example, consider a circuit where C_B is 0.1 µF, C_I is 0.22 µF and R_I is 10 kΩ. Inserting these values into Equation 6 results in: 400 ≤ 454 which satisfies the rule. Recommended values for bypass capacitor C_B are 0.1-µF to 1-µF, ceramic or tantalum low-ESR, for the best THD and noise performance.

APPLICATION INFORMATION (continued)

OUTPUT COUPLING CAPACITOR, C_C

In the typical single-supply, single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 7.

$$f_C = \frac{1}{2\pi R_L C_C} \tag{7}$$

The main disadvantage, from a performance standpoint, is that the load impedances are typically small, which drives the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 µF is chosen and loads vary from 8 Ω, 32 Ω, and 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

Table 1. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
8 Ω	68 µF	293 Hz
32 Ω	68 µF	73 Hz
47,000 Ω	68 µF	0.05 Hz

As Table 1 indicates, most of the bass response is attenuated into 8-Ω loads while headphone response is adequate and drive into line level inputs (a home stereo for example) is good.

The output coupling capacitor required in single-supply, SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described previously still hold with the addition of the following relationship:

$$\frac{1}{\left(C_B \times 25\ \text{k}\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \ll \frac{1}{R_L C_C} \tag{8}$$

SHUTDOWN MODE

The TPA302 employs a shutdown mode of operation designed to reduce quiescent supply current, $I_{DD(q)}$, to the absolute minimum level during periods of nonuse for battery-power conservation. For example, during device sleep modes or when other audio-drive currents are used (i.e., headphone mode), the speaker drive is not required. The SHUTDOWN input terminal should be held low during normal operation when the amplifier is in use. Pulling SHUTDOWN high causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} ~ 0.6 µA. SHUTDOWN should never be left unconnected because amplifier operation would be unpredictable.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this applications section. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

THERMAL CONSIDERATIONS

A prime consideration when designing an audio amplifier circuit is internal power dissipation in the device. The curve in Figure 43 provides an easy way to determine what output power can be expected out of the TPA302 for a given system ambient temperature in designs using 5-V supplies. This curve assumes no forced airflow or additional heat sinking.

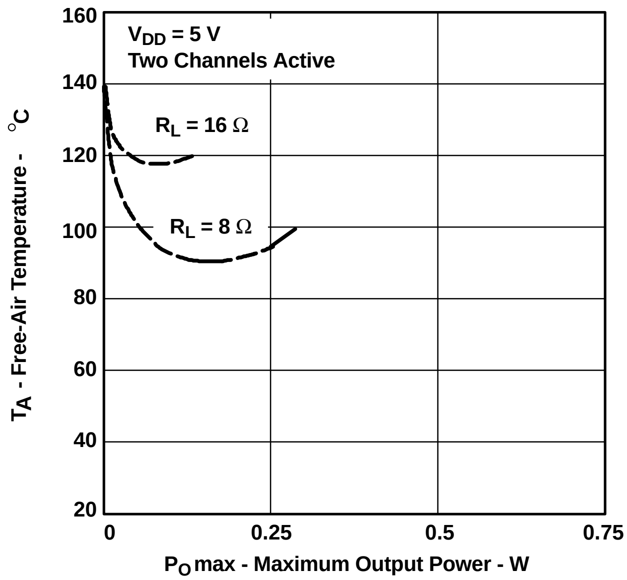


Figure 43. Free-Air Temperature Versus Maximum Output Power

5-V VERSUS 3.3-V OPERATION

The TPA302 was designed for operation over a supply range of 2.7 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation because they are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. Supply current is slightly reduced from 4 mA (typical) to 2.25 mA (typical). The most important consideration is that of output power. Each amplifier in the TPA302 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed when $V_{O(PP)}$ = 4 V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into the load before distortion begins to become significant.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA302D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TPA302	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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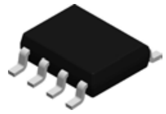
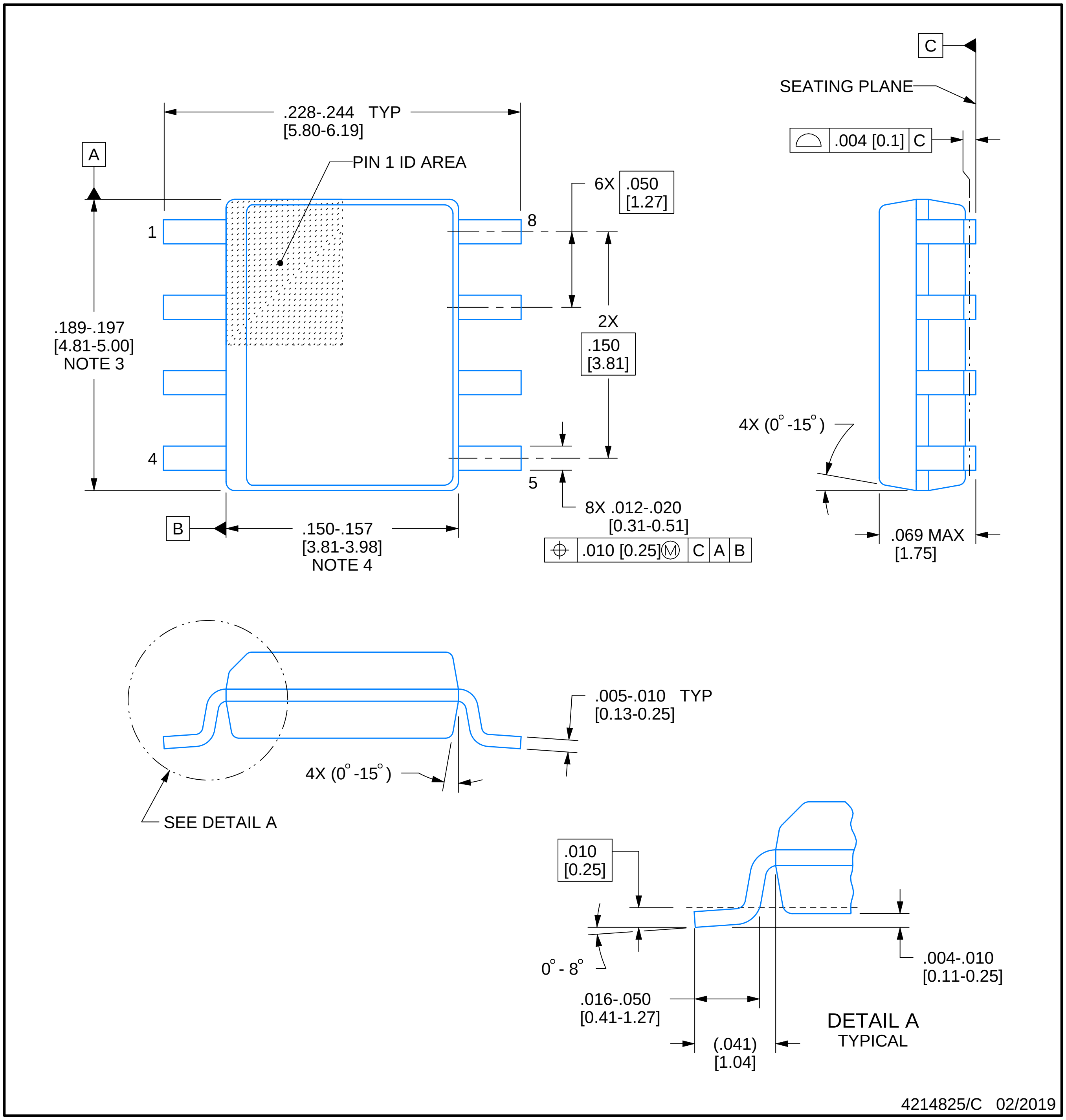


PACKAGE OUTLINE

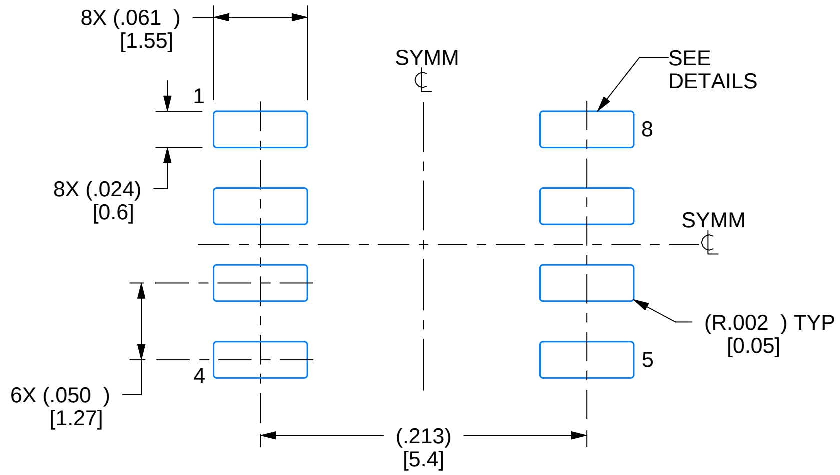
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

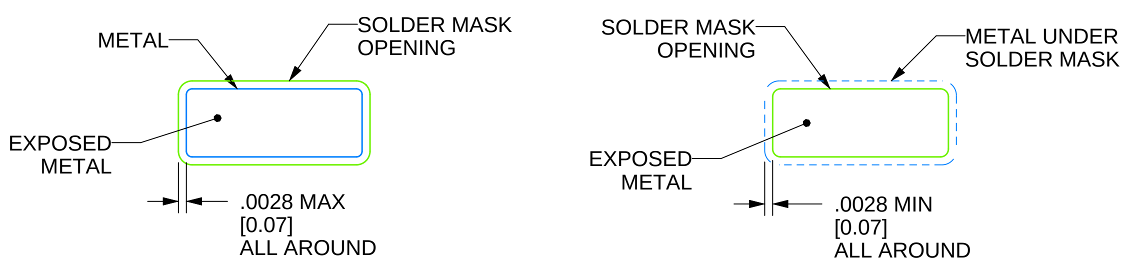


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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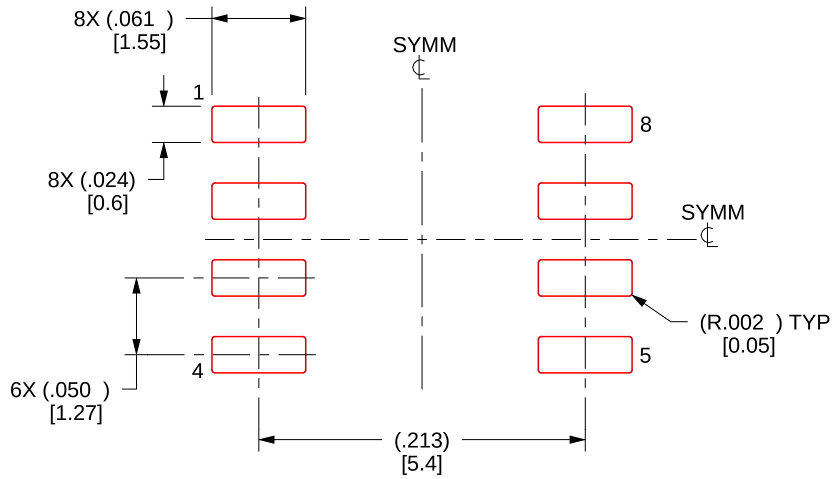
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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