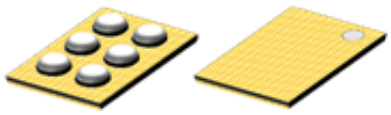
LD57100

Datasheet

1 A ultra low-dropout LDO with bias



Flip Chip6 (0.8x1.2 mm)

Features

- Input voltage from V_{OUT} to 5.5 V
- Input bias supply pin from 3.0 V to 5.5 V
- Ultra low-dropout voltage (40 mV typ. at 1 A load)
- Low ground current (35 µA typ. at no load)
- Output voltage tolerance: ±1% all over temperature range, ±0.5% at 25 °C
- 1 A guaranteed output current
- 50 mV output voltage step available from 0.4 V to 1.8 V
- 100 mV output voltage step available from 1.9 V to 3.6 V
- Adjustable version from 0.5 V to 3.0 V
- Logic-controlled electronic shutdown
- Internal current limit
- Thermal shutdown
- Output active discharge function
- Available in Flip Chip6 (0.8x1.2 mm) package
- Temperature range: -40 °C to 85 °C

Applications

Product status link
LD57100

- Smartphones
- Cameras
- Low voltage, low noise post regulation

Description

The LD57100 is a high accuracy voltage regulator, which provides 1 A of current. It is equipped with an NMOS pass transistor, whose gate is biased by a dedicated pin, thus allowing the ultra-low drop performance even at very low input voltages.

It is available in Flip Chip6 (0.8x1.2 mm), maximizing the space saving. This device is stabilized with a small ceramic capacitor on the output. The ultra low drop, low quiescent current and short-circuit protection make the LD57100 suitable for low power battery-operated applications.

An enable logic control function puts the LD57100 in shutdown mode allowing a total current consumption lower than 0.1 µA. Thermal protection is also included.

1 Diagrams

Figure 1. **Block diagram fixed version**

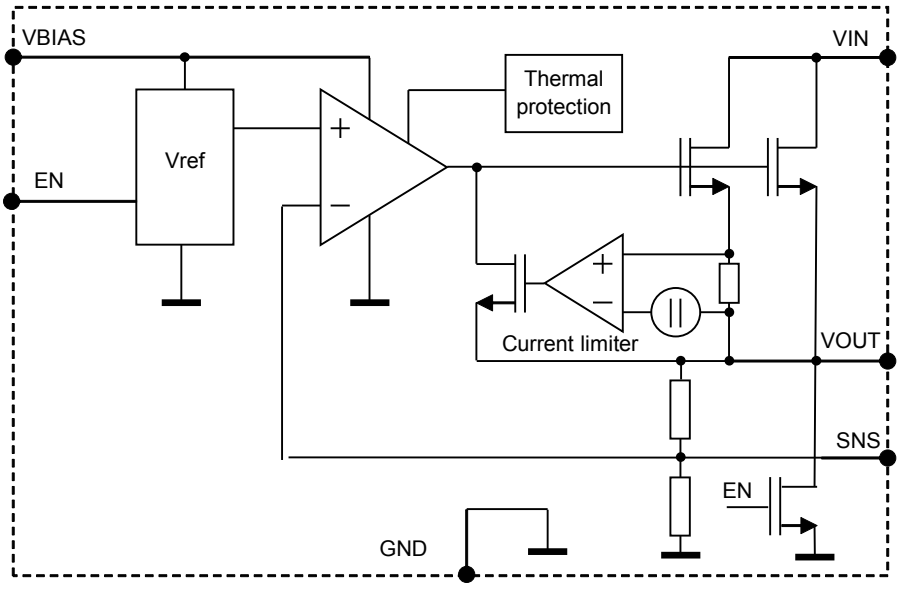
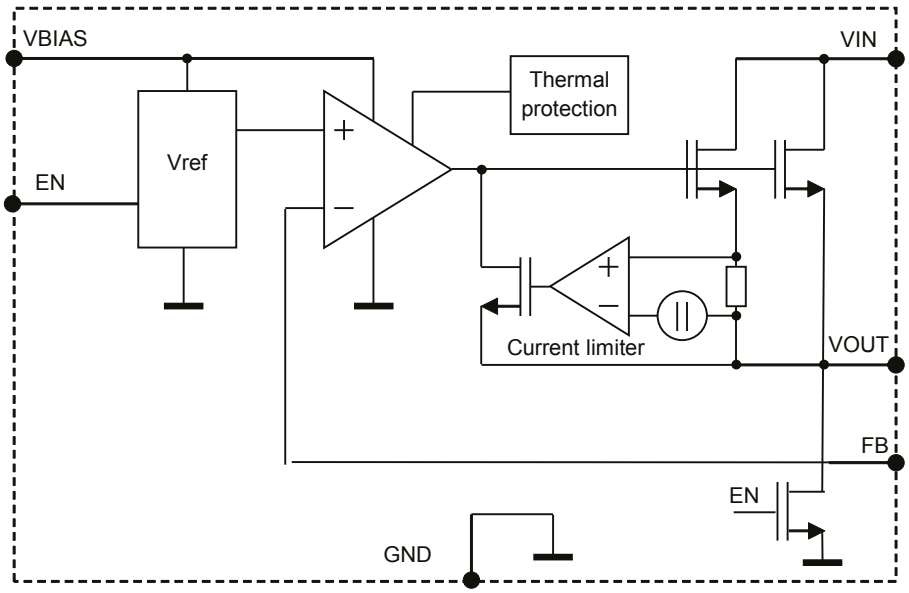


Figure 2. **Block diagram adjustable version**



2 Pin configuration

Figure 3. **Pin connection (top view)**

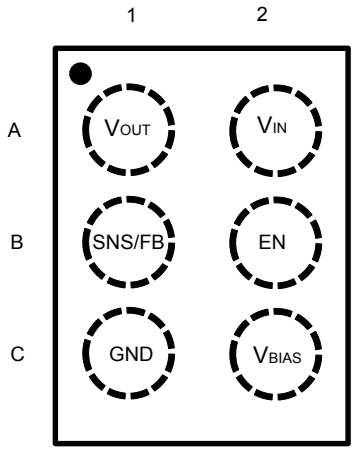


Table 1. **Pin description**

Pin #	Symbol	Functions
A1	V_{OUT}	Output voltage
A2	V_{IN}	Input voltage
B1	SNS / FB	Output voltage sense pin in fixed version. Connect to the load with a separate PCB track. Feedback pin in adjustable version. Connect to the resistor divider central node
B2	EN	Enable pin logic input: low = shutdown, high = active
C1	GND	Common ground
C2	V_{BIAS}	Bias supply input

3 Typical application circuits

Figure 4. **Typical application for fixed version**

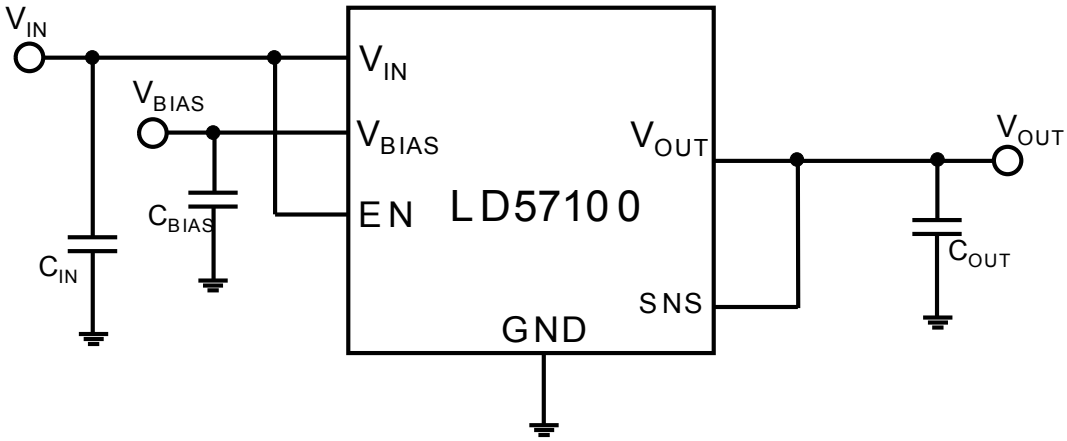


Figure 5. **Typical application for adjustable version**

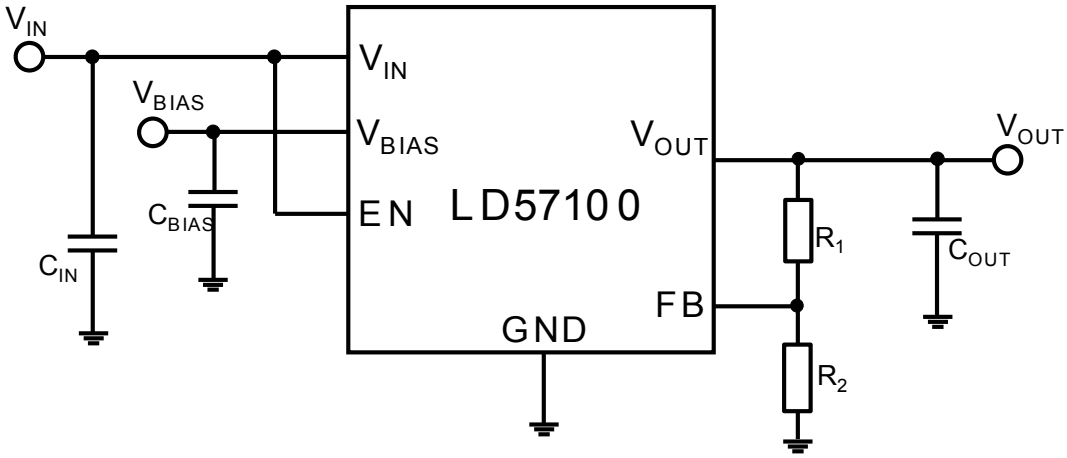


Table 2. **Typical application components**

Symbol	Value	Description	Note
C_{IN}	1 µF	Input capacitor	Ceramic type
C_{BIAS}	4.7 µF	Control logic bypass capacitor	Ceramic type
C_{OUT}	10 µF	Output capacitor	Ceramic type
R_1		Output voltage side resistor	See Section 6.4 VOUT setting (adjustable version)
R_2		Ground side resistor	<500 kΩ max.

4 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}, V_{BIAS}	Input voltage	-0.3 to 7	V
V_{OUT}, V_{FB}, V_{SNS}	Output voltage	-0.3 to V_{IN} + 0.3	V
V_{EN}	Enable input voltage	-0.3 to 7	V
I_{OUT}	Output current	Internally limited (see I_{SC} in Table 6. Electrical characteristics)	A
T_{STG}	Storage temperature range	- 40 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient(1)	60	°C/W

1. *We considered the STD JEDEC board 4 layers (2s2p) 101.5 x114.5 mm with a top copper plane of 4x4 mm.*

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
		CDM	500	V

5 Electrical characteristics

V_{BIAS} = 3.0 V or V_{OUT} + 1.6 V (whichever is greater); V_{IN} = $V_{OUT(NOM)}$ + 0.3 V; I_{OUT} = 1 mA; C_{IN} = 4.7 µF, C_{OUT} = 10 µF; C_{BIAS} = 1 µF, V_{EN} = 1 V; typical values are at T_J = 25 °C; min./max. values are at -40 °C ≤ T_J ≤ 85 °C, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		V_{OUT} + V_{DROP}		5.5	V
V_{BIAS}	Operating bias voltage		(V_{OUT} + 1.60) ≥ 3.0		5.5	V
V_{UVLO}	Bias undervoltage lockout	V_{BIAS} rising T_J = 25 °C	1.45	1.6	1.75	V
		Hysteresis T_J = 25 °C	0.15	0.2	0.25	V
V_{REF}	Reference voltage for adjustable devices	T_J = 25 °C;		0.5		V
V_{OUT}	Output voltage accuracy	All versions, as per conditions above		± 0.5		%
		$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ $V_{OUT(NOM)}$ + 1.0 V; 3.0 V or $V_{OUT(NOM)}$ + 1.6 V (whichever is greater) ≤ V_{BIAS} ≤ 5.5 V; I_{OUT} = 1 mA to 1 A; -40 °C ≤ T_J ≤ 85 °C	-1.0		+1.0	%
ΔV_{OUT-IN}	V_{IN} static regulation	$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 5.0 V, T_J = 25 °C		0.01	0.1	% / V
$\Delta V_{OUT-BIAS}$	V_{BIAS} line regulation	3.0 V or $V_{OUT(NOM)}$ + 1.6 V (whichever is greater) ≤ V_{BIAS} ≤ 5.5 V, T_J = 25 °C		0.01	0.1	% / V
$\Delta V_{OUT-LOAD}$	Static load regulation	I_{OUT} = 1 mA to 1 A, T_J = 25 °C		1.0	2.0	mV
V_{DROP}	Dropout voltage	I_{OUT} = 1 A; V_{OUT} = 97% of $V_{OUT(NOM)}$		40	80	mV
$V_{DROP-BIAS}$	Bias dropout voltage (1)	V_{BIAS}=V_{IN}; I_{OUT} = 1 A; V_{OUT} = 97% of $V_{OUT(NOM)}$		1.05	1.5	V
I_{LIM}	Output current limit	V_{OUT} = 90% $V_{OUT(NOM)}$	1.5	2	2.6	A
		V_{OUT} = 90% $V_{OUT(NOM)}$, −30 °C ≤ T_J ≤ 85 °C	1.55	2	2.6	
I_{FB}, I_{SNS}	FB/SNS pin operating current			0.1	0.5	µA
I_{BIAS}	VBIAS operating current	V_{BIAS} = 3.0 V, I_{OUT} = 0 mA		35	50	µA
$I_{Standby-BIAS}$	V_{BIAS} standby current	V_{BIAS} input current in OFF mode: V_{EN} = GND		0.1	1	µA
$I_{Standby-IN}$	V_{IN} standby current	V_{IN} input current in OFF mode: V_{EN} = GND		0.1	1	µA
V_{EN}	Enable input logic low				0.4	V
	Enable input logic high		0.9			

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{EN}	Enable pin input current	V_{EN} = V_{BIAS} = 5.5 V		0.2	1	µA
T_{ON}	Turn-on time	From assertion of V_{EN} to V_{OUT} = 98% $V_{OUT(NOM)}$, $V_{OUT(NOM)}$ = 1.0 V		160		µs
SVR_{IN-ADJ}	V_{IN} supply voltage rejection (adj version)	V_{IN} = $V_{OUT(NOM)}$+ 0.5 V +/- V_{RIPPLE} V_{RIPPLE} = 0.2 V; freq=1 kHz I_{OUT} = 10 mA; $V_{OUT(NOM)}$ = 1.0 V		70		dB
$SVR_{BIAS-ADJ}$	V_{BIAS} supply voltage rejection (adj version)	V_{BIAS} = 3.0 V +/- V_{RIPPLE}, V_{RIPPLE} = 0.2 V; freq=1 kHz; V_{IN} = $V_{OUT(NOM)}$+ 0.5 V I_{OUT} = 10 mA; $V_{OUT(NOM)}$ = 1.0 V		85		dB
e_{N-ADJ}	Output noise voltage (adj version)	V_{IN} = $V_{OUT(NOM)}$+ 0.5 V; $V_{OUT(NOM)}$ = 1.0 V; 10 Hz to 100 kHz, I_{OUT} = 1 mA		35 x V_{OUT} / V_{REF}		μV_{RMS}
SVR_{IN-FIX}	VIN supply voltage rejection (adj version)	V_{IN} = $V_{OUT(NOM)}$+ 0.5 V +/- V_{RIPPLE} V_{RIPPLE} = 0.2 V; freq=1 kHz I_{OUT} = 10 mA; $V_{OUT(NOM)}$ = 1.8 V		75		dB
$SVR_{BIAS-FIX}$	V_{BIAS} supply voltage rejection (fixed versions)	V_{BIAS} = 4.0 V +/- V_{RIPPLE} V_{RIPPLE} = 0.2 V; freq=1 kHz; V_{IN} = $V_{OUT(NOM)}$+ 0.5 V I_{OUT} = 10 mA; $V_{OUT(NOM)}$ = 1.8 V		85		dB
e_{N-FIX}	Output noise voltage (fixed versions)	V_{IN} = $V_{OUT(NOM)}$+ 0.5 V; $V_{OUT(NOM)}$ = 1.0 V; 10 Hz to 100 kHz, I_{OUT} = 1 mA		27		μV_{RMS}
R_{ON}	Output voltage discharge MOSFET			150		Ω
T_{SHDN}	Thermal shutdown			160		°C
	Hysteresis			20		

1. *Not applicable to fixed versions with $V_{OUT(NOM)}$ < 2.0 V.*

6 Application information

6.1 V_{BIAS} pin voltage requirements

The bias input is the supply of the internal driving and control circuitry. In order to assure a proper biasing of the N-channel power element, the bias pin must have a minimum voltage of 3.0 V and be 1.6 V (typically) higher than the output. If V_{IN} supply voltage meets these requirements then the bias pin can be tied to V_{IN}.

6.2 Output discharge function

The LD57100 integrates a MOSFET connected between V_{OUT} and GND. This transistor is activated when the EN pin goes to low logic level and has the function to quickly discharge the output capacitor when the device is disabled by the user.

6.3 Short-circuit and current limitation

The LD57100 is protected against short-circuit on the output. The load current is limited to the maximum value of I_{LIM} when V_{OUT} is equal to 90% of its nominal value.

6.4 V_{OUT} setting (adjustable version)

In the LD57100 adjustable version, the desired output voltage is set according to the formula below:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where R_2 cannot be higher than 500 kΩ.

Please, refer to Figure 5. Typical application for adjustable version for R_1 and R_2 connections.

6.5 Thermal protection

Thermal protection works when the junction temperature reaches 160 °C typical. At this point, the output of the IC shuts down. As soon as the junction temperature falls below the thermal hysteresis value, the device starts working again.

In order to calculate the maximum power that the device can dissipate, keeping the junction temperature below the maximum operating value, the following formula is used:

$$P_{DMAX} = \left(85 - T_{AMB}\right) / R_{thJA} \quad (2)$$

6.6 Input and output capacitors

The LD57100 requires external capacitors to assure the regulator control loop stability.

Any good quality ceramic capacitor can be used, however the X5R and the X7R are suggested since they guarantee a very stable combination of capacitance and ESR all over the temperature range.

It is recommended to place the input/output capacitors as close as possible to the relative pins. The LD57100 requires a V_{IN} capacitor with a minimum value of 1 µF and a V_{BIAS} capacitor of 100 nF minimum. These capacitors must be placed as close as possible to the input pins of the device and returned to a clean analog ground.

The control loop is designed to be stable with any good quality output ceramic capacitor (such as: X5R/X7R types) with a minimum value of 1.0 µF and equivalent series resistance in the [3 – 300 mΩ] range. It is important to highlight that the output capacitor must maintain its capacitance and ESR in the stable region over the full operating temperature, load and input voltage ranges, to assure stability. Therefore, capacitance and ESR variations must be taken into account in the design phase to be sure that the device works in the expected stability region.

7 Typical characteristics

C_{IN} = 1 µF; C_{OUT} = 10 µF, T_J = 25 °C unless otherwise specified.

Figure 6. V_{IN} drop vs temperature

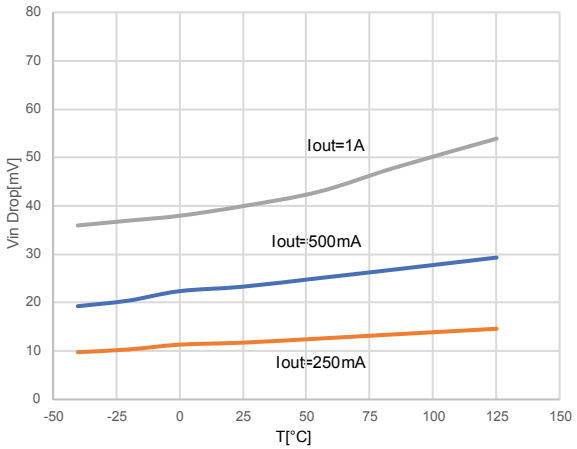


Figure 7. UVLO vs temperature

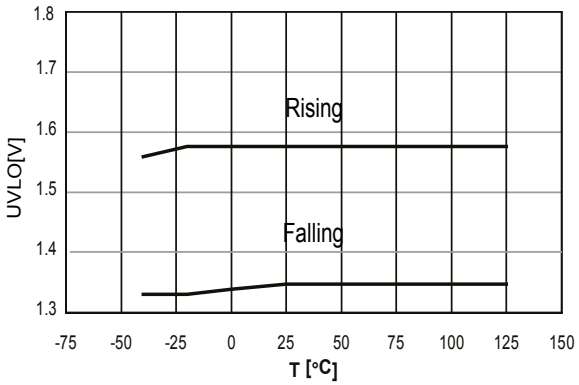


Figure 8. V_{OUT} vs temperature (V_{BIAS}@3 V, V_{IN}@V_{OUT} +0.3 V@1 mA)

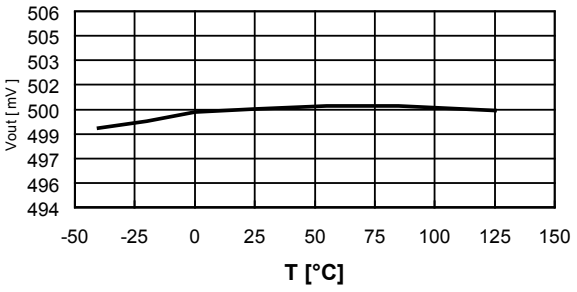


Figure 9. V_{OUT} vs temperature (V_{BIAS}@3 V, V_{IN}@V_{OUT} +0.3 V@1 A)

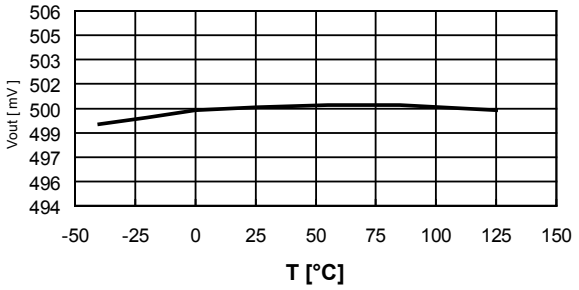


Figure 10. V_{in_line} vs temp. ($V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 5.0 V)

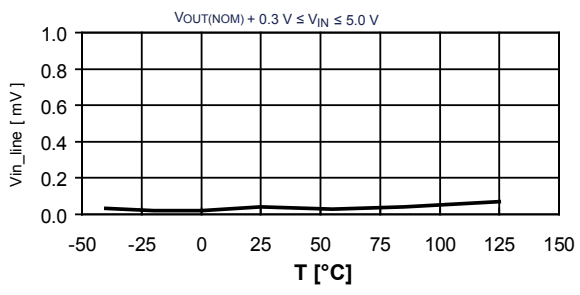


Figure 11. V_{BIAS_line} vs temp. (3.0 V or $V_{OUT(NOM)}$ + 1.6 V, whichever is greater, ≤ V_{BIAS} ≤ 5.5 V)

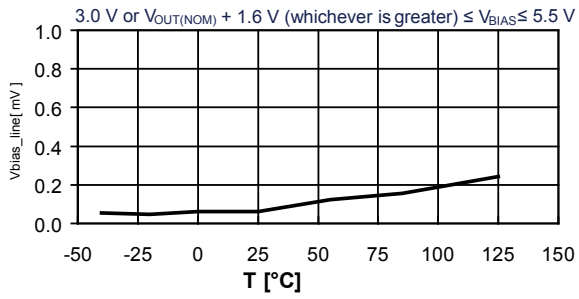


Figure 12. Load vs temperature

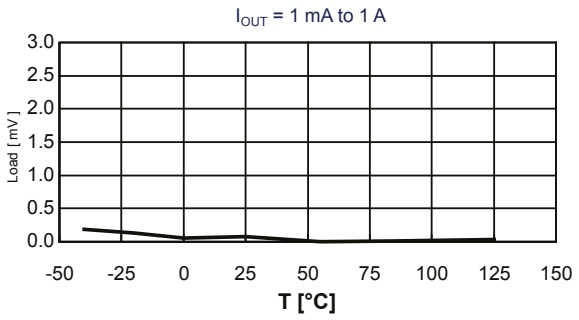


Figure 13. I_{SENSE} vs temperature

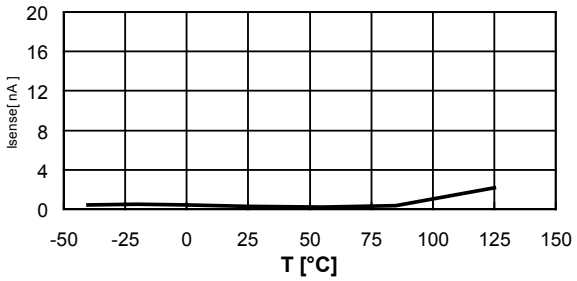


Figure 14. I_{BIAS} vs temperature

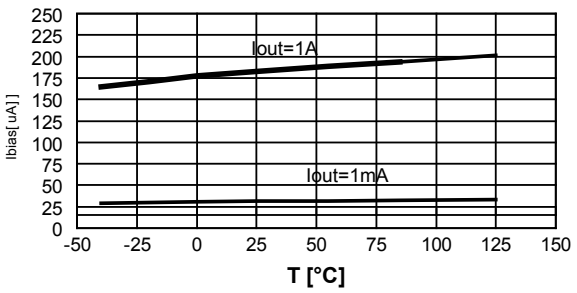


Figure 15. Enable high vs temperature (V_{BIAS} min.)

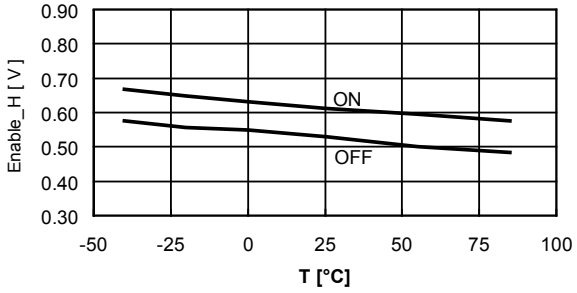


Figure 16. I_{ENABLE} vs temperature

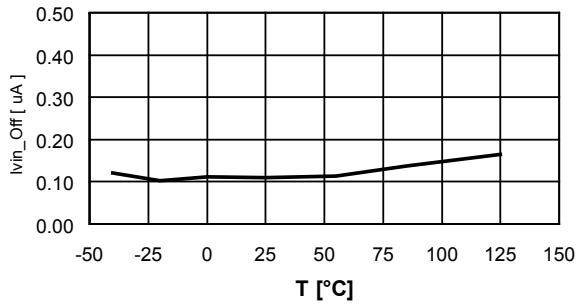
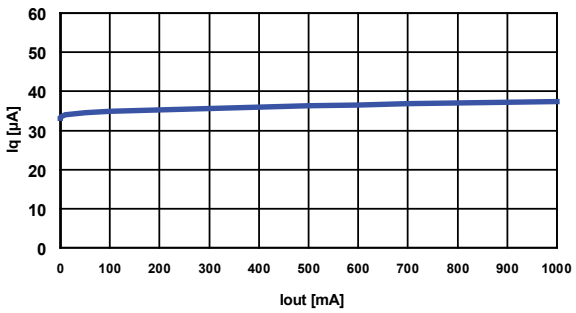


Figure 17. Ground pin current vs load current



V_{OUT} = 0.5 V, C_{IN} = 4.7 µF, C_{OUT} = 10 µF, C_{BIAS} = 1 µF, $t_{rise}/_{fall}$ = 5 µs

Figure 18. Input voltage turn-on (V_{IN}= from 0 V to 0.8 V, V_{BIAS}=3 V, V_{EN}=0.8 V, I_{OUT}=1 A)

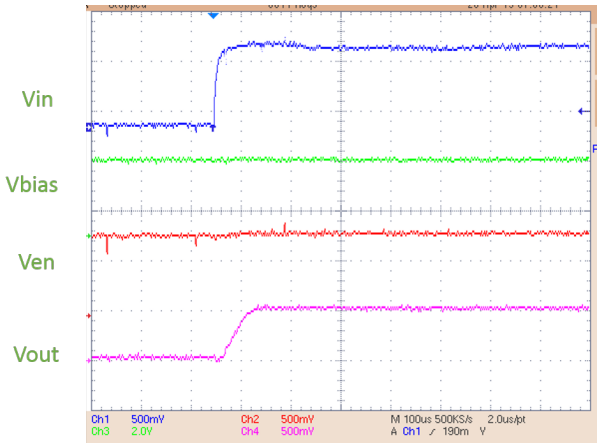


Figure 19. Load transient (V_{IN}=0.8 V, V_{BIAS}=3 V, V_{EN}=1 V, I_{OUT} from 1 mA to 1 A)

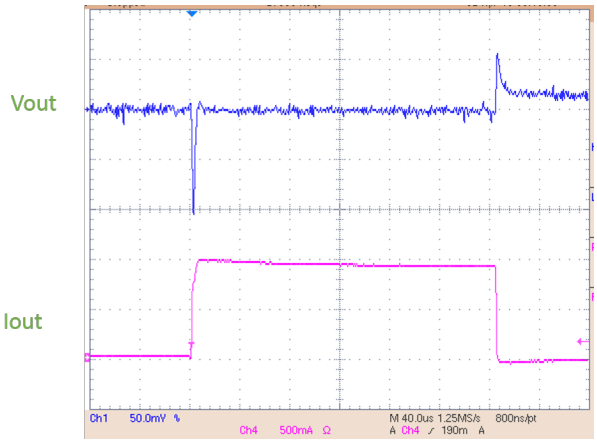


Figure 20. Line transient vs input voltage (V_{IN}= from 0.8 V to 1.08 V, V_{BIAS}=3 V, V_{EN}=1 V, I_{OUT} 100 mA)

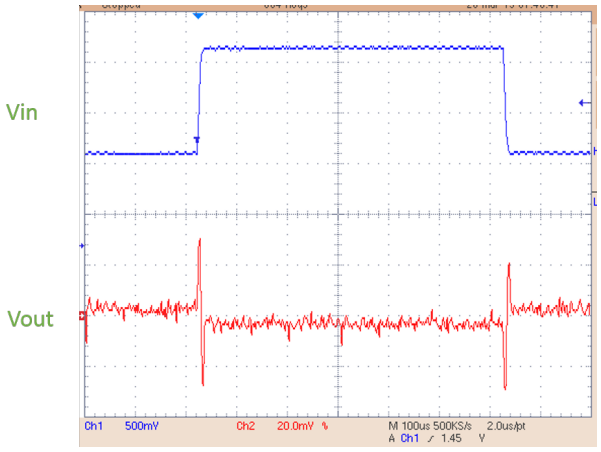


Figure 21. Line transient vs BIAS voltage (V_{IN}=0.8 V to 1.08 V, V_{BIAS}= from 2.8 to 3.8 V, V_{EN}=1 V, I_{OUT}=100 mA)

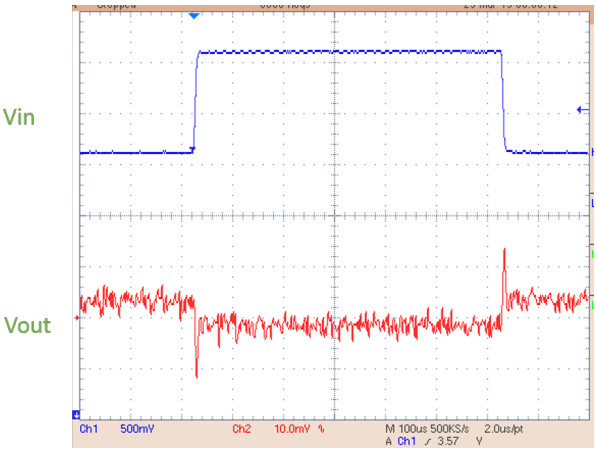


Figure 22. V_{BIAS} PSRR vs frequency

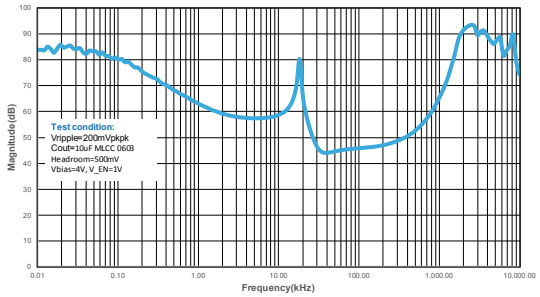


Figure 23. V_{IN} PSRR vs frequency

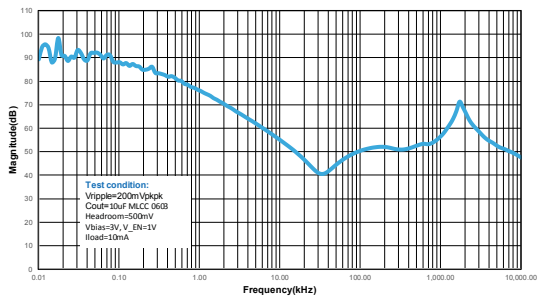


Figure 24. Output voltage spectral noise density vs frequency (V_{OUT}= 1 V adj.)

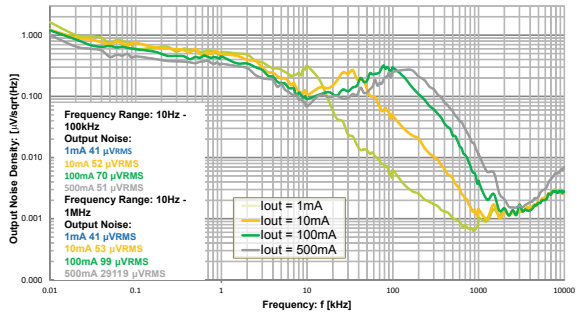


Figure 25. Output voltage spectral noise density vs frequency

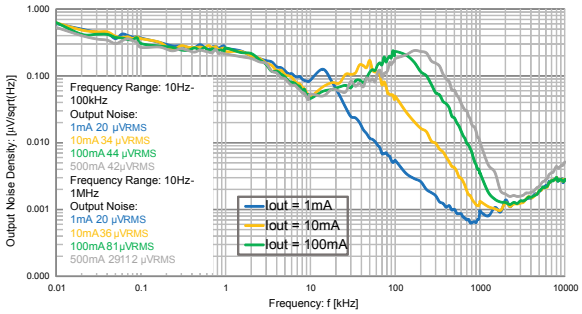
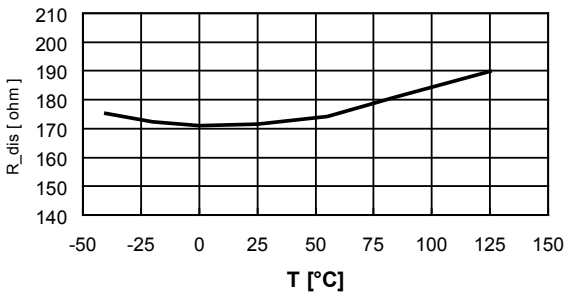


Figure 26. Discharge_RMOS vs temperature



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 Flip Chip6 (0.8x1.2 mm) package information

Figure 27. Flip Chip6 (0.8x1.2 mm) package outline

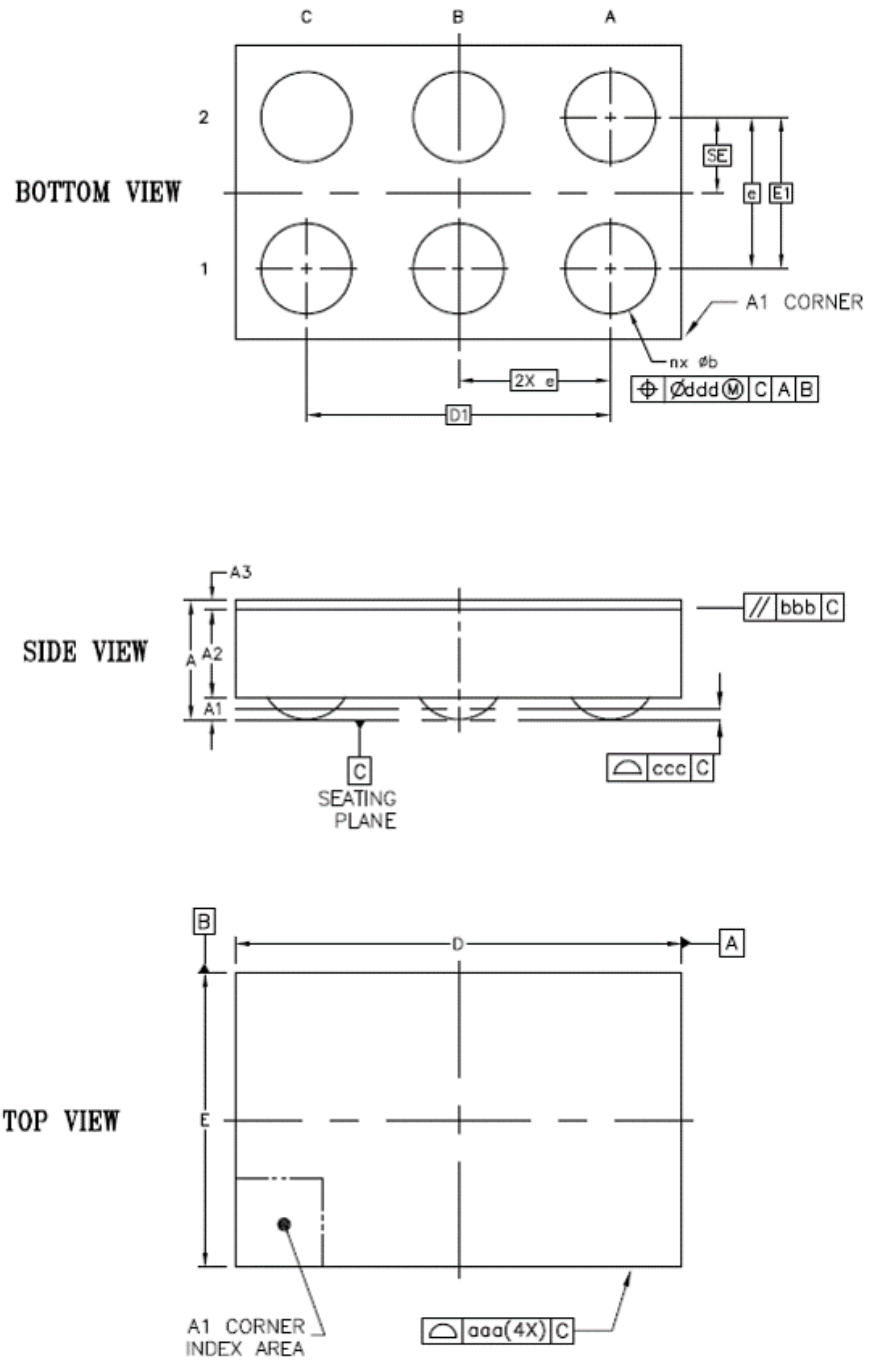
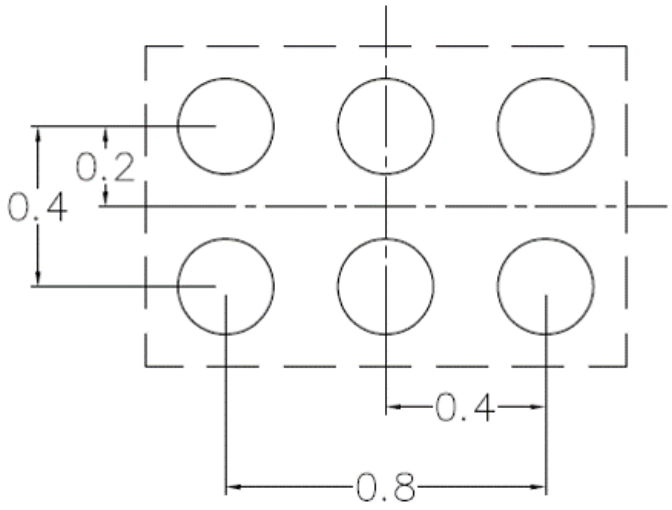


Table 7. Flip Chip6 (0.8x1.2 mm) package mechanical data

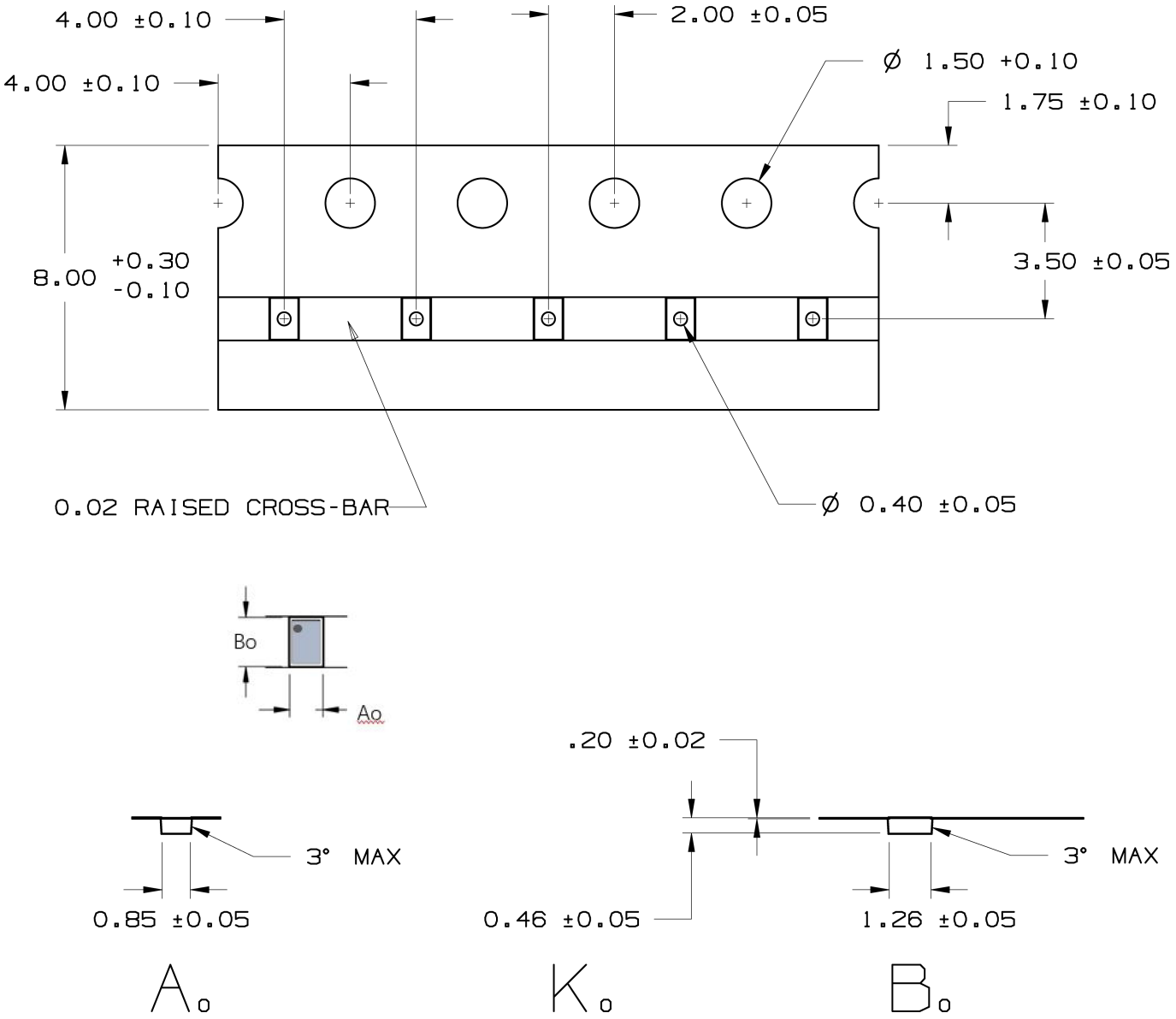
Symbol	Milimeters		
	Min.	Typ.	Max.
A	0.277	0.315	0.361
A1	0.045	0.060	0.075
A2	0.205	0.230	0.255
A3	0.022	0.025	0.028
b	0.210	0.240	0.270
D	1.155	1.175	1.195
E	0.755	0.775	0.795
D1	0.8 BSC		
E1	0.4 BSC		
e	0.4 BSC		
SE	0.2 BSC		
aaa	0.03		
bbb	0.06		
ccc	0.03		
ddd	0.015		

Figure 28. Flip Chip6 (0.8x1.2 mm) recommended footprint



8.2 Flip Chip6 (0.8x1.2 mm) packing information

Figure 29. **Flip Chip6 (0.8x1.2 mm) carrier tape outline**



9 Ordering information

Table 8. **Order codes**

Order code	V_{OUT}	Marking
LD57100J100R	1.00 V	JB
LD57100J105R	1.05 V	JC
LD57100J800R	0.8 V	JF
LD57100J110R	1.10 V	JD
LD57100JR	Adjustable	JA

Revision history

Table 9. Document revision history

Date	Version	Changes
30-Oct-2019	1	Initial release.
20-Dec-2019	2	Updated Figure 2. Block diagram adjustable version, Figure 22. V_{BIAS} PSRR vs frequency and Figure 23. V_{IN} PSRR vs frequency . Updated Table 3. Absolute maximum ratings and Table 6. Electrical characteristics.
20-Jan-2020	3	Updated Table 6. Electrical characteristics and Table 8. Order codes.

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