

N-channel 100 V, 0.038 Ω typ., 25 A STripFET™ II Power MOSFET in a DPAK package

Datasheet - production data

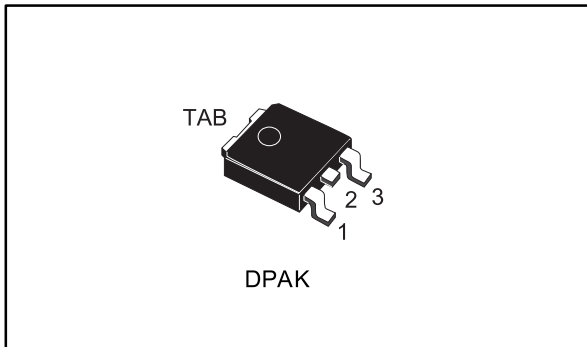
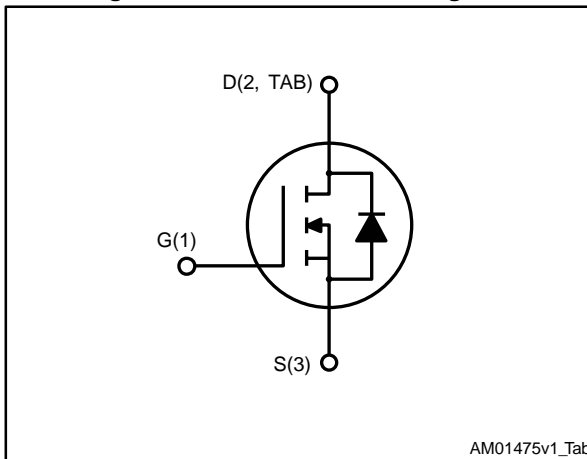


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STD20NF10T4	100 V	0.045 Ω	25 A

- Exceptional dv/dt capability
- Application oriented characterization

Applications

- Switching applications

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process is specifically designed to minimize input capacitance and gate charge. It is therefore ideal as a primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer applications. It is also suitable for any application with low gate charge drive requirements.

Table 1: Device summary

Order code	Marking	Package	Packing
STD20NF10T4	D20NF10	DPAK	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves).....	6
3	Test circuits	8
4	Package information	9
	4.1 DPAK (TO-252) type A package information.....	9
	4.2 DPAK (TO-252) type C package information	11
	4.3 DPAK (TO-252) packing information.....	14
5	Revision history	16

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25 \text{ }^\circ\text{C}$	25	A
I_D	Drain current (continuous) at $T_C = 100 \text{ }^\circ\text{C}$	21	A
$I_{DM}^{(1)}$	Drain current (pulsed)	100	A
P_{TOT}	Total dissipation at $T_C = 25 \text{ }^\circ\text{C}$	85	W
$E_{AS}^{(2)}$	Single pulse avalanche energy	300	mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	20	V/ns
T_j	Operating junction temperature range	- 55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature range		

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾Starting $T_J = 25 \text{ }^\circ\text{C}$, $I_D = 10 \text{ A}$, $V_{DD} = 27 \text{ V}$.

⁽³⁾ $I_{SD} \leq 25 \text{ A}$, $di/dt \leq 300 \text{ A}/\mu\text{s}$; $V_{DD} = V_{(BR)DSS}$, $T_J \leq T_{JMAX}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.76	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	$^\circ\text{C}/\text{W}$

Notes:

⁽¹⁾When mounted on 1 inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 4: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	100			V
I_{DSS}	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$ $T_C = 125\text{ °C}$ ⁽¹⁾			10	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 15\text{ A}$		0.038	0.045	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} ⁽¹⁾	Forward transconductance	$V_{DS} = 15\text{ V}$, $I_D = 15\text{ A}$	-	10	-	S
C_{ISS}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1200	-	pF
C_{OSS}	Output capacitance		-	180	-	pF
C_{RSS}	Reverse transfer capacitance		-	80	-	pF
Q_g	Total gate charge	$V_{DD} = 80\text{ V}$, $I_D = 30\text{ A}$		40	55	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{ V}$ $R_G = 4.7\text{ }\Omega$	-	8	-	nC
Q_{gd}	Gate-drain charge	See Figure 15: "Test circuit for gate charge behavior"	-	15	-	nC

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\text{ V}$, $I_D = 15\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	15	-	ns
t_r	Rise time		-	40	-	ns
$t_{d(off)}$	Turn-off delay time	See Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform"	-	45	-	ns
t_f	Fall time		-	10	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		30	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		120	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 30 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 55 \text{ V}$ $T_j = 150 \text{ }^\circ\text{C}$ See Figure 16: "Test circuit for inductive load switching and diode recovery times"	-	110		ns
Q_{rr}	Reverse recovery charge		-	390		nC
I_{RRM}	Reverse recovery current		-	7.5		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

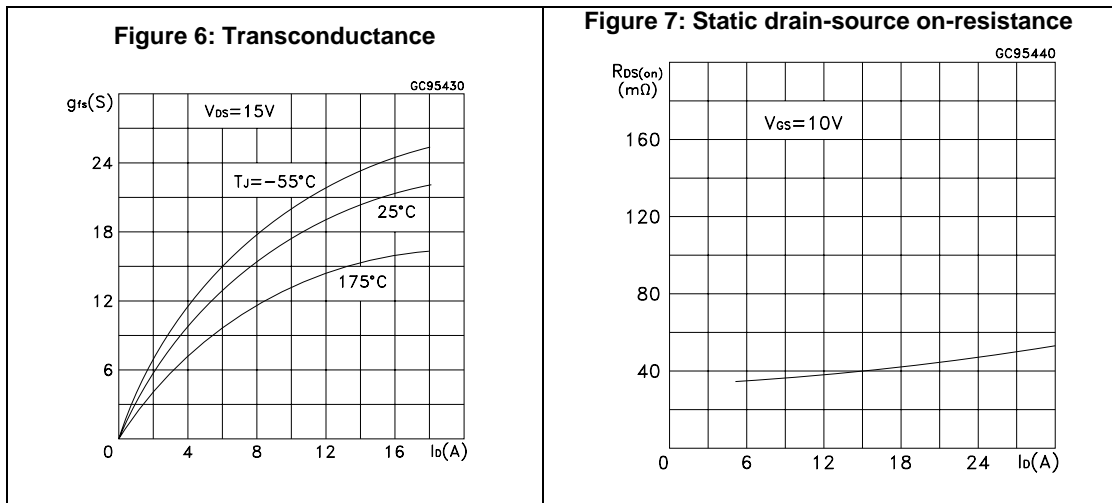
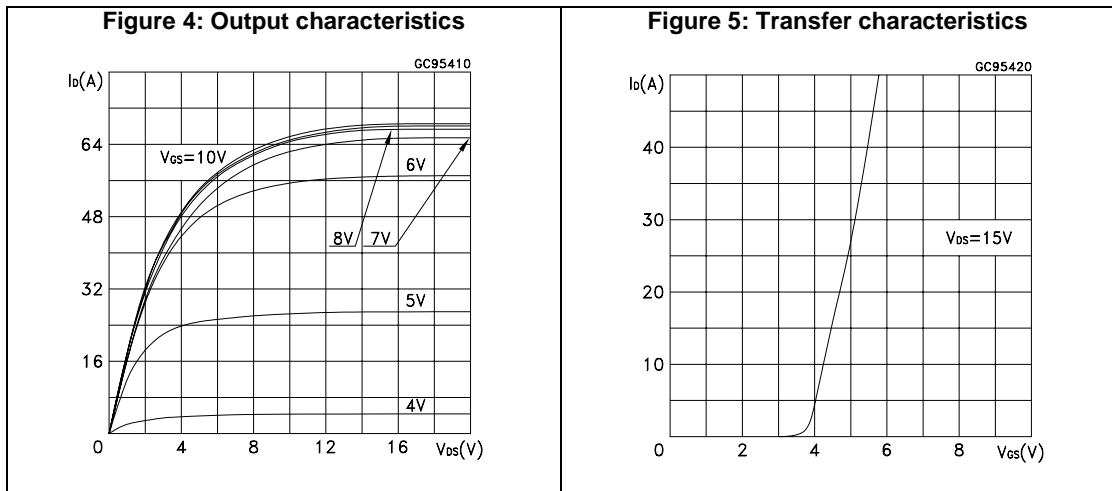
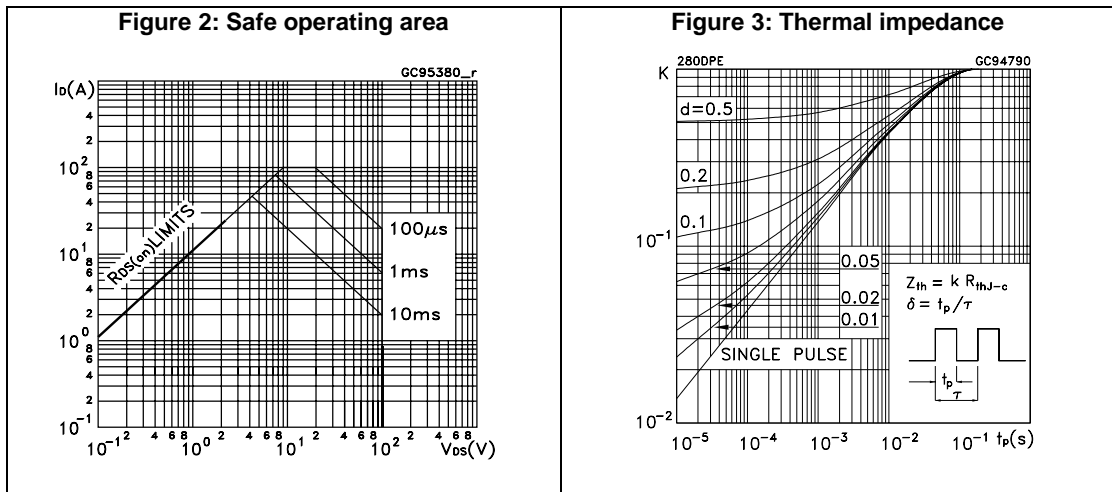


Figure 8: Gate charge vs. gate-source voltage

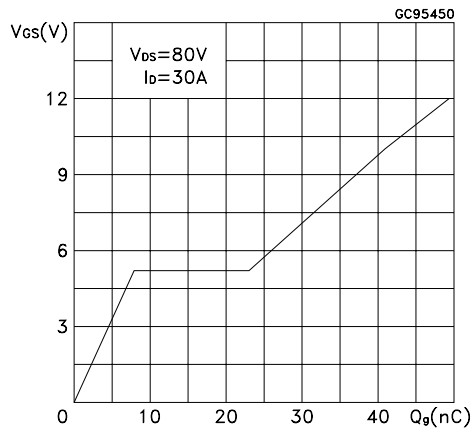


Figure 9: Capacitance variations

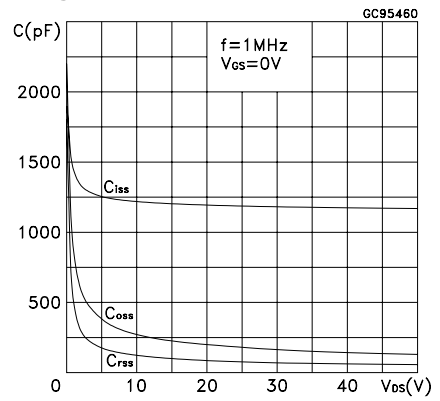


Figure 10: Normalized gate threshold voltage vs. temperature

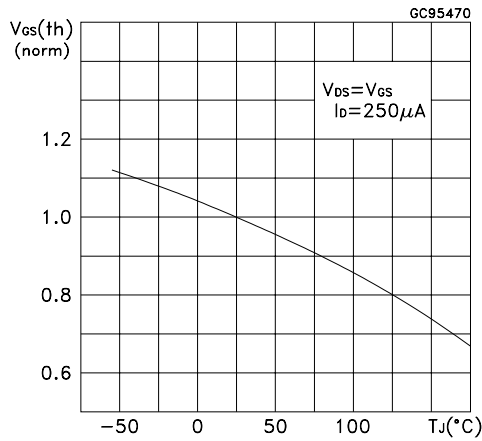


Figure 11: Normalized on-resistance vs. temperature

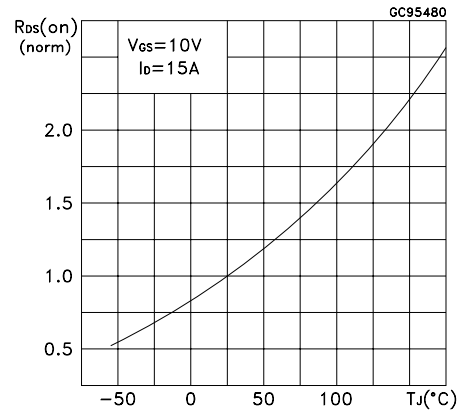


Figure 12: Source-drain diode forward characteristics

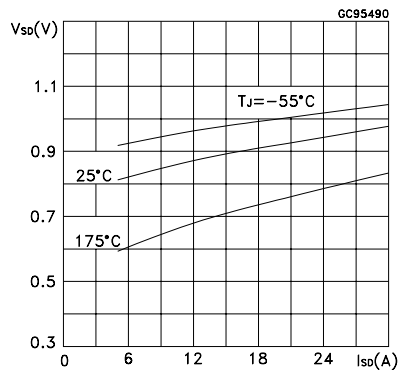
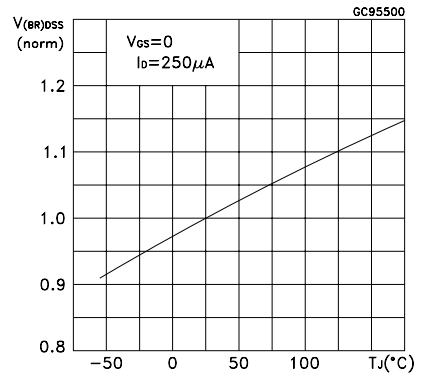
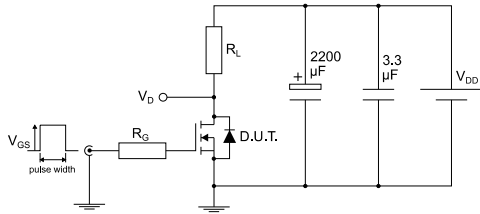


Figure 13: Normalized breakdown voltage vs. temperature



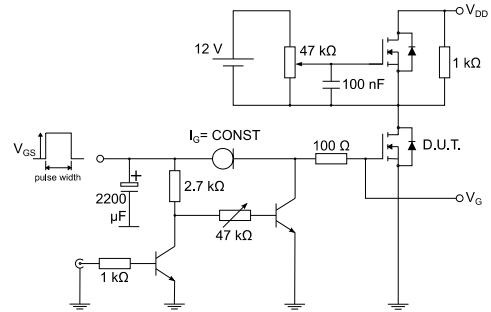
3 Test circuits

Figure 14: Test circuit for resistive load switching times



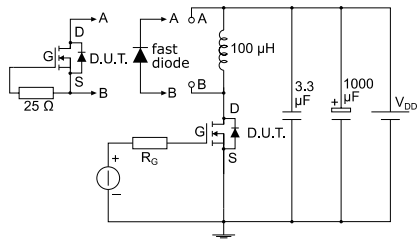
AM01468v1

Figure 15: Test circuit for gate charge behavior



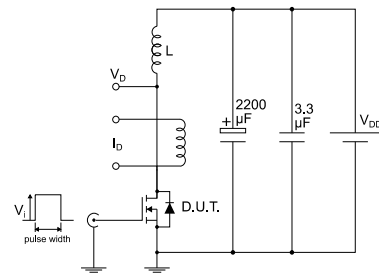
AM01469v1

Figure 16: Test circuit for inductive load switching and diode recovery times



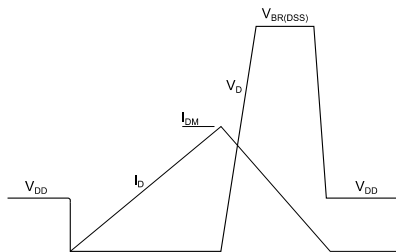
AM01470v1

Figure 17: Unclamped inductive load test circuit



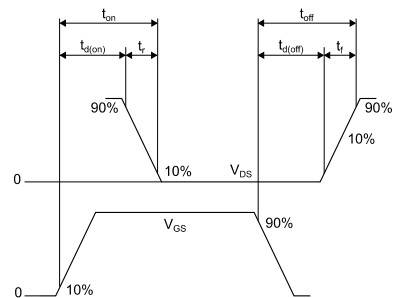
AM01471v1

Figure 18: Unclamped inductive waveform



AM01472v1

Figure 19: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 20: DPAK (TO-252) type A package outline

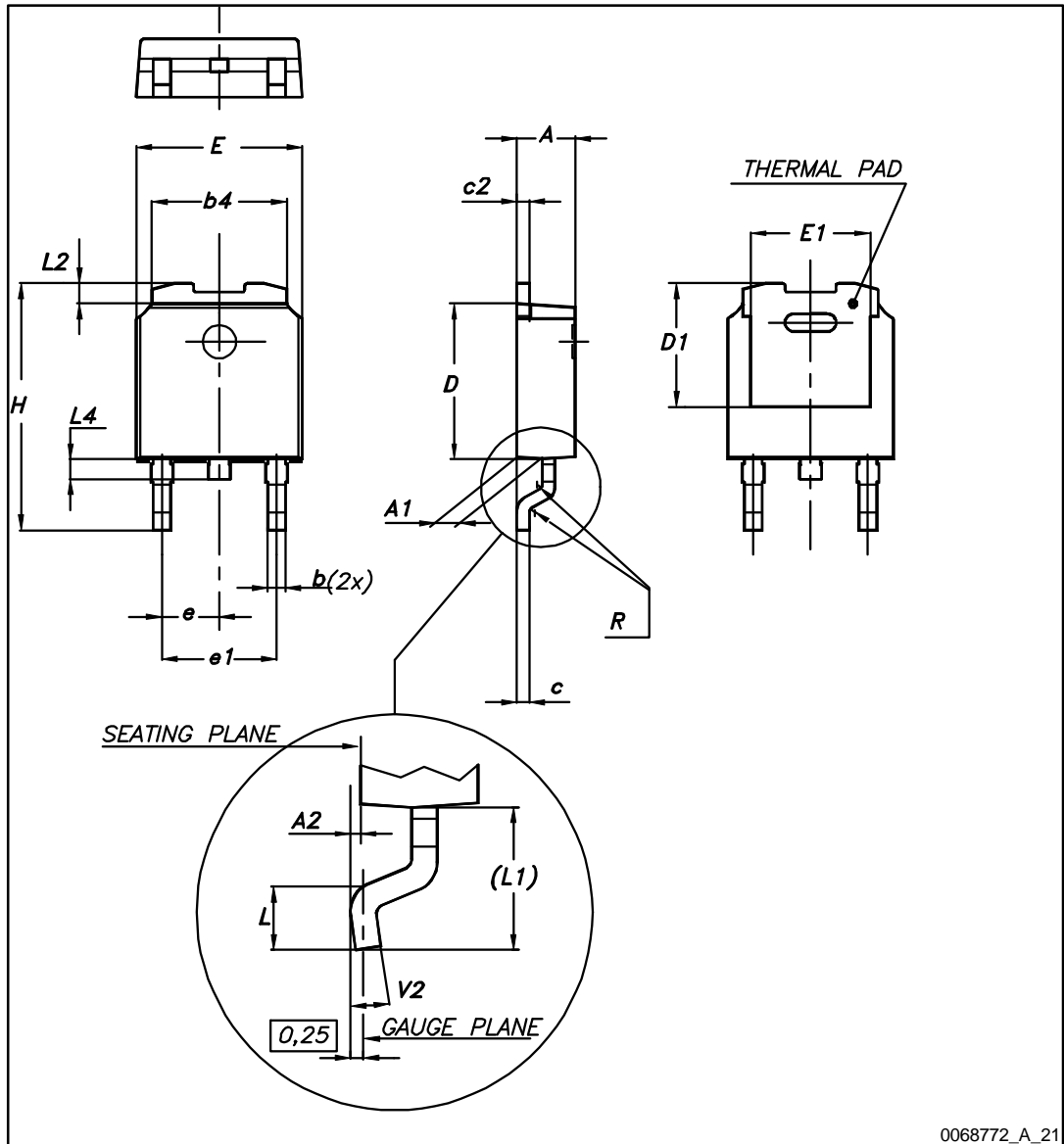


Table 8: DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C package information

Figure 21: DPAK (TO-252) type C package outline

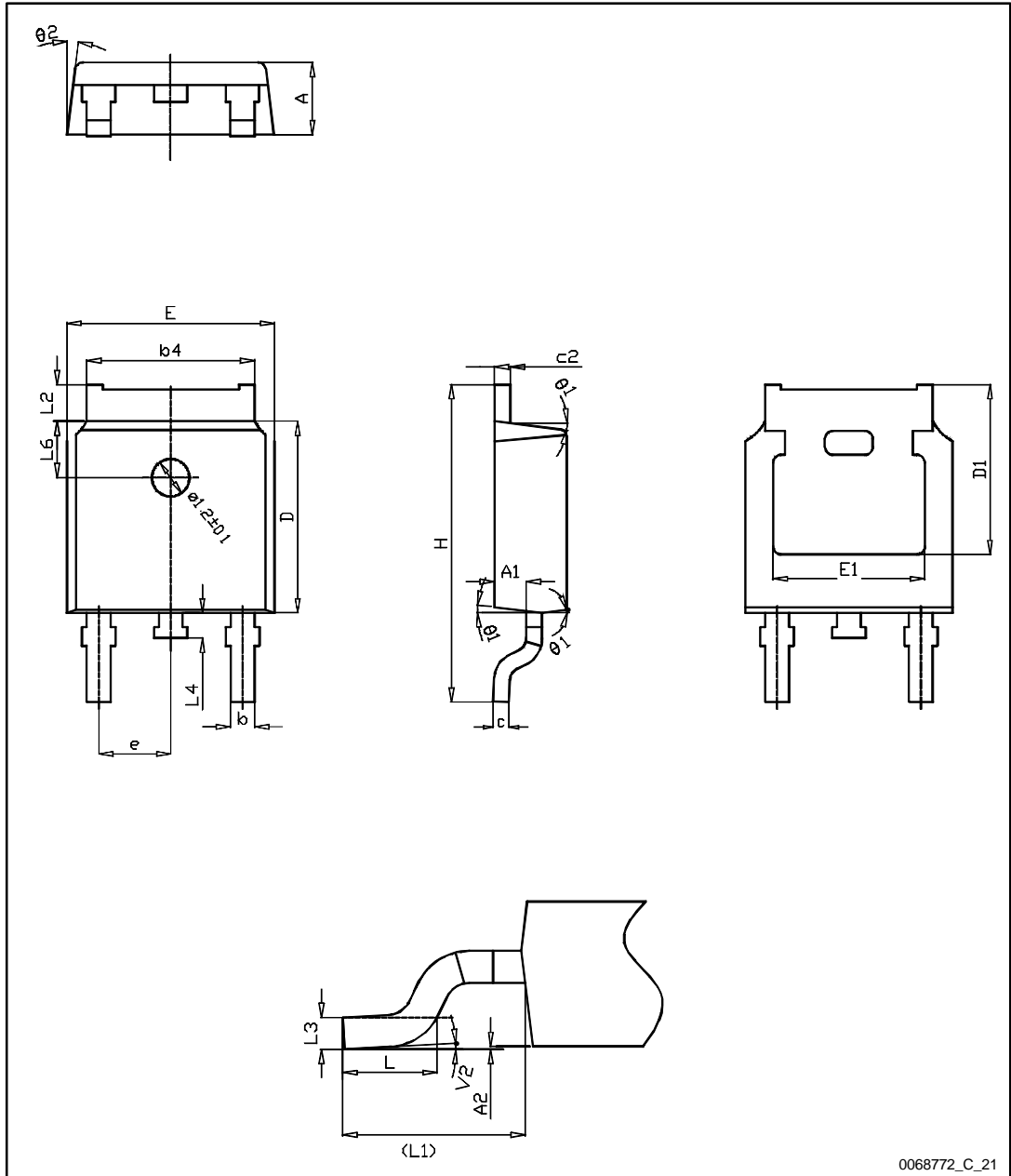
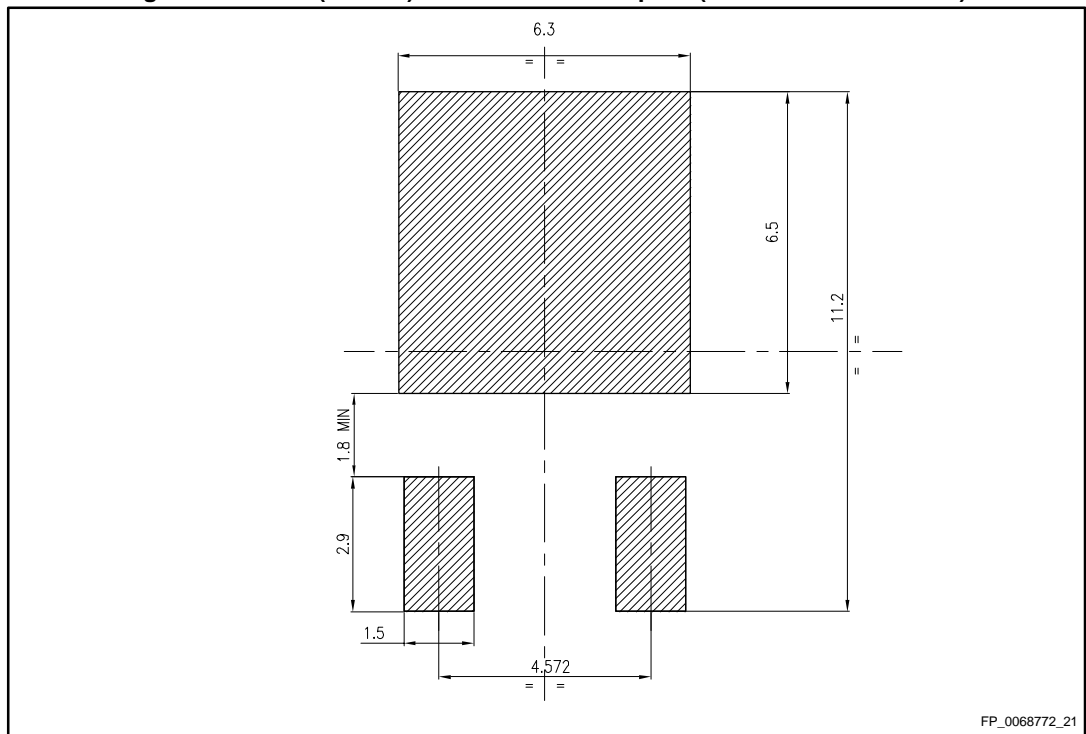


Table 9: DPAK (TO-252) type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 22: DPAK (TO-252) recommended footprint (dimensions are in mm)



4.3 DPAK (TO-252) packing information

Figure 23: DPAK (TO-252) tape outline

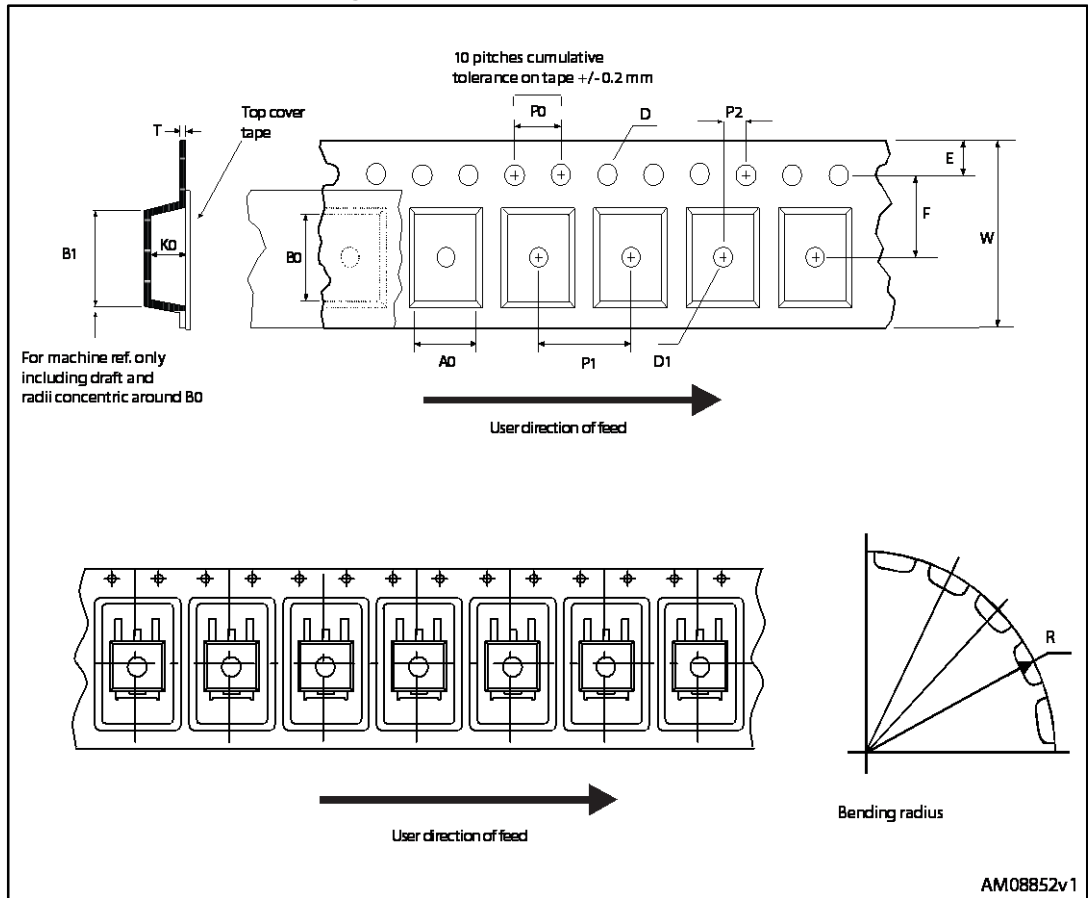
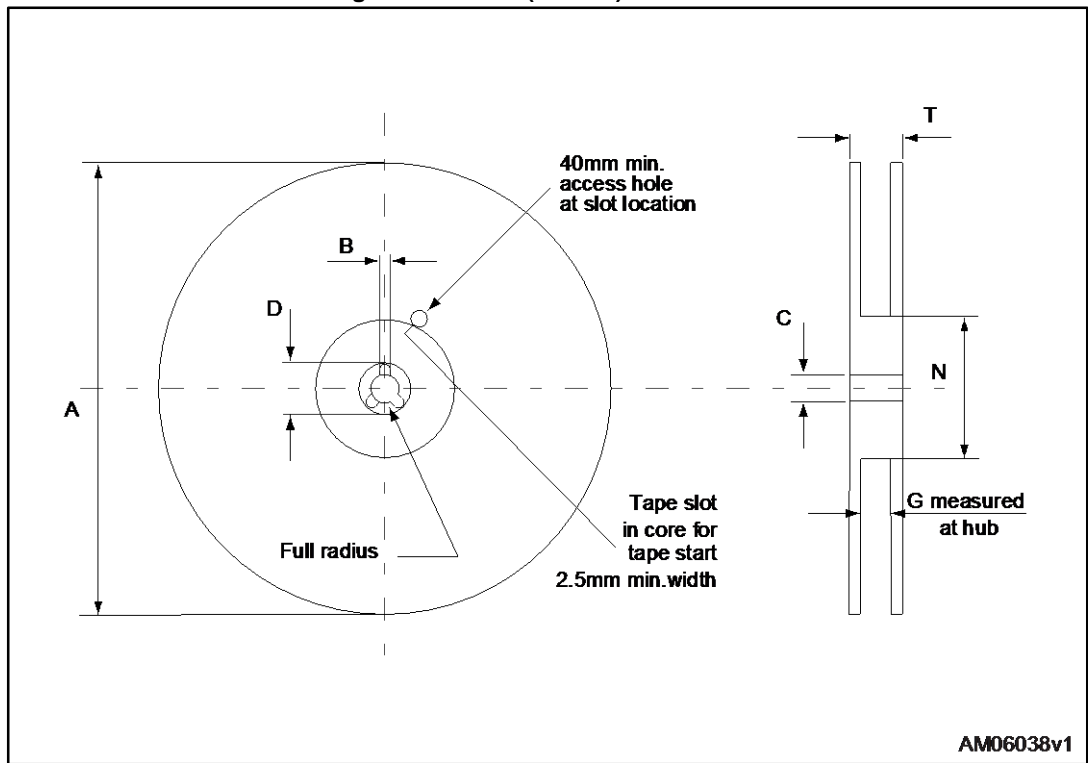


Figure 24: DPAK (TO-252) reel outline



AM06038v1

Table 10: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
06-Apr-2016	1	First release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[STMicroelectronics:](#)

[STD20NF10T4](#)