*Click **here** to ask an associate for production status of specific part numbers.*

MAX17291

High-Voltage, 1A Micropower Boost Converter with Short-Circuit Protection and True Shutdown

General Description

The MAX17291 is a low quiescent current boost (step-up) DC-DC converter with a 1A peak inductor current limit and True Shutdown™. True Shutdown disconnects the output from the input with no forward or reverse current. The output voltage is set with an external resistor-divider.

The MAX17291 offers low quiescent current, small total solution size, and high efficiency throughout the entire load range. The MAX17291 is a highly integrated boost converter designed for applications requiring high voltage and tiny solution size, such as sensor modules. It integrates a power switch, power diode, and output load switch. It can output up to 20V. The load switch is turned off under shutdown mode, truly disconnecting the load from the input voltage, thus minimizing the leakage current during shutdown mode. The device operates with a switching frequency of 1.0MHz in continuous conduction mode (CCM). The MAX17291 switch current limit is 1A. It has 2.2ms built-in soft-start time to minimize inrush current. The device features short-circuit and thermal protection.

The MAX17291 is offered in space-saving, cost-effective 1.27mm x 0.87mm, 6-bump WLP (3 x 2, 0.4mm pitch) and 2mm x 2mm, 8-pin TDFN packages. The operating temperature range is from -40°C to +125°C.

Applications

- Sensor Power Supply
- Wearable Devices
- Portable Medical Equipment

Benefits and Features

- 28µA Quiescent Supply Current from Input
- Output Short-Circuit Protection
- Overtemperature Protection
- Constant Frequency in CCM
- True Shutdown Mode
  - 0.05µA Shutdown Current
  - No Reverse Current from OUT
- 91% Peak Efficiency
- 1.8V to 5.5V Input Range
- 5.5V to 20V Output Voltage Range
- 1A Peak Inductor Current Limit
- Multiple Package Options
  - 1.27mm x 0.87mm, 6-Bump (3 x 2), 0.4mm Pitch WLP
  - 2mm x 2mm, 8-Pin TDFN
- -40°C to +125°C Operating Temperature Range

True Shutdown is a trademark of Maxim Integrated Products.

***Ordering Information** appears at end of data sheet.*

19-100778; Rev 3; 02/23

Typical Application Circuit

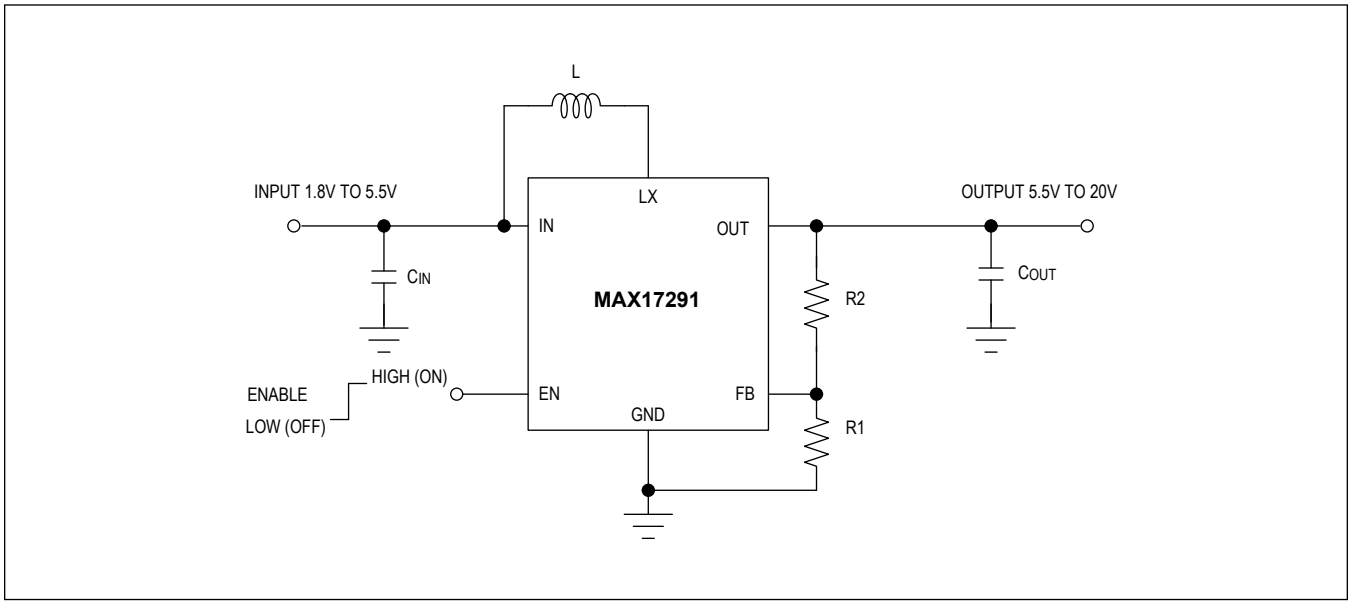


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Absolute Maximum Ratings

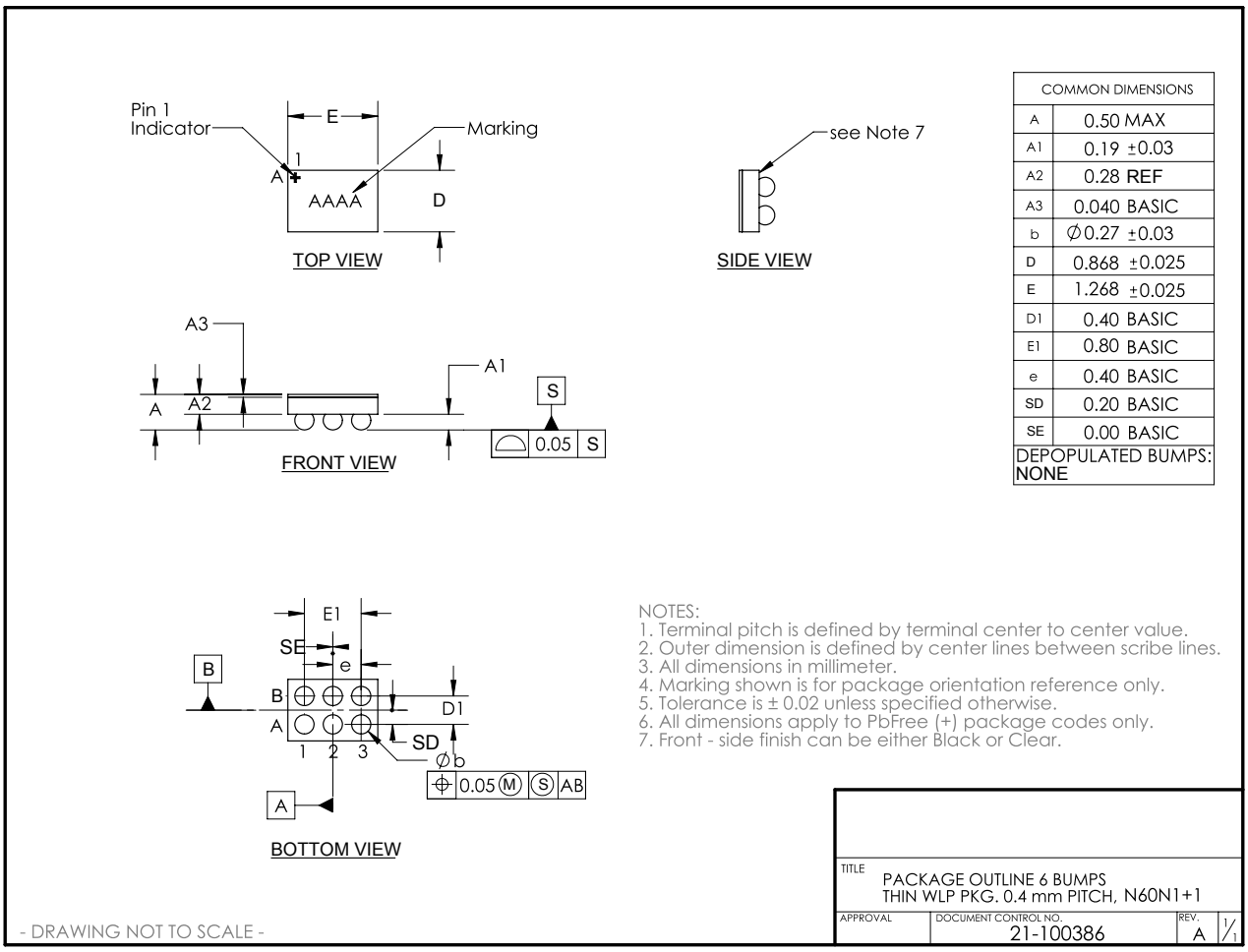
EN, IN to GND ..... -0.3V to +6V
FB, POK to GND ..... -0.3V to +6V
OUT, LX to GND ..... -0.3V to +22V
AGND to GND ..... -0.3V to +0.3V
LX RMS Current WLP ..... -1.6A_{RMS} to +1.6A_{RMS}
LX RMS Current TDFN ..... -1.0A_{RMS} to +1.0A_{RMS}
WLP Continuous Power Dissipation (T_A = +70°C, derate 10.51mW/°C above +70°C) 840mW
TDFN Continuous Power Dissipation (T_A = +70°C, derate 11.7mW/°C above +70°C) 937.9mW
Operating Temperature Range ..... -40°C to +125°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

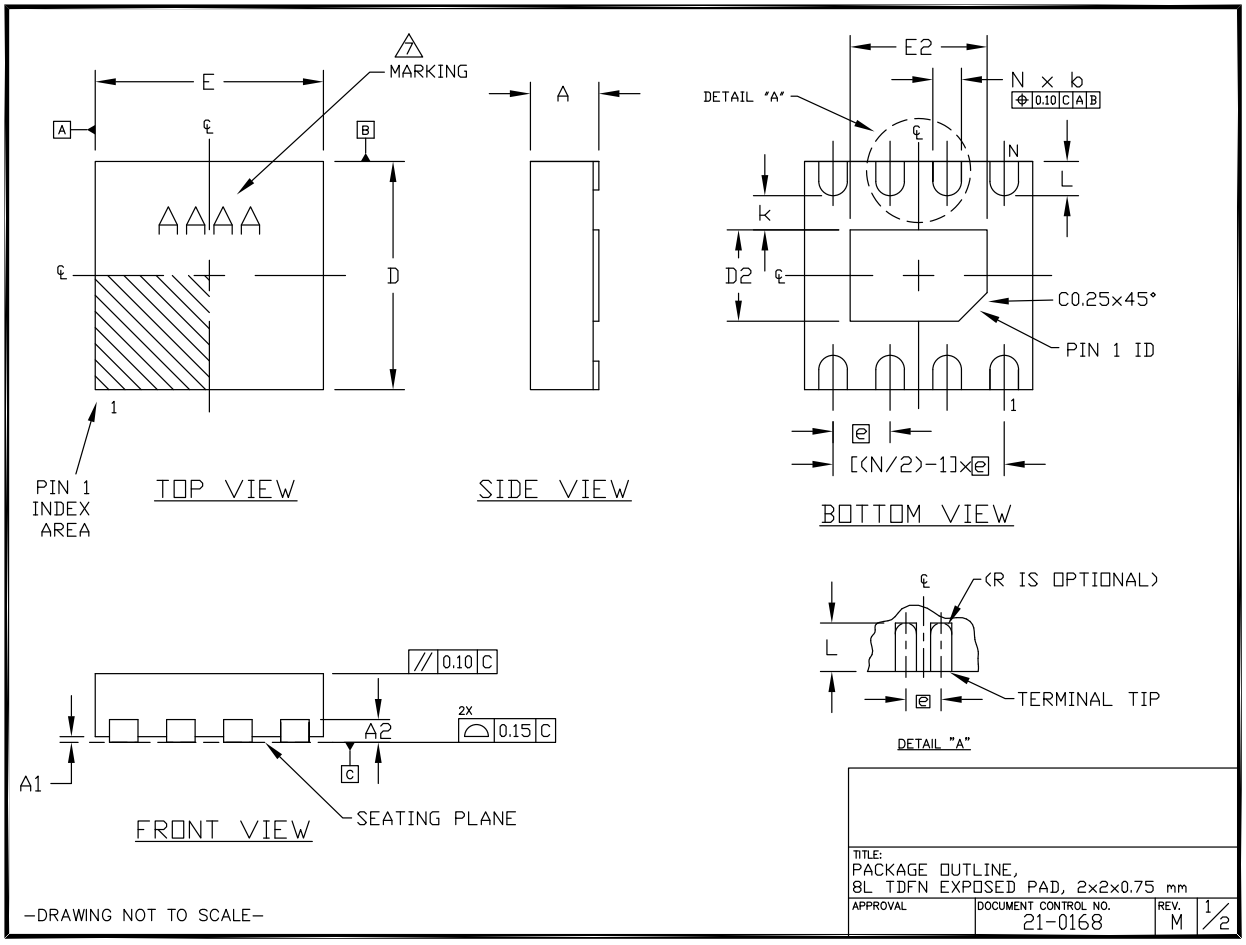
WLP

Package Code	N60N1+1
Outline Number	**21-100386**
Land Pattern Number	Refer to ***Application Note 1891***
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	95.15°C/W
Junction to Case (θ_{JC})	N/A



TDFN

Package Code	T822+3C
Outline Number	**21-0168**
Land Pattern Number	**90-0065**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	85.3°C/W
Junction to Case (θ_{JC})	8.9°C/W


MARKING
E
A
B
AAAA
D
1
PIN 1
INDEX
AREA
TOP VIEW
A
SIDE VIEW
E2
N x b
0.10 C A B
DETAIL "A"
N
L
k
D2
C0.25x45°
PIN 1 ID
1
e
[(N/2)-1]xe
BOTTOM VIEW
(R IS OPTIONAL)
L
e
TERMINAL TIP
DETAIL "A"
0.10 C
2X
0.15 C
A2
A1
C
SEATING PLANE
FRONT VIEW
-DRAWING NOT TO SCALE-
TITLE:
PACKAGE OUTLINE,
8L TDFN EXPOSED PAD, 2x2x0.75 mm
APPROVAL
DOCUMENT CONTROL NO.
21-0168
REV.
M
1/2

COMMON DIMENSIONS			
SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
D	1.90	2.00	2.10
E	1.90	2.00	2.10
A1	0.00	--	0.05
L	0.20	0.30	0.40
k	0.25 MIN.		
A2	0.20 REF.		

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	b	r	[(N/2)-1] x e
T822-1	8	0.70±0.10	1.30±0.10	0.50 TYP.	0.25±0.05	0.125	1.50 REF
T822-1C	8	0.70±0.10	1.30±0.10	0.50 TYP.	0.25±0.05	0.125	1.50 REF
T822-2	8	0.80±0.10	1.20±0.10	0.50 TYP.	0.25±0.05	0.125	1.50 REF
T822-2C	8	0.80±0.10	1.20±0.10	0.50 TYP.	0.25±0.05	0.125	1.50 REF
T822-3	8	0.80±0.10	1.20±0.10	0.50 TYP.	0.25±0.05	0.125	1.50 REF
T822-3C	8	0.80±0.10	1.20±0.10	0.50 TYP.	0.25±0.05	0.125	1.50 REF
T822-5	8	0.80±0.10	1.20±0.10	0.50 TYP.	0.25±0.05	0.125	1.50 REF
T822-5C	8	0.80±0.10	1.20±0.10	0.50 TYP.	0.25±0.05	0.125	1.50 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. WARPAGE SHALL NOT EXCEED 0.08mm.
3. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
4. COMPLIES TO JEDEC MO229 EXCEPT D2 AND E2 DIMENSIONS.
5. "N" IS THE TOTAL NUMBER OF LEADS.
6. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
8. MATERIAL MUST BE COMPLIANT WITH MAXIM SPECIFICATION 10-0131 FOR SUBSTANCE CONTENT, MUST BE Eu RoHS COMPLIANT WITHOUT EXEMPTION AND PB-FREE.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

—DRAWING NOT TO SCALE—

TITLE:
PACKAGE OUTLINE,
8L TDFN EXPOSED PAD, 2x2x0.75 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0168	M	2/2

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_{IN} = V_{EN} = 3.6V, V_{OUT} = 12V, T_J = -40°C to +125°C, typical values are at T_J = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Guaranteed by LX minimum off-time	1.8		5.5	V
Input Undervoltage Threshold	V_{UVLO}	V_{IN} rising	1.7		1.8	V
Input Undervoltage Hysteresis	V_{UVLO_HYS}			100		mV
Output Voltage Range	V_{OUT}	V_{IN} < V_{OUT_TARGET}	5.5		20	V

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 3.6V, V_{OUT} = 12V, T_J = -40°C to +125°C, typical values are at T_J = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Feedback (FB) Accuracy	ACC_{CCM}	V_{FB} falling, when LX switching frequency is 1MHz (Note 2)		-1.5		+1.5	%
	ACC_{DCM}	V_{FB} falling, when LX switching frequency is <1MHz (Note 2)		1.239	1.258	1.277	V
Output Load Regulation	ACC_{LDREG}	10mA < I_{IN} < 160mA			2.0		%
Quiescent Supply Current into IN	I_{Q_IN}	Not switching, V_{OUT} = 104% of regulation	T_J = +25°C		28	45	µA
Quiescent Supply Current into OUT	I_{Q_OUT}	Not switching, V_{OUT} = 104% of regulation	T_J = +25°C		5	25	µA
Shutdown Current into IN	I_{SD_IN}	V_{EN} = 0V	T_J = +25°C		50	200	nA
LX Leakage Current	I_{LX_LK}	V_{LX} = 5.5V, V_{EN} = V_{OUT} = 0V, T_J = +25°C			10	500	nA
Inductor Peak Current Limit	I_{PEAK}	(Note 3)		0.8	1.0	1.2	A
Soft-Start Time	t_{SS}	V_{OUT} = 12V			2.2		ms
LX Maximum On-Time	t_{ON_MAX}			1.9	3.4	6.1	µs
LX Off-Time	t_{OFF}	(Note 4)	V_{IN} = 3.6V, T_J = +25°C	230	255	280	ns
			V_{IN} = 5.5V		350		
			V_{IN} = 5.0V, V_{OUT} = 7.0V		530		
			V_{IN} = 3.0V, V_{OUT} = 18V		147		
LX Switching Frequency	f_{SW}	V_{IN} = 3.6V, V_{OUT} = 12V			1.0		MHz
		V_{IN} = 5.0V, V_{OUT} = 7.0V			1.0		
		V_{IN} = 3.0V, V_{OUT} = 18V			1.0		
n-Channel On-Resistance	R_{DSON}	V_{IN} = 3.6V			320	650	mΩ
p-Channel On-Resistance	R_{DSON}	V_{IN} = 3.6V			320	650	mΩ
Diode Forward Voltage	V_F	V_{IN} = 3.6V, I_{LX} = 100mA			0.4		V
Enable Voltage Threshold	V_{IL}	V_{IN} = 1.8V to 5.5V, when LX stops switching, EN falling		400	800		mV
	V_{IH}	V_{IN} = 1.8V to 5.5V, EN rising			1200	1400	
Enable Input Leakage	I_{EN_LK}	V_{EN} = 0 to 5.5V, T_J = +25°C			0.5	100	nA
FB Leakage	I_{FB_LK}	V_{FB} = 1.25V, T_J = +25°C		-100	0.5	100	nA
POK Threshold (TDFN Package Only)		V_{OUT} when POK switches	V_{OUT} rising		92		%
			V_{OUT} falling		89.5		
POK Output Voltage Low (TDFN Package Only)	V_{POK_L}	I_{POK} = 2mA				0.4	V

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 3.6V, V_{OUT} = 12V, T_J = -40°C to +125°C, typical values are at T_J = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POK Leakage Current (TDFN Package Only)	I_{POK_LK}	V_{POK} = 5.5V, T_J = +25°C	-1		+1	µA
Overtemperature Lockout Threshold	T_{OTLO}	T_J rising, 15°C typical hysteresis		165		°C

Note 1: Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control (SQC) methods.

Note 2: Output accuracy does not include load, line, or ripple.

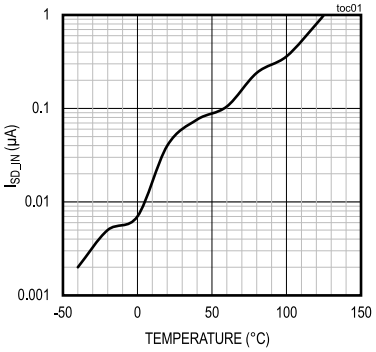
Note 3: This is a static measurement. The actual peak current limit depends upon V_{IN} and the inductor due to propagation delays.

Note 4: Measured opened loop. Propagation delays not included.

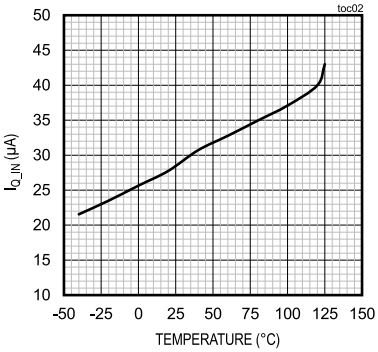
Typical Operating Characteristics

(MAX17291ANT, V_{IN} = V_{EN} = 3.6V, V_{OUT} = 12V, C_{IN} = 22µF, C_{OUT} = 10µF, L = 10µH, T_A = +25°C, unless otherwise noted.)

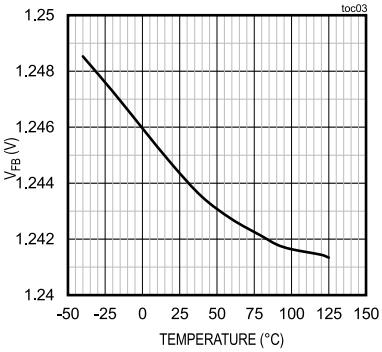
SHUTDOWN CURRENT INTO INPUT PIN vs. TEMPERATURE



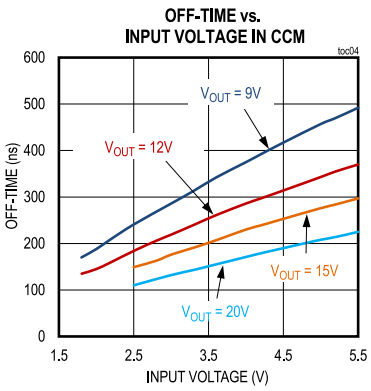
QUIESCENT CURRENT INTO INPUT PIN vs. TEMPERATURE



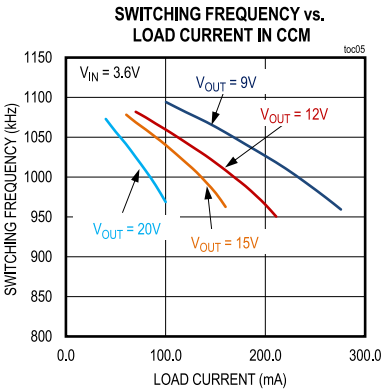
FEEDBACK PIN VOLTAGE vs. TEMPERATURE



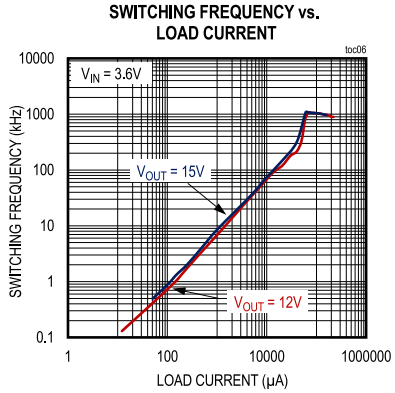
OFF-TIME vs. INPUT VOLTAGE IN CCM



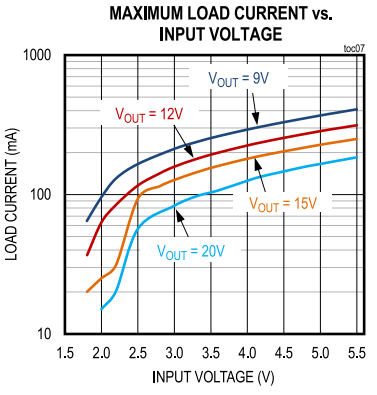
SWITCHING FREQUENCY vs. LOAD CURRENT IN CCM



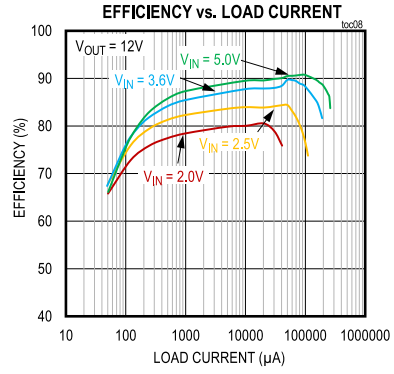
SWITCHING FREQUENCY vs. LOAD CURRENT



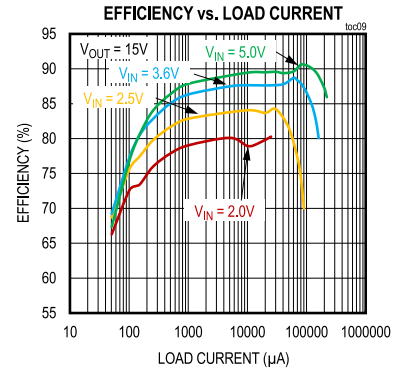
MAXIMUM LOAD CURRENT vs. INPUT VOLTAGE



EFFICIENCY vs. LOAD CURRENT



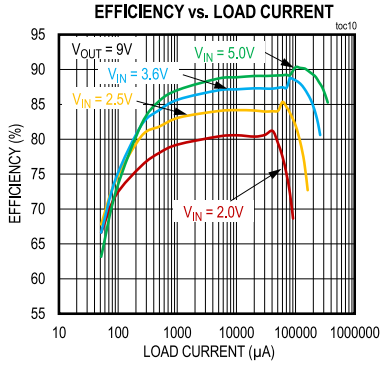
EFFICIENCY vs. LOAD CURRENT



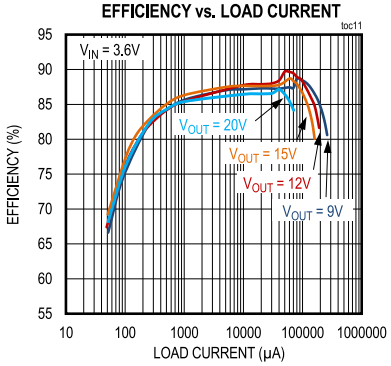
Typical Operating Characteristics (continued)

(MAX17291ANT, V_{IN} = V_{EN} = 3.6V, V_{OUT} = 12V, C_{IN} = 22µF, C_{OUT} = 10µF, L = 10µH, T_A = +25°C, unless otherwise noted.)

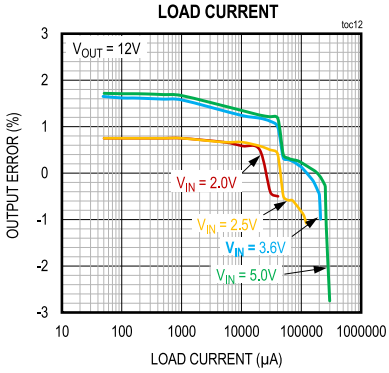
EFFICIENCY vs. LOAD CURRENT



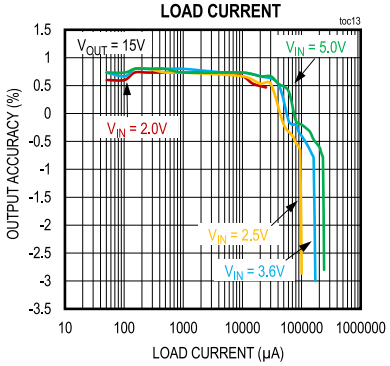
EFFICIENCY vs. LOAD CURRENT



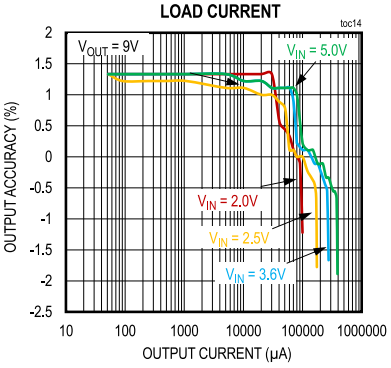
OUTPUT VOLTAGE ERROR vs. LOAD CURRENT



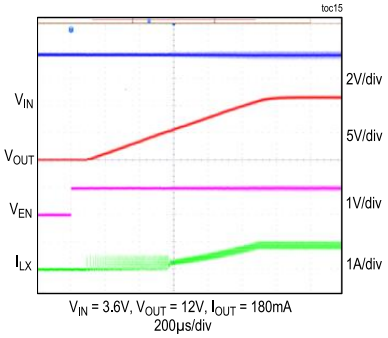
OUTPUT VOLTAGE ERROR vs. LOAD CURRENT



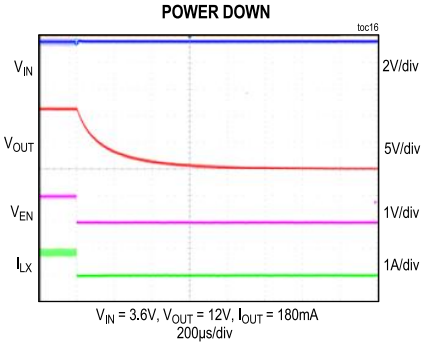
OUTPUT VOLTAGE ERROR vs. LOAD CURRENT



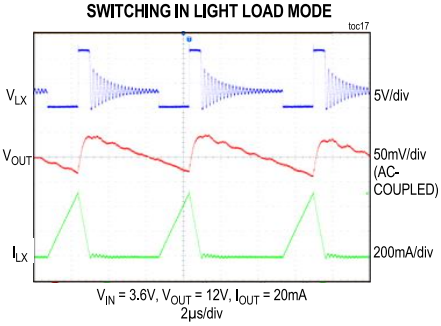
STARTUP



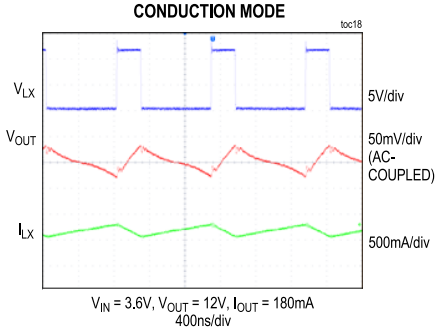
POWER DOWN



SWITCHING IN LIGHT LOAD MODE

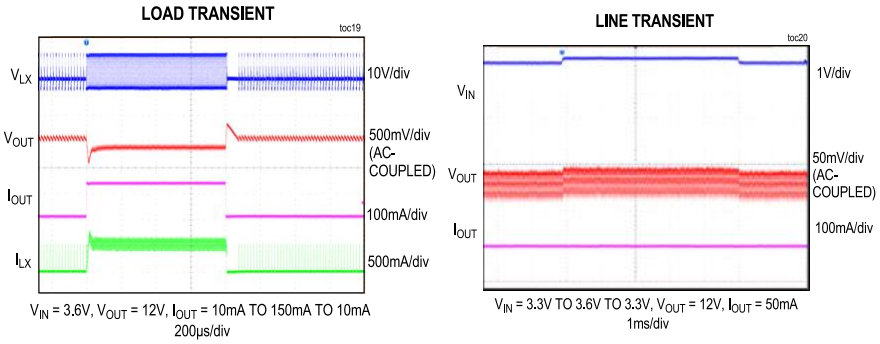


SWITCHING IN CONTINUOUS CONDUCTION MODE



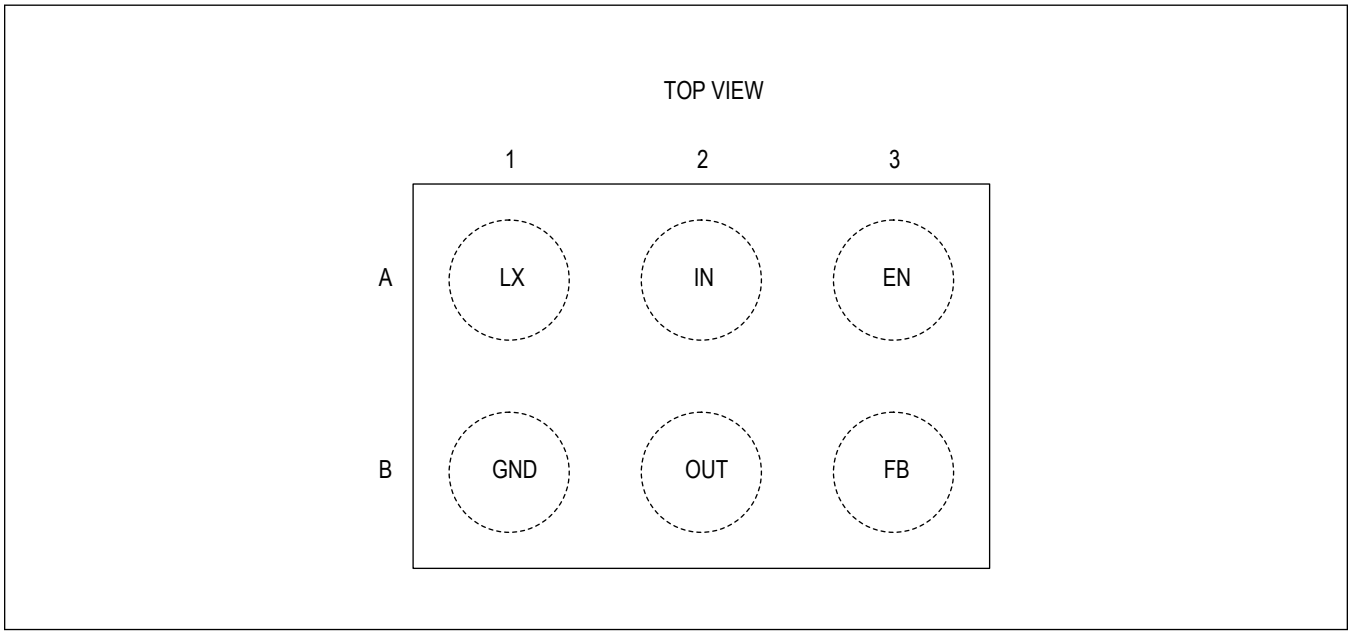
Typical Operating Characteristics (continued)

(MAX17291ANT, V_{IN} = V_{EN} = 3.6V, V_{OUT} = 12V, C_{IN} = 22µF, C_{OUT} = 10µF, L = 10µH, T_A = +25°C, unless otherwise noted.)

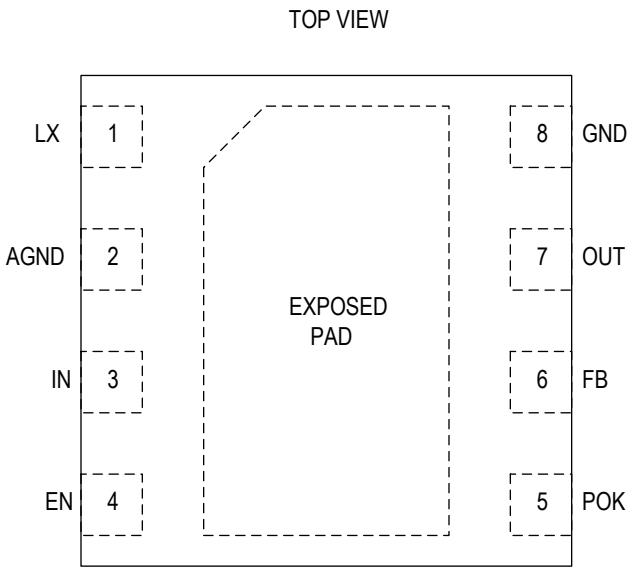


Pin Configurations

WLP



TDFN

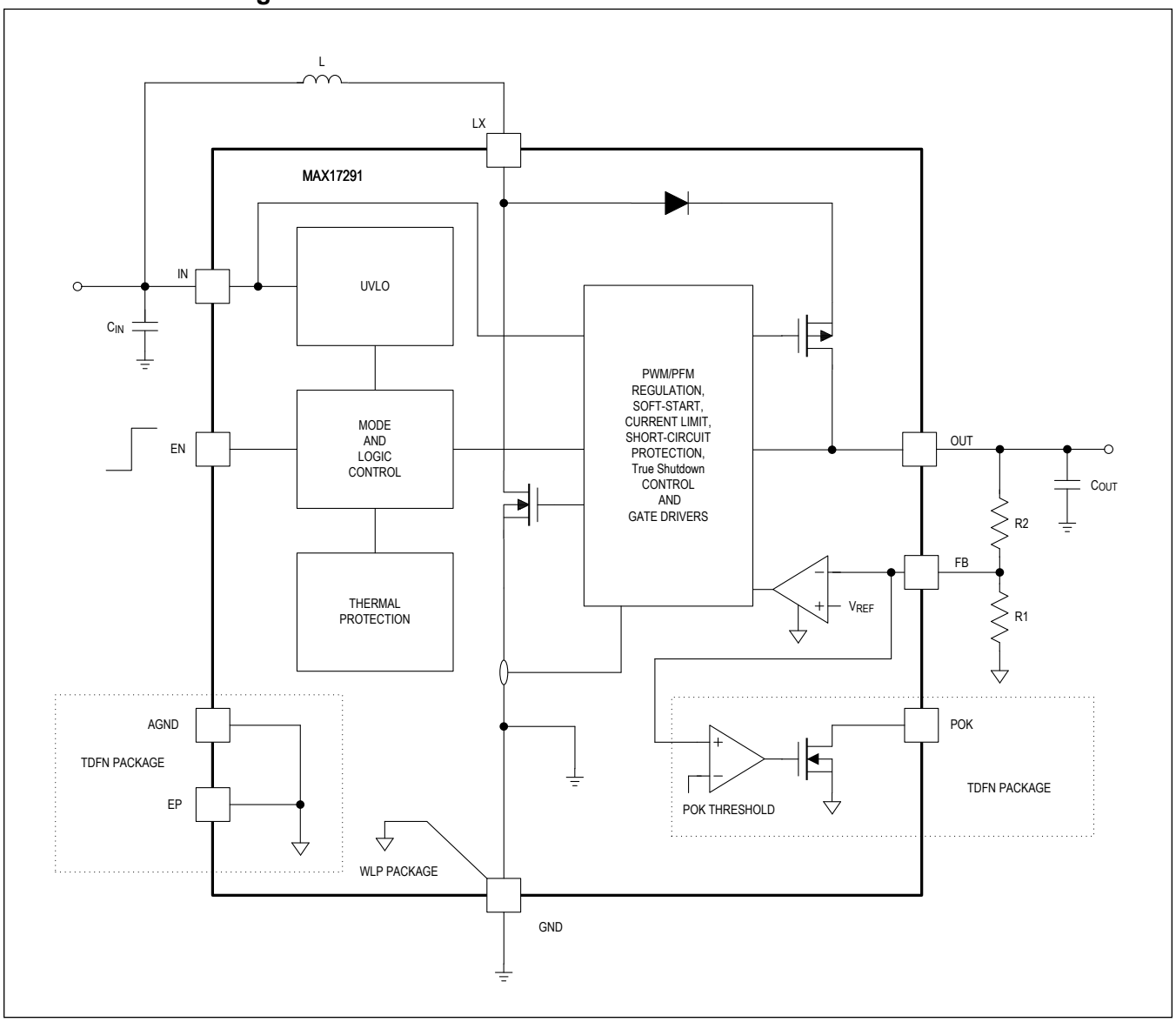


Pin Description

PIN		NAME	FUNCTION
WLP	TDFN		
A1	1	LX	Switching Node Pin. Connect the inductor from IN to LX.
—	2	AGND	Analog Ground Pin. Connect to the exposed pad (EP) externally in the PCB layout at a single point.
A2	3	IN	Input Pin. Connect to a voltage between 1.8V and 5.5V and bypass with a 22µF ceramic capacitor from IN to ground. Connect a 1000pF capacitor as close as possible from IN pin of IC to ground.
A3	4	EN	Active-High Enable Input. Force this pin high to enable the converter. Force this pin low to disable the converter and enter shutdown.
—	5	POK	POK Open-Drain Output Pin. It is held low when output is below regulation. External pullup resistor is required if the feature is used.
B3	6	FB	Feedback Pin. Connect to the center point of a resistor divider network from OUT to GND to set the target output voltage.
B2	7	OUT	Output Pin. Connect a ceramic capacitor between 10µF (C_{EFF} = 6µF) to 22µF (C_{EFF} = 12µF) from OUT to ground.
B1	8	GND	Power Ground Pin. In the TDFN package, applications connect to the exposed pad (EP) externally in the PCB layout at a single point.
—	EP	EP	Exposed Pad. Functionally connected to AGND. Connect GND and AGND pins to exposed pad (EP) externally in PCB layout with short traces under the device. The feedback resistor divider network references to the EP.

Functional Diagram

Functional Block Diagram



Detailed Description

The MAX17291 is a low quiescent current boost (step-up) DC-DC converter with a 1A peak inductor current limit and True Shutdown. True Shutdown disconnects the output from the input with no forward or reverse current. The output voltage is set with an external resistor-divider.

The MAX17291 offers low quiescent current, small total solution size, and high efficiency throughout the entire load range. The MAX17291 is a highly integrated boost converter designed for applications requiring high voltage and tiny solution size, such as sensor modules. It integrates a power switch, power diode, and output load switch. It can output up to 20V from 1.8V to 5.5V input supply. The load switch is turned off under shutdown mode, truly disconnecting the load from the input voltage, thus minimizing the leakage current during shutdown mode. The device operates with a switching frequency of 1.0MHz while in CCM. The MAX17291 switch current limit is 1A. It has 2.2ms built-in soft-start time to minimize the inrush current. The device features short-circuit and thermal protection.

Undervoltage Lockout

An undervoltage lockout (UVLO) circuit is implemented to assure proper behavior while the V_{IN} supply is ramping up or down. The UVLO enables the operation of the converter when the input voltage ramps above the typical UVLO threshold of 1.75V (V_{UVLO}). A hysteresis of 100mV (V_{UVLO_HYS}) assures the device will not stop regulation due to a small V_{IN} transient. Once V_{IN} drops below V_{UVLO} - V_{UVLO_HYS}, the converter is disabled.

Enable and Disable

When V_{IN} is above the UVLO rising threshold and the EN pin is pulled high (V_{EN} > V_{IH}), the MAX17291 is enabled. When the EN pin is pulled low (V_{EN} < V_{IL}), the MAX17291 goes into shutdown mode. While in shutdown mode, the device provides the isolation between the input and output. In this mode, 50nA current is consumed from V_{IN}.

Soft-Start

The soft-start feature provides a way to limit the inrush current drawn from the supply upon startup. The MAX17291 soft-start begins when the EN pin is pulled high above V_{IH}, after which switching is enabled. The output voltage ramp rate is 6V/ms.

Output Short-Circuit Protection

The MAX17291 limits the output current whenever the output voltage drops below the input voltage. This function protects the devices when the output is shorted to ground. When the V_{OUT} is shorted to ground, the peak inductor current is limited to 1A, and 2µs off-time is enforced. Upon recovery from the short-circuit event, the MAX17291 will ramp the output to regulation, maintaining constant input current until V_{OUT} exceeds V_{IN}, at which point V_{OUT} is ramped to the target level using the soft-start rate.

Thermal Shutdown

The MAX17291 goes into thermal shutdown once the junction temperature exceeds +165°C. When the junction temperature drops below the thermal shutdown temperature threshold less the hysteresis, typically to the +150°C level, the device starts operating again.

Device Functional Modes

The MAX17291 operates in two functional modes: light load efficiency and PWM.

Light Load Efficiency Mode

The MAX17291 employs a power-save mode with pulse frequency modulation (PFM) to improve efficiency at light loads. In this mode, the on-time is determined by a peak inductor current limit of 500mA. Once the inductor current hits its limit, the on-time is terminated and the power diode is forward-biased. During the off-time, charge is transferred to output capacitance, causing its voltage to rise. The off-time gets terminated once the inductor current ramps down to zero. The load is supplied by the output capacitor and the output voltage declines. When the FB voltage falls below the PFM reference voltage, the device initiates the on-time again to bring the output voltage up. The MAX17291 will regulate the output to 1% above nominal output target in the light load efficiency mode of operation.

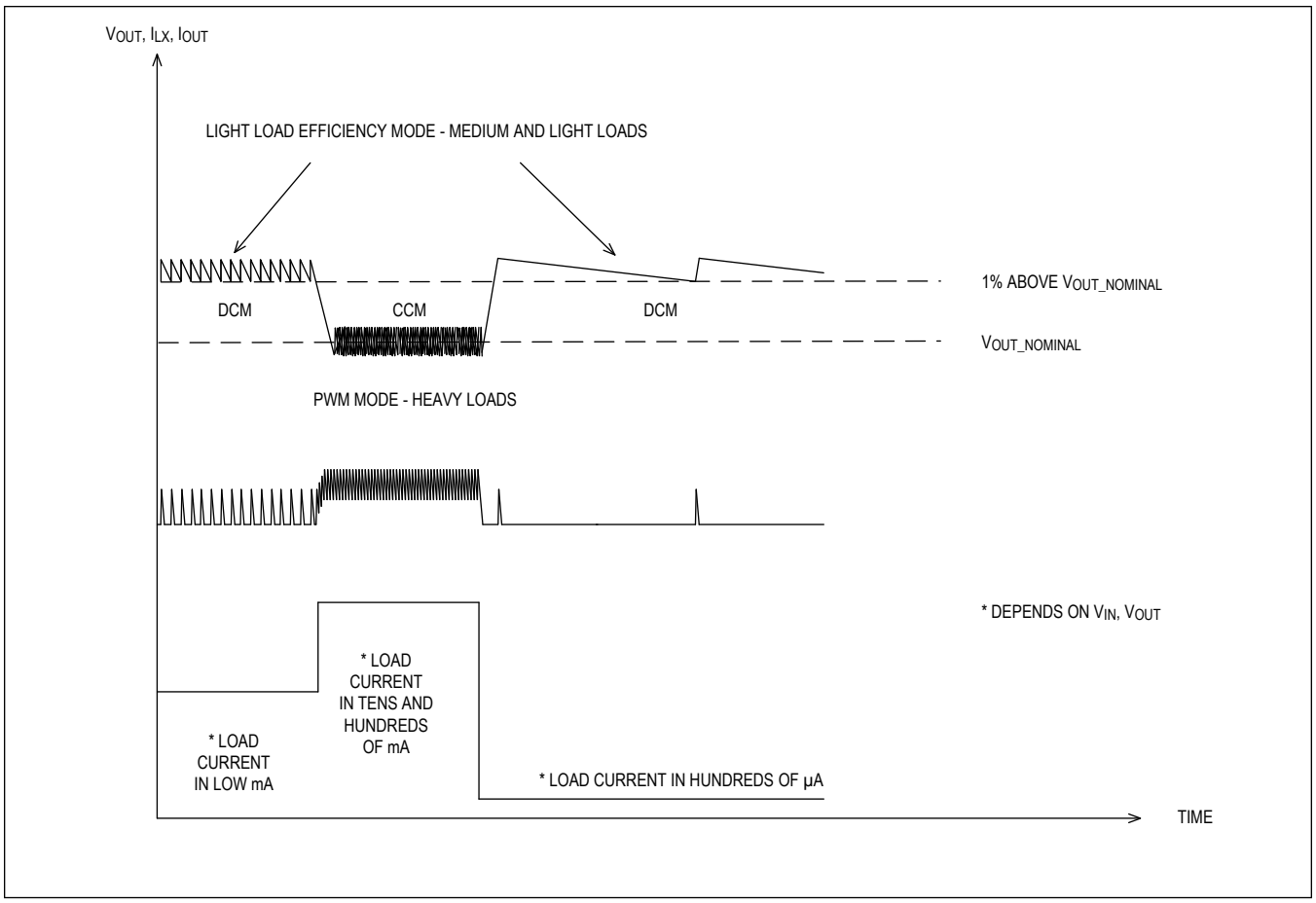


Figure 1. Light Load Efficiency Mode and PWM Mode Waveforms

PWM Mode

The MAX17291 uses a quasi-constant 1.0MHz switching frequency pulse width modulation (PWM) at load current levels in CCM. Based on the input voltage to output voltage ratio, the circuit predicts the required off-time. At the beginning of the switching cycle, the nMOS switching FET is turned on. The input voltage is applied across the inductor and the inductor current ramps up. In this phase, the output capacitor is discharged by the load current. When the inductor current hits the current threshold that is set by the output of the error amplifier, the nMOS switching FET is turned off, and the power diode is forward-biased. The inductor transfers its stored energy to the output capacitor to replenish charge and supply the load. When the off-time expires, the next switching cycle starts again. The error amplifier compares the FB pin voltage with an internal reference voltage, and its output determines the inductor peak current. The MAX17291 has an internal compensation circuit that can accommodate a wide range of input voltage, output voltage, inductor, and output capacitor values for stable operation.

Applications Information

The MAX17291 is a boost DC-DC converter with integrated switching FET, a power diode, and an output load switch. The device supports up to 20V output with an input range from 1.8V to 5.5V. The MAX17291 features current-mode control with adaptive constant off-time. The switching frequency is quasi-constant at 1.0MHz. The load switch disconnects the output from the input during shutdown to minimize leakage current. The following design procedure can be used to select component values for the MAX17291.

Typical Application

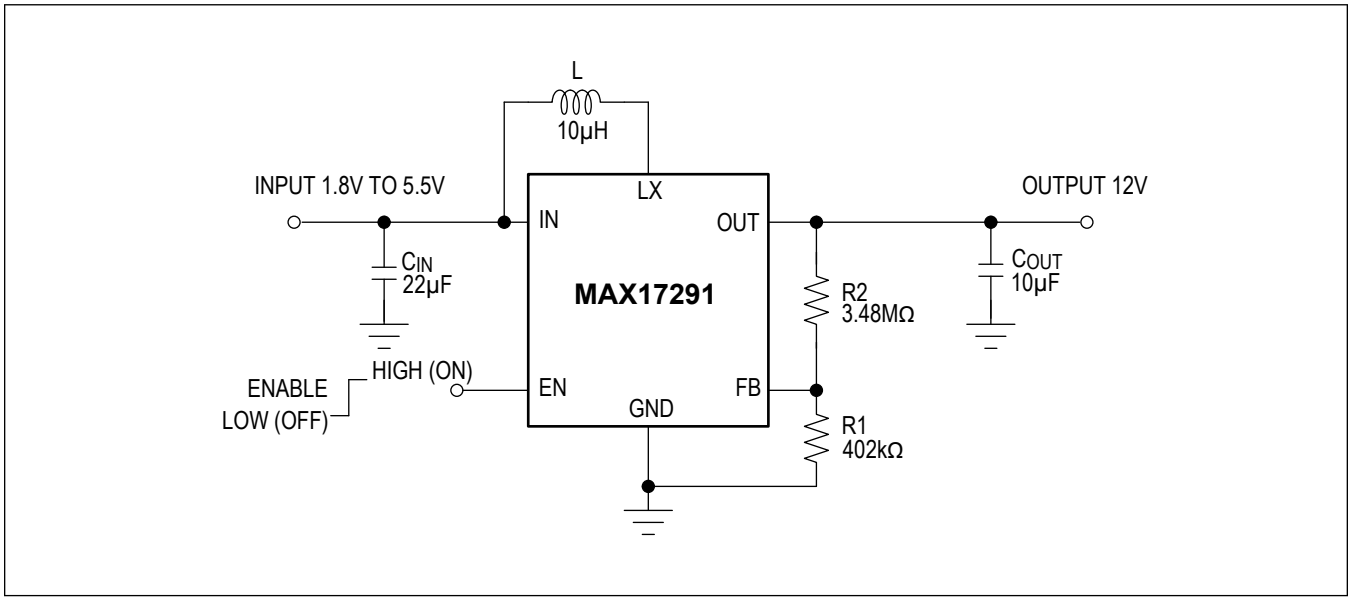


Figure 2. 12V Boost Converter Using the MAX17291

Design Requirements

Table 1. 12V Boost Converter Design Requirements

PARAMETERS	VALUES
Input Voltage	2.0V to 5.0V
Output Voltage	12V
Output Current	50mA
Output Voltage Ripple	±50mV

Detailed Design Procedure

Programming the Output Voltage

The MAX17291 programs V_{OUT} using an external resistor-divider. By selecting the external resistor-divider R1 and R2, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical voltage at the FB pin is 1.25V.

$R2 = ((V_{OUT} / V_{FB}) – 1) \times R1$

Where:

- V_{OUT} is the desired output voltage

- V_{FB} is the internal reference voltage at the FB pin, 1.25V (typ)

For best accuracy, R1 is recommended to have value smaller than 475kΩ to ensure that the current flowing through it is significantly larger than the FB pin bias current. Additionally, using R1 values that are lower increases immunity against noise injection. The advantage of using the higher value R1 is reduction of quiescent current for achieving the highest efficiency at light load currents.

Inductor Selection

Because the selection of the inductor affects steady-state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. The three inductor specifications of importance are: inductance value, saturation current, and DC resistance (DCR). The MAX17291 is designed to work with inductor values between 4.7µH and 15µH. Use the following equations to calculate the inductor's peak current for the application. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To have enough design margin, choose the inductor value with -30% tolerance and a low power conversion efficiency for the calculation.

The inductor's DC current ($I_{L(DC)}$) in amperes can be calculated using the following formula:

$$I_{L(DC)} = (V_{OUT} \times I_{OUT}) / (V_{IN} \times \eta)$$

Where:

V_{OUT} = output voltage

I_{OUT} = output current

V_{IN} = input voltage

η = power conversion efficiency; use 80% for most applications

The inductor ripple current ($\Delta I_{L(PK-PK)}$) in amperes is calculated with the following equation for an asynchronous boost converter in CCM.

$$\Delta I_{L(PK-PK)} = (V_{IN} \times (V_{OUT} + 0.4V - V_{IN})) / ((L \times f_{SW} \times (V_{OUT} + 0.4V))$$

Where:

$\Delta I_{L(PK-PK)}$ = peak-to-peak inductor ripple current in amperes

L = inductance value

f_{SW} = switching frequency, 1MHz (typ)

V_{OUT} = output voltage

V_{IN} = input voltage

Therefore, the inductor peak current ($I_{L(PK)}$) in amperes is calculated with this equation:

$$I_{L(PK)} = I_{L(DC)} + (\Delta I_{L(PK-PK)} / 2)$$

Normally, if the power supply is expected to operate in CCM, it is advisable to work with an inductor peak-to-peak current ripple of less than 40% of the average inductor current. Smaller ripple from a larger valued inductor reduces EMI and the magnetic losses in the inductor. However, load transient response time is increased. Because the MAX17291 is used for relatively small output current applications, the inductor peak-to-peak current ripple could be higher, in which case the MAX17291 will operate mostly in the discontinuous current mode (DCM) of operation.

Table 2. Inductor Value Recommendations

V_{OUT} (V)	L (µH)
5.5 to 7	4.7
7 to 9	6.8
9 to 11	8.2
11 to 17	10
17 to 20	15

Input and Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. This ripple voltage is related to the capacitance and equivalent series resistance (ESR). The ESR impact on the output ripple must be considered. Refer to the capacitor data sheet for ESR information. Effective capacitance is a function of bias, aging, temperature, and AC signal, so proper derating must be taken into account. Always use margin on the voltage rating to ensure adequate capacitance at the required output voltage. Choose a ceramic capacitor because they have the lowest ESR, smallest size, and lowest cost. For output voltages at 8V and below, it is recommended to use 22µF C_{OUT} (12µF effective capacitance). For output voltages above 8V, it is recommended to use 10µF C_{OUT} (6µF effective capacitance). The output capacitor affects the small signal control loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable. Increasing the output capacitor makes the output voltage ripple smaller. In applications where V_{IN} is approaching V_{OUT}, more output capacitance will be required to minimize output voltage ripple.

Input capacitors reduce current peaks from the input supply and increase efficiency. For the input capacitor, choose a ceramic capacitor because they have the lowest equivalent series resistance (ESR), smallest size, and lowest cost. Other capacitor types can be used as well, but will have larger ESR. The biggest downside of ceramic capacitors is their capacitance derating with higher DC bias and, therefore, at minimum a standard 22µF ceramic capacitor (12µF effective capacitance) is recommended at the input for all applications. In applications where V_{IN} approaches V_{OUT}, more input capacitance is required to minimize input voltage ripple. For example, in $5.5V_{OUT}$ applications, an additional 22µF C_{IN} is recommended if V_{IN} is above 4.0V.

Refer to the capacitor data sheet for proper DC bias, AC ripple, and temperature capacitance derating.

Layout Guidelines

As with all switching power supplies, especially those running at a high switching frequency, special attention needs to be paid to printed circuit board (PCB) layout. If the board is not carefully laid out, the regulator could suffer from instability, noise problems, and inefficiency. Due to fast switching edges, in order to prevent radiation of high-frequency noise (EMI), proper layout of the high-frequency switching paths is essential. Minimize the length and area of all traces connected to the LX pin, and always use a ground plane under the switching regulator. The most critical current path for a boost converter is from the switching FET, through the rectifier power diode and output capacitor, and then back to the switching FET through the GND connection. This high-current path contains nanosecond rise and fall time switching edges and should be kept as short as possible. Therefore, the output capacitor needs to be connected as close to OUT and GND pins as possible to reduce parasitic overshoot at the LX and OUT.

The input capacitor connections to IN and GND need to be short to reduce supply voltage ripple. Route the output voltage sensing away from the inductor and LX switching node to minimize noise and magnetic interference. The inductor and LX node need to be separated from the feedback pin and its resistor-divider network by the device itself and component placement clearance. The inductor should be placed on an opposite side from the feedback pin and its resistive-divider network as shown in Figure 3 and Figure 4. The resistor-divider ground reference needs to have a Kelvin connection back to the GND pin. In the TDFN applications, the resistor-divider network reference is routed through the exposed pad back to the AGND pin. Maximize the size of the ground metal on the component side to help with thermal dissipation. Use a ground plane with several vias connecting to the component-side ground to further reduce noise interference on sensitive circuit nodes. It is recommended to consult the MAX17291 EV kit layouts.

Following are layout examples for both WLP and TDFN packages.

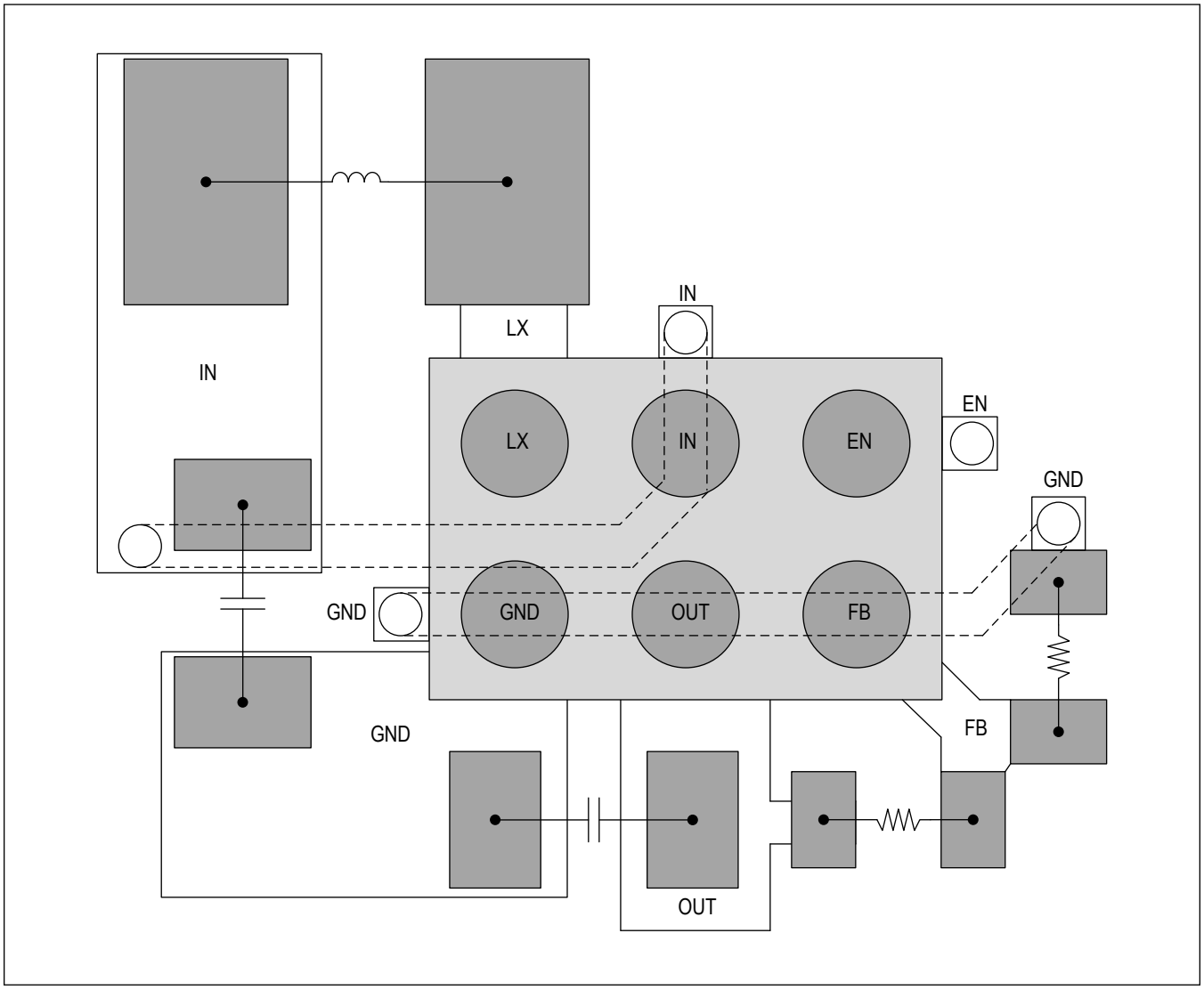


Figure 3. PCB Layout Example WLP Package

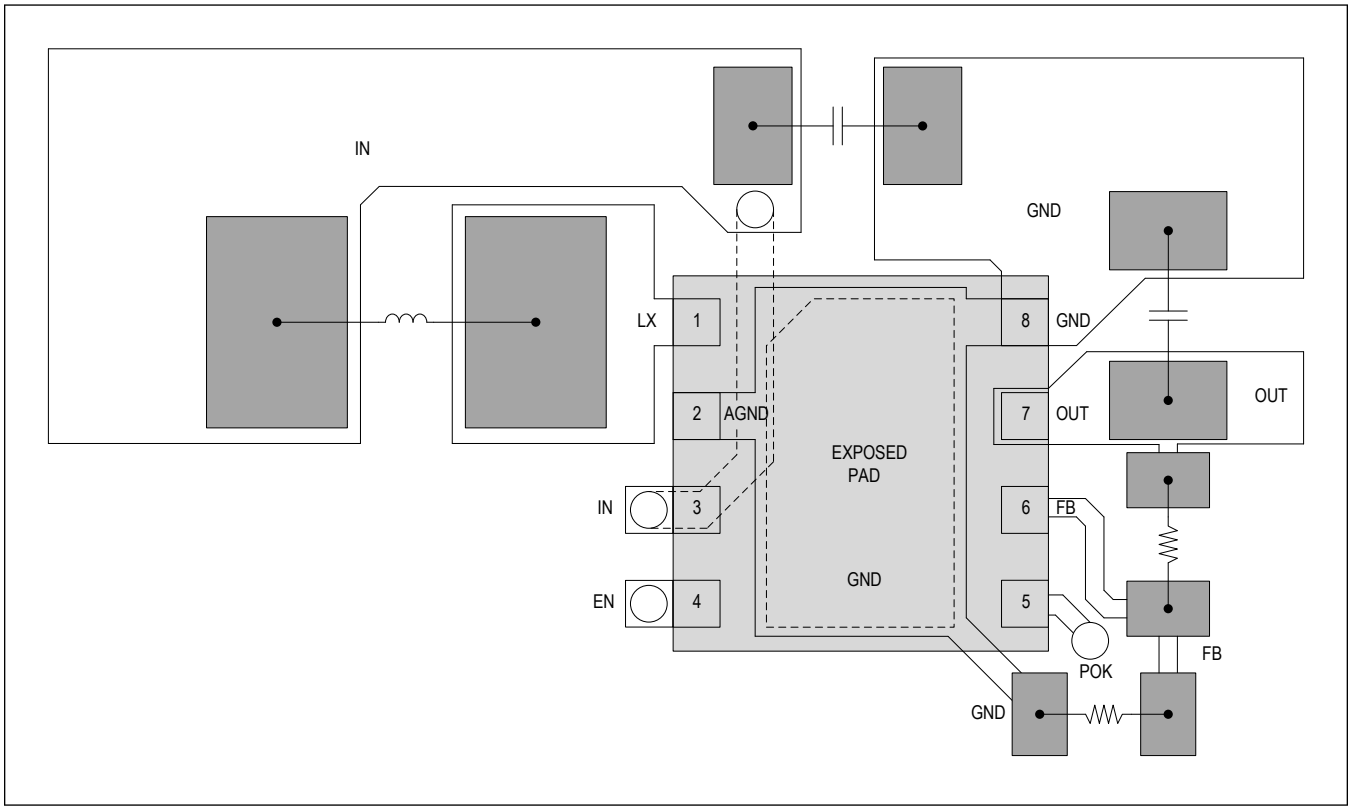


Figure 4. PCB Layout Example TDFN Package

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX17291ANT+T	-40°C to +125°C	6 WLP
MAX17291ATA+T	-40°C to +125°C	8 TDFN-EP

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	03/20	Initial release	—
1	10/20	Updated General Description, Benefits and Features, Typical Application Circuit, Absolute Maximum Ratings, Electrical Characteristics, Typical Operating Characteristics, Pin Description, Functional Diagram, Detailed Description, Applications Information, Ordering Information	1, 2, 6–18, 20
2	11/20	Updated Electrical Characteristics, Ordering Information	7, 8, 20
3	02/23	Package Information - Added POD for WLP and TDFN Packages	7, 8, 9

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX17291ANT+ MAX17291ANT+T MAX17291ATA+T MAX17291ATA+