swissbit®

Product Data Sheet

Industrial CompactFlash™ Card

C-500 Series
up to UDMA6 / MDMA4 / PIO6

Commercial and Industrial Temperature Grade

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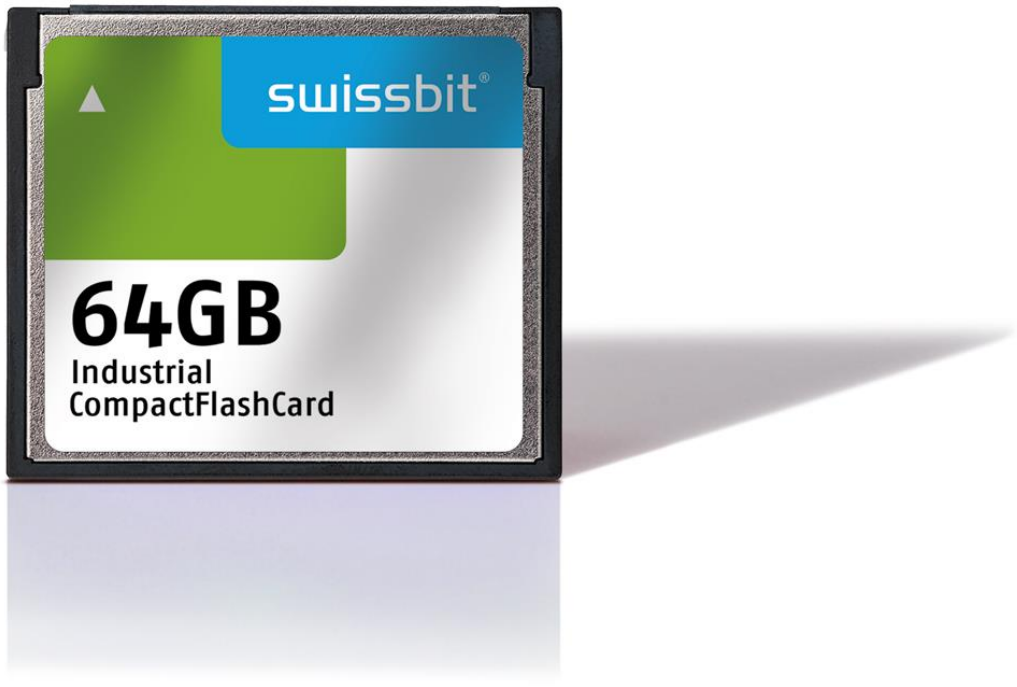


made in germany

Contents

C-500 Series – Industrial CompactFlash™ Card, SLC
128 MBytes up to 64 GBytes

1. Product Summary

- **Capacities:** 128 Mbytes, 256 Mbytes, 512 MBytes, 1 GByte, 2 GBytes, 4 GBytes, 8 GBytes, 16 GBytes, 32 GBytes, 64 GBytes
- **Form Factor:** CompactFlash Card Type I (36.4 mm x 42.8 mm x 3.3 mm)
- **Compliance:** CompactFlash™ specification 5.0 (6.1 compatible)
- **Command Sets:** 48bit, CFA feature set, Security, HPA, download Microcode, Advanced Power Management, S.M.A.R.T.
- **High Performance:**
  - Burst Transfer Rate: Up to 133 MBytes/s UDMA6
  - Read Performance: Sequential Read up to 64 MBytes/s, Random Read IOPS up to 3,200
  - Write Performance: Sequential Write up to 44 MBytes/s, Random Write IOPS up to 1,900
- **Operating Temperature Range[1]:**
  - Commercial: 0 °C to 70 °C
  - Industrial: -40 °C to 85 °C
- **Storage Temperature Range:** -50 °C to 100 °C
- **Operating Voltage:** 3.3V ± 10% / 5V ± 10%
- **Power (Max Capacity):**
  - Read (Active): 120mA
  - Write (Active): 100mA
  - Idle: 4.5mA
- **Data Retention:** 10 Years @ Life Begin; 1 Year @ Life End
- **Endurance[2]:** TeraBytes Written (TBW) @ Max Capacity
  - Enterprise WL: > 409
- **Shock/Vibration:** 1,500 *g* / 20 *g*
- **High-Performance 32-Bit Processor with Integrated, Parallel Flash Interface Engines:**
  - Single-Level Cell (SLC) NAND Flash
  - Hardware BCH Code ECC (up to 60bit correction per 1 KByte page depending on configuration)
- **High Reliability:**
  - Mean Time Between Failure (MTBF): > 3,000,000 hours
  - Data Reliability: < 1 non-recoverable error per 10^{17} bits read

[1] Adequate airflow is required to ensure the drive temperature, as reported in the S.M.A.R.T. data, does not exceed the specified maximum operating temperature.
[2] According to JEDEC (JESD47I), the time to write the full TBW is 18 months. Higher average daily data volume reduces the specified TBW.

2. Product Features

- SLC Flash with 100,000 Program/Erase Cycles and Reduced Write Amplification
- Global, Dynamic and Static Wear Leveling to maximize system write endurance
- Page Mode Flash Translation Layer (FTL) for best in class write performance and endurance
- Data Care Management
  - Read Disturb Management and Dynamic Data Refresh for maximized retention
  - Passive: Background Media Scan
- Lifetime Enhancements
  - Dynamic Bad Block Remapping
  - Write Amplification Reduction
  - Intelligent Garbage Collection
- Management of unexpected power loss
- Up to UDMA6, MDMA4, PIO6 interface speed (max 133 MBytes/s burst)
- Security Feature Set Support
- Optimized for fast boot-up times
- In-Field Firmware Update without user data loss
- Detailed Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.)
- Life Cycle Management
- Controlled "Locked" BOM
- Swissbit Life Time Monitoring (SBLTM) Tool and SDK for SBLTM (on request)

3. Ordering Information

Table 1: Standard Product List

Capacity	Temperature	
	Commercial	Industrial
	Part Number	Part Number
128 MBytes	SFCF0128HxAF1T0-C-MS-5y7-STD	SFCF0128HxAF1T0-I-MS-5y7-STD
256 MBytes	SFCF0256HxAF1T0-C-MS-5y7-STD	SFCF0256HxAF1T0-I-MS-5y7-STD
512 MBytes	SFCF0512HxAF1T0-C-MS-5y7-STD	SFCF0512HxAF1T0-I-MS-5y7-STD
1 GByte	SFCF1024HxAF2T0-C-MS-5y7-STD	SFCF1024HxAF2T0-I-MS-5y7-STD
2 GBytes	SFCF2048HxAF2T0-C-DS-5y7-STD	SFCF2048HxAF2T0-I-DS-5y7-STD
4 GBytes	SFCF4096HxAF2T0-C-QT-5y7-STD	SFCF4096HxAF2T0-I-QT-5y7-STD
8 GBytes	SFCF008GHxAF2T0-C-MS-5y7-STD	SFCF008GHxAF2T0-I-MS-5y7-STD
16 GBytes	SFCF016GHxAF4T0-C-MS-5y7-STD	SFCF016GHxAF4T0-I-MS-5y7-STD
32 GBytes	SFCF032GHxAF2T0-C-QT-5y7-STD	SFCF032GHxAF2T0-I-QT-5y7-STD
64 GBytes	SFCF064GHxAF4T0-C-QT-5y7-STD	SFCF064GHxAF4T0-I-QT-5y7-STD

x = product generation and y = firmware revision

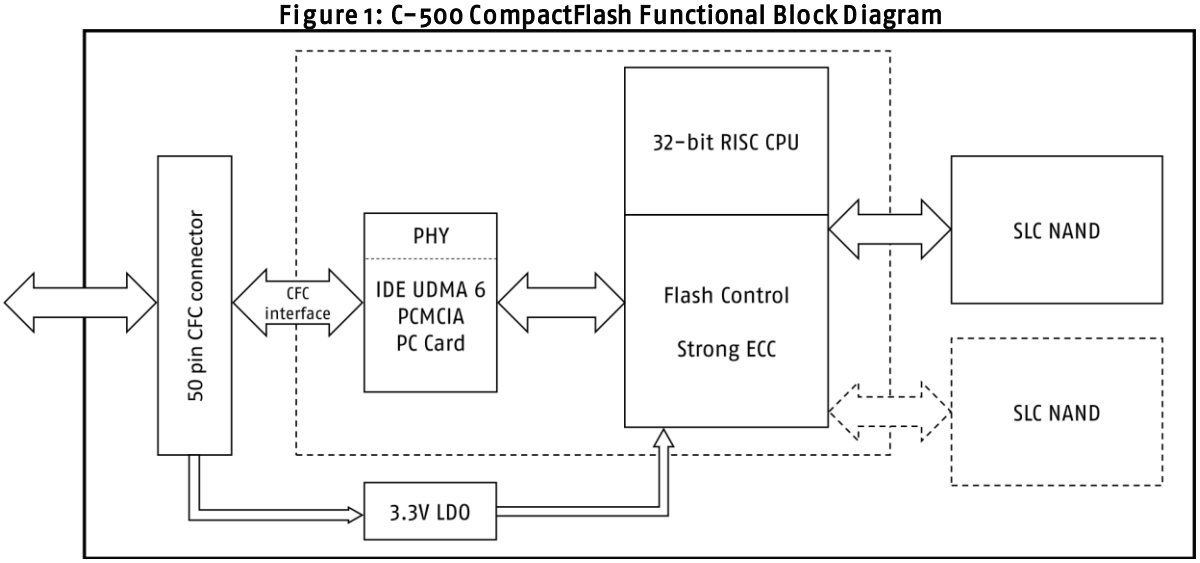
Table 2: Available Part Numbers

Capacity	Temperature	
	Commercial	Industrial
	Part Number	Part Number
128 MBytes	SFCF0128H1AF1T0-C-MS-527-STD	SFCF0128H1AF1T0-I-MS-527-STD
256 MBytes	SFCF0256H1AF1T0-C-MS-527-STD	SFCF0256H1AF1T0-I-MS-527-STD
512 MBytes	SFCF0512H1AF1T0-C-MS-527-STD	SFCF0512H1AF1T0-I-MS-527-STD
1 GByte	SFCF1024H1AF2T0-C-MS-527-STD	SFCF1024H1AF2T0-I-MS-527-STD
2 GBytes	SFCF2048H1AF2T0-C-DS-527-STD	SFCF2048H1AF2T0-I-DS-527-STD
4 GBytes	SFCF4096H1AF2T0-C-QT-527-STD	SFCF4096H1AF2T0-I-QT-527-STD
8 GBytes	SFCF008GH1AF2T0-C-MS-527-STD	SFCF008GH1AF2T0-I-MS-527-STD
16 GBytes	SFCF016GH1AF4T0-C-MS-527-STD	SFCF016GH1AF4T0-I-MS-527-STD
32 GBytes	SFCF032GH1AF2T0-C-QT-527-STD	SFCF032GH1AF2T0-I-QT-527-STD
64 GBytes	SFCF064GH1AF4T0-C-QT-527-STD	SFCF064GH1AF4T0-I-QT-527-STD

4. Product Description

The Swissbit® C-500 continues Swissbit's line of CompactFlash™ memory cards of small form factor non-volatile high capacity storage. The CompactFlash™ card is an established removable device for industrial and NetCom applications as boot device or data storage. The C-500 is using a page based flash translation layer (FTL) mapping which allows high write data volume especially for logging of small data packages while maintaining best endurance.
Multiple firmware features as global, static and dynamic wear leveling, bad block remapping and a sophisticated page based mapping leverage best in class endurance even for critical application. Data care management provides at the same time best retention for infrequently written data sections.
The C-500 has an internal high performance 32-bit RISC controller, which manages interface protocols, data storage and retrieval as well as hardware BCH-code Error Correction Code (ECC), defect handling, diagnostics and clock control.
The firmware structure and CPU performance enable fast boot times in the system.

Figure 1: C-500 CompactFlash Functional Block Diagram



The C-500 operates in three basic modes:

- PC card ATA I/O mode
- PC card ATA memory mode
- True IDE mode up to UDMA6, MDMA2,PIO4

The CompactFlash™ also supports Advanced Timing modes. Advanced Timing modes are ATA I/O modes that are 100ns or faster, ATA Memory modes that are 100ns or 80ns.
Standard cards are configured as max. UDMA6 (30ns) and PIO6/MDMA4 (80ns).
If the cards should be used in extended speed modes, they should be qualified on the target system and the system should fulfill the signal requirements.
It conforms to the PCMCIA Card Specification 8.0 when operating in the ATA I/O mode, and in the ATA Memory mode (Personal Computer Memory Card International Association standard, JEIDA in Japan), and to the ATA specification when operating in True IDE Mode. CompactFlash™ Cards can be used with passive adapters in a PC-Card Type I, II, or Type III socket.
Once the card has been configured by the host, it behaves as a standard ATA (IDE) disk drive. The card has a voltage detector and a powerful power-loss management feature to prevent data corruption after unexpected power-down.
The specification has been realized and approved by the CompactFlash™ Association (CFA).
This non-proprietary specification enables users to develop CF products that function correctly and are compatible with future CF design.

Related Documentation

- CF+ and CompactFlash™ Specification Revision 6.1
- AT Attachment Interface Document, American National Standards Institute, ATA-7, 2005
- PCMCIA PC Card Standard, 1995
- PCMCIA PC Card ATA Specification 8.0

Detailed description in the CompactFlash specification
https://www.compactflash.org/cfa-specifications

4.1 Performance Specifications

The C-500 read/write sequential and random performance benchmarks are detailed in the following Table 3.

Table 3: Read/Write Performance[3]

Capacity	Sequential Read (MBPS)	Sequential Write (MBPS)	Random Read 4k (IOPS)	Random Write 4k (IOPS)
128 MBytes	32.2	19.9	2,960	1,870
256 MBytes	32.2	19.9	2,960	1,870
512 MBytes	32.2	19.9	2,960	1,870
1 GByte	64.1	29.0	3,060	1,380
2 GBytes	62.9	28.6	2,840	1,370
4 GBytes	62.0	37.5	3,180	1,430
8 GBytes	64.3	39.0	3,030	1,290
16 GBytes	64.4	43.6	2,870	1,320
32 GBytes	64.4	43.5	2,870	1,330
64 GBytes	64.5	42.8	2,880	1,330

4.2 Current Consumption

The drive-level current consumption as a function of operating mode is shown below in Table 4.
The current is about the same at 3.3V as for 5V.

Table 4: Current Consumption for max transfer speed at 5V (and 3.3V)[4]

Drive Capacity	Sequential Read	Sequential Write	Random Read 4k	Random Write 4k	Idle	Unit
128 MBytes	65	50	44	43	4.5	mA
256 MBytes	65	50	44	43	4.5	
512 MBytes	65	50	44	43	4.5	
1 GByte	90	70	44	43	4.5	
2 GBytes	95	70	44	43	4.5	
4 GBytes	100	100	44	43	4.5	
8 GBytes	100	70	47	43	4.5	
16 GBytes	100	85	47	43	4.5	
32 GBytes	110	95	50	45	4.5	
64 GBytes	120	100	53	47	4.5	

[3] The values are measured using CrystalDiskMark 6.0.0 x64 (CDM) at IDE interface in UDMA6 mode (Seq Q32T1 and 4KiB Q8T8). Performance depends on flash type and number, file/cluster size, and burst speed.
[4] All values are the typical recorded at 25 °C, with 5V supply voltage at fastest CrystalDiskMark 6.0.0 x64 at IDE interface.

4.3 Environmental Specifications

4.3.1 Recommended Operating Conditions[5]

The recommended operating conditions for the C-500 CompactFlash Cards are provided in Table 5 below.

Table 5: Recommended Operating Conditions

Parameter	Value
Commercial Operating Temperature	0 °C to 70 °C
Industrial Operating Temperature	-40 °C to 85 °C
Power Supply V_{CC} Voltage	3.3 V ± 10% or 5V ± 10%

4.3.2 Recommended Storage Conditions

The recommended storage conditions are listed in the following Table 6.

Table 6: Recommended Storage Conditions

Parameter	Value
Commercial Storage Temperature	-50 °C to 100 °C [6]
Industrial Storage Temperature	-50 °C to 100 °C [6]

4.3.3 Shock, Vibration and Humidity

The maximum shock, vibration and humidity conditions are listed below in the Table 7.

Table 7: Shock, Vibration and Humidity

Parameter	Value
Non-Operating Shock	1,500 *g* Peak (JESD22-B110)
Non-Operating Vibration	20 *g* Peak, 10-2000 Hz
Humidity (Non-Condensing)	85% RH 85 °C, 1000 hrs (JESD22-A101)

[5] Adequate airflow is required to ensure the drive temperature, as reported in the S.M.A.R.T. data, does not exceed the specified maximum operating temperature.

[6] The retention at high temperature is reduced. The acceleration factor at 100°C compared with 55°C is 110, i.e. the initial endurance at 10 years@55°C is reduced to 33 days@100°C.

4.4 Regulatory Compliance

The C-500 devices comply with the standards listed in the following Table 8.

Table 8: Regulatory Compliance

Compliance	Country	Type	Standard(s)/Directive
CE	European Union	Certificate	EMC, RoHS, WEEE
CE/ EMC	European Union	Compliance	2014/30/EU EN61000-6-2 :2005 CISPR 32 :2015 EN 55032:2015 IEC 61000-4-2 :2008 IEC 61000-4-3 :2010-04
CE/ RoHS	European Union	Compliance	2011/65/EU, 2015/863
CE/ WEEE	European Union	Compliance	2012/19/EU
REACH	European Union	Certificate	1907/2006
FCC	United States	Compliance	47 CFR Part 15, class B
UL	United States	Compliance	Conformity by subparts

4.5 Mechanical Specifications

The C-500 Card has a female 50-pin CompactFlash™ connector. Physical dimensions are detailed in Table 9 below. Figure 2 at page 13 illustrates the C-500 dimensions and connector location.

Table 9: Measured Physical Dimensions

Physical Dimensions		Unit
Length	36.40±0.15	mm
Width	42.80±0.10	
Thickness (Max)	3.30±0.10	
Weight (Max Capacity)	10	g

4.6 Reliability and Endurance

The Mean Time Between Failure (MTBF) is specified to exceed the value listed in the following Table 10. Data reliability with effective error tolerance and data retention at the beginning and end of life is also provided.

Table 10: Reliability

Parameter	Value
MTBF (at 25 °C)	> 3,000,000 hours
Data Reliability	< 1 Non-Recoverable Error per 10^{17} Bits Read
Data Retention	10 Years at Start (JESD47), 1 Year at EOL

Endurance represented as both TeraBytes Written (TBW) and full Drive Writes Per Day (DWPD) is provided in the following Table 11.

Table 11: Endurance[7]

Card Capacity	Enterprise	
	TBW	DWPD
128 MBytes[8]	35.4	151.74
256 MBytes[8]	26.8	57.43
512 MBytes	2.3	2.53
1 GByte	4.1	2.23
2 GBytes	8.2	2.24
4 GBytes	17.5	2.40
8 GBytes	38.2	2.62
16 GBytes	89.3	3.06
32 GBytes	163.5	2.80
64 GBytes	409.3	3.50

4.7 Drive Geometry Specification

The C-500 CompactFlash card geometry is set to LBA settings as shown below in Table 12.

Table 12: Drive Geometry

Card Capacity	Cylinders	Heads	Sectors / track	Sectors (LBA)	Total addressable capacity (Bytes)
128 MBytes	937	8	32	239,872	122,814,464
256 MBytes	980	16	32	501,760	256,901,120
512 MBytes	993	16	63	1,000,944	512,483,328
1 GByte	1986	16	63	2,001,888	1,024,966,656
2 GBytes	3,970	16	63	4,001,760	2,048,901,120
4 GBytes	7,964	16	63	8,027,712	4,110,188,544
8 GBytes	15,880	16	63	16,007,040	8,195,604,480
16 GBytes	16,383 [9]	16	63	31,717,728	16,239,476,736
32 GBytes	16,383 [9]	16	63	64,028,160	32,782,417,920
64 GBytes	16,383 [9]	16	63	125,313,024	64,160,268,288

[7] Enterprise workloads follow the JEDEC JESD219 standard. Enterprise workload values are measured based on 168 hours of runtime. DWPD values with consideration of warranty period of 5 years for SLC.
[8] Based on 512 MBytes NAND size
[9] The CHS addressing is limited to about 8GB. Larger drives should be used in LBA mode.

5. Electrical Interface

5.1 *Electrical description*

The CompactFlash™ Memory Card operates in three basic modes:

- PC Card ATA using I/O Mode
- PC Card ATA using Memory Mode
- True IDE Mode with MWDMA and UDMA, which is compatible with most disk drives

The signal/pin assignments are listed in Table 13 Low active signals have a '-' prefix. Pin types are Input, Output or Input/Output.

The configuration of the Card is controlled using the standard PC card configuration registers starting at address 200h in the Attribute Memory space of the memory card. Inputs are signals sourced from the host while Outputs are signals sourced from the Card. The signals are described for each of the three operating modes.

All outputs from the Card are totem pole except the data bus signals that are bi-directional tri-state. Refer to the section titled "Electrical Specifications" for definitions of Input and Output type.

Detailed description in the CompactFlash specification
https://www.compactflash.org/cfa-specifications

Table 13: Pin Assignment and Pin Type

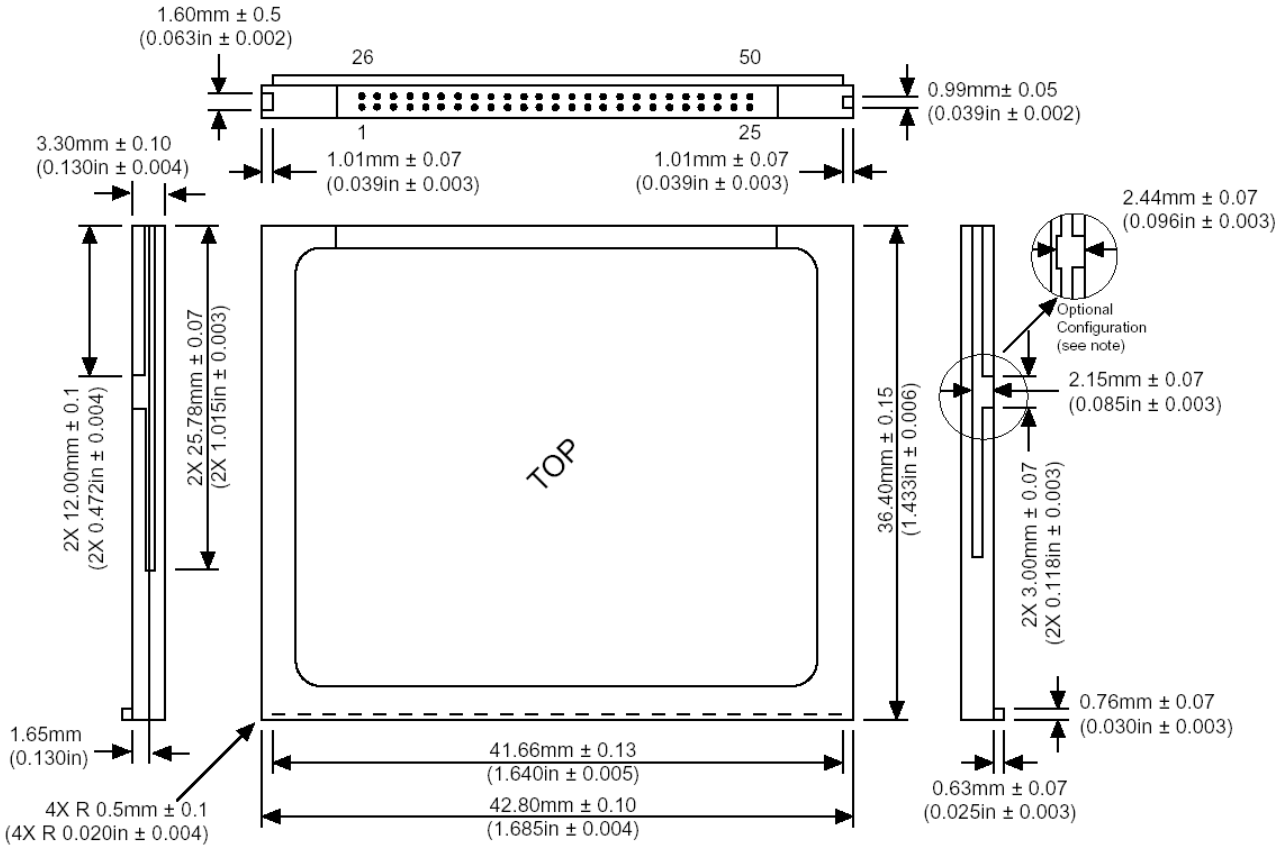
Pin Num	PC Card Memory Mode			PC Card I/O Mode			True IDE Mode(4)		
	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type
1	GND		Ground	GND		Ground	GND		Ground
2	D3	I/O	I1Z,OZ3	D3	I/O	I1Z,OZ3	D3	I/O	I1Z,OZ3
3	D4	I/O	I1Z,OZ3	D4	I/O	I1Z,OZ3	D4	I/O	I1Z,OZ3
4	D5	I/O	I1Z,OZ3	D5	I/O	I1Z,OZ3	D5	I/O	I1Z,OZ3
5	D6	I/O	I1Z,OZ3	D6	I/O	I1Z,OZ3	D6	I/O	I1Z,OZ3
6	D7	I/O	I1Z,OZ3	D7	I/O	I1Z,OZ3	D7	I/O	I1Z,OZ3
7	-CE1	I	I3U	-CE1	I	I3U	-CS0	I	I3Z
8	A10	I	I1Z	A10	I	I1Z	A10(2)	I	I1Z
9(1)	-OE	I	I3U	-OE	I	I3U	-ATASEL	I	I3U
10	A9	I	I1Z	A9	I	I1Z	A9(2)	I	I1Z
11	A8	I	I1Z	A8	I	I1Z	A8(2)	I	I1Z
12	A7	I	I1Z	A7	I	I1Z	A7(2)	I	I1Z
13	Vcc		Power	Vcc		Power	Vcc		Power
14	A6	I	I1Z	A6	I	I1Z	A6(2)	I	I1Z
15	A5	I	I1Z	A5	I	I1Z	A5(2)	I	I1Z
16	A4	I	I1Z	A4	I	I1Z	A4(2)	I	I1Z
17	A3	I	I1Z	A3	I	I1Z	A3(2)	I	I1Z
18	A2	I	I1Z	A2	I	I1Z	A2	I	I1Z
19	A1	I	I1Z	A1	I	I1Z	A1	I	I1Z
20	A0(11)	I	I1Z	A0(11)	I	I1Z	A0	I	I1Z
21	D0	I/O	I1Z,OZ3	D0	I/O	I1Z,OZ3	D0	I/O	I1Z,OZ3
22	D1	I/O	I1Z,OZ3	D1	I/O	I1Z,OZ3	D1	I/O	I1Z,OZ3
23	D2	I/O	I1Z,OZ3	D2	I/O	I1Z,OZ3	D2	I/O	I1Z,OZ3
24	WP	0	OT3	-IOIS16(10)	0	OT3	-IOIS16	0	ON3
25	-CD2	0	Ground	-CD2	0	Ground	-CD2	0	Ground
26	-CD1	0	Ground	-CD1	0	Ground	-CD1	0	Ground
27	D11(1)	I/O	I1Z,OZ3	D11(1)	I/O	I1Z,OZ3	D11(1)	I/O	I1Z,OZ3
28	D12(1)	I/O	I1Z,OZ3	D12(1)	I/O	I1Z,OZ3	D12(1)	I/O	I1Z,OZ3
29	D13(1)	I/O	I1Z,OZ3	D13(1)	I/O	I1Z,OZ3	D13(1)	I/O	I1Z,OZ3

Pin Num	PC Card Memory Mode			PC Card I/O Mode			True IDE Mode[4]		
	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type
30	D14[1]	I/O	I1Z,OZ3	D14[1]	I/O	I1Z,OZ3	D14[1]	I/O	I1Z,OZ3
31	D15[1]	I/O	I1Z,OZ3	D15[1]	I/O	I1Z,OZ3	D15[1]	I/O	I1Z,OZ3
32	-CE2[1]	I	I3U	-CE2[1]	I	I3U	-CS1[1]	I	I3Z
33	-VS1	O	Ground	-VS1	O	Ground	-VS1	O	Ground
34	-IORD	I	I3U	-IORD	I	I3U	-IORD[7] HSTROBE[8] -HDMARDY[9]	I	I3Z
35	-IOWR	I	I3U	-IOWR	I	I3U	-IOWR[7] STOP[8][9]	I	I3Z
36	-WE	I	I3U	-WE	I	I3U	-WE[3]	I	I3U
37	READY	O	OT1	-IREQ	O	OT1	INTRQ	O	OZ1
38	Vcc		Power	Vcc		Power	Vcc		Power
39	-CSEL[5]	I	I2Z	-CSEL[5]	I	I2Z	-CSEL	I	I2U
40	-VS2	O	OPEN	-VS2	O	OPEN	-VS2	O	OPEN
41	RESET	I	I2U	RESET	I	I2U	-RESET	I	I2U
42	-WAIT -DDMARDY[10] -DSTROBE[11]	O	OT1	-WAIT -DDMARDY[10] -DSTROBE[11]	O	OT1	IORDY[7] -DDMARDY[8] DSTROBE[9]	O	ON1
43	-INPACK -DMARQ[12]	O	OT1	-INPACK -DMARQ[12]	O	OT1	DMARQ	O	OZ1
44	-REG -DMACK[12]	I	I3U	-REG -DMACK[12]	I	I3U	-DMACK[6]	I	I3U
45	BVD2	I/O	I1U,OT1	-SPKR	I/O	I1U,OT1	-DASP	I/O	I1U,ON1
46	BVD1	I/O	I1U,OT1	-STSCHG	I/O	I1U,OT1	-PDIAG	I/O	I1U,ON1
47	D8[1]	I/O	I1Z,OZ3	D8[1]	I/O	I1Z,OZ3	D8[1]	I/O	I1Z,OZ3
48	D9[1]	I/O	I1Z,OZ3	D9[1]	I/O	I1Z,OZ3	D9[1]	I/O	I1Z,OZ3
49	D10[1]	I/O	I1Z,OZ3	D10[1]	I/O	I1Z,OZ3	D10[1]	I/O	I1Z,OZ3
50	GND		Ground	GND		Ground	GND		Ground

1. These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
2. The signal should be grounded by the host.
3. The signal should be tied to VCC by the host.
4. The mode is required for CompactFlash™ Storage Cards.
5. The –CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.
6. If DMA operations are not used, the signal must be held high or tied to VCC by the host.
7. Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.
8. Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.
9. Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.
10. Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Write is active.
11. Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Read is active.
12. Signal usage in PC Card I/O and Memory Mode when Ultra DMA protocol is active.
13. Signal is a totem-pole output during Ultra DMA data bursts in True IDE mode.

6. Package Mechanical

Figure 2: Type I CompactFlash™ Memory Card Dimensions in mm (inch)



7. ATA Commands

This section defines the software requirements and the format of the commands the Host sends to the Card. Commands are issued to the Card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. There are three classes of command acceptance, all dependent on the host not issuing commands unless the Card is not busy (BSY is '0').

- **Class 1:** Upon receipt of a Class 1 command, the Card sets BSY within 400ns.
- **Class 2:** Upon receipt of a Class 2 command, the Card sets BSY within 400ns, sets up the sector buffer for a write operation, sets DRQ within 700µs, and clears BSY within 400ns of setting DRQ.
- **Class 3:** Upon receipt of a Class 3 command, the Card sets BSY within 400ns, sets up the sector buffer for a write operation, sets DRQ within 20ms (assuming no re-assignments), and clears BSY within 400ns of setting DRQ.

For reasons of backward compatibility some commands are implemented as 'no operation' NOP.
Table 14 summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.
Details in the CompactFlash or ATA specification.

Table 14: CF-ATA Command Set

Class	Command	Code	FR(1)	SC(2)	SN(3)	CY(5:4)	DH(6)	LBA(5:3)
1	Check Power Mode	E5h or 98h					D	
2	Data Set Management	06h		YY			D	YY
2	Download Microcode	92h	Y	Y	Y		Y	
2	Download Microcode DMA	93h	Y	Y	Y		Y	
1	Erase Sector(s)	C0h		Y	Y	Y	Y	Y
1	Execute Drive Diagnostic	90h					D	
1	Flush cache	E7h					D	
1	Flush cache Ext	EAh					D	
2	Format track	50h		Y		Y	Y	Y
1	Identify Drive	ECh					D	
1	Idle	E3h or 97h		Y			D	
1	Idle Immediate	E1h or 95h					D	
1	Initialize Drive Parameters	91h		Y			Y	
1	Media Lock	DEh					D	
1	Media Unlock	DFh					D	
1	NOP	00h					D	
1	Read Buffer	E4h					D	
1	Read DMA	C8h or C9h		Y	Y	Y	Y	Y
1	Read DMA Ext	25h		YY	YY	YY	D	YY
1	Read Log Ext	2Fh		YY	YY	YY	D	YY
1	Read Log DMA Ext	47h		YY	YY	YY	D	YY
1	Read Multiple	C4h		Y	Y	Y	Y	Y
1	Read Multiple Ext	29h		YY	YY	YY	D	YY
1	Read native max address	F8h					D	
1	Read native max addr Ext	27h					D	
1	Read Sector(s)	20h or 21h		Y	Y	Y	Y	Y
1	Read Sector(s) Ext	24h		YY	YY	YY	D	YY
1	Read Verify Sector(s)	40h or 41h		Y	Y	Y	Y	Y
1	Read Verify Sector(s) Ext	42h		YY	YY	YY	D	YY
1	Recalibrate	1Xh					D	
1	Request Sense	03h					D	
1	Security Disable Password	F6h					D	
1	Security Erase Prepare	F3h					D	

Class	Command	Code	FR(1)	SC(2)	SN(3)	CY(5:4)	DH(6)	LBA(5:3)
1	Security Erase Unit	F4h					D	
1	Security Freeze Lock	F5h					D	
1	Security Set Password	F1h					D	
1	Security Unlock	F2h					D	
1	Seek	7Xh			Y	Y	Y	Y
1	Set Features	EFh	Y				D	
	Set max address	F9h		Y	Y	Y	Y	Y
	Set max address Ext	37h		YY	YY	YY	D	YY
1	Set Multiple Mode	C6h		Y			D	
1	Set Sleep Mode	E6h or 99h					D	
1	S.M.A.R.T.	Boh	Y	Y		Y	D	
1	Stand By	E2h or 96h					D	
1	Stand By Immediate	Eoh or 94h					D	
1	Translate Sector	87h		Y	Y	Y	Y	Y
2	Write Buffer	E8h					D	
2	Write DMA	CAh or CBh		Y	Y	Y	Y	Y
2	Write DMA Ext	35h		YY	YY	YY	D	YY
2	Write DMA FUA Ext	3Dh		Y	Y	Y	Y	Y
2	Write Log Ext	3Fh		YY	YY	YY	D	YY
2	Write Log DMA Ext	57h		YY	YY	YY	D	YY
3	Write Multiple	C5h		Y	Y	Y	Y	Y
3	Write Multiple Ext	39h		YY	YY	YY	D	YY
3	Write Multiple FUA Ext	CEh		Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDh		Y	Y	Y	Y	Y
2	Write Sector(s)	30h or 31h		Y	Y	Y	Y	Y
2	Write Sector(s) Ext	34h		YY	YY	YY	D	YY
2	Write Sector(s) w/o Erase	38h		Y	Y	Y	Y	Y
3	Write Verify	3Ch		Y	Y	Y	Y	Y

FR = Features Register (1),
SC = Sector Count Register (2),
SN = Sector Number Register (3),
CY = Cylinder Registers (5:4),
DH = Card/Drive/Head Register (6),
LBA = Logical Block Address Mode Supported (see command descriptions for use),
Y – The register contains a valid parameter for this command. For the Drive/Head Register Y means both the CompactFlash™ Memory Card and head parameters are used.
YY – registers must be written twice for 48bit LBA commands
D – only the Compact Flash Memory Card parameter is valid and not the head parameter C – the register contains command specific data (see command descriptors for use).

8. Identify Device Information

The following table describes the 512 bytes of data the drive returns for the Identify Device command (ECh).

Table 15: Identify Device Information

Word(s)	Default Value	Total Bytes	Data Field Type Information
0	045Ah* 848Ah	2	Standard Configuration Fixed in IDE mode Standard Configuration removable in PC card mode
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4-5	0000h	4	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per drive (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (right-justified)
20-21	0000h	4	Obsolete
22	0004h	2	# ECC bytes passed on Read/Write Long Commands
23-26	aaaa	8	Firmware revision in ASCII (big-endian byte order in Word)
27-46	XXXX*	40	Model number in ASCII (right-justified)
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Double word not supported
49	0F00h*	2	Capabilities: DMA, LBA, IORDY supported
50	4001h	2	Capabilities: device specific standby timer minimum
51	0200h	2	PIO data transfer cycle timing mode 2
52	0000h	2	DMA data transfer cycle timing mode not supported
53	0007h*	2	Data Fields 54 to 58, 64 to 70 and 88 are valid
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in LBAs (Word 57 = LSW, Word 58 = MSW)
59	010Xh*	2	Multiple sector setting (host changeable)
60-61	XXXXh	4	Total number of sectors addressable in LBA mode
62	0000h	2	Single Word DMA transfer not implemented
63	0X07h*	2	Multiword DMA transfer support modes 2, 1, and 0
64	0003h	2	Advanced PIO modes supported
65	0078h*	2	Minimum Multiword DMA transfer cycle time per Word
66	0078h*	2	Recommended Multiword DMA transfer cycle time
67	0078h*	2	Minimum PIO transfer cycle time without flow control
68	0078h*	2	Minimum PIO transfer cycle time with IORDY flow control
69	4100h	2	Deterministic read after DSM Trim , Download Microcode DMA supported
70-79	0000h	20	Reserved
80	01E0h	2	Major version number, ATA-5 to ATA-8 support
81	0000h	2	Minor version number, not reported
82	746Bh*	2	Command set: NOP, READ BUFFER, WRITE BUFFER, Host Protected Area, look-ahead, volatile write cache, power management feature set, Security Mode feature set, SMART feature set

Word(s)	Default Value	Total Bytes	Data Field Type Information
83	750Dh*	2	Command set: FLUSH CACHE, FLUSH CACHE EXT, LBA48, Set Max Security Extension, Advanced Power Management, CFA feature set, DOWNLOAD MICROCODE
84	4063*h	2	Command set/feature supported extension: Write FUA Ext, General Purpose Logging, SMART self-test, SMART error logging
85	74XXh*	2	Command set enabled: NOP, READ BUFFER, WRITE BUFFER, Host Protected Area, look-ahead enabled/disabled, volatile write cache enabled/disabled , power management feature set, Security Mode feature set enabled/disabled, SMART feature set enabled/disabled
86	B40Dh*	2	Command set enabled: FLUSH CACHE, FLUSH CACHE EXT, LBA48, CFA feature set, DOWNLOAD MICROCODE, words 119 and 120 supported
87	4063*h	2	Command set/feature default
88	XX7Fh*	2	UDMA transfer mode enabled and supported
89	00XXh*	2	Time for Security Erase Unit
90	00XXh*	4	Time for enhanced security erase completion
91	00XXh	2	Power Management
92	XXXXh*	2	Master password revision code
93	XXXXh* 0000h	2	Hardware Reset Result not supported in PC-Card mode
94-99	0000h*	12	Reserved
100-103	XXXXh	8	Total number of sectors addressable in LBA48 Mode
104	0000h	2	Reserved
105	0001h	2	Number of sectors per Data Set Management command
106-118	0000h	26	Reserved
119-120	4008h 4008h	4	Read Log DMA Ext and Write Log DMA Ext commands supported Read Log DMA Ext and Write Log DMA Ext commands enabled
121-127	0000h	14	Reserved
128	0021h*	2	Security status (may change in operation)
129	0x00h*	2	Write Protect Status. Bit 9 = permanent write protect from vendor command Bit 8 = temporary write protect from vendor command
130-155	XXXXh	52	Vendor specific
156-159	0000h	8	Reserved
160	a064h	2	CFA Power Mode: no power level 1, max 100mA
161	0000h	2	Reserved
162	0000h	2	Key Management Schemes: CPRM not supported
163	0012h*	2	CFA advanced modes: supported and enabled bits
164	ed9bh*	2	CFA advanced modes: 80ns I/O and Memory supported, I/O and Memory UDMA modes supported and selected
165-166	0000h	4	Reserved
167	6100h	2	CFA Specification 6.1 supported
168	0000h	2	Reserved
169	0000h	2	Trim bit in Data Set Management NOT supported (supported on request)
170-216	0000h	94	Reserved
217	0001h	2	Nominal media rotation rate: Solid State Device
218-254	0000h	74	Reserved
255	XXA5h	2	Integrity Word

* Standard values for full functionality are listed. Values depend on device configuration.

9. S.M.A.R.T. Functionality

The C-500 CompactFlash Card fully supports the ATA Specification for Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.). For details about the S.M.A.R.T. subcommands and attributes, see the *S.M.A.R.T. Attribute Technical Reference Guide*.

9.1 S.M.A.R.T. Subcommands

The following table lists the supported S.M.A.R.T. subcommands and the Features register values.

Table 16: S.M.A.R.T. Features Supported

Features	Operation
D0h	S.M.A.R.T. Read Data
D1h	S.M.A.R.T. Read Attribute Thresholds
D2h	S.M.A.R.T. Enable/Disable Autosave
D3h	S.M.A.R.T. Save Attribute Values
D4h	S.M.A.R.T. Execute Off-Line Immediate
D5h	S.M.A.R.T. Read Log
D6h	S.M.A.R.T. Write Log
D7h	S.M.A.R.T. Write Attribute Thresholds
D8h	S.M.A.R.T. Enable Operations
D9h	S.M.A.R.T. Disable Operations
DAh	S.M.A.R.T. Return Status

The device aborts any S.M.A.R.T. subcommands with Features register values not listed in the above table.

9.2 S.M.A.R.T. Read Data

When the drive receives the S.M.A.R.T. Read Data subcommand, it returns one sector (512 bytes) of data. See the following table for the data structure of this sector.

Table 17: S.M.A.R.T. Data Structure

Byte(s)	Value	Description
0-1	0010h	S.M.A.R.T. structure version
2-361	XXh	Attribute entries 1 to 30 (see Table 19)
362	00h	Off-line data collection status (no off-line data collection started)
363	00h	Self-test execution status byte (self-test completed)
364-365	0000h	Total time, in seconds, to complete off-line data collection
366	00h	Vendor specific
367	00h	Off-line data collection capability (no off-line data collection)
368-369	0003h	S.M.A.R.T. capabilities
370	00h	No Error logging capability
371	00h	Vendor specific
372	00h	Short self-test routine recommended polling time, in minutes
373	00h	Extended self-test routine recommended polling time, in minutes
374-385	00h	Reserved
386-387	0004h	SMART Version
388-510	XXh	Vendor specific
511	XXh	Data structure checksum

9.3 S.M.A.R.T. Attributes

The C-500 drives support the S.M.A.R.T. attributes listed in the following table.

Table 18: S.M.A.R.T. Attributes

ID dec	ID hex	Value	Worst	Threshold	Attribute	Description	RAW values Offset 5-10
196	C4h	X%	100	25	Spare Block Count	Number of total available NAND spare blocks	Initial and current number of spare blocks
213	D5h	X%	100	25	Spare Block Count worst channel	Spare block count for the NAND with the lowest number of remaining spare blocks	Initial and current number of spare blocks of the channel with the lowest current number of spare blocks
229	E5h	X%	X%	1	Total Erase Count	Estimated number of total NAND block erases	Estimated number of total NAND block erases
203	CBh	100	100	0	Total ECC Errors	All recorded ECC errors	Total number of ECC errors (correctable and uncorrectable)
204	CCh	100	100	0	Correctable ECC Errors	Total recorded ECC errors that were corrected during the life of the drive	Total number of correctable ECC errors
199	C7h	100	100	0	UDMA CRC Errors	Dummy attribute, included for legacy reasons	This value is fixed at 0.
232	E8h	100	100	0	Total Number of Reads	Total number of NAND READ commands	Total number of NAND READ commands
12	0Ch	100	100	0	Power-On Count	Count of power-on events	Number of power cycles
241	F1h	100	100	0	Total LBAs Written	Total amount of data written to the drive	Total number of LBAs written to the disk, divided by 65536
242	F2h	100	100	0	Total LBAs Read	Total amount of data read from the drive	Total number of LBAs read from the disk, divided by 65536
214	D6h	100	100	0	Management Block status	Total number of times the management block has been updated	Management block write count
194	C2h	X°C	Max °C	0	Temperature Status	Device temperature in Celsius (°C)	Current/Min/Max temperature

9.4 S.M.A.R.T. Attribute Entry Structure

Each attribute entry consists of 12 bytes. See the following table for the data structure of each entry.

Table 19: Attribute Entry

Byte(s)	Value	Description
0	XXh	Attribute ID (see Table 18)
1-2	000Xh	Flags (little-endian) X=2 Advisory type, X=3 Prefail type
3	XXh	Attribute value as a percentage (64h=100%)
4	XXh	Worst value as a percentage (64h=100%)
5-10	XXXXh	Raw value (little-endian)
11	00h	Reserved

10. CIS information (typical)

In PC-Card mode the C-500 card returns the Card information structure (CIS) with detailed information about the properties.

```
0000: Code 01, link 03
D9 01 FF
```

- Device Info Tuple
- Link is 3 bytes
- I/O Device, No WPS, speed=250ns if no wait
- (One) 2 Kilobytes of address space
- End of CISTPL_DEVICE

```
000A: Code 1C, link 04
02 D9 01 FF
```

- Other Conditions Info Tuple
- Link is 4 bytes
- Conditions: 3V operation is allowed, and WAIT is used
- I/O Device, No WPS, speed = 250 ns if no wait
- (One) 2 Kilobytes of address space
- End of CISTPL_DEVICE

```
0016: Code 18, link 02
DF 01
```

- JEDEC programming info Tuple
- Link is 2 bytes
- Device manufacturer ID
- Manufacturer specific info

```
001E: Code 20, link 04
00 00 00 00
```

- Manufacturer ID Tuple
- Link length is 4 bytes
- PC Card manufacturer code
- Manufacturer specific info

```
002A: Code 21, link 02
04 01
```

- Function ID Tuple
- Link length is 2 bytes
- Fixed disk drive
- R=0: no expansion ROM; P=1: configure at POST

```
0032: Code 22, link 02
01 01
```

- Function Extension Tuple
- Link length is 2 bytes
- Disk interface information
- PC card ATA interface

003A: Code 22, link 03
02 04 07

- Function Extension Tuple
- Link length is 3 bytes
- PC card ATA basic features
- D=0: single drive on card; U=0: no unique serial number; S=1: silicon device; V=0: no VPP required
- I=0: twin IOIS16# unspecified; E=0: index bit not emulated; N=0: I/O includes 0x3F7; P=7: sleep, standby, idle supported

0044: Code 1A, link 05
01 07 00 02 07

- Configuration Tuple
- Link length is 5 bytes
- RFS: reserved; RMS: 1 byte register mask; RAS: 2 bytes base address
- Last configuration entry is 07H
- Configuration registers are located at 0200h
- Configuration registers 0 to 2 are present

0052: Code 1B, link 0B
C0 C0 A1 27 55 4D 5D 75 08 00 20

- Configuration Tuple
- Link length is 11 bytes
- Memory mapped configuration, index=0; I=1: Interface byte follows; D=1: Default entry
- W=1: wait required; R=1: ready/busy active; P=0: WP not used; B=0: BVD1, BVD2 not used; Type=0: Memory interface
- M=1: misc info present; MS=1: 2 byte memory length; IR=0: no interrupt is used; IO=0: no I/O space is used; T=0: no timing info specified; Power=1: VCC info, no VPP
- DI: no power-down current; PI=1: peak current info; AI: no average current info; SI: no static current info; HV=1: max voltage info; LV=1: min voltage info; NV=1: nominal voltage info
- Nominal voltage 5.0V
- Minimum voltage 4.5V
- Maximum voltage 5.5V
- Peak current 80 mA
- Length of memory space is 2 Kbyte
- X=0: no more misc fields; P=1: power-down supported; RO=0: read/write media; A=0: audio not supported; T=0: no twins supported

006C: Code 1B, link 06
00 01 21 B5 1E 4D

- Configuration Tuple
- Link length is 6 bytes
- Memory mapped configuration, index=0
- Power=1: VCC info, no VPP
- PI=1: peak current info; NV=1: nominal voltage info
- X=1: extension byte present
- Nominal voltage 3.30V
- Peak current 45 mA

007C: Code 1B, link 0D
C1 41 99 27 55 4D 5D 75 64 F0 FF FF 20

- Configuration Tuple
- Link length is 11 bytes
- Memory mapped configuration, index=0; I=1: Interface byte follows; D=1: Default entry
- W=1: wait required; R=1: ready/busy active; P=0: WP not used; B=0: BVD1, BVD2 not used; Type=0: Memory interface
- M=1: misc info present; MS=1: 2 byte memory length; IR=0: no interrupt is used; IO=0: no I/O space is used; T=0: no timing info specified; Power=1: VCC info, no VPP
- DI: no power-down current; PI=1: peak current info; AI: no average current info; SI: no static current info; HV=1: max voltage info; LV=1: min voltage info; NV=1: nominal voltage info
- Nominal voltage 5.0V
- Minimum voltage 4.5V
- Maximum voltage 5.5V
- Peak current 80 mA
- Length of memory space is 2 Kbyte
- X=0: no more misc fields; P=1: power-down supported; RO=0: read/write media; A=0: audio not supported; T=0: no twins supported

009A: Code 1B, link 06
01 01 21 B5 1E 4D

- Configuration Tuple
- Link length is 6 bytes
- I/O mapped, index=1
- Power=1: VCC info, no VPP
- PI=1: peak current info; NV=1: nominal voltage info
- X=1: extension byte present
- Nominal voltage 3.30V
- Peak current 45 mA

00AA: Code 1B, link 12
C2 41 99 27 55 4D 5D 75 EA 61 F0 01 07 F6 03 01 EE 20

- Configuration Tuple
- Link length is 18 bytes
- I/O mapped, index=2; I=1: Interface byte follows; D=1: Default entry
- W=0: wait not required; R=1: ready/busy active; P=0: WP not used; B=0: BVD1, BVD2 not used; Type=1: I/O interface
- M=1: misc info present; MS=0: no memory space info; IR=1: interrupt is used; IO=1: I/O space is used; T=0: no timing info specified; Power=1: VCC info, no VPP
- DI: no power-down current; PI=1: peak current info; AI: no average current info; SI: no static; current info; HV=1: max voltage info; LV=1: min voltage info; NV=1: nominal voltage info
- Nominal voltage 5.0V
- Minimum voltage 4.5V
- Maximum voltage 5.5V
- Peak current 80 mA
- R=1: range follows; S=1: support 16 bit hosts; E=1: support 8 bit hosts; IO=10: 10 lines decoded
- LS=1: 1 byte length; AS=2: 2 byte address; NR=1: 2 address ranges
- Address range 1 0x1F0 to 0x1F7
- Address range 2 0x3F6 to 0x3F7
- S=1: interrupt sharing logic; P=1: pulse mode supported; L=1: level mode supported; M=0: masks V..N not present; IRQN=14: use interrupt 14
- X=0: no more misc fields; P=1: power-down supported; RO=0: read/write media; A=0: audio not supported; T=0: no twins supported

00D2: Code 1B, link 06
02 01 21 B5 1E 4D

- Configuration Tuple
- Link length is 6 bytes
- I/O mapped, index=2
- Power=1: VCC info, no VPP

- PI=1: peak current info; NV=1: nominal voltage info
- X=1: extension byte present
- Nominal voltage 3.30V
- Peak current 45 mA

00E2: Code 1B, link 12
C3 41 99 27 55 4D 5D 75 EA 61 70 01 07 76 03 01 EE 20

- Configuration Tuple
- Link length is 18 bytes
- I/O mapped, index=2; I=1: Interface byte follows; D=1: Default entry
- W=0: wait not required; R=1: ready/busy active; P=0: WP not used; B=0: BVD1, BVD2 not used; Type=1: I/O interface
- M=1: misc info present; MS=0: no memory space info; IR=1: interrupt is used; IO=1: I/O space is used; T=0: no timing info specified; Power=1: VCC info, no VPP
- DI: no power-down current; PI=1: peak current info; AI: no average current info; SI: no static; current info; HV=1: max voltage info; LV=1: min voltage info; NV=1: nominal voltage info
- Nominal voltage 5.0V
- Minimum voltage 4.5V
- Maximum voltage 5.5V
- Peak current 80 mA
- R=1: range follows; S=1: support 16 bit hosts; E=1: support 8 bit hosts; IO=10: 10 lines decoded
- LS=1: 1 byte length; AS=2: 2 byte address; NR=1: 2 address ranges
- Address range 1 0x170 to 0x177
- Address range 2 0x376 to 0x377
- S=1: interrupt sharing logic; P=1: pulse mode supported; L=1: level mode supported; M=0: masks V..N not present; IRQN=14: use interrupt 14
- X=0: no more misc fields; P=1: power-down supported; RO=0: read/write media; A=0: audio not supported; T=0: no twins supported

010A: Code 1B, link 06
03 01 21 B5 1E 4D

- Configuration Tuple
- Link length is 6 bytes
- I/O mapped, index=3
- Power=1: VCC info, no VPP
- PI=1: peak current info; NV=1: nominal voltage info
- X=1: extension byte present
- Nominal voltage 3.30V
- Peak current 45 mA

011A: Code 14, link 00

- No link control Tuple
- Link length is 0 bytes

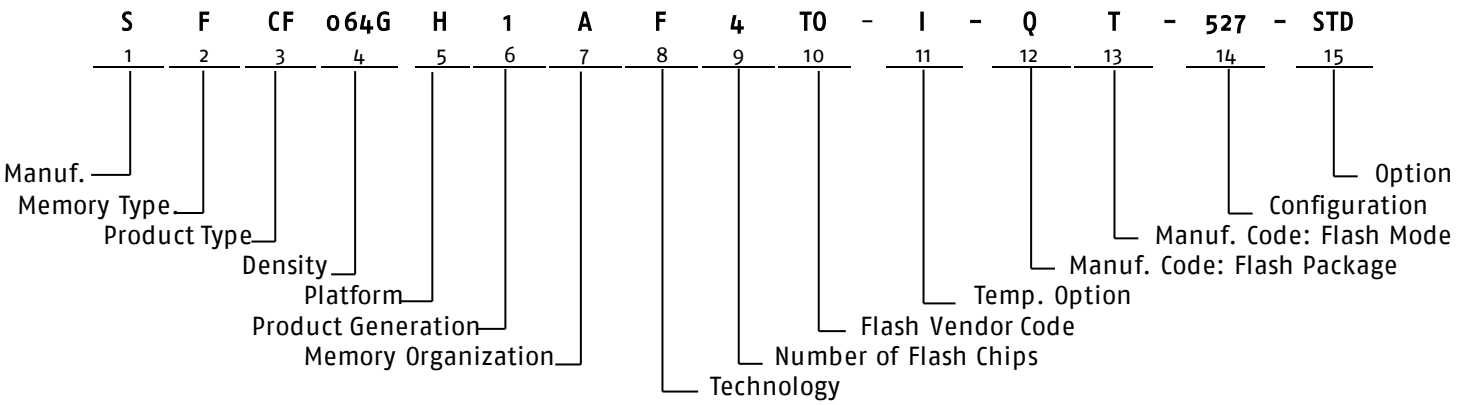
011E: Code 15, link ***14*)***
04 01 ***53 77 69 73 73 62 69 74 00 43 46 20 43 61 72 64*** 00 FF *)

- Level 1 version/product info
- Link length is 21 bytes
- PCMCIA2.0/JEIDA4.1
- PCMCIA2.0/JEIDA4.1
- Product name: "***Swissbit***" "***CF Card***" *) can vary in different configurations
- ***The length of the strings will affect the following tuple start addresses***

014A: Code FF, link FF

- End of CISTPL_VERS_1
- End of CIS

11. Part Number Decoder



11.1 Manufacturer

Swissbit code	S

11.2 Memory Type

Flash	F

11.3 Product Type

CompactFlash	CF

11.4 Density

128 MBytes	0128
256 MBytes	0256
512 MBytes	0512
1 GBytes	1024
2 GBytes	2048
4 GBytes	4096
8 GBytes	008G
16 GBytes	016G
32 GBytes	032G
64 GBytes	064G

11.5 Platform

CompactFlash	H

11.6 Product Generation

First generation	1

11.7 Memory Organization

x8	A

11.8 Technology

C-5xx Series	F

11.9 Number of Flash Chips

1 Flash	1
2 Flash	2
4 Flash	4

11.10 Flash Code

Toshiba / Kioxia	T0

11.11 Temperature Option

Industrial Temperature Range: -40 °C to 85 °C	I
Standard Temperature Range: 0 °C to 70 °C	C

11.12 Die Classification

SLC MONO (single die package)	M
SLC DDP (dual die package)	D
SLC QDP (quad die package)	Q
SLC ODP (octal die package)	N

11.13 Pin Mode

Single nCE and Single R/nB	S
Dual nCE and Dual R/nB	T
Quad nCE and Quad R/nB	U

11.14 Drive Configuration XYZ

X = Type

Removable/fix		PIO	DMA support	X
True IDE Mode	PC Card Mode			
Removable		yes	yes	1
Fix		yes	yes	2
Fix		yes	-	3
Removable		yes	-	4
Fix	Removable	yes	yes	5*
Fix	Removable	yes	-	6

**default*

Y = Firmware Revision

FW Revision	Y
First FW Revision	1
Second FW Revision	2

Z = Max Transfer Mode

Max PIO Mode / CIS	**Z**
PIO4 (MDMA2 if enabled)	1
PIO6 (MDMA4 if enabled)	2
UDMA4 (PIO6, MDMA4)	3
UDMA6 (MDMA2, PIO4)	6
UDMA6 (MDMA4, PIO6)	7*

**default*

11.15 Option

Swissbit/Standard	STD
Customized version	XXX

12. Marking Specification

12.1 Top View

12.2 Bottom View

12.3 Label Content

- Swissbit logo
- CF logo
- Part number (defined by the data sheet)
- Barcode as assembly lot number (Code128)
- Lot number
- CE logo
- RoHS logo
- WEEE logo
- Manufacturing date
- "Made in Germany"

13. Revision History

Table 20: Document Revision History

Date	Revision	Description	Revision Details
24-Aug-2018	0.91	Initial preliminary draft.	
31-Oct-2018	1.00	Initial release.	Doc. req. no. 2580
17-Mar-2020	1.01	Updated document template and part number decoder, added FW2 part numbers and new product pictures	Doc. req. no. 3539
01-Apr-2020	1.02	Added 128 MBytes and 256 MBytes product variants	Doc. req. no. 3571

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