MAX14775E/MAX14776E

±65V Fault Protected 500kpbs/20Mbps Half-Duplex RS-485/RS-422 Transceivers

General Description

The MAX14775E/MAX14776E fault-protected RS-485/RS-422 transceivers feature ±65V protection for overvoltage signal faults on communication bus lines, ensuring communication in harsh industrial environments. Each device contains one driver and one receiver and operates over the 3V to 5.5V supply range. The MAX14775E is optimized for high-speed data rates up to 20Mbps. The MAX14776E features slew-rate limited outputs for data rates up to 500kbps.

These transceivers are optimized for robust communication in noisy environments. A large 200mV (typ) hysteresis on receiver inputs ensure for high noise rejection and a fail-safe feature guarantees a logic-high on the receiver output when the inputs are open or shorted. Driver outputs are protected against short-circuit conditions.

The MAX14775E/MAX14776E receivers feature a 1/3-unit load input impedance, allowing up to 100 transceivers on a bus.

The MAX14775E/MAX14776E are available in 8-pin SOIC and 8-pin TDFN-EP packages and operate over the -40°C to +125°C temperature range.

Benefits and Features

- Integrated Protection Ensures for Robust Communication
  - ±65V Fault Protection Range on Driver Outputs/Receiver Inputs
  - ±25V Common Mode Range on the Receiver Inputs
  - Large Receiver Hysteresis Increases Noise Tolerance
  - Hot-Swap Protection
  - Thermal Shutdown
- High-Performance Transceiver Enables Flexible Designs
  - Compliant with RS-485 EIA/TIA-485 Standard
  - 20Mbps (MAX14775E)/500kbps (MAX14776E) Maximum Data Rate
  - 3V to 5.5V Supply Range
  - Up to 100 Devices on the Bus

Applications

- Industrial Field Bus Networks
- Motion Controllers
- HVAC

***Ordering Information* appears at end of data sheet.**

Selector Guide

PART NUMBER	MAX DATA RATE	PIN-PACKAGE
MAX14775EASA+	20Mbps	8 SOIC
MAX14775EATA+	20Mbps	8 TDFN-EP
MAX14776EASA+	500kbps	8 SOIC
MAX14776EATA+	500kbps	8TDFN-EP

19-8614; Rev 0; 9/16

Absolute Maximum Ratings

(All voltages referenced to GND)
V_{CC} ....-0.3V to +6V
RO ....-0.3V to (V_{CC} + 0.3V)
DE, DI, $\overline{RE}$..-0.3V to +6V
A, B (I_{MAX} = ±1mA) ....-70V to +70V
Short-Circuit Duration (RO, A, B) ....Continuous

Continuous Power Dissipation (T_A = +70°C)
8-pin SOIC (derate 7.60mW/°C above +70°C) 606.1mW
8-pin TDFN (derate 24.4mW/°C above +70°C) 1951.2mW
Operating Temperature Range........................ -40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

SOIC
Junction-to-Ambient Thermal Resistance (θ_{JA}).......132°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....38°C/W

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).........41°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....8°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{CC} = 3.0V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER						
Supply Voltage	V_{CC}		3.0		5.5	V
Supply Current	I_{CC}	DE = high, $\overline{RE}$ = low, no load, no switching		3	5.3	mA
Shutdown Supply Current	I_{SH}	DE = high, $\overline{RE}$ = low		4		µA
Shutdown Short-Circuit Supply Current	I_{SHDN_SHRT}	A or B shorted to ±65V, DE = high, $\overline{RE}$ = low		240		µA
DRIVER						
Differential Driver Output	$\|V_{OD}\|$	R_L = 54Ω, Figure 1a	1.5			V
		R_L = 100Ω, Figure 1a	2.0			
Change in Magnitude of Differential Driver Output Voltage	ΔV_{OD}	R_L = 100Ω or 54Ω, Figure 1a (Note 3)	-0.2		+0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R_L = 100Ω or 54Ω, Figure 1a		V_{CC}/ 2	3	V
Change in Magnitude of Common-Mode Voltage	ΔV_{OC}	R_L = 100Ω or 54Ω, Figure 1a (Note 3)	-0.2		+0.2	V
Single-Ended Driver Output Voltage High	V_{OH}	A and B outputs, output is high, I_{SOURCE} = 3mA	V_{CC}-0.2			V
Single-Ended Driver Output Voltage Low	V_{OL}	A and B outputs, output is low, I_{SINK} = 3mA			0.2	V
Driver Short-Circuit Output Current	I_{OSD1}	-65V ≤ V_A or V_B < 0V or V_{CC} < V_A or V_B ≤ +65V (Note 4)			200	mA

DC Electrical Characteristics (continued)

(V_{CC} = 3.0V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Average Driver Short-Circuit Output Current	I_{OSD2}	0V ≤ V_A or V_B ≤ V_{CC}				250	mA
RECEIVER							
Input Current (A, B)	I_A, I_B	DE = low, 0V ≤ V_{CC} ≤ 5.5V	V_{CM} = +12V			+280	µA
			V_{CM} = -7V	-200			
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ +12V		38			kΩ
Common Mode Voltage Range	V_{CM}			-25		+25	V
Receiver Differential Threshold Voltage Rising	V_{THH}	-25V ≤ V_{CM} ≤ +25V		+40		+200	mV
Receiver Differential Threshold Voltage Falling	V_{THL}	-25V ≤ V_{CM} ≤ +25V		-200		-40	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V, time from last transition < t_{D_FS}			250		mV
Differential Input Fail-safe Threshold	V_{TH_FSH}	25V ≤ V_{CM} ≤ +25V, time from last transition > t_{D_FS}		-40		+40	mV
Differential Input Capacitance	$C_{A,B}$	Measured between A and B, f = 1MHz			50		pF
LOGIC OUTPUTS (RO)							
RO Output Logic High Voltage	V_{OH}	I_{SOURCE} = 3mA, (V_A - V_B) ≥ +200mV		V_{CC}-0.4			V
RO Output Logic Low Voltage	V_{OL}	I_{SINK} = 3mA, (V_A - V_B) < +200mV				0.4	V
RO Leakage Current	I_{OZR}	$\overline{RE}$ = high, 0V ≤ V_{RO} ≤ V_{CC}		-1		+1	µA
RO Short-Circuit Current	I_{OSR}	0V ≤ V_{RO} ≤ V_{CC}			70		mA
LOGIC INPUTS (DE, DI, $\overline{RE}$)							
Input Logic High Voltage	V_{IH}			0.67 x V_{CC}			V
Input Logic Low Voltage	V_{IL}					0.33 x V_{CC}	V
Input Hysteresis	V_{HYS}				100		mV
Input Leakage Current	I_{IN}			-1		+1	µA
Input Impedance on First Transition	R_{IN_FT}	DE, $\overline{RE}$		1		10	kΩ
PROTECTION							
Thermal-Shutdown Threshold	T_{SHDN}	Temperature rising			+162		°C
Thermal-Shutdown Hysteresis	T_{HYST}				12		°C
ESD Protection (A, B Pins to GND)		Human Body Model			±8		kV
		IEC 61000-4-2- Contact Discharge			±5		
ESD Protection (All Other Pins)		Human Body Model			±2		kV
Fault Protection Range (A, B Pins to GND)				-65		+65	V

Switching Electrical Characteristics (MAX14775E)

(V_{CC} = 3.0V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
Driver Propagation Delay	t_{DPLH}, t_{DPHL}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3			40	ns
Differential Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3 (Note 7)			9	ns
Driver Differential Output Rise or Fall Time	t_{LH}, t_{HL}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3 (Note 7)		8	15	ns
Maximum Data Rate	DR_{MAX}		20			Mbps
Driver Enable to Output High	t_{DZH}	R_L = 110Ω, C_L = 50pF, Figure 4			90	ns
Driver Enable to Output Low	t_{DZL}	R_L = 110Ω, C_L = 50pF, Figure 5			90	ns
Driver Enable Time	t_D	-20V ≤V_{CM} ≤+25V, 4.5V ≤V_{CC} ≤5.5V, Figure 1a			1000	ns
Driver Disable Time From Low	t_{DLZ}	R_L = 110Ω, C_L = 50pF, Figure 5			50	ns
Driver Disable Time From High	t_{DHZ}	R_L = 110Ω, C_L = 50pF, Figure 4			50	ns
Driver Enable Time from Shutdown to Output High	$t_{DLZ(SHDN)}$	R_L = 110Ω, C_L = 50pF, Figure 4 (Note 5)			170	µs
Driver Enable Time from Shutdown to Output Low	$t_{DHZ(SHDN)}$	R_L = 110Ω, C_L = 50pF, Figure 4 (Note 5)			170	µs
Time to Shutdown	t_{SHDN}	(Note 5)	50		800	ns
RECEIVER (Note 6)						
Receiver Propagation Delay	t_{RPLH}, t_{RPHL}	C_L = 15pF, Figure 6 and Figure 7			50	ns
Receiver Output Skew	t_{RSKEW}	C_L = 15pF, Figure 6 and Figure 7 (Note 7)			5	ns
Receiver Enable to Output High	t_{RZH}	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8			50	ns
Receiver Enable to Output Low	t_{RZL}	R_L = 1kΩ, C_L = 15pF, S1 closed, Figure 8			50	ns
Receiver Disable Time From Low	t_{RLZ}	R_L = 1kΩ, C_L = 15pF, S1 closed, Figure 8			50	ns
Receiver Disable Time From High	t_{RHZ}	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8			50	ns
Receiver Enable from Shutdown to Output Low	$t_{RLZ(SHDN)}$	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8 (Note 5)			170	µs
Receiver Enable from Shutdown to Output High	$t_{RHZ(SHDN)}$	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8 (Note 5)			170	µs
Time to Shutdown	t_{SHDN}	(Note 5)	50		800	ns
Delay to Fail-Safe Operation	t_{D_FS}			10		µs

Switching Electrical Characteristics (MAX14776E)

(V_{CC} = 3.0V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
Driver Propagation Delay	t_{DPLH}, t_{DPHL}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3	100		1000	ns
Differential Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3 (Note 7)			140	ns
Driver Differential Output Rise or Fall Time	t_{LH}, t_{HL}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3; 3V ≤ V_{CC} ≤ 3.6V	105		600	ns
		R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3; 4.5V ≤ V_{CC} ≤ 5.5V	105		600	ns
Maximum Data Rate	DR_{MAX}		500			kbps
Driver Enable to Output High	t_{DZH}	R_L = 110Ω, C_L = 50pF, Figure 4			2500	ns
Driver Enable to Output Low	t_{DZL}	R_L = 110Ω, C_L = 50pF, Figure 5			2500	ns
Driver Enable Time	t_D	-20V ≤ V_{CM} ≤ +25V, 4.5V ≤ V_{CC} ≤5.5V, Figure 1a			3500	ns
Driver Disable Time From Low	t_{DLZ}	R_L = 110Ω, C_L = 50pF, Figure 5			100	ns
Driver Disable Time From High	t_{DHZ}	R_L = 110Ω, C_L = 50pF, Figure 4			100	ns
Driver Enable Time from Shutdown to Output High	$t_{DLZ(SHDN)}$	R_L = 110Ω, C_L = 50pF, Figure 4 (Note 5)			170	µs
Driver Enable Time from Shutdown to Output Low	$t_{DHZ(SHDN)}$	R_L = 110Ω, C_L = 50pF, Figure 4 (Note 5)			170	µs
Time to Shutdown	t_{SHDN}	(Note 5)	50		800	ns
RECEIVER (Note 6)						
Receiver Propagation Delay	t_{RPLH}, t_{RPHL}	C_L = 15pF, Figure 6 and Figure 7			200	ns
Receiver Output Skew	t_{RSKEW}	C_L = 15pF, Figure 6 and Figure 7 (Note 7)			30	ns
Receiver Enable to Output High	t_{RZH}	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8			50	ns
Receiver Enable to Output Low	t_{RZL}	R_L = 1kΩ, C_L = 15pF, S1 closed, Figure 8			50	ns
Receiver Disable Time from Low	t_{RLZ}	R_L = 1kΩ, C_L = 15pF, S1 closed, Figure 8			50	ns
Receiver Disable Time from High	t_{RHZ}	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8			50	ns
Receiver Enable from Shutdown to Output High	$t_{RLZ(SHDN)}$	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8			170	µs
Receiver Enable from Shutdown to Output Low	$t_{RHZ(SHDN)}$	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8			170	µs
Time to Shutdown	t_{SHDN}	(Note 5)	50		800	ns
Delay to Fail-Safe Operation	t_{D_FS}			10		µs

Switching Electrical Characteristics (MAX14776E) (continued)

(V_{CC} = 3.0V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Note 2)

Note 2: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 3: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.
Note 4: The short-circuit current is 200mA (max) for a short period (35µs, typ). If the short circuit persists, the outputs are then set to high impedance for 300ms (typ).
Note 5: Shutdown is enabled when $\overline{RE}$ is high and DE is low. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are held in this state for at least 800ns, the device is guaranteed to have entered shutdown.
Note 6: Capacitive load includes test probe and fixture capacitance.
Note 7: Guaranteed by design. Not production tested.

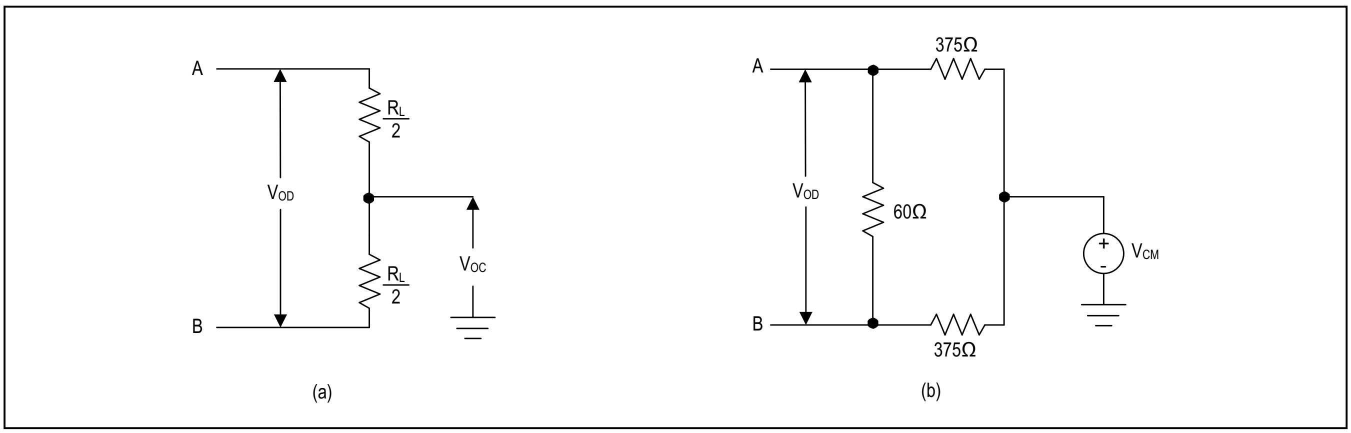


Figure 1. Driver DC Test Load

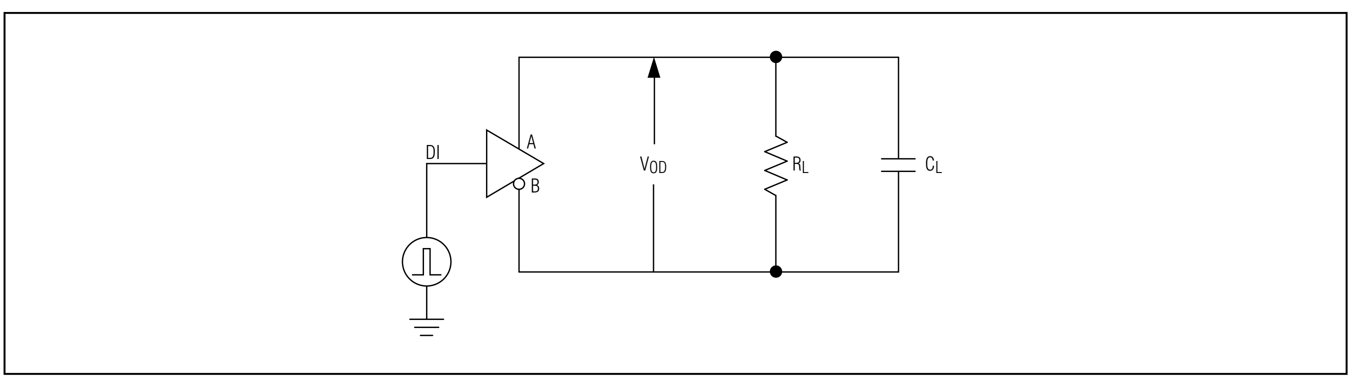


Figure 2. Driver Timing Test Circuit

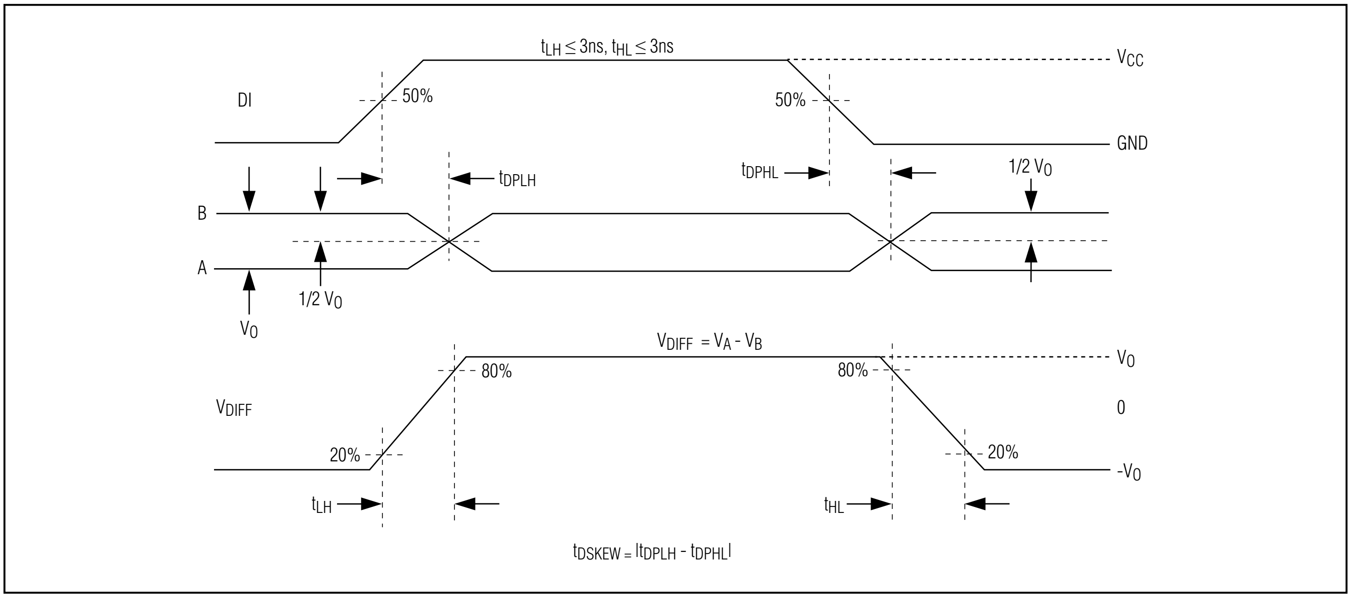


Figure 3. Driver Propagation Delays

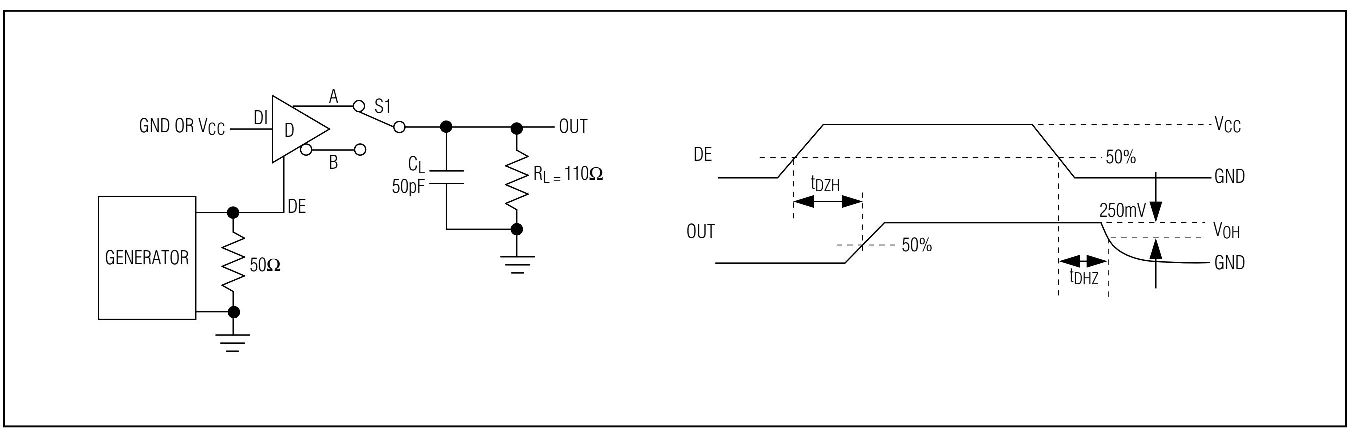


Figure 4. Driver Enable and Disable Times (t_{DHZ}, t_{DZH})

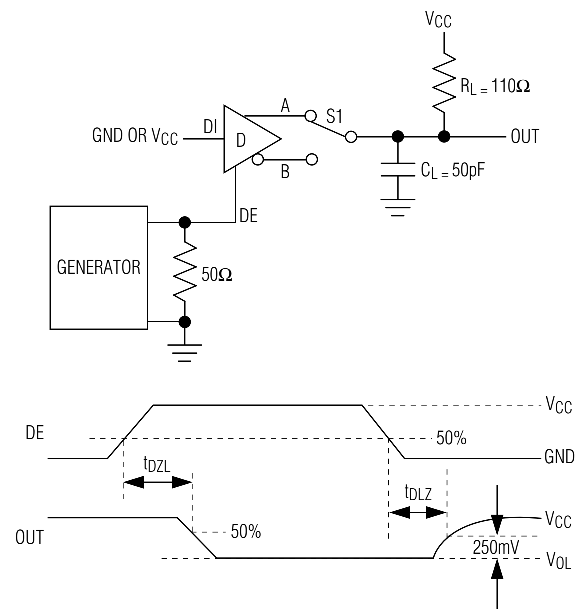


Figure 5. Driver Enable and Disable Times (t_{DZL}, t_{DLZ})

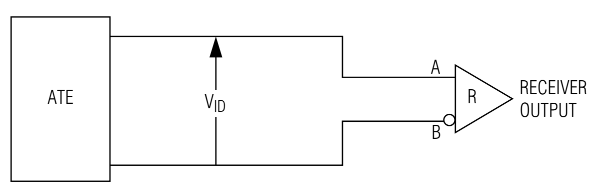


Figure 6. Receiver Propagation Delay Test Circuit

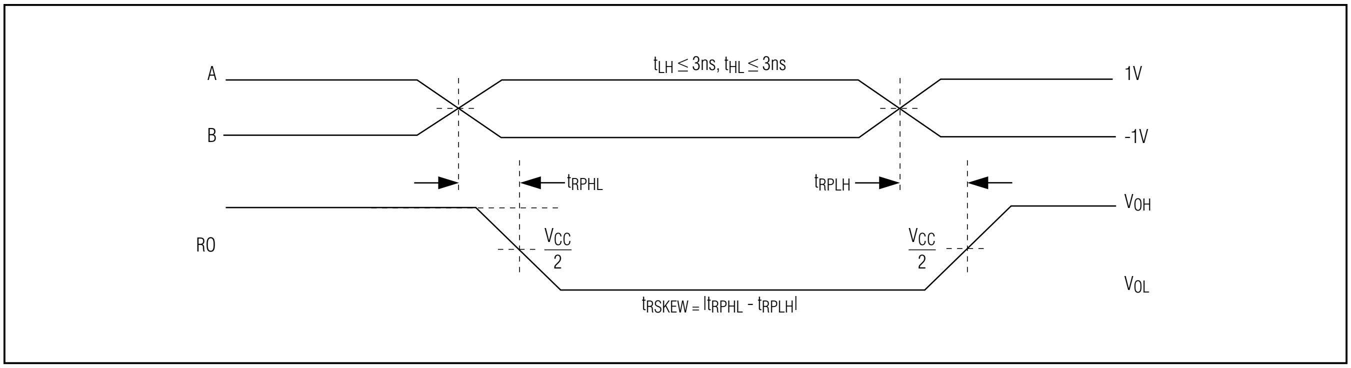


Figure 7. Receiver Propagation Delays

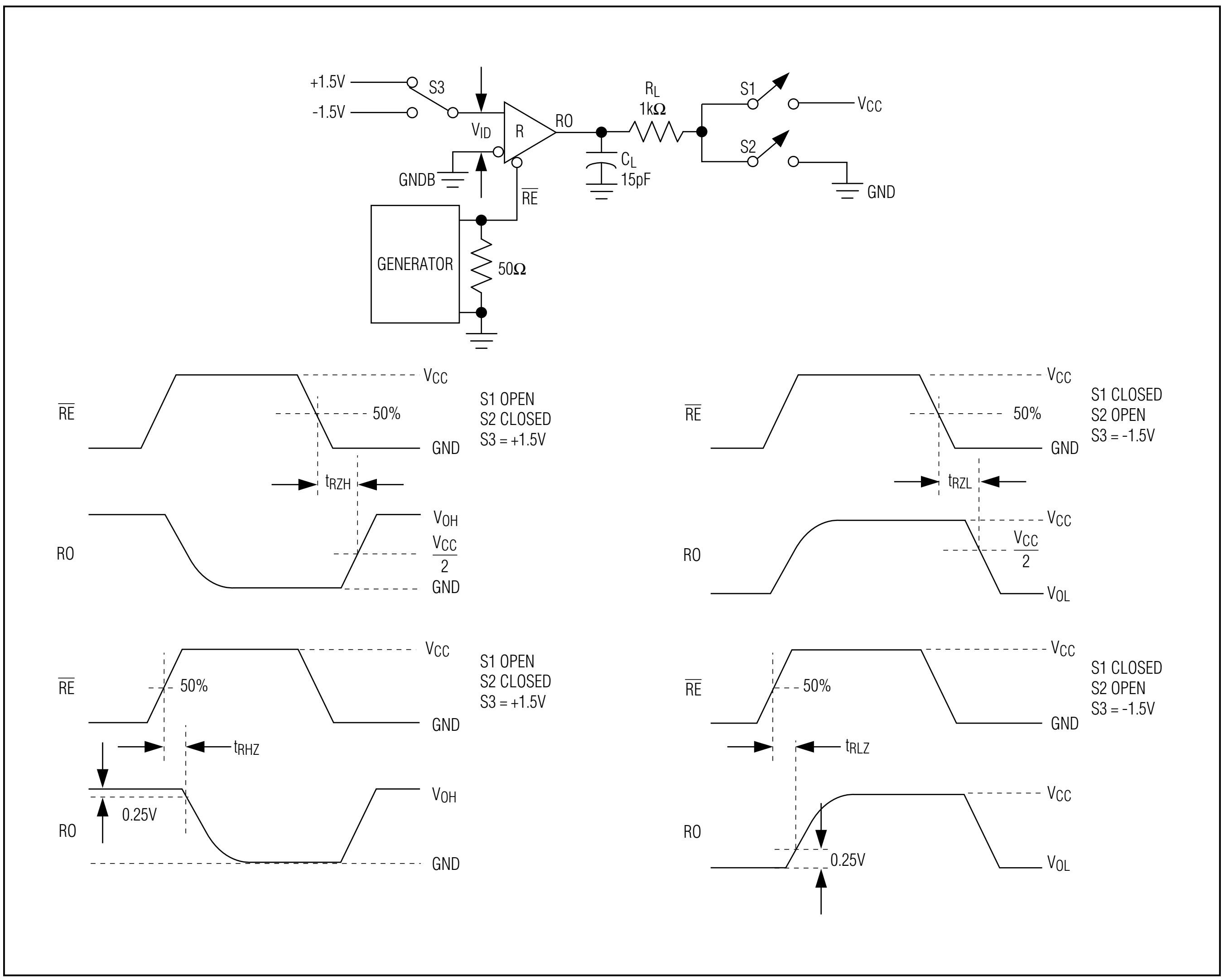
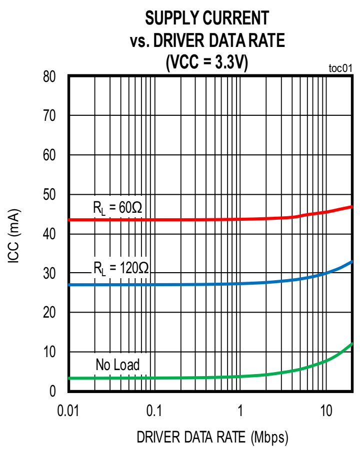
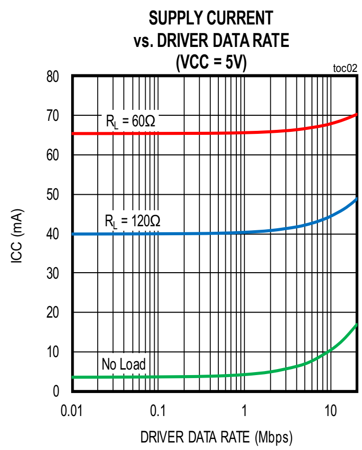


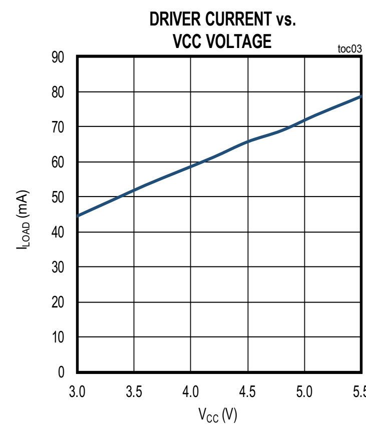
Figure 8. Receiver Enable and Disable Times

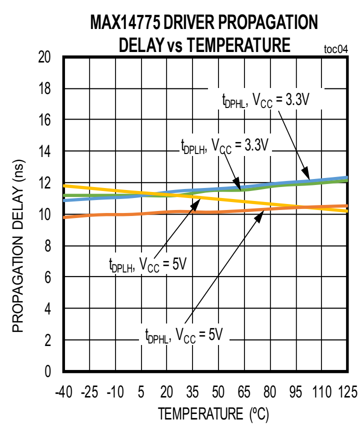
Typical Operating Characteristics

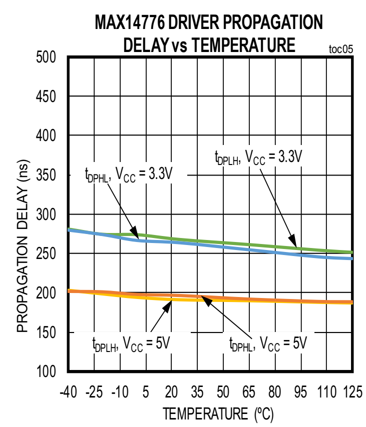
(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

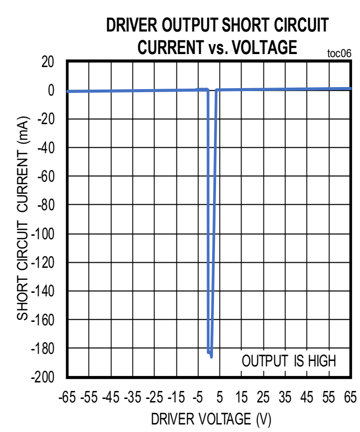


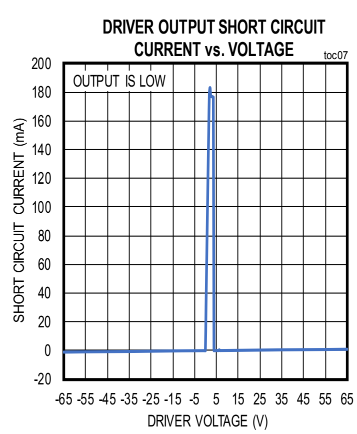


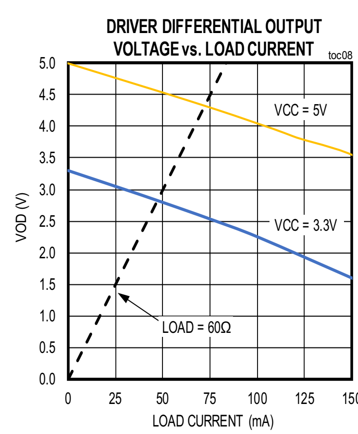


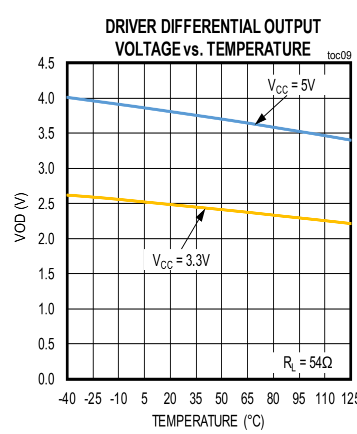






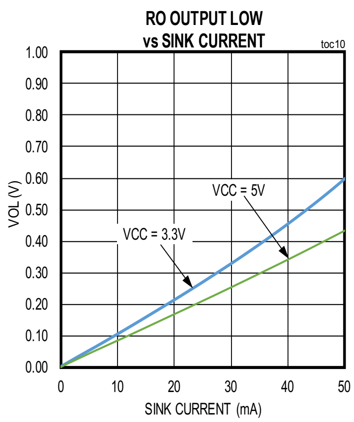


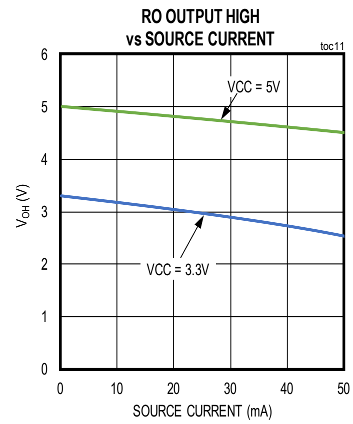


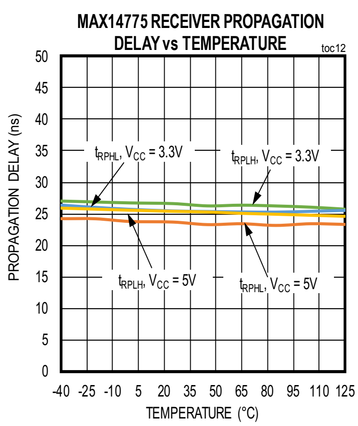


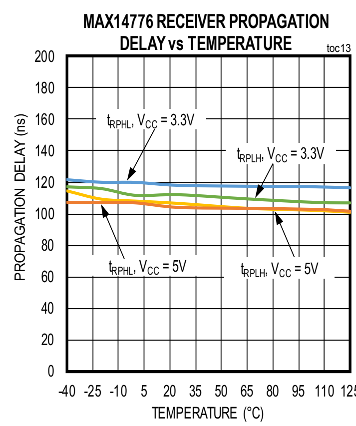
Typical Operating Characteristics (continued)

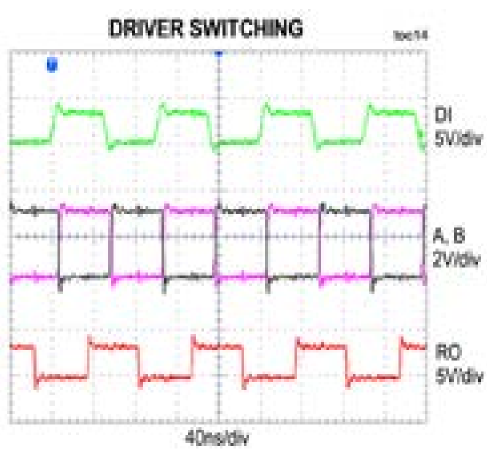
(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)



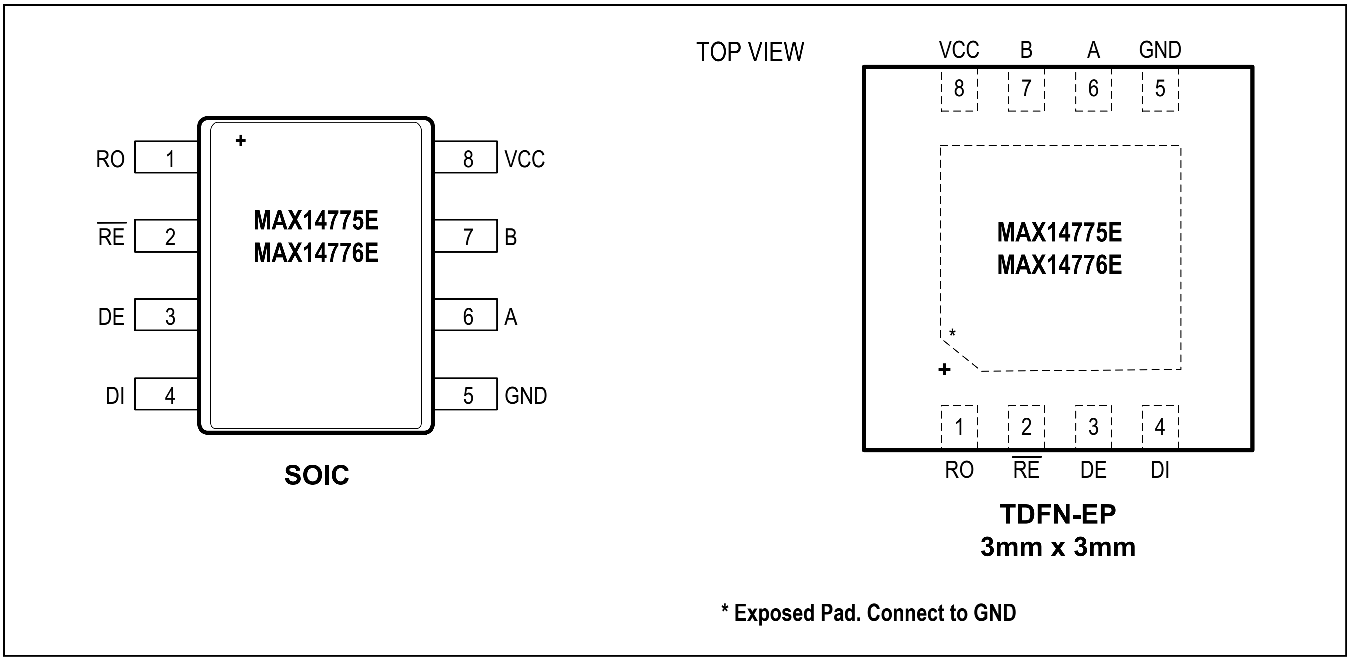








Pin Configurations



Pin Description

PIN	NAME	FUNCTION
1	RO	Receiver Data Output. See the *Function Tables* for more information.
2	$\overline{RE}$	Receiver Output Enable. Drive $\overline{RE}$ low or connect to GND to enable RO. Drive $\overline{RE}$ high to disable the receiver. RO is high impedance when $\overline{RE}$ is high. Drive $\overline{RE}$ high and DE low to force the IC into low-power shutdown mode.
3	DE	Driver Output Enable. Drive DE high to enable the driver. Drive DE low or connect to GND to disable the driver. Drive DE low and $\overline{RE}$ high to force the IC into low-power shutdown mode.
4	DI	Driver Input. With DE high, a low on DI forces the noninverting output (A) low and the inverting output (B) high. Similarly, a high on DI forces the noninverting output high and the inverting output low.
5	GND	Ground
6	A	Noninverting Driver Output/Receiver Input
7	B	Inverting Driver Output/Receiver Input
8	V_{CC}	Power Supply Input. Bypass V_{CC} to GND with a 0.1µF capacitor as close as possible to the device.
–	EP	Exposed Pad. TDFN package only. Connect EP to GND. EP is not intended as the main ground connection.

Function Tables

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	High Impedance	High Impedance
1	0	X	Shutdown. A and B are high impedance.	

***Note**: X = Don't care.*

RECEIVING				
INPUTS				OUTPUTS
$\overline{RE}$	DE	$(V_A - V_B)$	Time from Last A-B Transition	RO
0	X	≥ +200mV	Always	1
0	X	-200mV < $(V_A - V_B)$ < +200mV	< t_{D_FS}	Indeterminate. RO is latched to previous value.
0	X	-40mV < $(V_A - V_B)$ < +40mV	> t_{D_FS}	1
0	X	≤ - 200mV	Always	0
0	X	Open/Shorted	> t_{D_FS}	1
1	1	X	X	High impedance
1	0	X	X	Shutdown. RO is high impedance.

***Note**: X = Don't care.*

Detailed Description

The MAX14775E/MAX14776E half-duplex transceivers are optimized for RS-485/RS-422 applications that require up to ±65V protection from faults on communication bus lines. These devices contain one differential driver and one differential receiver. The devices feature a 1/3 unit load, allowing up to 100 transceivers on a single bus.

The MAX14775E supports data rates up to 20Mbps. The MAX14776E supports data rates up to 500kbps.

Driver

The driver accepts a single-ended, logic-level input (DI) and transfers it to a differential RS-485 level output on the A and B driver outputs.

Set the driver enable input (DE) low to disable the driver. A and B are high impedance when the driver is disabled.

Receiver

The receiver accepts a differential, RS-485 level input on the A and B inputs and transfers it to a single-ended, logic-level output (RO).

Drive the receiver enable input ($\overline{RE}$) low to enable the receiver. Driver $\overline{RE}$ high to disable the receiver. RO is high impedance when $\overline{RE}$ is high.

Low-Power Shutdown

Drive DE low and $\overline{RE}$ high for at least 800ns to put the MAX14775E/MAX14776E into low-power shutdown mode. Supply current drops to 20µA when the device is in shutdown mode.

A glitch protection feature ensures that the MAX14775E/MAX14776E will not accidentally enter shutdown mode due to logic skews between DE and $\overline{RE}$ when switching between transmit and receive modes.

±65V Fault Protection

The driver outputs/receiver inputs of transceivers connected to an industrial RS-485 network often experience faults when shorted to voltages that exceed the -7V to +12V input range specified in the EIA/TIA-485 standard. Under such circumstances, ordinary RS-485 transceivers that have a typical absolute maximum voltage rating of -8V to +12.5V require costly external protection devices which can compromise the RS-485 performance. To reduce system complexity and the need for external protection, the driver outputs/receiver inputs of the MAX14775E/MAX14776E are designed to withstand voltage faults of up to ±65V with respect to ground without damage. Protection is guaranteed regardless whether the transceiver is active, in shutdown or without power.

When a fault is detected on A or B, the affected driver output is switched into a high-impedance state. After 300ms (typ), the driver output is re-enabled for 30µs (typ). If the fault condition persists, the driver output is again disabled. If the fault has been removed, the driver outputs remain on and the transceiver operates normally.

Driving a non-terminated cable may cause the voltage seen at the driver outputs (A or B) to exceed the absolute maximum voltage rating if the DI input is switched during a ±65V fault on the A or B pins. Therefore, a termination resistor is recommended in order to maximize the overvoltage fault protection while the DI input is being switched.

If the DI input does not change state while the fault condition is present, the MAX14775E/MAX14776E will withstand up to ±65V on the RS-485 inputs, regardless of the termination status of the data cable.

Fail-Safe

The devices' receiver features symmetrical thresholds to improve the duty cycle of the received signal, ensuring that it is 50% when the received signal amplitude is small. Additionally, a high input hysteresis (250mV, typ) increases the resilience to noise on the receiver.

The MAX14775E/MAX14776E also include a fail-safe feature that ensures the receiver output (RO) is high when the receiver inputs are shorted or open, or when they are connected to a differentially terminated transmission line with all drivers disabled for longer than t_{D_FS} (10µs, typ).

Hot-Swap Functionality

Hot-Swap Inputs

Inserting circuit boards into a hot, or powered backplane may cause voltage transients on DE, $\overline{RE}$, and receiver inputs A and B that can lead to data errors. For example, upon initial circuit board insertion, the processor undergoes a power-up sequence. During this period, the high-impedance state of the output drivers makes them unable to drive the MAX14775E/MAX14776E enable inputs to a defined logic level. Meanwhile, leakage currents of up to 10µA from the high-impedance output, or capacitively coupled noise from V_{CC} or GND, could cause an input to drift to an incorrect logic state. To prevent such a condition from occurring, the MAX14775E/MAX14776E features hot-swap input circuitry on DE and $\overline{RE}$ to safeguard against unwanted driver activation during hot-swap situations. When VCC rises, an internal pulldown circuit holds DE low and $\overline{RE}$ high for at least 10µs. After the initial power-up sequence, the internal pulldown/pullup circuitry becomes transparent, resetting the hot-swap tolerable inputs.

Thermal Shutdown Protection

The MAX14775E/MAX14776E feature thermal-shutdown protection circuitry to protect the device. When the junction temperature exceeds +165°C (typ), the driver outputs are disabled and RO is high impedance. Driver and receiver outputs are re-enabled when the junction temperature falls below 150°C (typ).

Applications Information

100 Transceivers on the Bus

The MAX14775E/MAX14776E transceivers have 0.32-unit load receiver, allowing up to 100 MAX14775E/MAX14776E transceivers connected in parallel on a shared communication line. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit loads to the line.

Typical Application

The MAX14775E/MAX14776E half-duplex transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figure 9 shows a typical network applications circuit. To minimize reflections, the bus should be terminated at the receiver inputs in its characteristics impedance, and stub lengths off the main line should be kept as short as possible.

Power Considerations for the MAX14775E/MAX14776E

At high data rates, the power dissipation of an RS-485 transceiver can be high. The power dissipation of a half-duplex transceiver is determined by a number of factors, including:

- The data rate
- The time that the driver is transmitting
- The termination impedance
- The power supply voltage

Higher data rates result in higher power dissipation due to switching losses in the transceiver. Switching losses increase even more when capacitance is applied to the A and B pins. External capacitance should be kept to a minimum to help reduce power dissipation at high data rates.

Similarly, the power dissipation in a transceiver is much higher when the driver is transmitting, compared to when the transceiver is receiving. In half-duplex communication, the period of transmission relative to the idle or receiving intervals (i.e., the duty cycle) should be taken into consideration when calculating the average power dissipation.

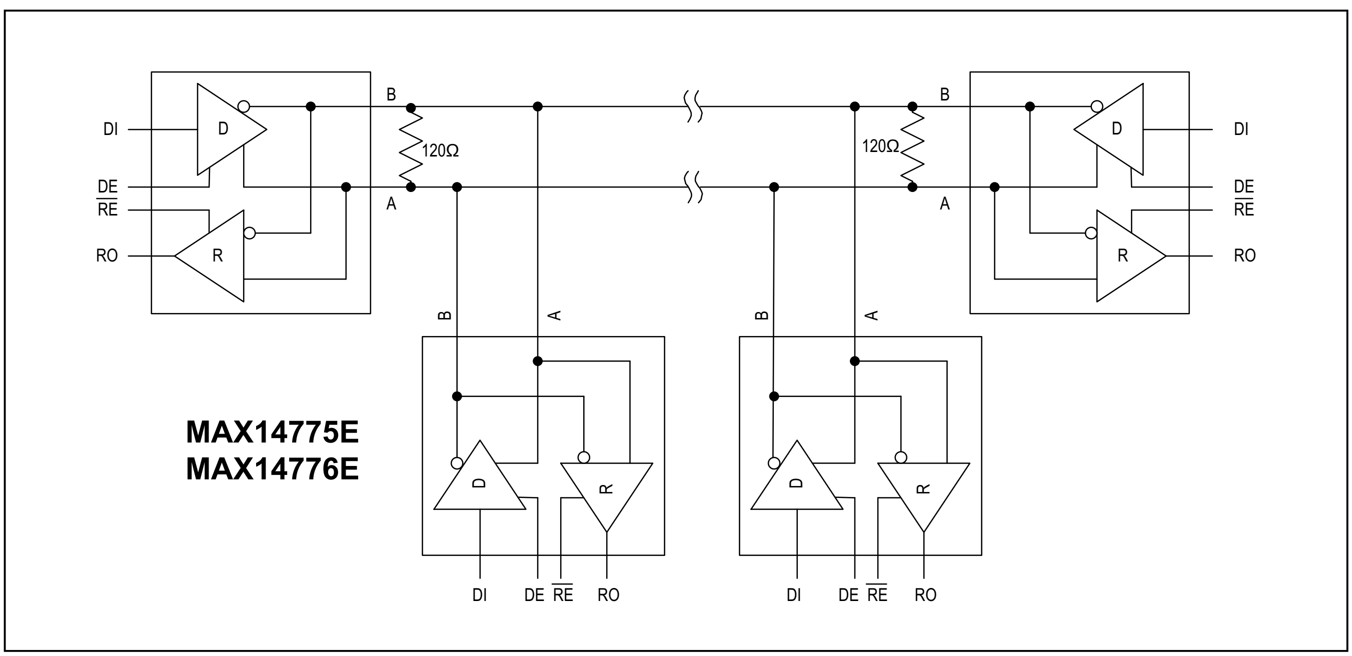


Figure 9. Typical RS-485 Network

The line termination resistance/impedance determines the driver's load current during transmission and the differential output voltage (V_{OD}) on the driver is determined by the supply voltage. A higher supply voltage results in a larger differential output voltage at the driver driving the line, which in turn results in a higher current draw from the supply (I_{CC}).

The power dissipation in the chip is calculated as the product of supply current times supply voltage, subtracting the power dissipated in the external termination resistor[2]:

$$P_{DIS} = (V_{CC} \times I_{CC}) - (V_{OD}^2/R_{LOAD})$$

Use the Typical Operation Characteristics to determine the supply current at a given supply voltage and data rate.

For example, assuming a data rate of 20Mbps with a 5V supply on a fully loaded bus (R_L = 60Ω), we can calculate that the power dissipation (at room temperature) is:

$$P_{DIS} = (5V \times 70mA) - (4.3V^2/60\Omega) = 42mW$$

Ensure that power dissipation of the transceiver is kept below the value listed in the *Absolute Maximum Ratings* section to protect the device from entering thermal shutdown or from damage. If the calculated power dissipation nears the specified limits, select a package with a lower thermal resistance which also allows for higher power dissipation.

ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharge encountered during handling and assembly. The driver outputs and receiver inputs of the MAX14775E/MAX14776E have extra protection against static electricity. The ESD structures withstand high ESD in normal operation and when powered down. After an ESD event, the devices keep working without latch-up or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the devices are characterized for protection to the cable-side ground (GNDB) to the following limits:

- ±8kV HBM
- ±5kV using the Contact Discharge method specified in the IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model (HBM)

Figure 10 shows the HBM test model and Figure 11 shows the current waveform it generates when discharged in a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged in to the test device through a 1.5kΩ resistor.

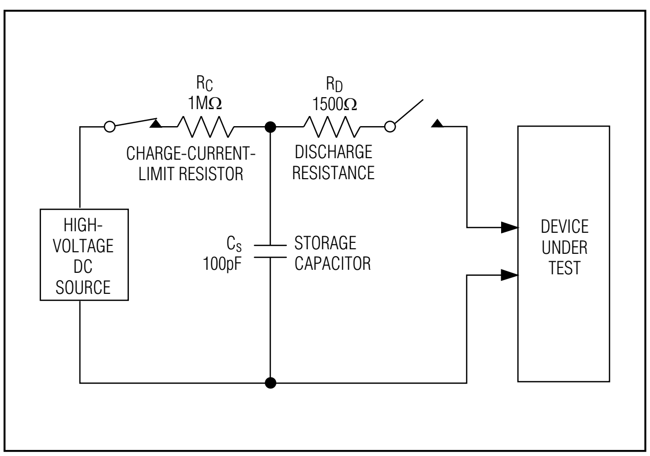


Figure 10. Human Body ESD Test Model

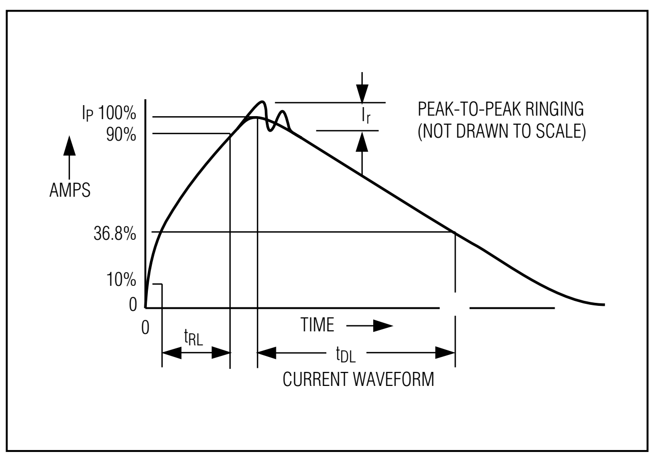


Figure 11. Human Body Current Waveform

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX14775E/MAX14776E help in designing equipment to meet IEC 61000-4-2 without the need for additional ESD protection components.

The major difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the HBM. Figure 12 shows the IEC 61000-4-2 model and Figure 13 shows the current waveform for IEC 61000-4-2 ESD Contact Discharge Test.

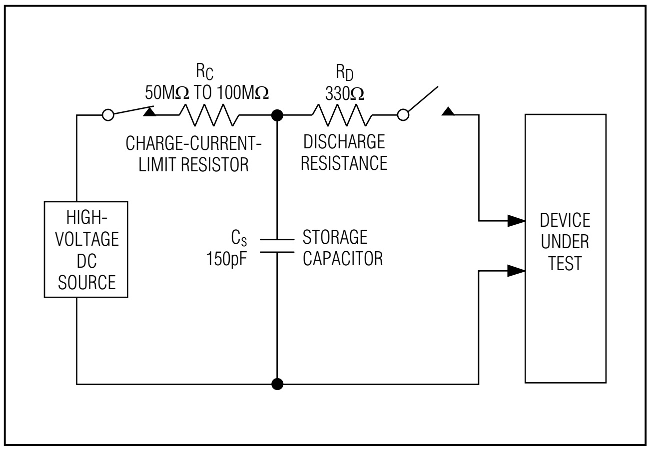


Figure 12. IEC 61000-4-2 ESD Test Model

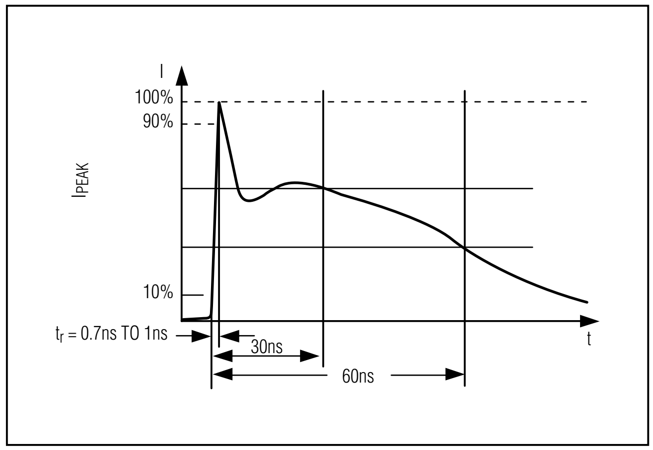
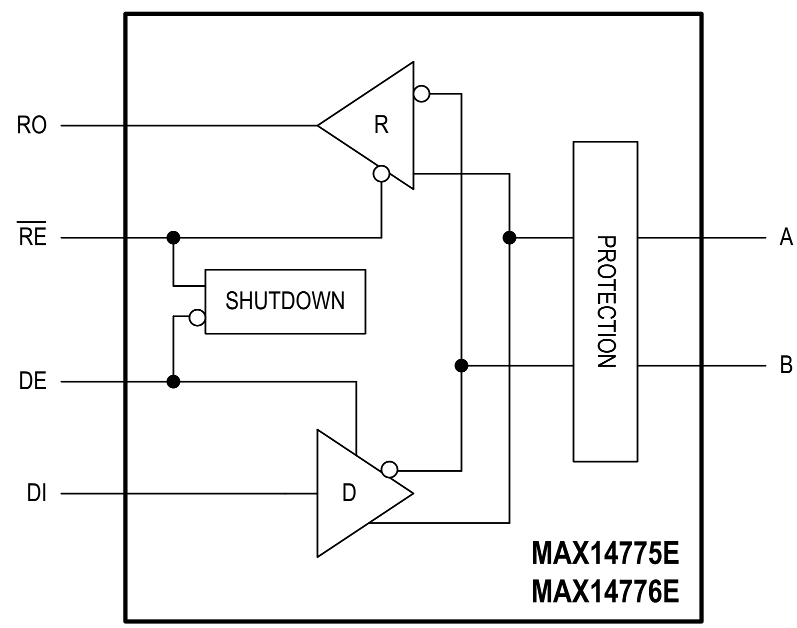


Figure 13. IEC 61000-4-2 ESD Generator Current Waveform

Functional Diagram



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14775EASA+	-40°C to +125°C	8 SOIC
MAX14775EASA+T	-40°C to +125°C	8 SOIC
MAX14775EATA+	-40°C to +125°C	8 TDFN-EP
MAX14775EATA+T	-40°C to +125°C	8 TDFN-EP
MAX14776EASA+	-40°C to +125°C	8 SOIC
MAX14776EASA+T	-40°C to +125°C	8 SOIC
MAX14776EATA+	-40°C to +125°C	8 TDFN-EP
MAX14776EATA+T	-40°C to +125°C	8 TDFN-EP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and Reel

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SOIC	S8+4	**21-0041**	**90-0096**
8 TDFN-EP	T833+2	**21-0137**	**90-0059**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/16	Initial release	—

