14-Bit, 500 MSPS LVDS, Dual Analog-to-Digital Converter

FEATURES

- Parallel LVDS (DDR) outputs
- 1.1 W total power per channel at 500 MSPS (default settings)
- SFDR = 85 dBFS at 170 MHz f_{IN} (500 MSPS)
- SNR = 68.6 dBFS at 170 MHz f_{IN} (500 MSPS)
- ENOB = 10.9 bits at 170 MHz f_{IN}
- DNL = ±0.5 LSB
- INL = ±2.5 LSB
- Noise density = −153 dBFS/Hz at 500 MSPS
- 1.25 V, 2.50 V, and 3.3 V supply operation
- No missing codes
- Internal analog-to-digital converter (ADC) voltage reference
- Flexible input range and termination impedance
  - 1.46 V p-p to 2.06 V p-p (2.06 V p-p nominal)
  - 400 Ω, 200 Ω, 100 Ω, and 50 Ω differential
- SYNC± input allows multichip synchronization
- DDR LVDS (ANSI-644 levels) outputs
- 2 GHz usable analog input full power bandwidth
- >96 dB channel isolation/crosstalk
- Amplitude detect bits for efficient AGC implementation
- Two integrated wideband digital processors per channel
  - 12-bit numerically controlled oscillator (NCO)
  - 3 cascaded half-band filters
- Differential clock inputs
  - Serial port control
  - Integer clock divide by 2, 4, or 8
- Small signal dither

APPLICATIONS

- Communications
- Diversity multiband, multimode digital receivers
  - 3G/4G, TD-SCDMA, W-CDMA, MC-GSM, LTE
- General-purpose software radios
- Ultrawideband satellite receiver
- Instrumentation (spectrum analyzers, network analyzers, integrated RF test solutions)
- Radar
- Digital oscilloscopes
- High speed data acquisition systems
- DOCSIS CMTS upstream receiver paths
- HFC digital reverse path receivers

FUNCTIONAL BLOCK DIAGRAM

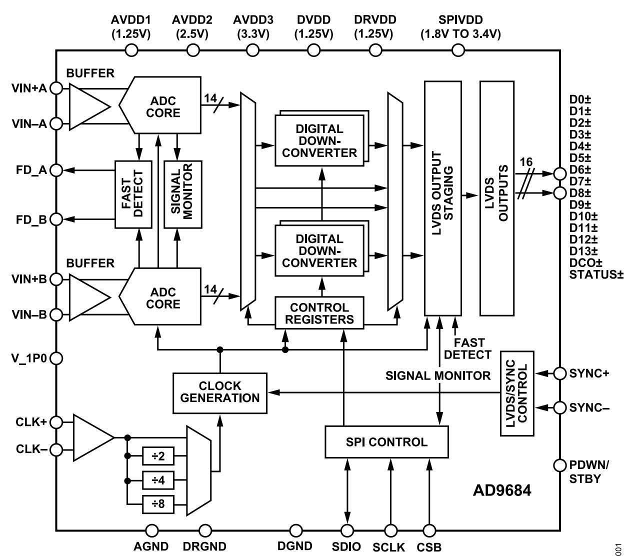

Figure 1.

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REVISION HISTORY

6/2023—Rev. 0 to Rev. A

Change to Note 2, Table 4 ... 7
Change to Figure 5 Caption ... 9
Change to Figure 7 Caption ... 10
Moved Table 9 ... 24
Added Dither Section ... 25
Changes to Table 16 ... 39
Changes to Table 26 ... 49
Changes to Table 29 ... 52
Changes to Ordering Guide ... 63

4/2015—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9684 is a dual, 14-bit, 500 MSPS ADC. The device has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed for sampling wide bandwidth analog signals. The AD9684 is optimized for wide input bandwidth, a high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth buffered inputs, supporting a variety of user selectable input ranges. An integrated voltage reference eases design considerations. Each ADC data output is internally connected to an optional decimate by 2 block.

The analog input and clock signals are differential inputs. Each ADC data output is internally connected to two digital downconverters (DDCs). Each DDC consists of four cascaded signal processing stages: a 12-bit frequency translator (NCO), and three half-band decimation filters supporting a divide by factor of two, four, and eight.

The AD9684 has several functions that simplify the automatic gain control (AGC) function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly reduce the system gain to avoid an overrange condition at the ADC input. In addition to the fast detect outputs, the AD9684 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal that the ADC digitized.

The dual ADC output data is routed directly to the one external, 14-bit LVDS output port, supporting double data rate (DDR) formatting. An external data clock and status bit are offered for data capture flexibility.

The LVDS outputs have several configurations, depending on the acceptable rate of the receiving logic device and the sampling rate of the ADC. Multiple device synchronization is supported through the SYNC± input pins.

The AD9684 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 1.8 V to 3.4 V capable 3-wire serial port interface (SPI).

The AD9684 is available in a Pb-free, 196-ball ball grid array (BGA) and is specified over the −40°C to +85°C industrial temperature range. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Wide full power bandwidth supports intermediate frequency (IF) sampling of signals up to 2 GHz.
2. Buffered inputs with programmable input termination ease filter design and implementation.
3. Four integrated wideband decimation filters and NCO blocks supporting multiband receivers.
4. Flexible SPI controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection and signal monitoring.
6. SYNC± input allows synchronization of multiple devices.
7. 12 mm × 12 mm, 196-ball BGA_ED.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (500 MSPS), 1.7 V p-p full-scale differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	Full	14			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−0.3	0	+0.3	% FSR
Offset Matching	Full		0	+0.3	% FSR
Gain Error	Full	−6.5	0	+6.5	% FSR
Gain Matching	Full		0	+5.0	% FSR
Differential Nonlinearity (DNL)	Full	−0.6	±0.5	+0.7	LSB
Integral Nonlinearity (INL)	Full	−4.5	±2.5	+5.0	LSB
TEMPERATURE DRIFT					
Offset Error	25°C		±3		ppm/°C
Gain Error	25°C		−39		ppm/°C
INTERNAL VOLTAGE REFERENCE	Full		1.0		V
INPUT-REFERRED NOISE					
V_{REF} = 1.0 V	25°C		2.63		LSB rms
ANALOG INPUTS					
Differential Input Voltage Range (Programmable)	Full	1.46	2.06	2.06	V p-p
Common-Mode Voltage (V_{CM})	25°C		2.05		V
Differential Input Capacitance[1]	25°C		1.5		pF
Analog Input Full Power Bandwidth	25°C		2		GHz
POWER SUPPLY					
AVDD1	Full	1.22	1.25	1.28	V
AVDD2	Full	2.44	2.50	2.56	V
AVDD3	Full	3.2	3.3	3.4	V
DVDD	Full	1.22	1.25	1.28	V
DRVDD	Full	1.22	1.25	1.28	V
SPIVDD	Full	1.22	1.8	3.4	V
I_{AVDD1}	Full		448	503	mA
I_{AVDD2}	Full		396	455	mA
I_{AVDD3}	Full		103	124	mA
I_{DVDD}	Full		108	127	mA
I_{DRVDD}	Full		106	119	mA
I_{SPIVDD}	Full		2	6	mA
POWER CONSUMPTION					
Total Power Dissipation[2]	Full		2.2		W
Power-Down Dissipation	Full		710		mW
Standby	Full		1.0		W

1 Differential capacitance is measured between the VIN+x and VIN−x pins (x = A or B).

2 Parallel interleaved LVDS mode. The power dissipation on DRVDD changes with the output data mode used.

SPECIFICATIONS

AC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (500 MSPS), 1.7 V p-p full-scale differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
ANALOG INPUT FULL SCALE	Full		2.06		V p-p
NOISE DENSITY[2]	Full		−153		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)[3]					
f_{IN} = 10 MHz	25°C		69.2		dBFS
f_{IN} = 170 MHz	Full	67.5	68.6		dBFS
f_{IN} = 340 MHz	25°C		68.4		dBFS
f_{IN} = 450 MHz	25°C		68.0		dBFS
f_{IN} = 765 MHz	25°C		64.4		dBFS
f_{IN} = 985 MHz	25°C		63.8		dBFS
f_{IN} = 1950 MHz	25°C		60.5		dBFS
SIGNAL-TO-NOISE RATIO AND DISTORTION RATIO (SINAD)[3]					
f_{IN} = 10 MHz	25°C		68.7		dBFS
f_{IN} = 170 MHz	Full	67	68.5		dBFS
f_{IN} = 340 MHz	25°C		67.6		dBFS
f_{IN} = 450 MHz	25°C		67.2		dBFS
f_{IN} = 765 MHz	25°C		63.8		dBFS
f_{IN} = 985 MHz	25°C		62.5		dBFS
f_{IN} = 1950 MHz	25°C		58.3		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 10 MHz	25°C		11.1		Bits
f_{IN} = 170 MHz	Full	10.8	10.9		Bits
f_{IN} = 340 MHz	25°C		10.8		Bits
f_{IN} = 450 MHz	25°C		10.8		Bits
f_{IN} = 765 MHz	25°C		10.3		Bits
f_{IN} = 985 MHz	25°C		10.1		Bits
f_{IN} = 1950 MHz	25°C		9.5		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)[3]					
f_{IN} = 10 MHz	25°C		83		dBFS
f_{IN} = 170 MHz	Full	76	85		dBFS
f_{IN} = 340 MHz	25°C		82		dBFS
f_{IN} = 450 MHz	25°C		86		dBFS
f_{IN} = 765 MHz	25°C		81		dBFS
f_{IN} = 985 MHz	25°C		76		dBFS
f_{IN} = 1950 MHz	25°C		69		dBFS
WORST HARMONIC, SECOND OR THIRD[3]					
f_{IN} = 10 MHz	25°C		−83		dBFS
f_{IN} = 170 MHz	Full		−85	−76	dBFS
f_{IN} = 340 MHz	25°C		−82		dBFS
f_{IN} = 450 MHz	25°C		−86		dBFS
f_{IN} = 765 MHz	25°C		−81		dBFS
f_{IN} = 985 MHz	25°C		−76		dBFS
f_{IN} = 1950 MHz	25°C		−69		dBFS
WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC[3]					
f_{IN} = 10 MHz	25°C		−93		dBFS

SPECIFICATIONS

Table 2. (Continued)

Parameter[1]	Temperature	Min	Typ	Max	Unit
f_{IN} = 170 MHz	Full		−92	−76	dBFS
f_{IN} = 340 MHz	25°C		−90		dBFS
f_{IN} = 450 MHz	25°C		−92		dBFS
f_{IN} = 765 MHz	25°C		−89		dBFS
f_{IN} = 985 MHz	25°C		−89		dBFS
f_{IN} = 1950 MHz	25°C		−85		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD), A_{IN1} AND A_{IN2} = −7 dBFS					
f_{IN1} = 185 MHz, f_{IN2} = 188 MHz	25°C		−88		dBFS
f_{IN1} = 338 MHz, f_{IN2} = 341 MHz	25°C		−87		dBFS
CROSSTALK[4]	25°C		96		dB
FULL POWER BANDWIDTH	25°C		2		GHz

1 See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.

2 Noise density is measured at a low analog input frequency (30 MHz).

3 See #unique_18/unique_18_Connect_42_T9 for the recommended settings for full-scale voltage and buffer current control.

4 Crosstalk is measured at 170 MHz with a −1.0 dBFS analog input on one channel and no input on the adjacent channel.

DIGITAL SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (500 MSPS), 1.7 V p-p full-scale differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	600	1200	1800	mV p-p
Input Common-Mode Voltage	Full		0.85		V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF
SYNC INPUTS (SYNC+, SYNC−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance (Differential)	Full			2.5	pF
LOGIC INPUTS (SDIO, SCLK, CSB, PDWN/STBY)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full		0.8 × SPIVDD		V
Logic 0 Voltage	Full	0	0.2 × SPIVDD		V
Input Resistance	Full		30		kΩ
LOGIC OUTPUT (SDIO)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage (I_{OH} = 800 μA)	Full		0.8 × SPIVDD		V
Logic 0 Voltage (I_{OL} = 50 μA)	Full		0.2 × SPIVDD		V
LOGIC OUTPUTS (FD_A, FD_B)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8	SPIVDD		V
Logic 0 Voltage	Full	0	0		V

SPECIFICATIONS

Table 3. (Continued)

Parameter	Temperature	Min	Typ	Max	Unit
Input Resistance	Full		30		kΩ
DIGITAL OUTPUTS (Dx±,[1] DCO±, STATUS±)					
Logic Compliance	Full		LVDS		
Differential Output Voltage	Full	230		430	mV p-p
Output Common-Mode Voltage (V_{CM})					
AC-Coupled	25°C	0		1.8	V
Short-Circuit Current (I_{DSHORT})	25°C	−100		+100	mA
Differential Return Loss (RL_{DIFF})[2]	25°C	8			dB
Common-Mode Return Loss (RL_{CM})[2]	25°C	6			dB
Differential Termination Impedance	Full	80	100	120	Ω

1 Where x = 0 to 13.

2 Differential and common-mode return loss is measured from 100 MHz to 0.75 MHz × baud rate.

SWITCHING SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.7 V p-p full-scale differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK					
Clock Rate (at CLK+/CLK− Pins)	Full	0.25		4	GHz
Maximum Sample Rate[1]	Full	500			MSPS
Minimum Sample Rate[2]	Full	250			MSPS
Clock Pulse Width					
High	Full	1000			ps
Low	Full	1000			ps
LVDS DATA OUTPUT PARAMETERS					
Data Propagation Delay (t_{PD})[3]	Full		2.225		ns
DCO± Propagation Delay (t_{DCO})[3]	Full		2.2		ns
DCO± to Data Skew					
Rising Edge Data (t_{SKEWR})[3]	Full	−150	−25	+100	ps
Falling Edge Data (t_{SKEWF})[3]	Full	850	1.025	1100	ps
STATUS± Propagation Delay (t_{STATUS})[4]	Full		2.2		ns
DCO± to STATUS± Skew (t_{FRAME})[4]	Full	−150	−25	+100	ps
Data Propagation Delay (t_{PD})[3]	Full		2.225		ns
DCO± Propagation Delay (t_{DCO})[3]	Full		2.2		ns
LATENCY[5]					
Pipeline Latency	Full		35		Clock cycles
Fast Detect Latency	Full			28	Clock cycles
HB1 Filter Latency[3]	Full		50		Clock cycles
HB1 + HB2 Filter Latency[3]	Full		101		Clock cycles
HB1 + HB2 + HB3 Filter Latency[3]	Full		217		Clock cycles
HB1 + HB2 + HB3 + HB4 Filter Latency[3]	Full		433		Clock cycles
Fast Detect Latency	Full		28		Clock cycles
Wake-Up Time[6]					
Standby	25°C		1		ms
Power-Down	25°C			4	ms

SPECIFICATIONS

Table 4. (Continued)

Parameter	Temperature	Min	Typ	Max	Unit
APERTURE					
Aperture Delay (t_A)	Full		530		ps
Aperture Uncertainty (Jitter, t_j)	Full		55		fs rms
Out of Range Recovery Time	Full		1		Clock Cycles

[1] The maximum sample rate is the clock rate after the divider.

[2] The minimum sample rate operates at 250 MSPS.

[3] This specification is valid for parallel interleaved, channel multiplexed, and byte mode output modes.

[4] This specification is valid for byte mode output mode only.

[5] No DDCs used.

[6] Wake-up time is defined as the time required to return to normal operation from power-down mode or standby mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Description	Min	Typ	Max	Unit
CLK± to SYNC± TIMING REQUIREMENTS	See Figure 2				
t_{SU_SR}	Device clock to SYNC± setup time		117		ps
t_{H_SR}	Device clock to SYNC± hold time		−96		ps
SPI TIMING REQUIREMENTS	See Figure 3				
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 3)	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 3)	10			ns

Timing Diagrams

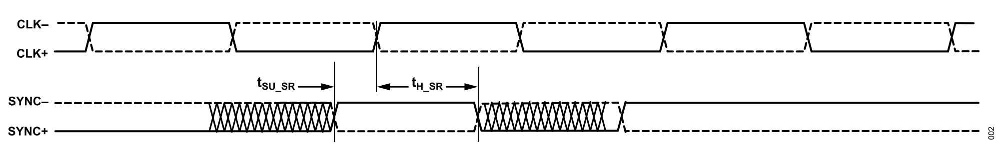


Figure 2. SYNC± Setup and Hold Timing

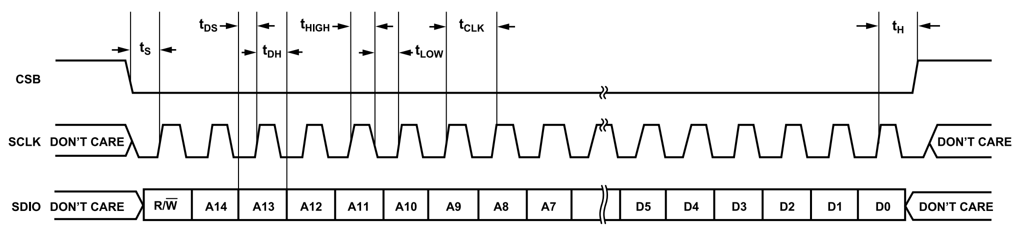


Figure 3. Serial Port Interface Timing Diagram

SPECIFICATIONS

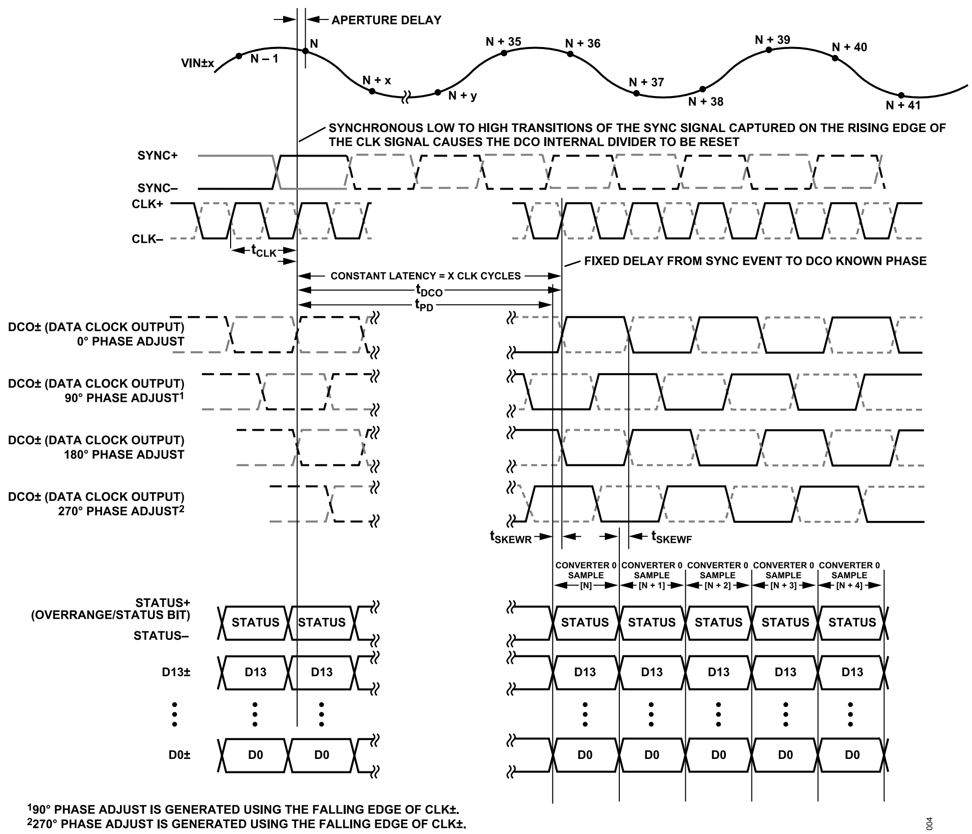


Figure 4. Parallel Interleaved Mode—One Converter, ≤14-Bit Data

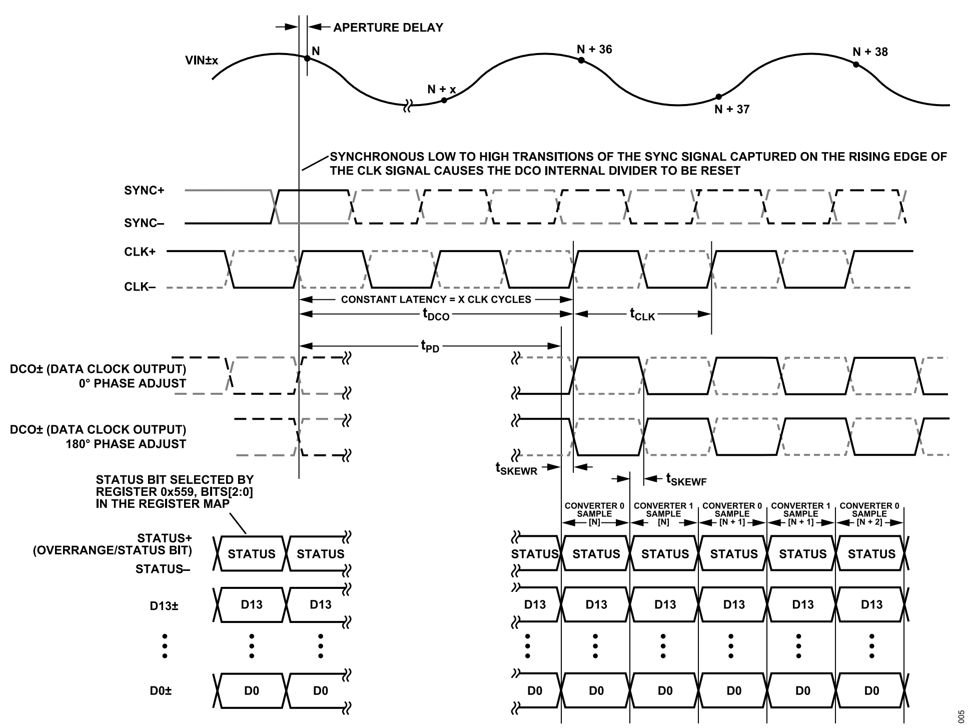


Figure 5. Parallel Interleaved Mode—Two Converters, ≤14-Bit Data, Output Sample Rate < 500 MSPS

SPECIFICATIONS

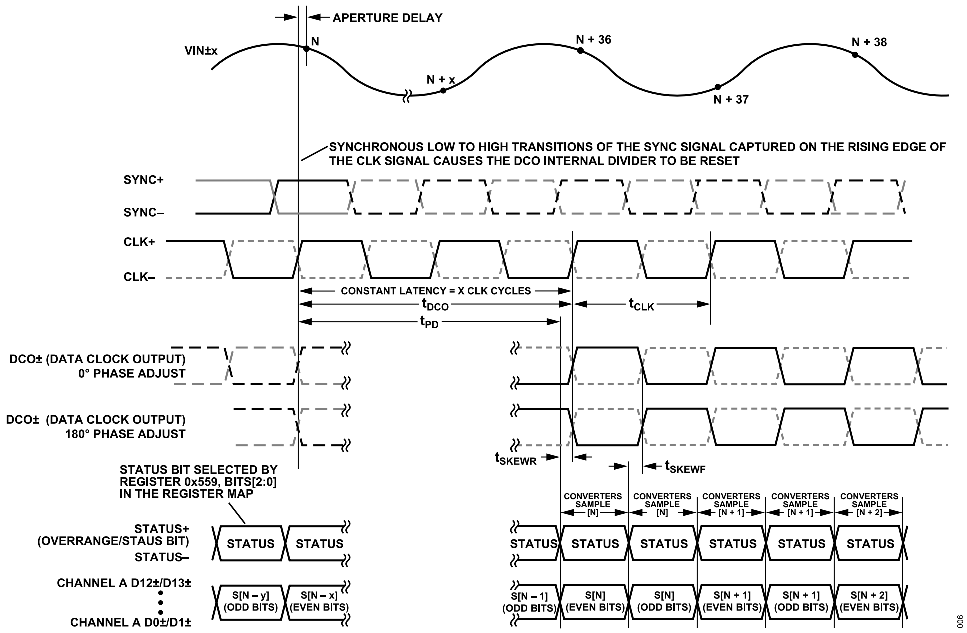


Figure 6. Channel Multiplexed (Even/Odd) Mode—One Converter, ≤14-Bit Data

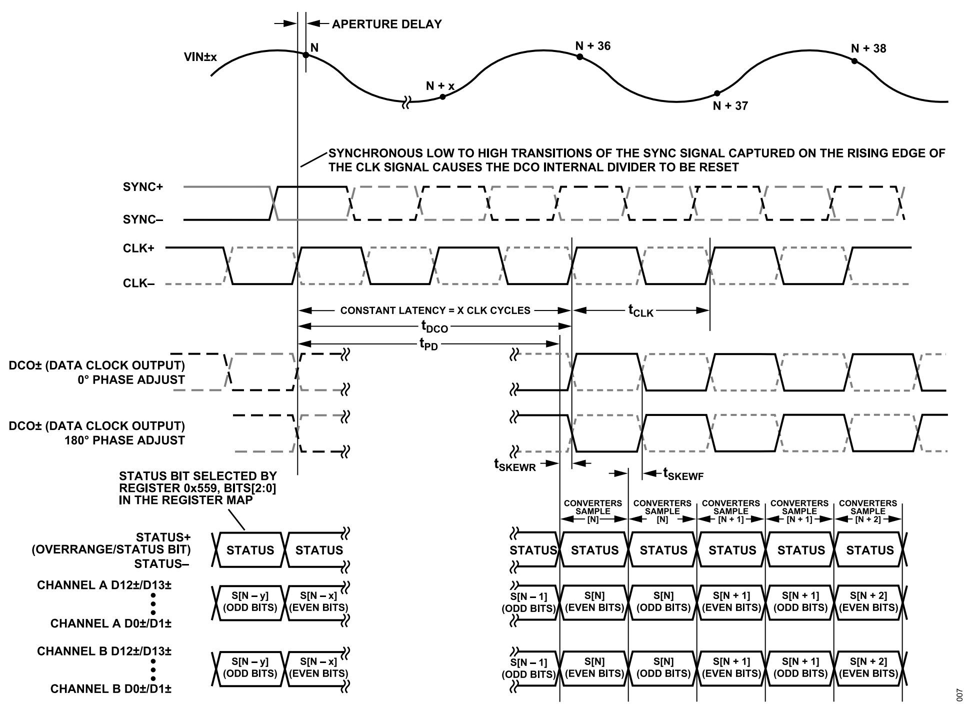
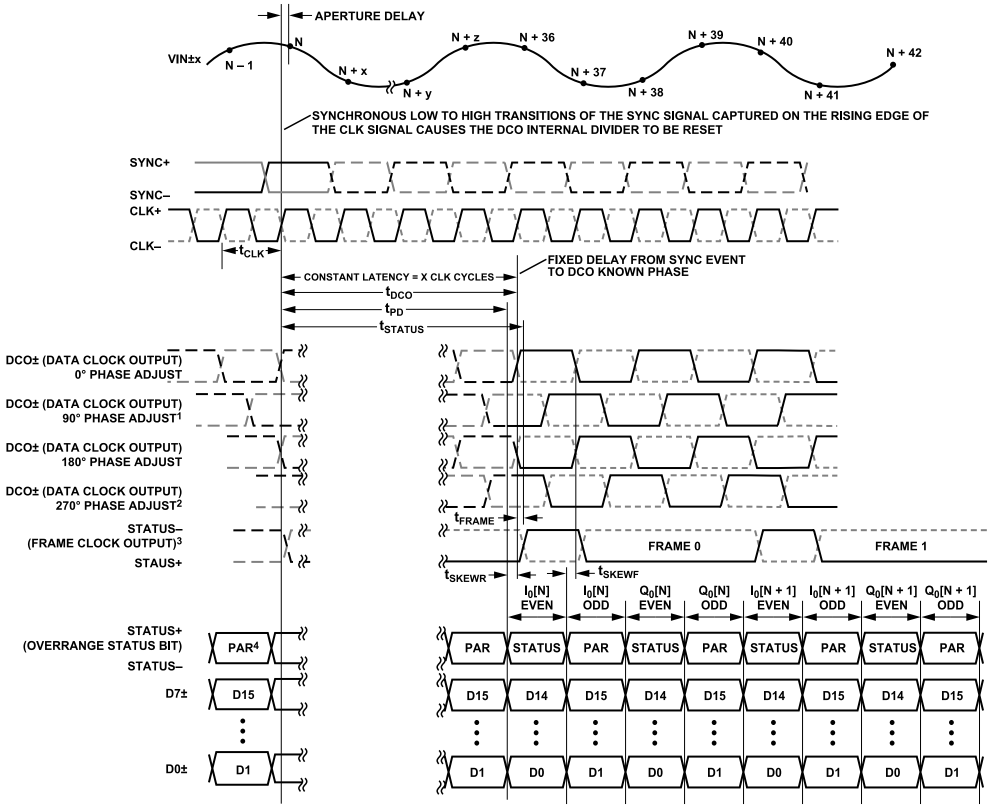


Figure 7. Channel Multiplexed (Even/Odd) Mode—Two Converters, ≤14-Bit Data, Output Sample Rate < 500 MSPS

SPECIFICATIONS



1 90° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
2 270° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
3 FRAME CLOCK OUTPUT SUPPORTS 3 MODES OF OPERATION:
1) ENABLED (ALWAYS ON).
2) DISABLED (ALWAYS OFF).
3) GAPPED PERIODIC (CONDITIONALLY ENABLED BASED ON PSEUDO-RANDOM BIT).
4 STATUS BIT SELECTED BY REGISTER 0x559, BITS[2:0] IN THE REGISTER MAP.

Figure 8. LVDS Byte Mode—Two Virtual Converters, One DDC, I/Q Data Decimate by 4

SPECIFICATIONS

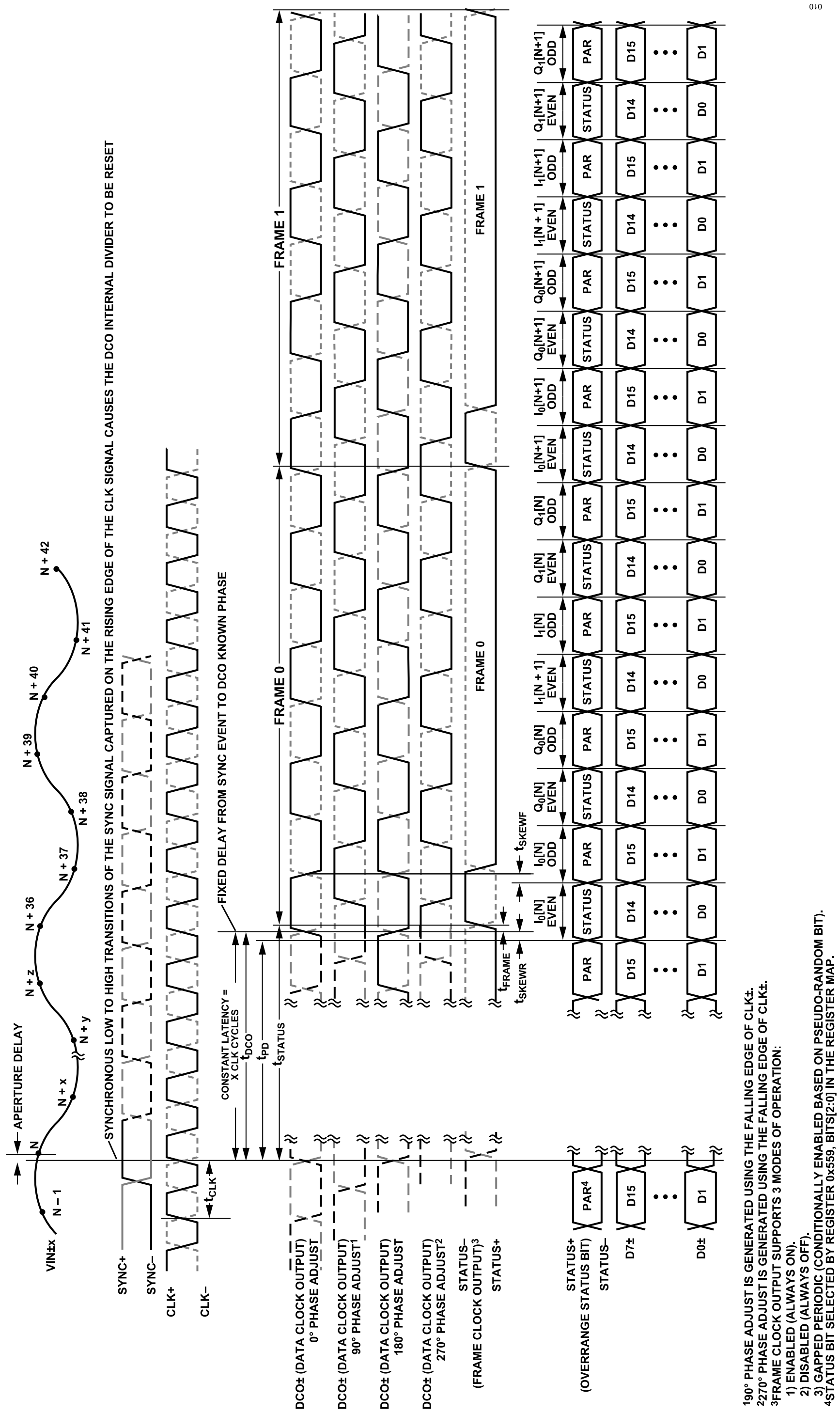


Figure 9. LVDS Byte Mode—Four Virtual Converters, Two DDCs, ≤16-Bit Data, I/Q Data Decimate by 8

SPECIFICATIONS

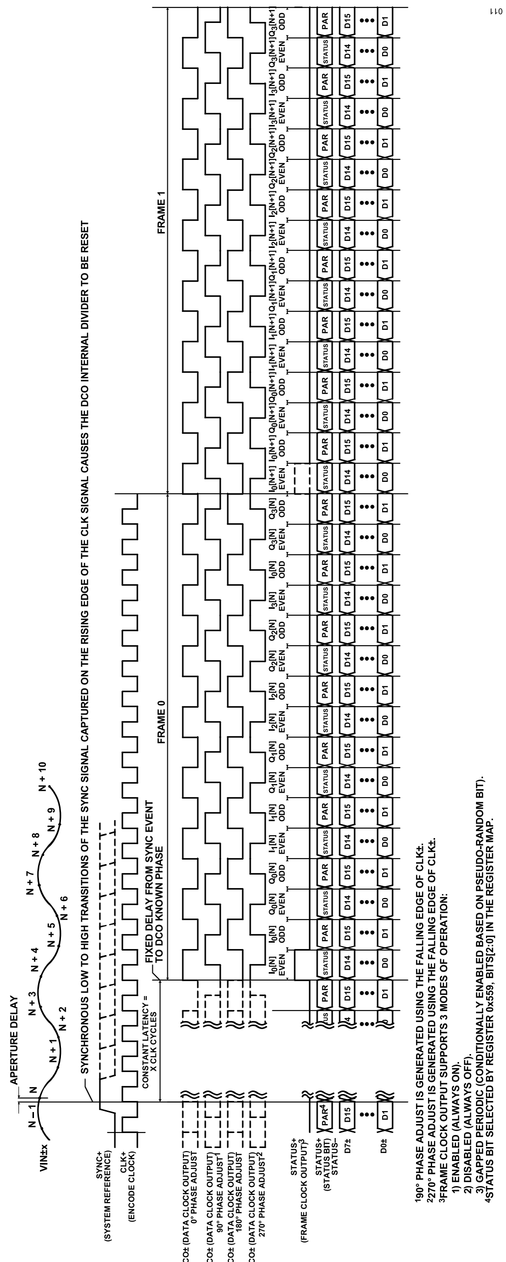


Figure 10. LVDS Byte Mode—Eight Virtual Converters, Four DDCs, ≤16-Bit Data, I/Q Data Decimate by 16

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.32 V
AVDD2 to AGND	2.75 V
AVDD3 to AGND	3.63 V
DVDD to DGND	1.32 V
DRVDD to DRGND	1.32 V
SPIVDD to AGND	3.63 V
AGND to DRGND	−0.3 V to +0.3 V
VIN±x to AGND	3.2 V
SCLK, SDIO, CSB to AGND	−0.3 V to SPIVDD + 0.3 V
VIN±x Maximum Swing	4.3 V p-p
PDWN/STBY to AGND	−0.3 V to SPIVDD + 0.3 V
Environmental	
Operating Temperature Range (T_{CASE})	−40°C to +85°C
Maximum Junction Temperature	125°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA}, θ_{JB}, and θ_{JC} are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation effectively reducing θ_{JA} and θ_{JB}. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 7.

Table 7. Simulated Thermal Data

PCB Type	Airflow Velocity (m/sec)	θ_{JA}	θ_{JB}	θ_{JC_TOP}	θ_{JC_BOT}	Unit
JEDEC 2s2p Board	0.0	17.8[1, 2]	6.3[1, 3]	4.7[1, 4]	1.2[1, 4]	°C/W
	1.0	15.6[1, 2]	5.9[1, 3]	N/A[5]	N/A[5]	°C/W
	2.5	15.0[1, 2]	5.7[1, 3]	N/A[5]	N/A[5]	°C/W
10-Layer PCB	0.0	13.8	4.6	4.7	1.2	°C/W
	1.0	12.7	4.6	N/A[5]	N/A[5]	°C/W
	2.5	12.0	4.6	N/A[5]	N/A[5]	°C/W

1 Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.

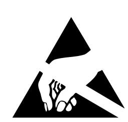
2 Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).

3 Per JEDEC JESD51-8 (still air).

4 Per MIL-STD 883, Method 1012.1.

5 N/A means not applicable.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	AGND	AGND	AGND	AVDD2	AVDD1	AGND	CLK+	CLK–	AGND	AVDD1	AVDD2	AGND	AGND	AGND	A
B	AVDD3	AGND	AGND	AVDD2	AVDD1	AGND	AGND	AGND	AGND	AVDD1	AVDD2	AGND	AGND	AVDD3	B
C	AVDD3	AGND	AGND	AVDD2	AVDD1	AGND	SYNC+	SYNC–	AGND	AVDD1	AVDD2	AGND	AGND	AVDD3	C
D	AGND	AGND	AGND	AVDD2	AVDD1	AGND	AVDD1	AGND	AGND	AVDD1	AVDD2	AGND	AGND	AGND	D
E	VIN–B	AGND	AGND	AVDD2	AVDD1	AGND	AGND	AGND	AGND	AVDD1	AVDD2	AGND	AGND	VIN–A	E
F	VIN+B	AGND	AGND	AVDD2	AGND	AGND	AGND	AGND	AGND	AGND	AVDD2	AGND	AGND	VIN+A	F
G	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AVDD2	AGND	AGND	AGND	G
H	AGND	AGND	AGND	CSB	AGND	AGND	AGND	AGND	AGND	V_1P0	AGND	AGND	AGND	AGND	H
J	FD_B	AGND	AGND	SCLK	SPIVDD	AGND	AGND	AGND	AGND	AVDD2	SPIVDD	AGND	PDWN/STBY	FD_A	J
K	DGND	DGND	AGND	SDIO	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DCO–	DCO+	K
L	DVDD	DVDD	DGND	DGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	STATUS–	STATUS+	L
M	D1+	D1–	DVDD	DVDD	DRVDD	DRVDD	DRVDD	DRGND	DRGND	DRGND	DRGND	DRGND	D13–	D13+	M
N	D2–	D3–	D4–	D5–	D6–	D0–	DRVDD	DRGND	D7–	D8–	D9–	D10–	D11–	D12–	N
P	D2+	D3+	D4+	D5+	D6+	D0+	DRVDD	DRGND	D7+	D8+	D9+	D10+	D11+	D12+	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 11. Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
Power Supplies			
A5, A10, B5, B10, C5, C10, D5, D7, D10, E5, E10	AVDD1	Supply	Analog Power Supply (1.25 V Nominal).
A4, A11, B4, B11, C4, C11, D4, D11, E4, E11, F4, F11, G11, J10	AVDD2	Supply	Analog Power Supply (2.50 V Nominal).
B1, B14, C1, C14	AVDD3	Supply	Analog Power Supply (3.3 V Nominal)
L1, L2, M3, M4	DVDD	Supply	Digital Power Supply (1.25 V Nominal).
M5, M6, M7, N7, P7	DRVDD	Supply	Digital Driver Power Supply (1.25 V Nominal).
J5, J11	SPIVDD	Supply	Digital Power Supply for SPI (1.8 V to 3.4 V).
K1, K2, L3, L4	DGND	Ground	Ground Reference for DVDD.
M8 to M12, N8, P8	DRGND	Ground	Ground Reference for DRVDD.
A1, A2, A3, A6, A9, A12, A13, A14, B2, B3, B6, B7, B8, B9, B12, B13, C2, C3, C6, C9, C12, C13, D1, D2, D3, D6, D8, D9, D12, D13, D14, E2, E3, E6 to E9, E12, E13, F2, F3, F5 to F10, F12, F13, G1 to G10, G12, G13, G14, H1, H2, H3, H5 to H9, H11 to H14, J2, J3, J6 to J9, J12, K3, K5 to K12, L5 to L12	AGND	Ground	Ground Reference for AVDD.
Analog			
E14, F14	VIN−A, VIN+A	Input	ADC A Analog Input Complement/True.
E1, F1	VIN−B, VIN+B	Input	ADC B Analog Input Complement/True.
H10	V_1P0	Input/DNC	1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or as an input. Do not connect this pin if using the internal reference. This pin requires a 1.0 V reference voltage input if using an external voltage reference source.
A7, A8	CLK+, CLK−	Input	Clock Input True/Complement.
CMOS Outputs			
J14, J1	FD_A, FD_B	Output	Fast Detect Outputs for Channel A and Channel B.
Digital Inputs			
C7, C8	SYNC+, SYNC−	Input	Active High LVDS SYNC Input—True/Complement.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 8. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type	Description
Data Outputs			
N6, P6	D0−, D0+	Output	LVDS Lane 0 Output Data—Complement/True.
M1, M2	D1+, D1−	Output	LVDS Lane 1 Output Data—True/Complement.
N1, P1	D2−, D2+	Output	LVDS Lane 2 Output Data—Complement/True.
N2, P2	D3−, D3+	Output	LVDS Lane 3 Output Data—Complement/True.
N3, P3	D4−, D4+	Output	LVDS Lane 4 Output Data—Complement/True.
N4, P4	D5−, D5+	Output	LVDS Lane 5 Output Data—Complement/True.
N5, P5	D6−, D6+	Output	LVDS Lane 6 Output Data—Complement/True.
N9, P9	D7−, D7+	Output	LVDS Lane 7 Output Data—Complement/True.
N10, P10	D8−, D8+	Output	LVDS Lane 8 Output Data—Complement/True.
N11, P11	D9−, D9+	Output	LVDS Lane 9 Output Data—Complement/True.
N12, P12	D10−, D10+	Output	LVDS Lane 10 Output Data—Complement/True.
N13, P13	D11−, D11+	Output	LVDS Lane 11 Output Data—Complement/True.
N14, P14	D12−, D12+	Output	LVDS Lane 12 Output Data—Complement/True.
M13, M14	D13−, D13+	Output	LVDS Lane 13 Output Data—Complement/True.
L13, L14	STATUS−, STATUS+	Output	LVDS Status Output Data—Complement/True.
K13, K14	DCO−, DCO+	Output	LVDS Digital Clock Output Data—Complement/True.
SPI Controls			
K4	SDIO	Input/output	SPI Serial Data Input/Output.
J4	SCLK	Input	SPI Serial Clock.
H4	CSB	Input	SPI Chip Select (Active Low).
J13	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 1.2 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.2 V, DRVDD = 1.2 V, SPIVDD = 1.8 V, sampling rate = 500 MHz, 1.6 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, 256k FFT sample, unless otherwise noted.

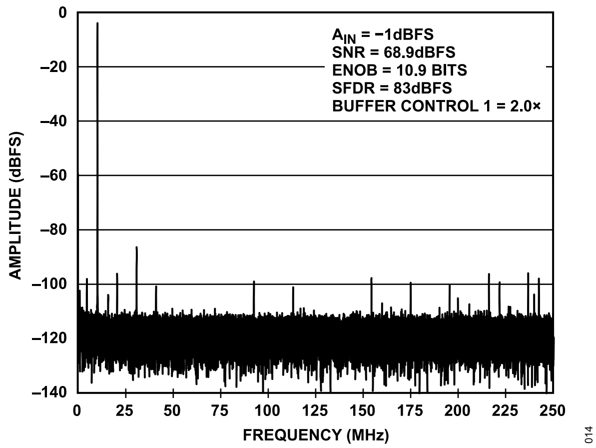


Figure 12. Single Tone FFT with f_{IN} = 10.3 MHz

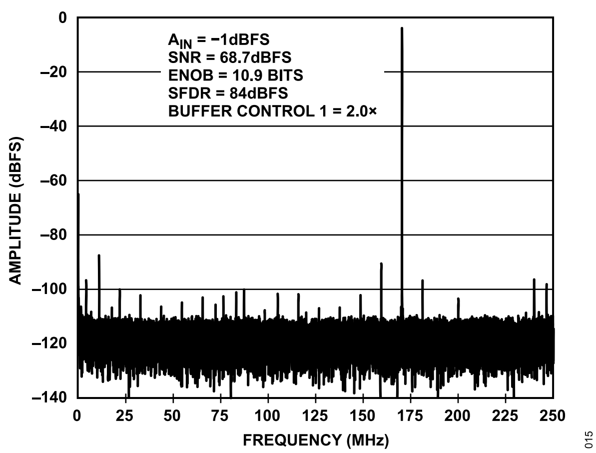


Figure 13. Single Tone FFT with f_{IN} = 170.3 MHz

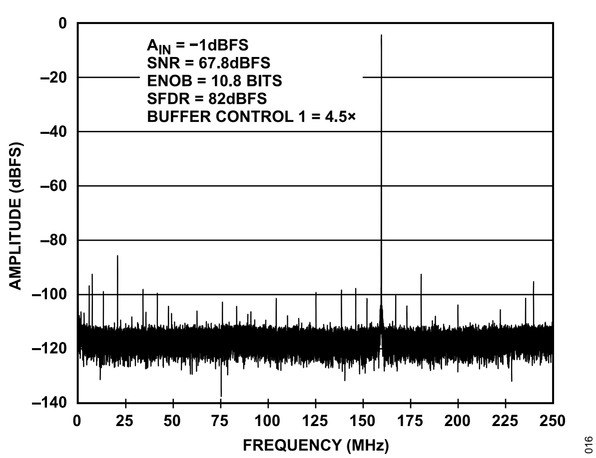


Figure 14. Single Tone FFT with f_{IN} = 340.3 MHz

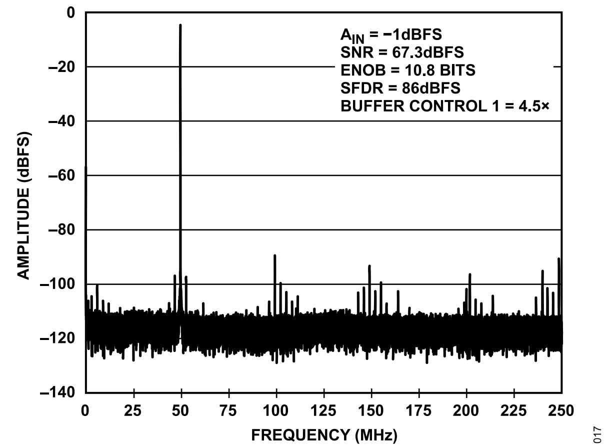


Figure 15. Single Tone FFT with f_{IN} = 450.3 MHz

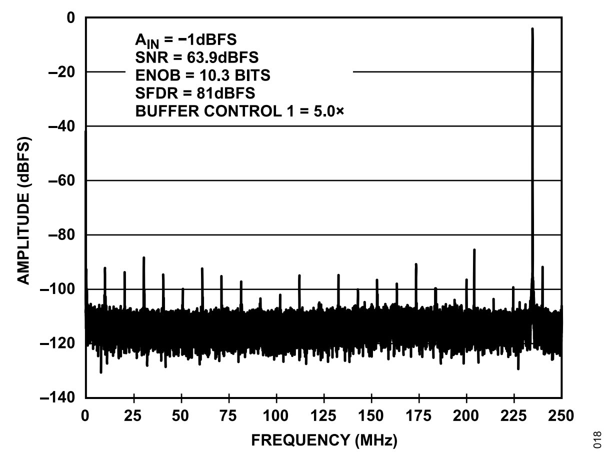


Figure 16. Single Tone FFT with f_{IN} = 765.3 MHz

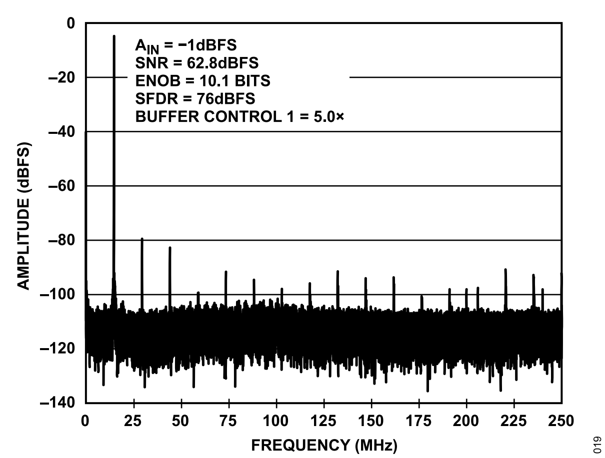


Figure 17. Single-Tone FFT with f_{IN} = 985.3 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

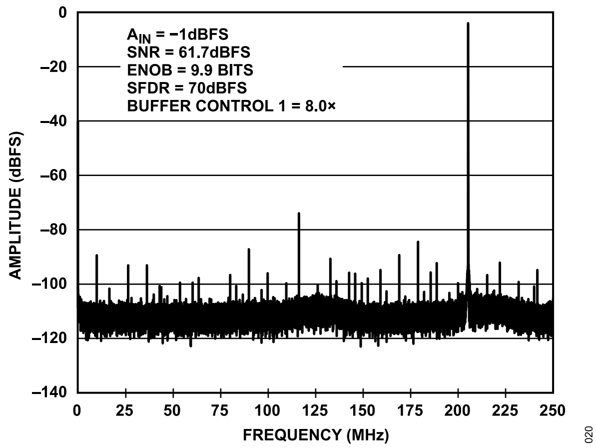


Figure 18. Single Tone FFT with f_{IN} = 1205.3 MHz

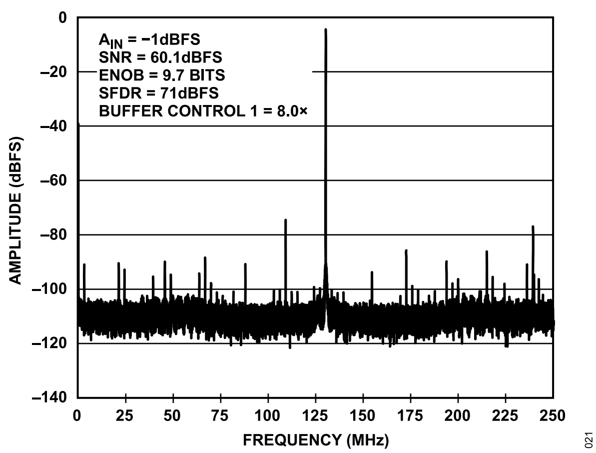


Figure 19. Single Tone FFT with f_{IN} = 1630.3 MHz

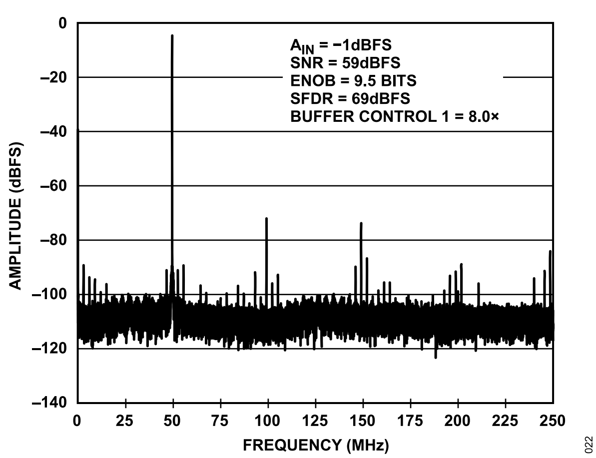


Figure 20. Single Tone FFT with f_{IN} = 985.3 MHz

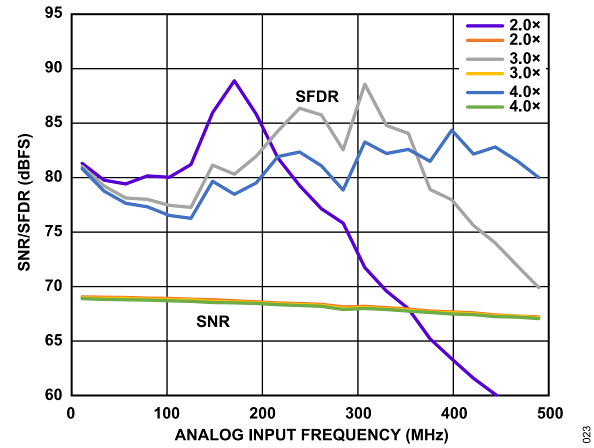


Figure 21. SNR/SFDR vs. Analog Input Frequency (f_{IN}); f_{IN} < 500 MHz; Buffer Control 1 Setting = 2.0×, 3.0×, and 4.0×

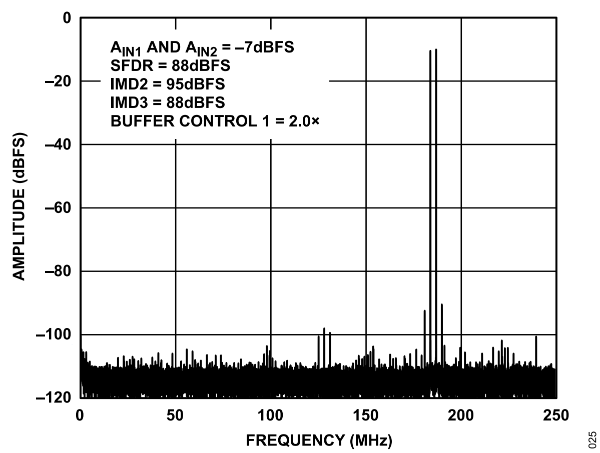


Figure 22. Two-Tone FFT with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

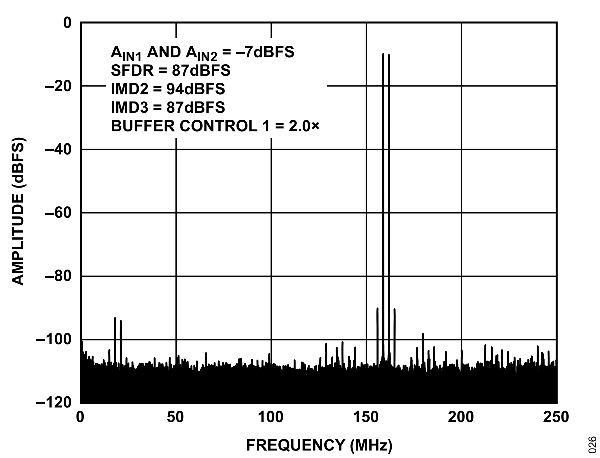


Figure 23. Two-Tone FFT; f_{IN1} = 338 MHz, f_{IN2} = 341 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

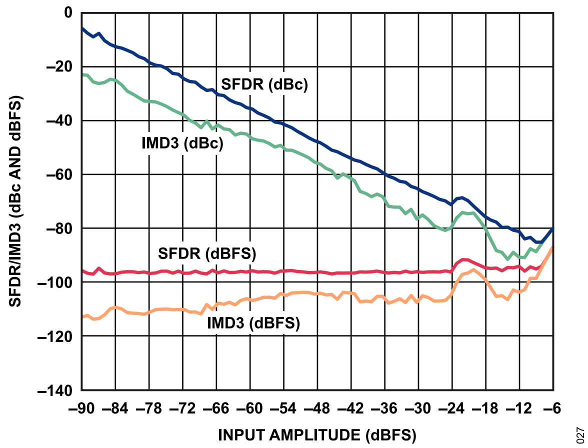


Figure 24. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

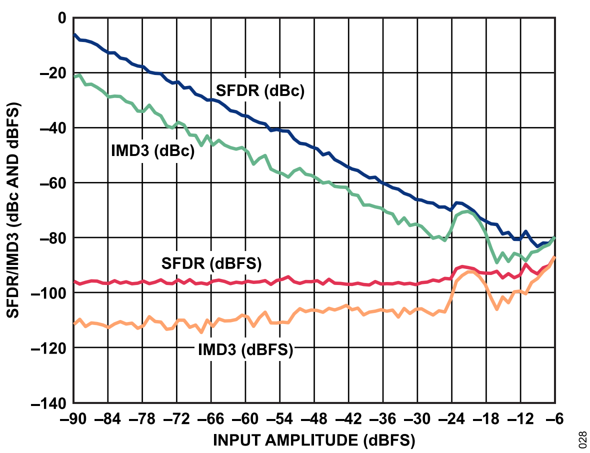


Figure 25. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 338 MHz and f_{IN2} = 341 MHz

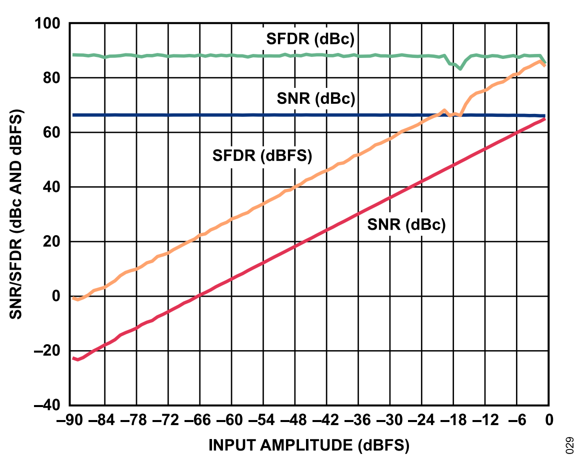


Figure 26. SNR/SFDR vs. Input Amplitude, f_{IN} = 170.3 MHz

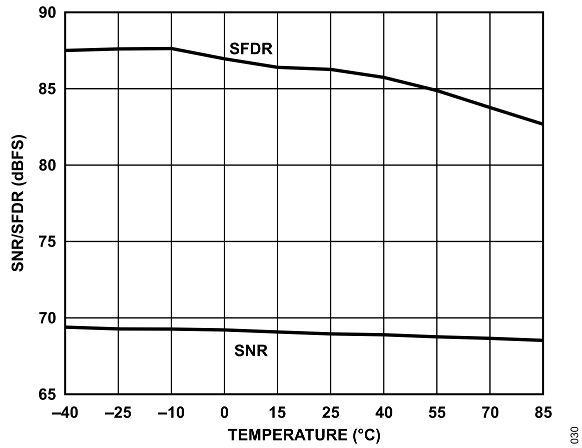


Figure 27. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

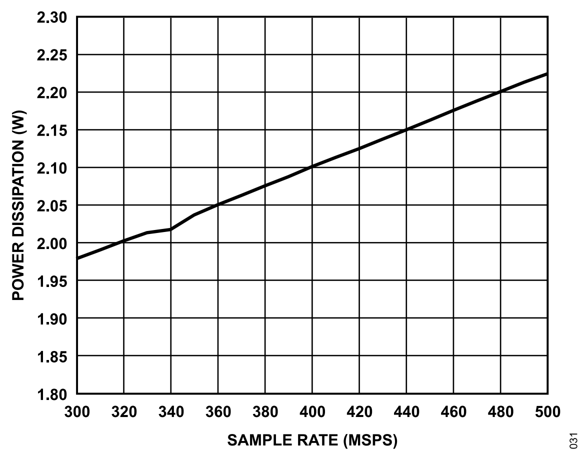


Figure 28. Power Dissipation vs. Sample Rate (f_S) (Default SPI)

EQUIVALENT CIRCUITS

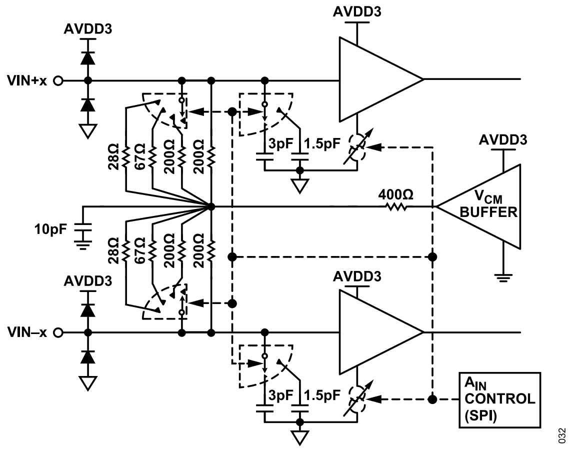


Figure 29. Analog Inputs

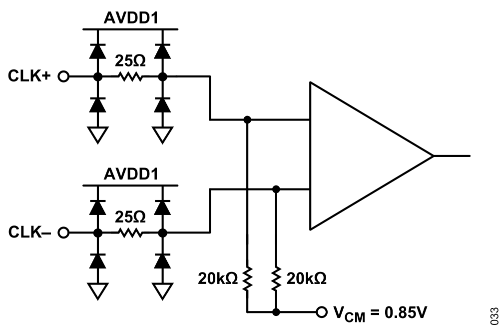


Figure 30. Clock Inputs

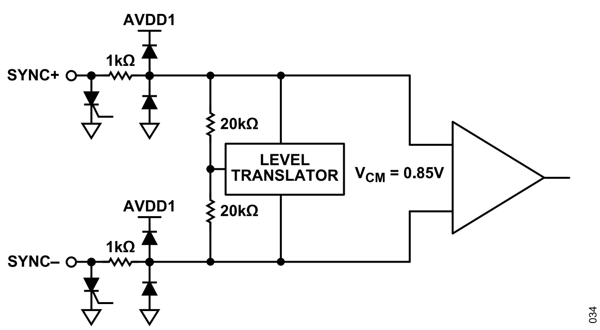


Figure 31. SYNC± Inputs

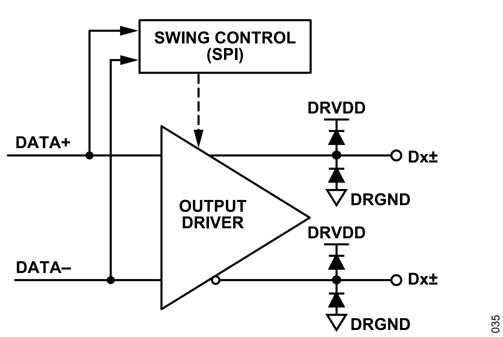


Figure 32. LVDS Digital Outputs, STATUS±, DCO±

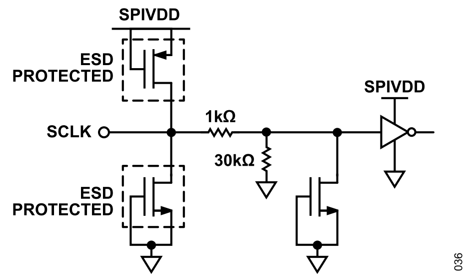


Figure 33. SCLK Inputs

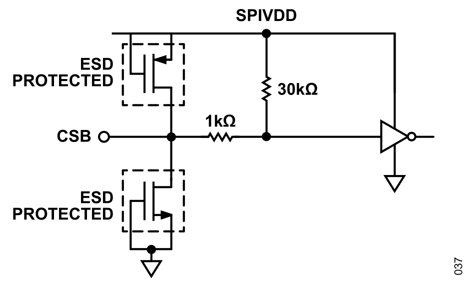


Figure 34. CSB Input

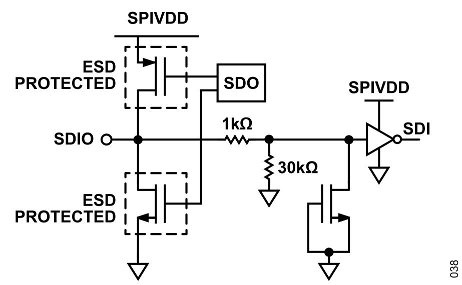


Figure 35. SDIO

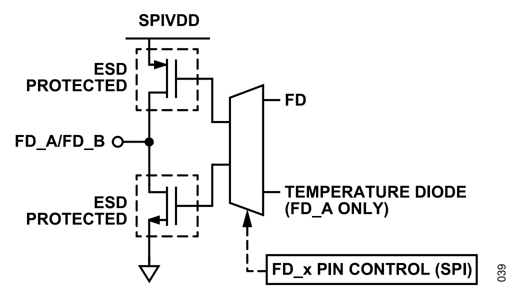


Figure 36. FD_A/FD_B Outputs

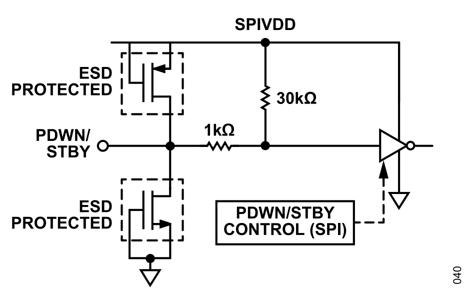


Figure 37. PDWN/STBY Input

EQUIVALENT CIRCUITS

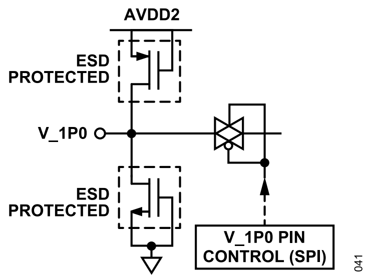


Figure 38. V_1P0 Input/Output

THEORY OF OPERATION

The AD9684 has two analog input channels and 14 LVDS output lane pairs. The ADC is designed to sample wide bandwidth analog signals of up to 2 GHz. The AD9684 is optimized for wide input bandwidth, a high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs that support a variety of user selectable input ranges. An integrated voltage reference eases design considerations.

The AD9684 has several functions that simplify the AGC function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly reduce the system gain to avoid an overrange condition at the ADC input.

The LVDS outputs can be configured depending on the decimation ratio. Multiple device synchronization is supported through the SYNC± input pins.

ADC ARCHITECTURE

The architecture of the AD9684 consists of an input buffered pipelined ADC. The input buffer provides a termination impedance to the analog input signal. This termination impedance can be changed using the SPI to meet the termination needs of the driver/amplifier. The default termination value is set to 400 Ω. The input buffer is optimized for high linearity, low noise, and low power.

The input buffer provides a linear high input impedance (for ease of drive) and reduces kickback from the ADC. The buffer is optimized for high linearity, low noise, and low power. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample, whereas the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9684 is a differential buffer. The internal common-mode voltage of the buffer is 2.05 V. The clock signal alternately switches the input circuit between sample mode and hold mode. When the input circuit is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor, in series with each input, helps reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, thus, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Place either a differential capacitor or two single-ended capacitors on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input, which limits unwanted broadband noise. For more information, see the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005). In general, the precise values depend on the application.

For best dynamic performance, the source impedances driving VIN+x and VIN−x must be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9684, the available span is 2.06 V p-p differential.

Differential Input Configurations

There are several ways to drive the AD9684, either actively or passively. However, optimum performance is achieved by driving the analog input differentially.

For applications in which SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9684.

For low to midrange frequencies, a double balun or double transformer network is recommended for optimum performance of the AD9684 (see Figure 39). For higher frequencies in the second and third Nyquist zones, it is better to remove some of the front-end passive components to ensure wideband operation (see Figure 40).

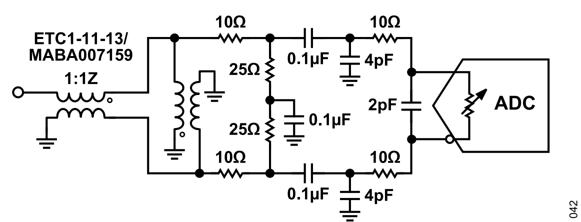


Figure 39. Differential Transformer-Coupled Configuration for First and Second Nyquist Frequencies

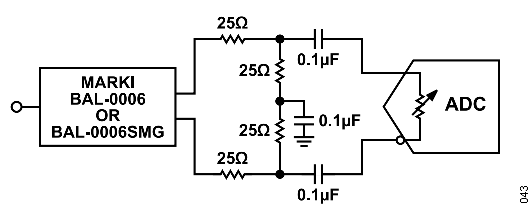


Figure 40. Differential Transformer-Coupled Configuration for Second and Third Nyquist Frequencies

THEORY OF OPERATION

Input Common Mode

The analog inputs of the AD9684 are internally biased to the common mode as shown in Figure 41. The common-mode buffer has a limited range in that the performance suffers greatly if the common-mode voltage drops by more than 100 mV. Therefore, in dc-coupled applications, set the common-mode voltage to 2.05 V ± 100 mV to ensure proper ADC operation.

Analog Input Controls and SFDR Optimization

The AD9684 offers flexible controls for the analog inputs, such as input termination and buffer current. All of the available controls are shown in Figure 41.

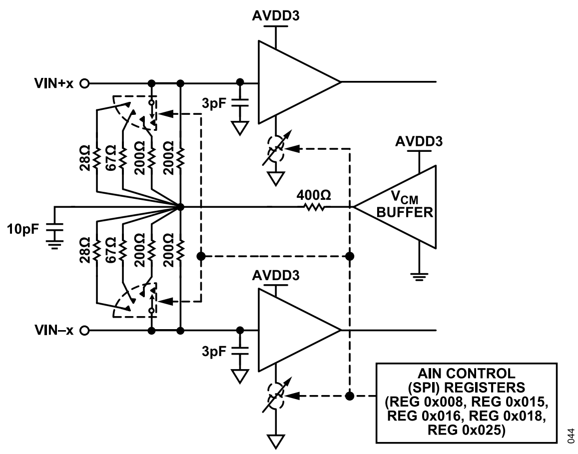


Figure 41. Analog Input Controls

Using Register 0x018, the buffer currents on each channel can be scaled to optimize the SFDR over various input frequencies and bandwidths of interest. As the input buffer currents are set, the amount of current required by the AVDD3 supply changes. For a complete list of buffer current settings, see Table 29.

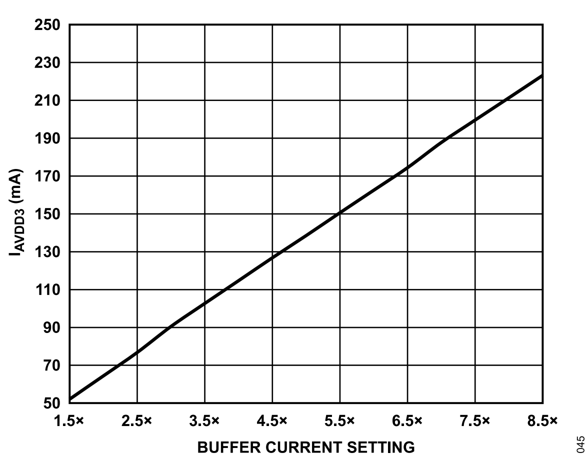


Figure 42. AVDD3 Power (I_{AVDD3}) vs. Buffer Current Control Setting in Register 0x018

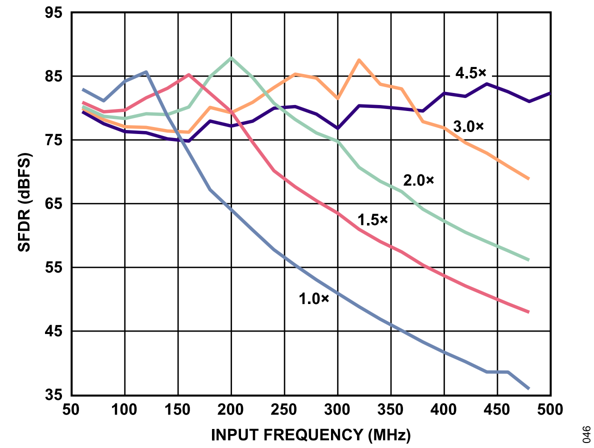


Figure 43. Buffer Current Sweeps (SFDR vs. Input Frequency and I_{BUFF}), 10 MHz < f_{IN} < 500 MHz

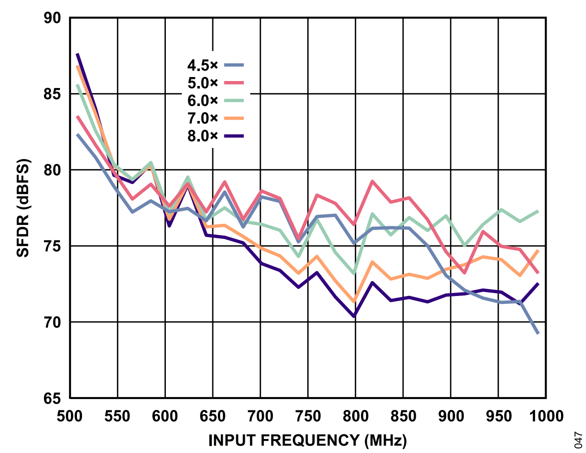


Figure 44. Buffer Current Sweeps (SFDR vs. Input Frequency and I_{BUFF}), 500 MHz < f_{IN} < 1000 MHz

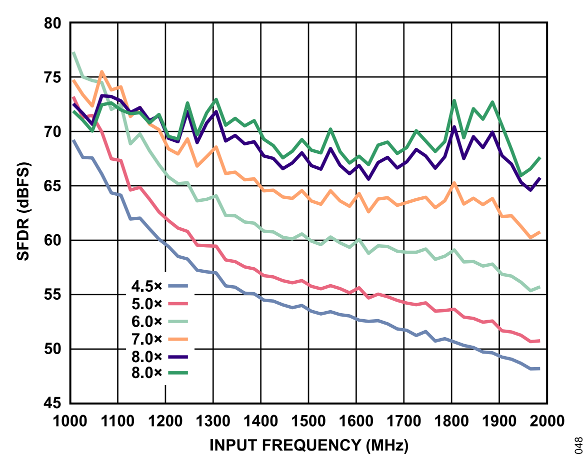


Figure 45. Buffer Current Sweeps (SFDR vs. Input Frequency and I_{BUFF}), 1 GHz < f_{IN} < 2 GHz, Front-End Network Shown in Figure 40

Figure 43, Figure 44, and Figure 45 show how the SFDR can be optimized using the buffer current setting in Register 0x018

THEORY OF OPERATION

for different Nyquist zones. At frequencies greater than 1 GHz, it is better to run the ADC at input amplitudes less than −1 dBFS (−3 dBFS, for example). This greatly improves the linearity of the converted signal without sacrificing SNR performance.

Table 9 shows the recommended buffer current and full-scale voltage settings for the different analog input frequency ranges.

Table 9. SFDR Optimization for Input Frequencies

Frequency	Buffer Control 1 (Register 0x018)	Input Full-Scale Range (Register 0x025)	Input Full-Scale Control (Register 0x030)	Input Termination (Register 0x016)[1]
DC to 250 MHz	0x20 (2.0×)	0x0C (2.06 V p-p)	0x04	0x0C/0x1C/0x6C
250 MHz to 500 MHz	0x70 (4.5×)	0x0C (2.06 V p-p)	0x04	0x0C/0x1C/0x6C
500 MHz to 1 GHz	0x80 (5.0×)	0x08 (1.46 V p-p)	0x18	0x0C/0x1C/0x6C
1 GHz to 2 GHz	0xF0 (8.5×)	0x08 (1.46 V p-p)	0x18	0x0C/0x1C/0x6C

[1] The input termination can be changed to accommodate the application with little or no impact to ac performance.

THEORY OF OPERATION

Absolute Maximum Input Swing

The absolute maximum input swing allowed at the inputs of the AD9684 is 4.3 V p-p differential. Signals operating near or at this level can cause permanent damage to the ADC.

Dither

The AD9684 has internal on-chip dither circuitry that improves the ADC linearity and SFDR, particularly at smaller signal levels. A known but random amount of white noise is injected into the input of the AD9684. This dither improves the small signal linearity within the ADC transfer function and is precisely subtracted out digitally. The dither is turned on by default and does not reduce the ADC input dynamic range. The data sheet specifications and limits are obtained with the dither turned on.

The dither is turned on by default. It is not recommended to turn it off.

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD9684. This internal 1.0 V reference sets the full-scale input range of the ADC. For more information on adjusting the input swing, see Table 29. Figure 46 shows the block diagram of the internal 1.0 V reference controls.

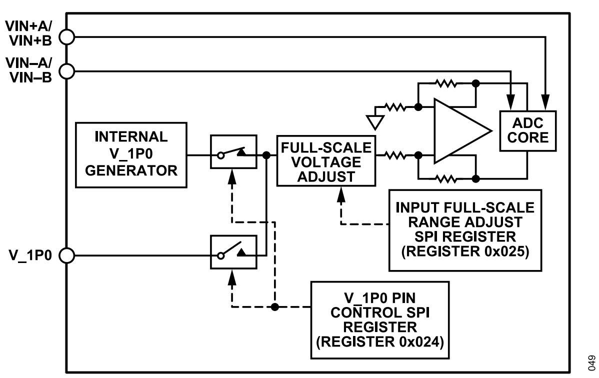


Figure 46. Internal Reference Configuration and Controls

Register 0x024 enables the user either to use this internal 1.0 V reference, or to provide an external 1.0 V reference. When using an external voltage reference, provide a 1.0 V reference. The full-scale adjustment is made using the SPI, irrespective of the reference voltage. For more information on adjusting the full-scale level of the AD9684, see the Memory Map Register Table section.

The use of an external reference may be necessary, in some applications, to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 47 shows the typical drift characteristics of the internal 1.0 V reference.

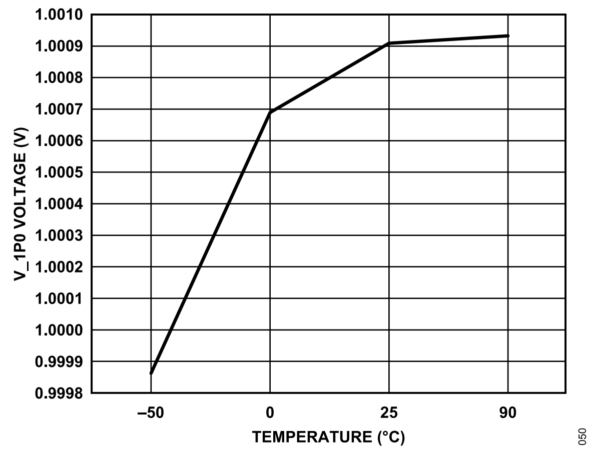


Figure 47. Typical V_1P0 Drift

The external reference must be a stable 1.0 V reference. The ADR130 is a good option for providing the 1.0 V reference. Figure 48 shows how the ADR130 can be used to provide the external 1.0 V reference to the AD9684. The grayed out areas show unused blocks within the AD9684 while using the ADR130 to provide the external reference.

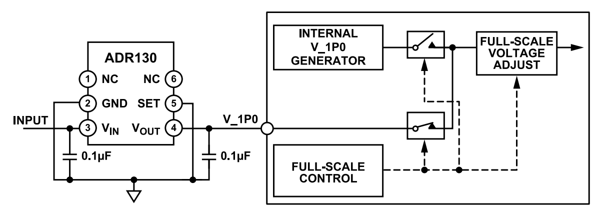


Figure 48. External Reference Using the ADR130

CLOCK INPUT CONSIDERATIONS

For optimum performance, drive the AD9684 sample clock inputs (CLK+ and CLK−) with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK− pins via a transformer or clock drivers. These pins are biased internally and require no additional biasing.

Figure 49 shows a preferred method for clocking the AD9684. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer.

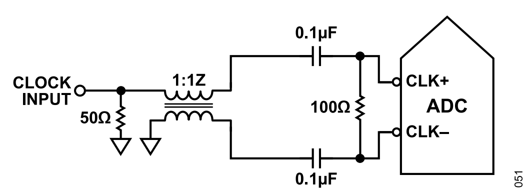


Figure 49. Transformer Coupled Differential Clock

Another option is to ac couple a differential CML or LVDS signal to the sample clock input pins, as shown in Figure 50 and Figure 51.

THEORY OF OPERATION

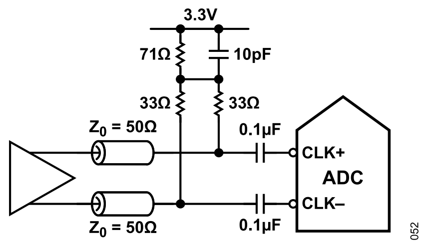


Figure 50. Differential CML Sample Clock

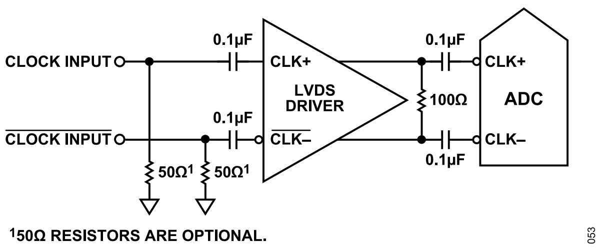


Figure 51. Differential LVDS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. In applications where the clock duty cycle cannot be guaranteed to be 50%, a higher multiple frequency clock can be supplied to the device. The AD9684 can be clocked at 2 GHz with the internal clock divider set to 2. The output of the divider offers a 50% duty cycle, high slew rate (fast edge) clock signal to the internal ADC. See the Memory Map section for more details on using this feature.

Input Clock Divider

The AD9684 contains an input clock divider with the ability to divide the Nyquist input clock by 1, 2, 4, and 8. The divider ratios can be selected using Register 0x10B. This is shown in Figure 52.

The maximum frequency at the CLK± inputs is 4 GHz. This is the limit of the divider. In applications where the clock input is a multiple of the sample clock, the appropriate divider ratio must be programmed into the clock divider before applying the clock signal. This ensures that the current transients during device startup are controlled.

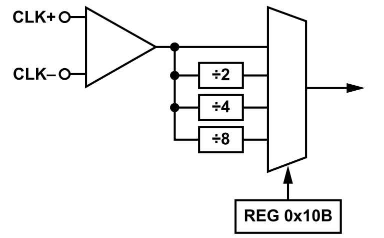


Figure 52. Clock Divider Circuit

The AD9684 clock divider can be synchronized using the external SYNC± input. A valid SYNC± input causes the clock divider to reset to a programmable state. This feature is enabled by setting Bit 7 of Register 0x10D. This synchronization feature allows multiple devices to have their clock dividers aligned to guarantee simultaneous input sampling.

Input Clock Divider ½ Period Delay Adjustment

The input clock divider inside the AD9684 provides phase delay in increments of ½ the input clock cycle. Program Register 0x10C to enable this delay independently for each channel.

Clock Fine Delay Adjustment

To adjust the AD9684 sampling edge instant, write to Register 0x117 and Register 0x118. Setting Bit 0 of Register 0x117 enables the fine delay feature, and Register 0x118, Bits[7:0] set the value of the delay. This value can be programmed individually for each channel. The clock delay can be adjusted from −151.7 ps to +150 ps in ~1.7 ps increments. The clock delay adjust takes effect immediately when it is enabled via SPI writes. Enabling the clock fine delay adjustment in Register 0x117 causes a datapath reset.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR = 20 \times \log 10 (2 \times \pi \times f_A \times t_J) \quad (1)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 53).

THEORY OF OPERATION

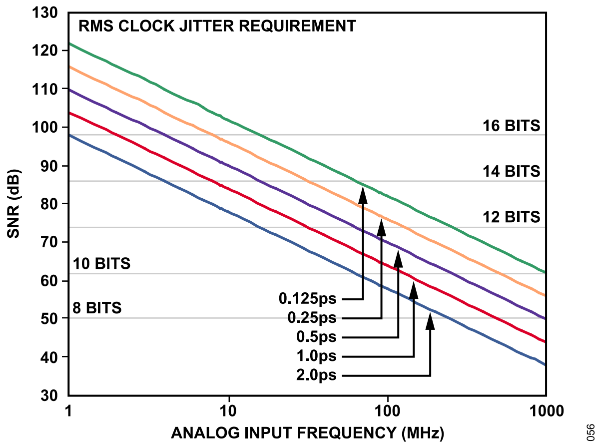


Figure 53. Ideal SNR vs. Analog Input Frequency and Jitter

Treat the clock input as an analog signal when aperture jitter may affect the dynamic range of the AD9684. Separate the power supplies for the clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. If the clock is generated from another type of source (by gating, dividing, or other methods), retime the clock by the original clock at the last step. For more in-depth information about jitter performance as it relates to ADCs, see the AN-501 Application Note and the AN-756 Application Note.

Figure 54 shows the estimated SNR of the AD9684 across the input frequency for different clock induced jitter values. Estimate the SNR using the following equation:

$$SNR(\text{dBFS}) = 10\log\left(10^{\left(\frac{-SNR_{ADC}}{10}\right)} + 10^{\left(\frac{-SNR_{JITTER}}{10}\right)}\right) \quad (2)$$

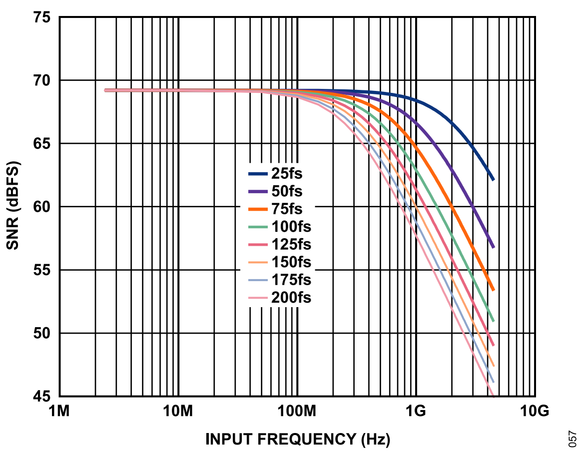


Figure 54. Estimated SNR Degradation for the AD9684 vs. Input Frequency and Clock Jitter

POWER-DOWN/STANDBY MODE

The AD9684 has a PDWN/STBY pin that configures the device in power-down or standby mode. The default operation is the power-down function. The PDWN/STBY pin is a logic high pin. The power-down option can also be set via Register 0x03F and Register 0x040.

TEMPERATURE DIODE

The AD9684 contains a diode-based temperature sensor for measuring the temperature of the die. This diode can output a voltage and serve as a coarse temperature sensor to monitor the internal die temperature.

The temperature diode voltage can be output to the FD_A pin using the SPI. Use Register 0x028, Bit 0 to enable or disable the diode. Register 0x028 is a local register. Channel A must be selected in the device index register (Register 0x008) to enable the temperature diode readout. Configure the FD_A pin to output the diode voltage by programming Register 0x040, Bits[2:0]. See Table 29 for more information.

The voltage response of the temperature diode (with SPIVDD = 1.8 V) is shown in Figure 55.

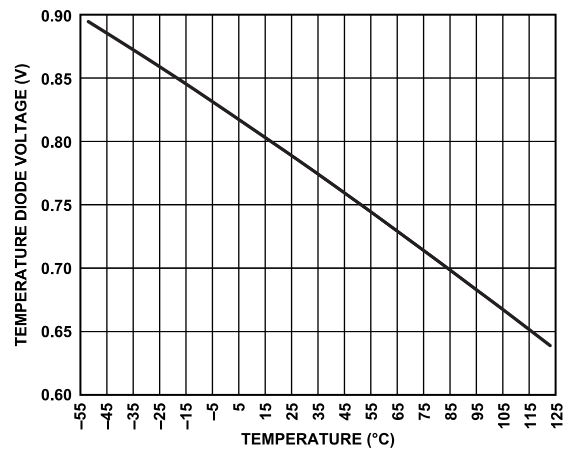


Figure 55. Diode Voltage vs. Temperature

ADC OVERRANGE AND FAST DETECT

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overrange pin outputs information on the state of the analog input. It is also helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs. In addition, because input signals can have significant slew rates, the latency of this function is of major concern. Highly pipelined converters can have significant latency. The AD9684 contains fast detect circuitry for individual channels to monitor the threshold and assert the FD_A and FD_B pins.

ADC OVERRANGE

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange indicator can be output on the STATUS± pins (when CSB > 0). The latency of this overrange indicator matches the sample latency.

The AD9684 also records any overrange condition in any of the four virtual converters. The overrange status of each virtual converter is registered as a sticky bit in Register 0x563. The contents of Register 0x563 can be cleared using Register 0x562, by toggling the bits corresponding to the virtual converter to set and reset the position.

FAST THRESHOLD DETECTION (FD_A AND FD_B)

The fast detect (FD) bit (enabled via the control bits in Register 0x559) is immediately set whenever the absolute value of the input signal exceeds the programmable upper threshold level. The FD bit is cleared only when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This feature provides hysteresis and prevents the FD bit from excessively toggling.

The operation of the upper threshold and lower threshold registers, along with the dwell time registers, is shown in Figure 56.

The FD_x indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, in Register 0x247 and Register 0x248. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 28 clock cycles (maximum). The approximate upper threshold magnitude is defined by

$$\textit{Upper Threshold Magnitude}\ (\text{dBFS}) = 20\log(\textit{Threshold Magnitude}/2^{13}) \quad (3)$$

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, in Register 0x249 and Register 0x24A. The fast detect lower threshold register is a 13-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency, but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

$$\textit{Lower Threshold Magnitude}\ (\text{dBFS}) = 20\log(\textit{Threshold Magnitude}/2^{13}) \quad (4)$$

For example, to set an upper threshold of −6 dBFS, write 0xFFF to Register 0x247 and Register 0x248. To set a lower threshold of −10 dBFS, write 0xA1D to Register 0x249 and Register 0x24A.

The dwell time can be programmed from 1 to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time registers, in Register 0x24B and Register 0x24C. See the Memory Map section (Register 0x040, and Register 0x245 to Register 0x24C in Table 29) for more details.

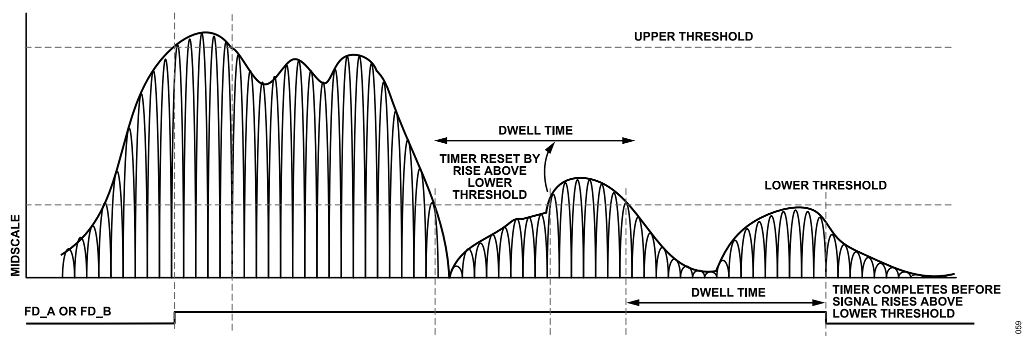


Figure 56. Threshold Settings for FD_A and FD_B Signals

SIGNAL MONITOR

The signal monitor block provides additional information about the signal being digitized by the ADC. The signal monitor computes the peak magnitude of the digitized signal. This information can be used to drive an AGC loop to optimize the range of the ADC in the presence of real-world signals.

The results of the signal monitor block can be obtained by reading back the internal values from the SPI port. A global, 24-bit programmable period controls the duration of the measurement. Figure 57 shows the simplified block diagram of the signal monitor block.

The peak detector captures the largest signal within the observation period. The detector only observes the magnitude of the signal. The resolution of the peak detector is a 13-bit value and the observation period is 24 bits and represents converter output samples.

Derive the peak magnitude using the following equation:

$$Peak\ Magnitude\ (\text{dBFS}) = 20\log(Peak\ Detector\ Value/2^{13}) \quad (5)$$

The magnitude of the input port signal is monitored over a programmable time period, which is determined by the signal monitor period register (SMPR). To enable the peak detector function, set Bit 1 of Register 0x270 in the signal monitor control register. The 24-bit SMPR must be programmed before activating this mode.

After enabling this mode, the value in the SMPR is loaded into a monitor period timer that decrements at the decimated clock rate. The magnitude of the input signal is compared with the value in the internal magnitude storage register (not accessible to the user), and the greater of the two is updated as the current peak level. The initial value of the magnitude storage register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 13-bit peak level value is transferred to the signal monitor holding register, which can be read through the memory map. The monitor period timer is reloaded with the value in the SMPR, and the countdown is restarted. In addition, the magnitude of the first input sample is updated in the magnitude storage register.

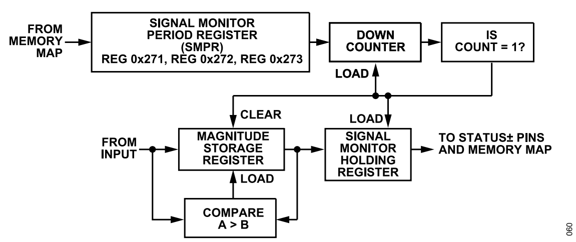


Figure 57. Signal Monitor Block

DIGITAL DOWNCONVERTERS (DDCS)

The AD9684 includes four digital downconverters that provide filtering and reduce the output data rate. This digital processing section includes an NCO, a half-band decimating filter, a finite impulse response (FIR) filter, a gain stage, and a complex to real conversion stage. Each of these processing blocks has a control line that allows the block to be independently enabled and disabled to provide the desired processing function. The DDCs can be configured to output either real data or complex output data.

DDC I/Q INPUT SELECTION

The AD9684 has two ADC channels and four DDC channels. Each DDC channel has two input ports that can be paired to support both real and complex inputs through the I/Q crossbar mux. For real signals, both DDC input ports must select the same ADC channel (that is, DDC Input Port I = ADC Channel A and DDC Input Port Q = ADC Channel A). For complex signals, each DDC input port must select different ADC channels (that is, DDC Input Port I = ADC Channel A and DDC Input Port Q = ADC Channel B).

The inputs to each DDC are controlled by the DDC input selection registers (Register 0x311, Register 0x331, Register 0x351, and Register 0x371). See Table 29 for information on how to configure the DDCs.

DDC I/Q OUTPUT SELECTION

Each DDC channel has two output ports that can be paired to support both real or complex outputs. For real output signals, only the DDC Output Port I is used (the DDC Output Port Q is invalid). For complex I/Q output signals, both DDC Output Port I and DDC Output Port Q are used.

The I/Q outputs to each DDC channel are controlled by the DDC complex to real enable bit in the DDC control registers (Bit 3 in Register 0x310, Register 0x330, Register 0x350, and Register 0x370).

The Chip I only bit in the chip application mode register (Register 0x200, Bit 5) controls the chip output muxing of all the DDC channels. When all DDC channels use real outputs, set this bit high to ignore all DDC Q output ports. When any of the DDC channels are set to use complex I/Q outputs, the user must clear this bit to use both DDC Output Port I and DDC Output Port Q.

DDC GENERAL DESCRIPTION

The four DDC blocks extract a portion of the full digital spectrum captured by the ADCs. They are intended for IF sampling or oversampled baseband radios requiring wide bandwidth input signals.

Each DDC block contains the following signal processing stages:

- Frequency translation stage (optional)
- Filtering stage
- Gain stage (optional)
- Complex to real conversion stage (optional)

Frequency Translation Stage (Optional)

This stage consists of a 12-bit complex NCO and quadrature mixers that can be used for frequency translation of both real or complex input signals. This stage shifts a portion of the available digital spectrum down to baseband.

Filtering Stage

After shifting down to baseband, this stage decimates the frequency spectrum using a chain of up to four half-band, low-pass filters for rate conversion. The decimation process lowers the output data rate, which, in turn, reduces the output interface rate.

Gain Stage (Optional)

Due to losses associated with mixing a real input signal down to baseband, this stage compensates by adding an additional 0 dB or 6 dB of gain.

Complex to Real Conversion Stage (Optional)

When real outputs are necessary, this stage converts the complex outputs back to real outputs by performing an $f_S/4$ mixing operation in addition to a filter to remove the complex component of the signal.

Figure 58 shows the detailed block diagram of the DDCs implemented in the AD9684.

DIGITAL DOWNCONVERTERS (DDCS)

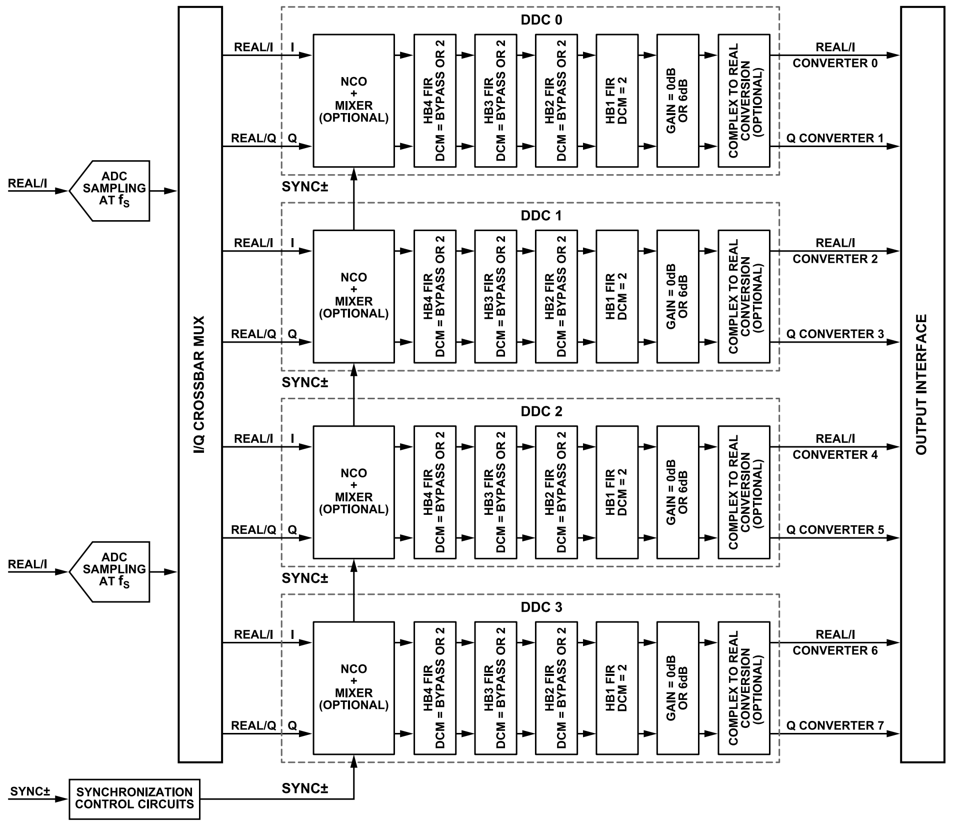


Figure 58. DDC Detailed Block Diagram

Figure 59 shows an example usage of one of the four DDC blocks with a real input signal and four half-band filters (HB4 + HB3 + HB2 + HB1). It shows both complex (decimate by 16) and real (decimate by 8) output options.

When DDCs have different decimation ratios, the chip decimation ratio (Register 0x201) must be set to the lowest decimation ratio for all the DDC blocks. In this scenario, samples of higher decimation ratio DDCs are repeated to match the chip decimation ratio sample rate. Whenever the NCO frequency is set or changed, the DDC soft reset must be issued. If the DDC soft reset is not issued, the output may potentially show amplitude variations.

Table 10 through Table 15 show the DDC samples when the chip decimation ratio is set to 1, 2, 4, 8, or 16, respectively. When DDCs have different decimation ratios, the chip decimation ratio must be set to the lowest decimation ratio of all the DDC channels. In this scenario, samples of higher decimation ratio DDCs are repeated to match the chip decimation ratio sample rate.

DIGITAL DOWNCONVERTERS (DDCS)

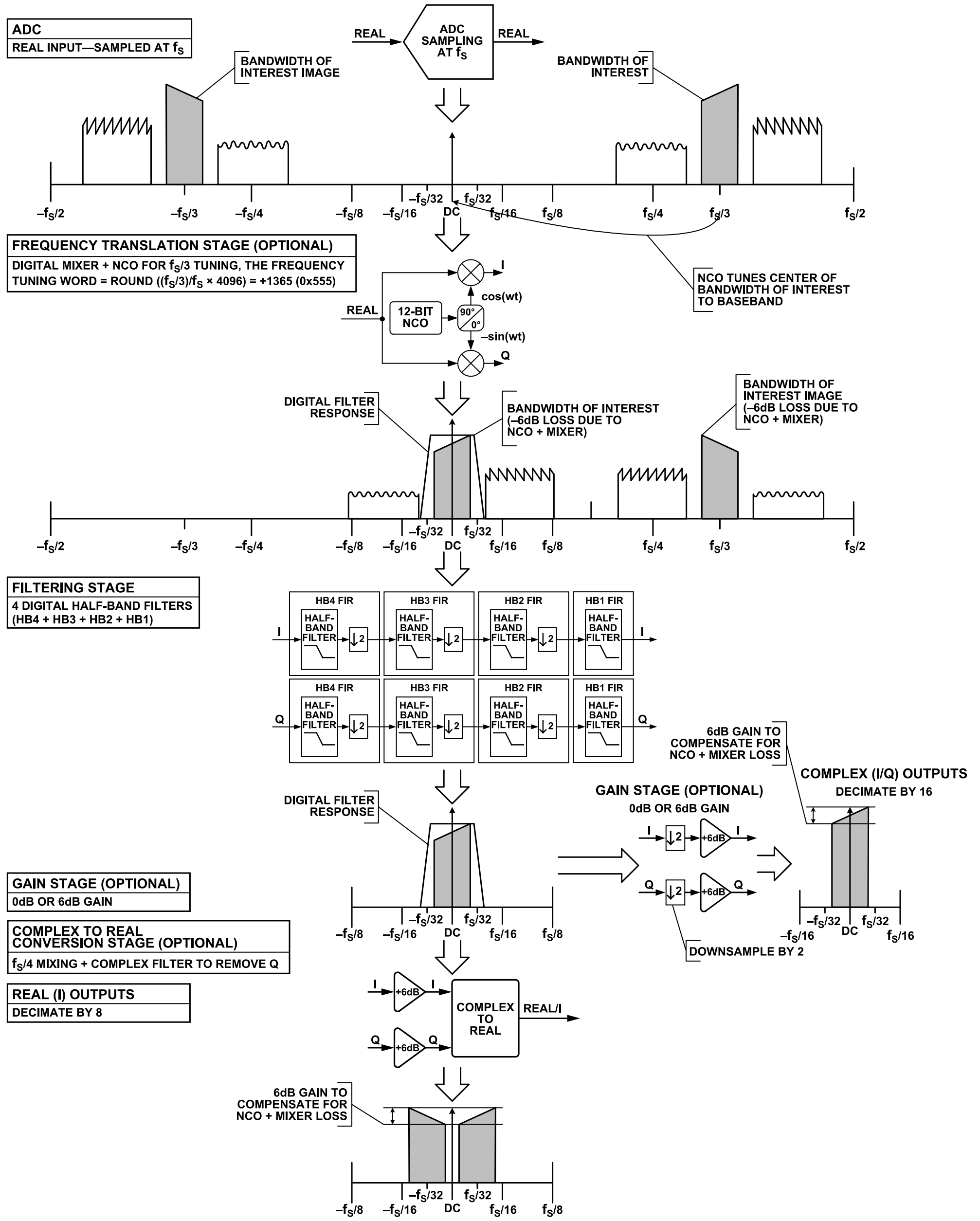


Figure 59. DDC Theory of Operation Example (Real Input, Decimate by 16)

Table 10. DDC Samples When the Chip Decimation Ratio = 1

Real (I) Output (Complex to Real Enabled)				Complex (I/Q) Outputs (Complex to Real Disabled)			
HB1 FIR (DCM[1] = 1)	HB2 FIR + HB1 FIR (DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB1 FIR (DCM[1] = 2)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N	N	N	N	N	N
N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1
N + 2	N	N	N	N	N	N	N
N + 3	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1
N + 4	N + 2	N	N	N + 2	N	N	N
N + 5	N + 3	N + 1	N + 1	N + 3	N + 1	N + 1	N + 1

DIGITAL DOWNCONVERTERS (DDCS)

Table 10. DDC Samples When the Chip Decimation Ratio = 1 (Continued)

Real (I) Output (Complex to Real Enabled)				Complex (I/Q) Outputs (Complex to Real Disabled)			
HB1 FIR (DCM[1] = 1)	HB2 FIR + HB1 FIR (DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB1 FIR (DCM[1] = 2)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N + 6	N + 2	N	N	N + 2	N	N	N
N + 7	N + 3	N + 1	N + 1	N + 3	N + 1	N + 1	N + 1
N + 8	N + 4	N + 2	N	N + 4	N + 2	N	N
N + 9	N + 5	N + 3	N + 1	N + 5	N + 3	N + 1	N + 1
N + 10	N + 4	N + 2	N	N + 4	N + 2	N	N
N + 11	N + 5	N + 3	N + 1	N + 5	N + 3	N + 1	N + 1
N + 12	N + 6	N + 2	N	N + 6	N + 2	N	N
N + 13	N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N + 1
N + 14	N + 6	N + 2	N	N + 6	N + 2	N	N
N + 15	N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N + 1
N + 16	N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N
N + 17	N + 9	N + 5	N + 3	N + 9	N + 5	N + 3	N + 1
N + 18	N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N
N + 19	N + 9	N + 5	N + 3	N + 9	N + 5	N + 3	N + 1
N + 20	N + 10	N + 4	N + 2	N + 10	N + 4	N + 2	N
N + 21	N + 11	N + 5	N + 3	N + 11	N + 5	N + 3	N + 1
N + 22	N + 10	N + 4	N + 2	N + 10	N + 4	N + 2	N
N + 23	N + 11	N + 5	N + 3	N + 11	N + 5	N + 3	N + 1
N + 24	N + 12	N + 6	N + 2	N + 12	N + 6	N + 2	N
N + 25	N + 13	N + 7	N + 3	N + 13	N + 7	N + 3	N + 1
N + 26	N + 12	N + 6	N + 2	N + 12	N + 6	N + 2	N
N + 27	N + 13	N + 7	N + 3	N + 13	N + 7	N + 3	N + 1
N + 28	N + 14	N + 6	N + 2	N + 14	N + 6	N + 2	N
N + 29	N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1
N + 30	N + 14	N + 6	N + 2	N + 14	N + 6	N + 2	N
N + 31	N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1

[1] DCM means decimation.

Table 11. DDC Samples When the Chip Decimation Ratio = 2

Real (I) Output (Complex to Real Enabled)			Complex (I/Q) Outputs (Complex to Real Disabled)			
HB2 FIR + HB1 FIR (DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB1 FIR (DCM[1] = 2)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N	N	N	N	N
N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1
N + 2	N	N	N + 2	N	N	N
N + 3	N + 1	N + 1	N + 3	N + 1	N + 1	N + 1
N + 4	N + 2	N	N + 4	N + 2	N	N
N + 5	N + 3	N + 1	N + 5	N + 3	N + 1	N + 1
N + 6	N + 2	N	N + 6	N + 2	N	N
N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N + 1
N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N
N + 9	N + 5	N + 3	N + 9	N + 5	N + 3	N + 1
N + 10	N + 4	N + 2	N + 10	N + 4	N + 2	N
N + 11	N + 5	N + 3	N + 11	N + 5	N + 3	N + 1

DIGITAL DOWNCONVERTERS (DDCS)

Table 11. DDC Samples When the Chip Decimation Ratio = 2 (Continued)

Real (I) Output (Complex to Real Enabled)			Complex (I/Q) Outputs (Complex to Real Disabled)			
HB2 FIR + HB1 FIR (DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB1 FIR (DCM[1] = 2)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N + 12	N + 6	N + 2	N + 12	N + 6	N + 2	N
N + 13	N + 7	N + 3	N + 13	N + 7	N + 3	N + 1
N + 14	N + 6	N + 2	N + 14	N + 6	N + 2	N
N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1

[1] DCM means decimation.

Table 12. DDC Samples When the Chip Decimation Ratio = 4

Real (I) Output (Complex to Real Enabled)		Complex (I/Q) Outputs (Complex to Real Disabled)		
HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N	N	N
N + 1	N + 1	N + 1	N + 1	N + 1
N + 2	N	N + 2	N	N
N + 3	N + 1	N + 3	N + 1	N + 1
N + 4	N + 2	N + 4	N + 2	N
N + 5	N + 3	N + 5	N + 3	N + 1
N + 6	N + 2	N + 6	N + 2	N
N + 7	N + 3	N + 7	N + 3	N + 1

[1] DCM means decimation.

Table 13. DDC Samples When the Chip Decimation Ratio = 8

Real (I) Output (Complex to Real Enabled)	Complex (I/Q) Outputs (Complex to Real Disabled)	
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N
N + 1	N + 1	N + 1
N + 2	N + 2	N
N + 3	N + 3	N + 1
N + 4	N + 4	N + 2
N + 5	N + 5	N + 3
N + 6	N + 6	N + 2
N + 7	N + 7	N + 3

[1] DCM means decimation.

Table 14. DDC Samples When the Chip Decimation Ratio = 16

Real (I) Output (Complex to Real Enabled)	Complex (I/Q) Outputs (Complex to Real Disabled)
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
Not applicable	N
Not applicable	N + 1
Not applicable	N + 2
Not applicable	N + 3

[1] DCM means decimation.

DIGITAL DOWNCONVERTERS (DDCS)

For example, if the chip decimation ratio is set to decimate by 4, DDC 0 is set to use HB2 + HB1 filters (complex outputs, decimate by 4) and DDC 1 is set to use HB4 + HB3 + HB2 + HB1 filters (real outputs, decimate by 8). DDC 1 repeats its output data two times for every one DDC 0 output. The resulting output samples are shown in Table 15.

Table 15. Chip Decimation Ratio = 4, DDC 0 Decimation = 4 (Complex), and DDC 1 Decimation = 8 (Real)

	DDC 0		DDC 1	
DDC Input Samples	Output Port I	Output Port Q	Output Port I	Output Port Q
N N + 1 N + 2 N + 3	I0 (N)	Q0 (N)	I1 (N)	Not applicable
N + 4 N + 5 N + 6 N + 7	I0 (N + 1)	Q0 (N + 1)	I1 (N + 1)	Not applicable
N + 8 N + 9 N + 10 N + 11	I0 (N + 2)	Q0 (N + 2)	I1 (N)	Not applicable
N + 12 N + 13 N + 14 N + 15	I0 (N + 3)	Q0 (N + 3)	I1 (N + 1)	Not applicable

FREQUENCY TRANSLATION

GENERAL DESCRIPTION

Frequency translation is accomplished using a 12-bit complex NCO with a digital quadrature mixer. The frequency translation translates either a real or complex input signal from an IF to a baseband complex digital output (carrier frequency = 0 Hz).

The frequency translation stage of each DDC can be controlled individually and supports four different IF modes using Bits[5:4] of the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370). These IF modes are

- Variable IF mode
- 0 Hz IF, or zero IF (ZIF), mode
- $f_S/4$ Hz IF mode
- Test mode

Variable IF Mode

The NCO and the mixers are enabled. The NCO output frequency can be used to digitally tune the IF frequency.

0 Hz IF (ZIF) Mode

The mixers are bypassed and the NCO is disabled.

$f_S/4$ Hz IF Mode

The mixers and the NCO are enabled in a special downmixing by $f_S/4$ mode to save power.

Test Mode

The input samples are forced to 0.999 × full scale to positive full scale. The NCO is enabled. This test mode allows the NCOs to drive the decimation filters directly.

Figure 60 and Figure 61 show examples of the frequency translation stage for both real and complex inputs.

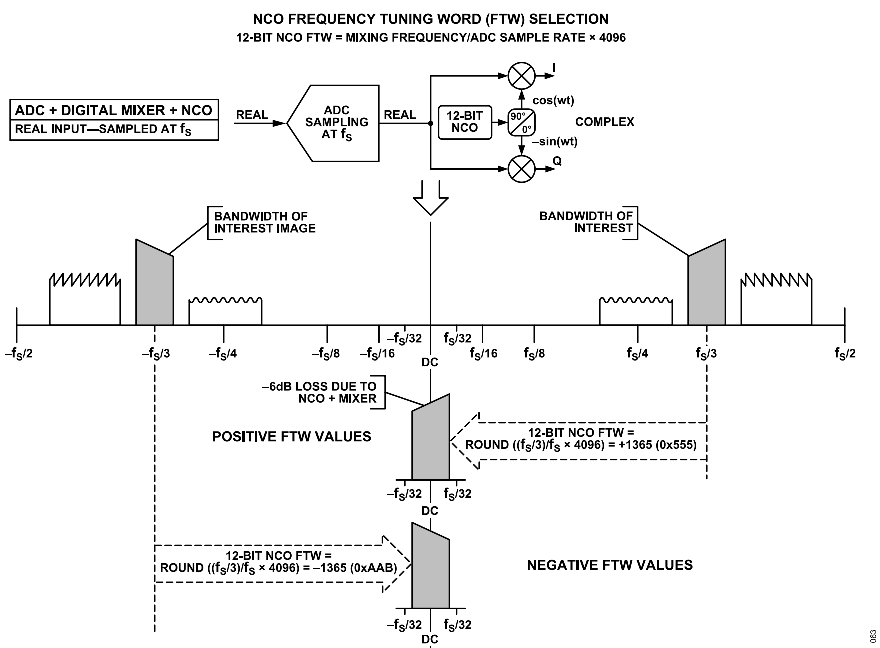


Figure 60. DDC NCO Frequency Tuning Word Selection—Real Inputs

FREQUENCY TRANSLATION

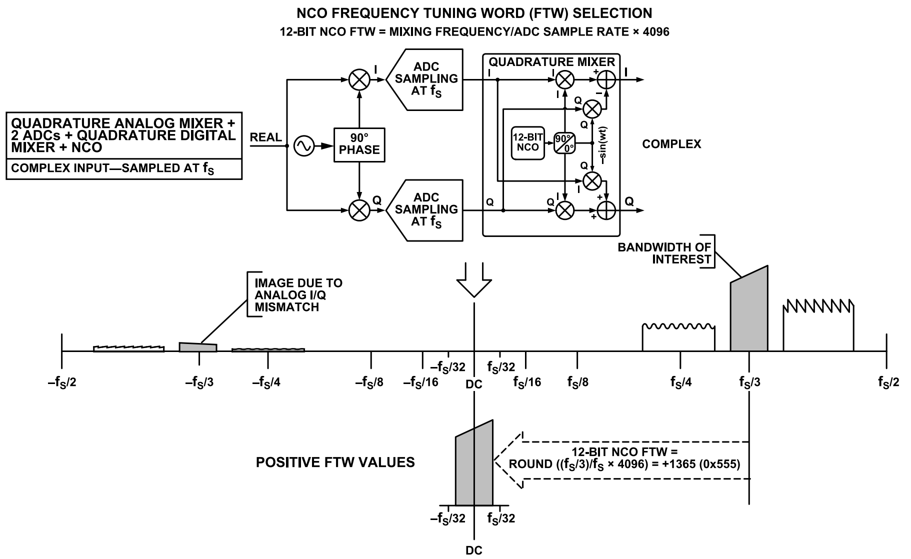


Figure 61. DDC NCO Frequency Tuning Word Selection—Complex Inputs

DDC NCO PLUS MIXER LOSS AND SFDR

When mixing a real input signal down to baseband, 6 dB of loss is introduced in the signal due to filtering of the negative image. The NCO introduces an additional 0.05 dB of loss. The total loss of a real input signal mixed down to baseband is 6.05 dB. For this reason, it is recommended to compensate for this loss by enabling the 6 dB of gain in the gain stage of the DDC to recenter the dynamic range of the signal within the full scale of the output bits.

When mixing a complex input signal down to baseband, the maximum value that each I/Q sample can reach is 1.414 × full scale after it passes through the complex mixer. To avoid an overrange of the I/Q samples and to keep the data bit-widths aligned with real mixing, introduce 3.06 dB of loss (0.707 × full-scale) in the mixer for complex signals. The NCO introduces an additional 0.05 dB of loss. The total loss of a complex input signal mixed down to baseband is −3.11 dB.

The worst case spurious signal from the NCO is greater than 102 dBc SFDR for all output frequencies.

NUMERICALLY CONTROLLED OSCILLATOR

The AD9684 has a 12-bit NCO for each DDC that enables the frequency translation process. The NCO allows the input spectrum to be tuned to dc, where it can be effectively filtered by the subsequent filter blocks to prevent aliasing. The NCO can be set up by providing a frequency tuning word (FTW) and a phase offset word (POW).

Setting Up the NCO FTW and POW

The NCO frequency value is given by the 12-bit, twos complement number entered in the NCO FTW. Frequencies between $\pm f_S/2$ ($+f_S/2$ excluded) are represented using the following frequency words:

- 0x800 represents a frequency of $-f_S/2$.
- 0x000 represents dc (frequency is 0 Hz).
- 0x7FF represents a frequency of $+f_S/2 - f_S/2^{12}$.

Calculate the NCO frequency tuning word using the following equation:

$$NCO\_FTW = round\left(2^{12}\frac{mod(f_C, f_S)}{f_S}\right) \quad (6)$$

where:
NCO_FTW is a 12-bit, twos complement number representing the NCO FTW.
f_C is the desired carrier frequency in Hz.
f_S is the AD9684 sampling frequency (clock rate) in Hz. mod( ) is a remainder function. For example, mod(110,100) = 10, and for negative numbers, mod(−32, +10) = −2. round( ) is a rounding function. For example, round(3.6) = 4, and for negative numbers, round(−3.4) = −3.

Note that this equation applies to the aliasing of signals in the digital domain (that is, aliasing introduced when digitizing analog signals).

For example, if the ADC sampling frequency (f_S) is 1250 MSPS and the carrier frequency (f_C) is 416.667 MHz,

$$NCO\_FTW = round\left(2^{12}\frac{mod(416.667, 1250)}{1250}\right) = 1365 \text{ MHz} \quad (7)$$

This, in turn, converts to 0x555 in the 12-bit, twos complement representation for NCO_FTW. Calculate the actual carrier frequency based on the following equation:

$$f_{C\_ACTUAL} = \frac{NCO\_FTW \times f_S}{2^{12}} = 416.56 \text{ MHz} \quad (8)$$

FREQUENCY TRANSLATION

A 12-bit POW is available for each NCO to create a known phase relationship between multiple AD9684 chips or individual DDC channels inside one AD9684 chip.

The following procedure must be followed to update the FTW and/or POW registers to ensure proper operation of the NCO:

1. Write to the FTW registers for all the DDCs.
2. Write to the POW registers for all the DDCs.
3. Synchronize the NCOs either through the DDC soft reset bit, accessible through the SPI, or through the assertion of the SYNC± pins.

Note that the NCOs must be synchronized either through the SPI or through the SYNC± pins after all writes to the FTW or POW registers are complete. This synchronization is necessary to ensure the proper operation of the NCO.

NCO Synchronization

Each NCO contains a separate phase accumulator word (PAW) that determines the instantaneous phase of the NCO. The initial reset value of each PAW is determined by the POW, described in the Setting Up the NCO FTW and POW section. The phase increment value of each PAW is determined by the FTW.

Use the following two methods to synchronize multiple PAWs within the chip:

- Using the SPI. Use the DDC NCO soft reset bit in the DDC synchronization control register (Register 0x300, Bit 4) to reset all the PAWs in the chip. This is accomplished by toggling the DDC NCO soft reset bit. Note that this method synchronizes DDC channels within the same AD9684 chip only.
- Using the SYNC± pins. When the SYNC± pins are enabled in the SYNC± control registers (Register 0x120 and Register 0x121), and the DDC synchronization is enabled in Bits[1:0] in the DDC synchronization control register (Register 0x300), any subsequent SYNC± event resets all the PAWs in the chip. Note that this method synchronizes DDC channels within the same AD9684 chip or DDC channels within separate AD9684 chips.

Mixer

The NCO is accompanied by a mixer, which operates similarly to an analog quadrature mixer. It performs the downconversion of input signals (real or complex) by using the NCO frequency as a local oscillator. For real input signals, this mixer performs a real mixer operation with two multipliers. For complex input signals, the mixer performs a complex mixer operation with four multipliers and two adders. The mixer adjusts its operation based on the input signal (real or complex) provided to each individual channel. The selection of real or complex inputs can be controlled individually for each DDC block using Bit 7 of the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370).

FIR FILTERS

GENERAL DESCRIPTION

There are four sets of decimate by 2, low-pass, half-band, FIR filters (labeled HB1 FIR, HB2 FIR, HB3 FIR, and HB4 FIR in Figure 58) following the frequency translation stage. After the carrier of interest is tuned down to dc (carrier frequency = 0 Hz), these filters efficiently lower the sample rate while providing sufficient alias rejection from unwanted adjacent carriers around the bandwidth of interest.

HB1 FIR is always enabled and cannot be bypassed. The HB2, HB3, and HB4 FIR filters are optional and can be bypassed for higher output sample rates.

Table 16 shows the different bandwidth options by including different half-band filters. In all cases, the DDC filtering stage of the AD9684 provides less than −0.001 dB of pass-band ripple and greater than 100 dB of stop band alias rejection.

Table 17 shows the amount of stop band alias rejection for multiple pass-band ripple/cutoff points. The decimation ratio of the filtering stage of each DDC can be controlled individually through Bits[1:0] of the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370).

Table 16. DDC Filter Characteristics

ADC Sample Rate (MSPS)	DDC Decimation Ratio	Real Output Sample Rate (MSPS)	Complex (I/Q) Output Sample Rate (MSPS)	Alias Protected Bandwidth (MHz)	Ideal SNR Improvement[1] (dB)	Pass-Band Ripple (dB)	Alias Rejection (dB)
500	2 (HB1)	500	250 (I) + 250 (Q)	192.5	1	<−0.001	>100
	4 (HB1 + HB2)	250	125 (I) + 125 (Q)	96.3	4		
	8 (HB1 + HB2 + HB3)	125	62.5 (I) + 62.5 (Q)	48.1	7		
	16 (HB1 + HB2 + HB3 + HB4)	62.5	31.25 (I) + 31.25 (Q)	24.1	10		

[1] The ideal SNR improvement due to oversampling and filtering = 10log(bandwidth/(f_S/2)).

Table 17. DDC Filter Alias Rejection

Alias Rejection (dB)	Pass-Band Ripple/Cutoff Point (dB)	Alias Protected Bandwidth for Real (I) Outputs[1]	Alias Protected Bandwidth for Complex (I/Q) Outputs[1]
>100	<−0.001	<38.5% × f_{OUT}	<77% × f_{OUT}
90	<−0.001	<38.7% × f_{OUT}	<77.4% × f_{OUT}
85	<−0.001	<38.9% × f_{OUT}	<77.8% × f_{OUT}
63.3	<−0.006	<40% × f_{OUT}	<80% × f_{OUT}
25	−0.5	44.4% × f_{OUT}	88.8% × f_{OUT}
19.3	−1.0	45.6% × f_{OUT}	91.2% × f_{OUT}
10.7	−3.0	48% × f_{OUT}	96% × f_{OUT}

[1] f_{OUT} = ADC input sample rate/DDC decimation ratio.

FIR FILTERS

HALF-BAND FILTERS

The AD9684 offers four half-band filters to enable digital signal processing of the ADC converted data. These half-band filters are bypassable and can be individually selected.

HB4 Filter

The first decimate by 2, half-band, low-pass FIR filter (HB4) uses an 15-bit, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB4 filter is used only when complex outputs (decimate by 16) or real outputs (decimate by 8) are enabled; otherwise, the filter is bypassed. Table 18 and Figure 62 show the coefficients and response of the HB4 filter.

Table 18. HB4 Filter Coefficients

HB4 Coefficient Number	Decimal Coefficient (15-Bit)
C1, C11	99
C2, C10	0
C3, C9	−808
C4, C8	0
C5, C7	4805
C6	8192

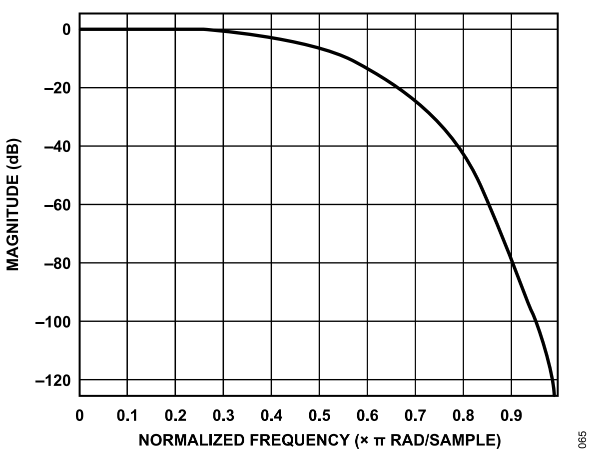


Figure 62. HB4 Filter Response

HB3 Filter

The second decimate by 2, half-band, low-pass, FIR filter (HB3) uses an 18-bit, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB3 filter is only used when complex outputs (decimate by 8 or 16) or real outputs (decimate by 4 or 8) are enabled; otherwise, the filter is bypassed. Table 19 and Figure 63 show the coefficients and response of the HB3 filter.

Table 19. HB3 Filter Coefficients

HB3 Coefficient Number	Decimal Coefficient (18-Bit)
C1, C11	859
C2, C10	0
C3, C9	−6661
C4, C8	0
C5, C7	38570
C6	65536

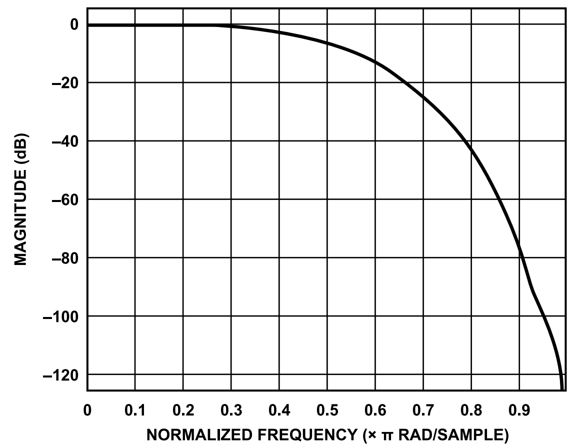


Figure 63. HB3 Filter Response

HB2 Filter

The third decimate by 2, half-band, low-pass FIR filter (HB2) uses a 19-bit, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB2 filter is only used when complex outputs (decimate by 4, 8, or 16) or real outputs (decimate by 2, 4, or 8) are enabled; otherwise, the filter is bypassed.

Table 20 and Figure 64 show the coefficients and response of the HB2 filter.

Table 20. HB2 Filter Coefficients

HB2 Coefficient Number	Decimal Coefficient (19-Bit)
C1, C19	161
C2, C18	0
C3, C17	−1328
C4, C16	0
C5, C15	5814
C6, C14	0
C7, C13	−19272
C8, C12	0
C9, C11	80,160
C10	131,072

FIR FILTERS

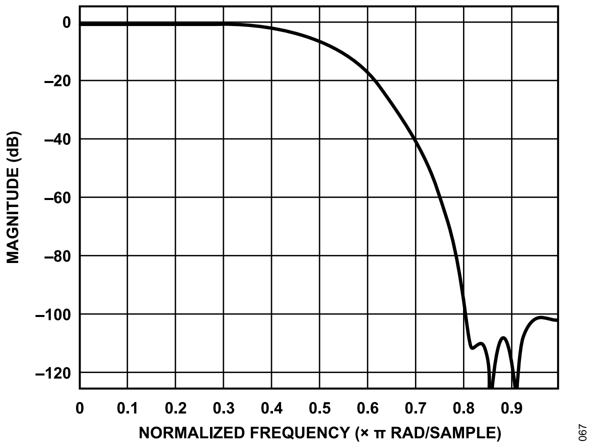


Figure 64. HB2 Filter Response

HB1 Filter

The fourth and final decimate by 2, half-band, low-pass FIR filter (HB1) uses a 21-bit, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB1 filter is always enabled and cannot be bypassed. Table 21 and Figure 65 show the coefficients and response of the HB1 filter.

Table 21. HB1 Filter Coefficients

HB1 Coefficient Number	Decimal Coefficient (21-Bit)
C1, C55	−24
C2, C54	0
C3, C53	102
C4, C52	0
C5, C51	−302
C6, C50	0
C7, C49	730
C8, C48	0
C9, C47	−1544
C10, C46	0
C11, C45	2964
C12, C44	0
C13, C43	−5284
C14, C42	0
C15, C41	8903
C16, C40	0
C17, C39	−14,383
C18, C38	0
C19, C37	22,640
C20, C36	0
C21, C35	−35,476
C22, C34	0
C23, C33	57,468
C24, C32	0

Table 21. HB1 Filter Coefficients (Continued)

HB1 Coefficient Number	Decimal Coefficient (21-Bit)
C25, C31	−105,442
C26, C30	0
C27, C29	331,792
C28	524,288

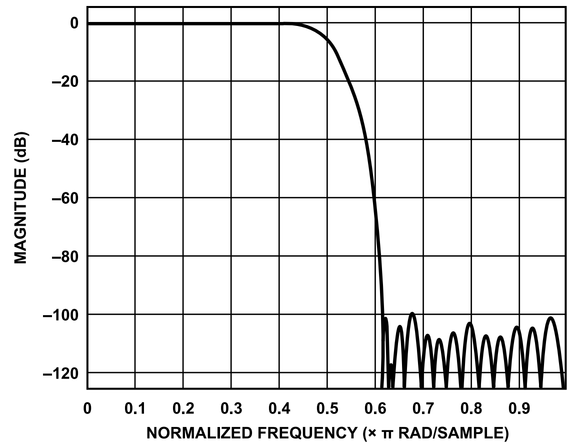


Figure 65. HB1 Filter Response

DDC GAIN STAGE

Each DDC contains an independently controlled gain stage. The gain is selectable as either 0 dB or 6 dB. When mixing a real input signal down to baseband, it is recommended to enable the 6 dB gain to recenter the dynamic range of the signal within the full scale of the output bits.

When mixing a complex input signal down to baseband, the mixer has already recentered the dynamic range of the signal within the full scale of the output bits and no additional gain is necessary. However, the optional 6 dB gain compensates for low signal strengths. The downsample by 2 portion of the HB1 FIR filter is bypassed when using the complex to real conversion stage (see Figure 66).

DDC COMPLEX TO REAL CONVERSION BLOCK

Each DDC contains an independently controlled complex to real conversion block. The complex to real conversion block reuses the last filter (HB1 FIR) in the filtering stage, along with an $f_S/4$ complex mixer to upconvert the signal.

After upconverting the signal, the Q portion of the complex mixer is no longer needed and is dropped.

Figure 66 shows a simplified block diagram of the complex to real conversion.

FIR FILTERS

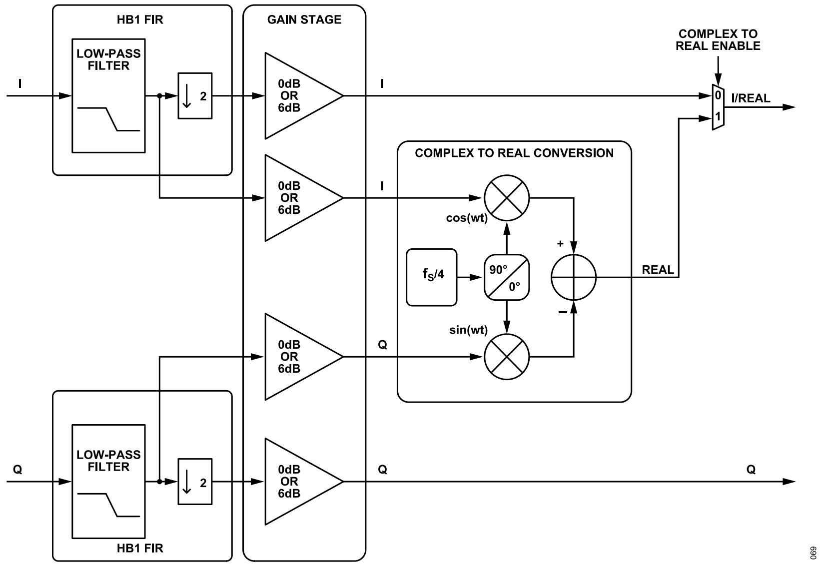


Figure 66. Complex to Real Conversion Block

DDC EXAMPLE CONFIGURATIONS

Table 22 describes the register settings for multiple DDC example configurations.

Table 22. DDC Example Configurations

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	Number of Virtual Converters Required (M)	Register Settings[2]
One DDC	2	Complex	Complex	77% × f_S	2	Register 0x200 = 0x01 (one DDC, I/Q selected) Register 0x201 = 0x01 (chip decimate by 2) Register 0x310 = 0x83 (complex mixer, 0 dB gain, variable IF, complex outputs, HB1 filter) Register 0x311 = 0x04 (DDC I input = ADC Channel A, DDC Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0
Two DDCs	4	Complex	Complex	38.5% × f_S	4	Register 0x200 = 0x02 (two DDCs, I/Q selected) Register 0x201 = 0x02 (chip decimate by 4) Register 0x310, Register 0x330 = 0x80 (complex mixer, 0 dB gain, variable IF, complex outputs, HB2 + HB1 filters) Register 0x311, Register 0x331 = 0x04 (DDC I input = ADC Channel A, DDC Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Complex	Real	19.25% × f_S	2	Register 0x200 = 0x22 (two DDCs, Q ignore selected) Register 0x201 = 0x02 (chip decimate by 4)

FIR FILTERS

Table 22. DDC Example Configurations (Continued)

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	Number of Virtual Converters Required (M)	Register Settings[2]
						Register 0x310, Register 0x330 = 0x89 (complex mixer, 0 dB gain, variable IF, real output, HB3 + HB2 + HB1 filters) Register 0x311, Register 0x331 = 0x04 (DDC I input = ADC Channel A, DDC Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Real	Real	19.25% × f_S	2	Register 0x200 = 0x22 (two DDCs, Q ignore selected) Register 0x201 = 0x02 (chip decimate by 4) Register 0x310, Register 0x330 = 0x49 (real mixer, 6 dB gain, variable IF, real output, HB3 + HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x05 (DDC 1 I input = ADC Channel B, DDC 1 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Real	Complex	38.5% × f_S	4	Register 0x200 = 0x02 (two DDCs, I/Q selected) Register 0x201 = 0x02 (chip decimate by 4) Register 0x310, Register 0x330 = 0x40 (real mixer, 6 dB gain, variable IF, complex output, HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x05 (DDC 1 I input = ADC Channel B, DDC 1 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Four DDCs	8	Real	Complex	19.25% × f_S	8	Register 0x200 = 0x03 (four DDCs, I/Q selected) Register 0x201 = 0x03 (chip decimate by 8) Register 0x310, Register 0x330, Register 0x350, Register 0x370 = 0x41 (real mixer, 6 dB gain, variable IF, complex output, HB3 + HB2 + HB1 filters)

FIR FILTERS

Table 22. DDC Example Configurations (Continued)

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	Number of Virtual Converters Required (M)	Register Settings[2]
						Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x00 (DDC 1 I input = ADC Channel A, DDC 1 Q input = ADC Channel A) Register 0x351 = 0x05 (DDC 2 I input = ADC Channel B, DDC 2 Q input = ADC Channel B) Register 0x371 = 0x05 (DDC 3 I input = ADC Channel B, DDC 3 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1 Register 0x354, Register 0x355, Register 0x360, Register 0x361 = FTW and POW set as required by application for DDC 2 Register 0x374, Register 0x375, Register 0x380, Register 0x381 = FTW and POW set as required by application for DDC 3
Four DDCs	16	Real	Complex	9.625% × f_S	8	Register 0x200 = 0x03 (four DDCs, I/Q selected) Register 0x201 = 0x04 (chip decimate by 16) Register 0x310, Register 0x330, Register 0x350, Register 0x370 = 0x42 (real mixer, 6 dB gain, variable IF, complex output, HB4 + HB3 + HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x00 (DDC 1 I input = ADC Channel A, DDC 1 Q input = ADC Channel A) Register 0x351 = 0x05 (DDC 2 I input = ADC Channel B, DDC 2 Q input = ADC Channel B) Register 0x371 = 0x05 (DDC 3 I input = ADC Channel B, DDC 3 Q input = ADC Channel B) Register 0x314, 0x315, 0x320, 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1 Register 0x354, Register 0x355, Register 0x360, Register 0x361 = FTW and POW set as required by application for DDC 2 Register 0x374, Register 0x375, Register 0x380, Register 0x381 = FTW and POW set as required by application for DDC 3

1 f_S is the ADC sample rate. Bandwidths listed are <−0.001 dB of pass-band ripple and >100 dB of stop band alias rejection.

2 The NCOs must be synchronized either through the SPI or through the SYNC± pins after all writes to the FTW or POW registers are complete. This ensures the proper operation of the NCO. See the NCO Synchronization section for more information.

DIGITAL OUTPUTS

DIGITAL OUTPUTS

The AD9684 output drivers are for standard ANSI LVDS, but optionally the drive current can be reduced using Register 0x56A. The reduced drive current for the LVDS outputs potentially reduces the digitally induced noise.

As detailed in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, the data format can be selected for offset binary, twos complement, or gray code when using the SPI control.

The AD9684 has a flexible three-state ability for the digital output pins. The three-state mode is enabled when the device is set for power-down mode.

As shown in Table 24, the function of the output pins changes based upon the selection of either parallel or byte output mode in Register 0x568.

Timing

The AD9684 provides latched data with a pipeline delay of 33 input sample clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

Minimize the length of the output data lines and the corresponding loads to reduce transients within the AD9684. These transients can degrade converter dynamic performance.

The lowest typical conversion rate of the AD9684 is 250 MSPS. At clock rates below 250 MSPS, dynamic performance may degrade.

Data Clock Output

The AD9684 also provides a data clock output (DCO) intended for capturing the data in an external register. The DCO relative to the data output can be adjusted using Register 0x569.

ADC OVERRANGE

The ADC overrange (OR) indicator is asserted when an overrange is detected on the input of the ADC. The overrange condition is determined at the output of the ADC pipeline and, therefore, is subject to a latency of 28 ADC clocks. An overrange at the input is indicated by the OR bit 28 clock cycles after it occurs.

Table 23. LVDS Output Configurations

Parallel Output Mode	Number of Virtual Converters Supported	Virtual Converter Resolution (Max)	LVDS Byte Mode Outputs Required
Parallel Interleaved, Two Converters (0x1)	2	14-bit	DCO + STATUS + D[13:0]
Parallel Channel Multiplexed, Two Converters (0x3)	2	14-bit	DCO + STATUS + D[13:7] = Channel AD[6:0] = Channel B
Byte Mode, Two Converters (0x5)	2	16-bit	1 DCO + 1 STATUS + 8 DATA[7:0]
Byte Mode, Four Converters (0x6)	4	16-bit	1 DCO + 1 STATUS + 8 DATA[7:0]
Byte Mode, Eight Converters (0x7)	8	16-bit	1 DCO + 1 STATUS + 8 DATA[7:0]

Table 24. Pin Mapping Between LVDS Parallel/Byte Modes

Pin Name	LVDS Parallel Mode Output	LVDS Byte Mode Output
DCO−, DCO+	DCO−, DCO+	DCO−, DCO+
STATUS−, STATUS+	OVR−, OVR+	FCO−, FCO+
D13−, D13+	D13−, D13+	STATUS−, STATUS+
D12−, D12+	D12−, D12+	DATA7−, DATA7+
D11−, D11+	D11−, D11+	DATA6−, DATA6+
D10−, D10+	D10−, D10+	DATA5−, DATA5+
D9−, D9+	D9−, D9+	DATA4−, DATA4+
D8−, D8+	D8−, D8+	DATA3−, DATA3+
D7−, D7+	D7−, D7+	DATA2−, DATA2+
D6−, D6+	D6−, D6+	DATA1−, DATA1+
D5−, D5+	D5−, D5+	DATA0−, DATA0+
D4−, D4+	D4−, D4+	Not applicable
D3−, D3+	D3−, D3+	Not applicable
D2−, D2+	D2−, D2+	Not applicable
D1−, D1+	D1−, D1+	Not applicable
D0−, D0+	D0−, D0+	Not applicable

MULTICHIP SYNCHRONIZATION

The AD9684 has a SYNC± input that allows the user flexible options for synchronizing the internal blocks. The SYNC± input is a source synchronous system reference signal that enables multichip synchronization. The input clock divider, DDCs, and signal monitor block LVDS output link can be synchronized using the SYNC± input. For the highest level of timing accuracy, SYNC± must meet the setup and hold requirements relative to the CLK± input.

The flowchart in Figure 67 shows the internal mechanism by which multichip synchronization can be achieved in the AD9684.

The AD9684 supports several features that aid users in meeting the requirements for capturing SYNC± signals. The SYNC± sample event can be defined as either a synchronous low to high transition or a synchronous high to low transition. Additionally, the AD9684 allows the SYNC± signal to be sampled using either the rising edge or the falling edge of the CLK± input. The AD9684 can also to ignore a programmable number (up to 16) of SYNC± events. The SYNC± control options can be selected using Register 0x120 and Register 0x121.

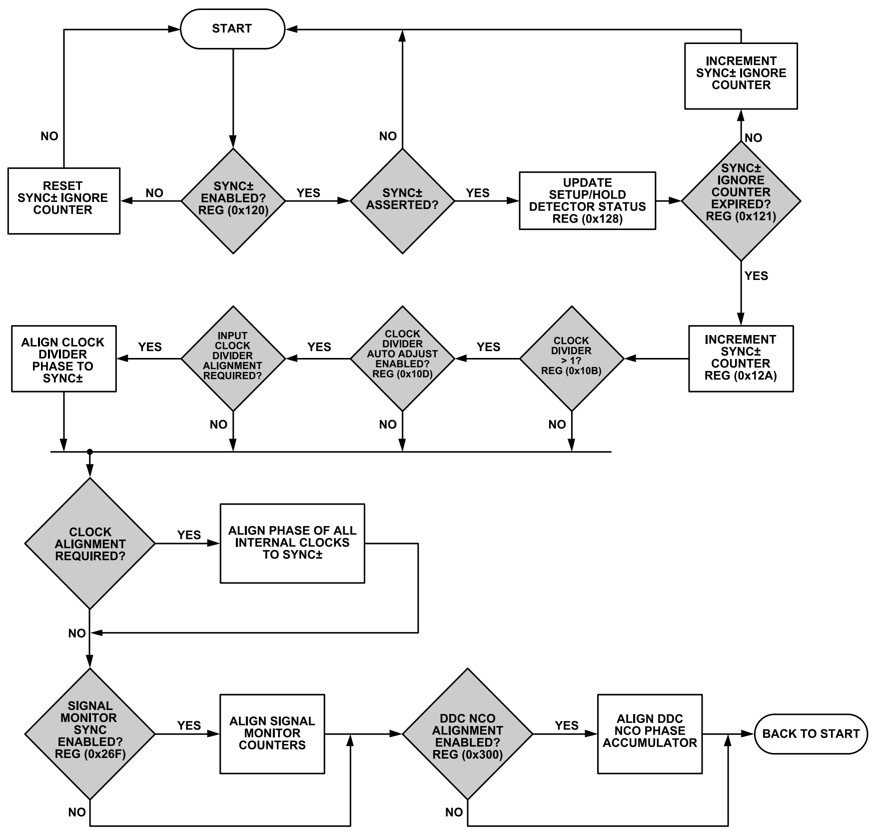


Figure 67. Multichip Synchronization

MULTICHIP SYNCHRONIZATION

SYNC± SETUP AND HOLD WINDOW MONITOR

To assist in ensuring a valid SYNC± capture, the AD9684 has a SYNC± setup and hold window monitor. This feature allows the system designer to determine the location of the SYNC± signals relative to the CLK± signals by reading back the amount of setup and hold margin on the interface through the memory map. Figure 68 and Figure 69 show the setup and hold status values for different phases of SYNC±.

The setup detector returns the status of the SYNC± signal before the CLK± edge and the hold detector returns the status of the SYNC± signal after the CLK± edge. Register 0x128 stores the status of SYNC± and alerts the user if the SYNC± signal is captured by the ADC.

Table 25 describes the contents of Register 0x128 and how to interpret those contents.

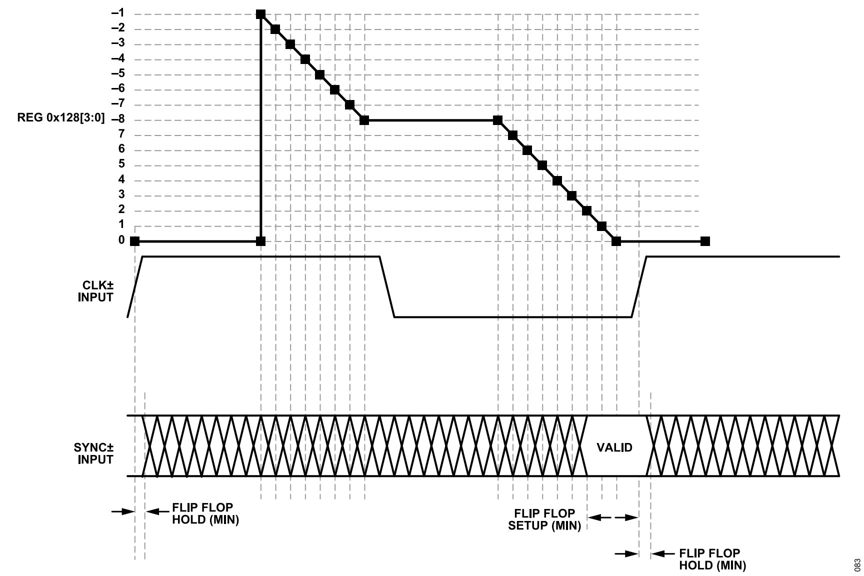


Figure 68. SYNC Setup Detector

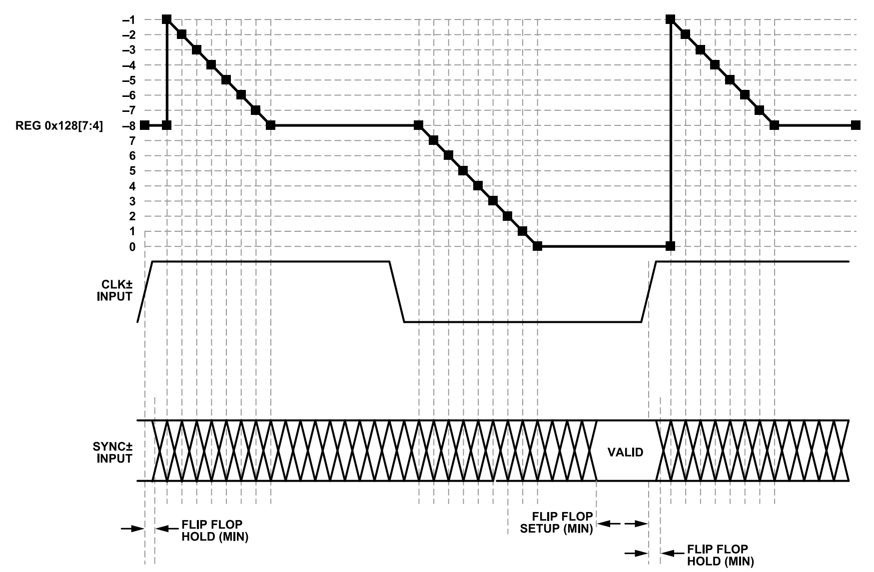


Figure 69. SYNC± Hold Detector

MULTICHIP SYNCHRONIZATION

Table 25. SYNC± Setup and Hold Monitor Register 0x128

Register 0x128, Bits[7:4], Hold Status	Register 0x128, Bits[3:0], Setup Status	Description
0x0	0x0 to 0x7	Possible setup error; the smaller this number, the smaller the setup margin
0x0 to 0x8	0x8	No setup or hold error (best hold margin)
0x8	0x9 to 0xF	No setup or hold error (best setup and hold margin)
0x8	0x0	No setup or hold error (best setup margin)
0x9 to 0xF	0x0	Possible hold error; the larger this number, the smaller the hold margin
0x0	0x0	Possible setup or hold error

TEST MODES

ADC TEST MODES

The AD9684 has various test options that aid in the system level implementation. The AD9684 has ADC test modes that are available in Register 0x550. These test modes are described in Table 26. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The pseudorandom number (PN) generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x550. These tests can be performed with or without an analog signal (if present, the analog signal is ignored); however, they do require an encode clock. For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Table 26. ADC Test Modes

Output Test Mode Bit Sequence	Pattern Name	Expression	Default/Seed Value	Sample (N, N + 1, N + 2, …)
0000	Off (default)	Not applicable	Not applicable	Not applicable
0001	Midscale short	00 0000 0000 0000	Not applicable	Not applicable
0010	+Full-scale short	01 1111 1111 1111	Not applicable	Not applicable
0011	−Full-scale short	10 0000 0000 0000	Not applicable	Not applicable
0100	Checkerboard	10 1010 1010 1010	Not applicable	0x1555, 0x2AAA, 0x1555, 0x2AAA, 0x1555
0101	PN sequence long	$x^{23} + x^{18} + 1$	0x3AFF	0x3FD7, 0x0002, 0x26E0, 0x0A3D, 0x1CA6
0110	PN sequence short	$x^9 + x^5 + 1$	0x0092	0x125B, 0x3C9A, 0x2660, 0x0c65, 0x0697
0111	One-/zero-word toggle	11 1111 1111 1111	Not applicable	0x0000, 0x3FFF, 0x0000, 0x3FFF, 0x0000
1000	User input	Register 0x551 to Register 0x558	Not applicable	For repeat mode: User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], User Pattern 1[15:2]… For single mode: User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], 0x0000…
1111	Ramp output	(x) % 2^{16}	Not applicable	(x) % 2^{14}x 4, $(x + 1)$ % 2^{14}x 4, $(x + 2)$ % 2^{14}x 4, $(x + 3)$ % 2^{14}x 4, ...

SERIAL PORT INTERFACE (SPI)

The AD9684 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the serial port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the Serial Control Interface Standard (Rev. 0).

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 27). The SCLK (serial clock) pin synchronizes the read and write data presented from/to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 27. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input, which synchronizes the serial interface reads and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. See Figure 3 and Table 5 for an example of the serial timing and its definitions.

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB pin can stall high between bytes to allow additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any secondary functions of the SPI pins.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This bit allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default configuration on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the Serial Control Interface Standard (Rev. 0).

HARDWARE INTERFACE

The pins described in Table 27 compose the physical interface between the user programming device and the serial port of the AD9684. The SCLK pin and the CSB pin function as inputs when using the SPI. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI is flexible enough to be controlled by either field programmable gate arrays (FPGAs) or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9684 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 28 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the Serial Control Interface Standard (Rev. 0). The AD9684 device specific features are described in the Memory Map section.

Table 28. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the clock divider via the SPI
DDC	Allows the user to set up the decimation filters for different applications
Test Input/Output	Allows the user to set the test modes to have known data on the output bits
Output Mode	Allows the user to set up outputs

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is divided into four sections: the Analog Devices, Inc., SPI registers (Register 0x000 to Register 0x00D), the ADC function registers (Register 0x015 to Register 0x278), The DDC function registers (Register 0x300 to Register 0x387), and the digital outputs and test modes registers (Register 0x550 to Register 0x05B).

Table 29 documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x561, the output mode register, has a hexadecimal default value of 0x01. This means that Bit 0 = 1, and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see the Table 29.

Unassigned and Reserved Locations

All address and bit locations that are not included in Table 29 are not currently supported for this device. Write unused bits of a valid address location with 0s unless the default value is set otherwise. Writing to these locations is required only when part of an address location is unassigned (for example, Address 0x561). If the entire address location is open (for example, Address 0x013), do not write to this address location.

Default Values

After the AD9684 is reset, critical registers are loaded with default values. The default values for the registers are given in Table 29.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."
- "X" denotes a "don't care" bit.

Channel-Specific Registers

Some channel setup functions, such as the input termination (Register 0x016), can be programmed to a different value for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 29 as local. These local registers and bits can be accessed by setting the appropriate Channel A or Channel B bits in Register 0x008. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, set only Channel A or Channel B to read one of the two registers. If both bits are set during an SPI read cycle, the device returns the value for Channel A. Registers and bits designated as global in Table 29 affect the entire device and the channel features for which independent settings are not allowed between channels. The settings in Register 0x005 do not affect the global registers and bits.

SPI Soft Reset

After issuing a soft reset by programming 0x81 to Register 0x000, the AD9684 requires 5 ms to recover. Therefore, when programming the AD9684 for application setup, ensure that an adequate delay is programmed into the firmware after asserting the soft reset and before starting the device setup.

MEMORY MAP

MEMORY MAP REGISTER TABLE

All address locations that are not included in Table 29 are not currently supported for this device and must not be written.

Table 29. Memory Map Registers

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
Analog Devices SPI Registers											
0x000	INTERFACE_ CONFIG_A	Soft reset (self clearing)	LSB first 0 = MSB 1 = LSB	Address ascension	0	0	Address ascension	LSB first 0 = MSB 1 = LSB	Soft reset (self clearing)	0x00	
0x001	INTERFACE_ CONFIG_B	Single instruction	0	0	0	0	0	Datapath soft reset (self clearing)	0	0x00	
0x002	DEVICE_CON FIG (local)	0	0	0	0	0	0	00 = normal operation 10 = standby 11 = power-down		0x00	
0x003	CHIP_TYPE					011 = high speed ADC				0x03	Read only
0x004	CHIP_ID (low byte)	1	1	0	1	0	0	1	1	0xD3	Read only
0x005	CHIP_ID (high byte)	0								0x00	Read only
0x006	CHIP_GRADE	Chip speed grade 0101 = 500 MSPS				0	1	0	X	0x5X	Read only
0x008	Device index	0	0	0	0	0	0	Channel B	Channel A	0x03	
0x00A	Scratch pad	0	0	0	0	0	0	0	0	0x00	
0x00B	SPI revision	0	0	0	0	0	0	0	1	0x01	
0x00C	Vendor ID (low byte)	0	1	0	1	0	1	1	0	0x56	Read only
0x00D	Vendor ID (high byte)	0	0	0	0	0	1	0	0	0x04	Read only
ADC Function Registers											
0x015	Analog input (local)	0	0	0	0	0	0	0	Input disable 0 = normal operation 1 = input disabled	0x00	
0x016	Input termination (local)	Analog input differential termination 0000 = 400 Ω (default) 0001 = 200 Ω 0010 = 100 Ω 0110 = 50 Ω				1	1	0	0	0x0C	
0x018	Input buffer current control (local)	0000 = 1.0× buffer current (default) 0001 = 1.5× buffer current 0010 = 2.0× buffer current 0011 = 2.5× buffer current 0100 = 3.0× buffer current 0101 = 3.5× buffer current … 1111 = 8.5× buffer current				0	0	0	0	0x20	

MEMORY MAP

Table 29. Memory Map Registers (Continued)

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x024	V_1P0 control	0	0	0	0	0	0	0	1.0 V reference select 0 = internal 1 = external	0x00	
0x025	Input full-scale range (local)	0	0	0	0	Full-scale adjust 0000 = 1.94 V 1000 = 1.46 V 1001 = 1.58 V 1010 = 1.70 V 1011 = 1.82 V 1100 = 2.06 V (default)				0x0C	V p-p differential; use in conjunction with Reg. 0x030
0x028	Temperature diode (local)	0	0	0	0	0	0	0	Diode selection 0 = no diode selected 1 = temperature diode selected	0x00	Used in conjunction with Reg. 0x040
0x030	Input full-scale control (local)	0	0	0	Full-scale control See #unique_18/unique_18_Connect_42_T9 for recommended settings for different frequency bands Default values: Full scale range ≥ 1.82 V = 001 Full scale range < 1.82 V = 110			0	0	0x04	Input full-scale control (local)
0x03F	PDWN/STBY pin control (local)	0 = PDWN/STBY enabled 1 = disabled	0	0	0	0	0	0	0	0x00	Used in conjunction with Reg. 0x040
0x040	Chip pin control	PDWN/STBY function 00 = power down 01 = standby 10 = disabled		Fast Detect B (FD_B) 000 = Fast Detect B output 001 = reserved 010 = reserved 111 = disabled			Fast Detect A (FD_A) 000 = Fast Detect A output 001 = reserved 010 = reserved 011 = temperature diode 111 = disabled			0x3F	
0x10B	Clock divider	0	0	0	0	0	000 = divide by 1 001 = divide by 2 011 = divide by 4 111 = divide by 8			0x00	
0x10C	Clock divider phase (local)	0	0	0	0	Independently controls Channel A and Channel B clock divider phase offset 0000 = 0 input clock cycles delayed 0001 = ½ input clock cycles delayed 0010 = 1 input clock cycles delayed 0011 = 1½ input clock cycles delayed 0100 = 2 input clock cycles delayed 0101 = 2½ input clock cycles delayed …				0x00	

MEMORY MAP

Table 29. Memory Map Registers (Continued)

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
						1111 = 7½ input clock cycles delayed					
0x10D	Clock divider and SYNC± control	Clock divider automatic phase adjustment 0 = disabled 1 = enabled	0	0	0	Clock divider negative skew window 00 = no negative skew 01 = 1 device clock of negative skew 10 = 2 device clocks of negative skew 11 = 3 device clocks of negative skew		Clock divider positive skew window 00 = no positive skew 01 = 1 device clock of positive skew 10 = 2 device clocks of positive skew 11 = 3 device clocks of positive skew		0x00	Clock divider must be >1
0x117	Clock delay control	0	0	0	0	0	0	0	Clock fine delay adjust enable 0 = disabled 1 = enabled	0x00	Enabling the clock fine delay adjustment causes a datapath soft reset
0x118	Clock fine delay (local)	Clock fine delay adjust, Bits[7:0] Twos complement coded control to adjust the fine sample clock skew in ~1.7 ps steps ≤−88 = −151.7 ps skew −87 = −150 ps skew … 0 = 0 ps skew … ≥+87 = +150 ps skew								0x00	Used in conjunction with Reg. 0x0117
0x11C	Clock status	0	0	0	0	0	0	0	0 = no input clock detected 1 = input clock detected	0x00	Read only
0x120	SYNC± Control 1	0	SYNC± flag reset 0 = normal operation 1 = flags held in reset	0	SYNC± transition select 0 = low to high 1 = high to low	CLK± edge select 0 = rising 1 = falling	SYNC± mode select 00 = disabled 01 = continuous 10 = N shot		0	0x00	
0x121	SYNC± Control 2	0	0	0	0	SYNC± N shot ignore counter select 0000 = next SYNC± only 0001 = ignore the first SYNC± transitions 0010 = ignore the first two SYNC± transitions … 1111 = ignore the first 16 SYNC± transitions				0x00	Mode select (Reg. 0x120, Bits[2:1]) must be N shot
0x123	SYNC± timestamp delay control		SYNC± timestamp delay, Bits[6:0] 0x00 = no delay 0x01 = 1 clock delay … 0x7F = 127 clocks delay							0x00	Ignored when Reg. 0x01FF = 0x00

MEMORY MAP

Table 29. Memory Map Registers (Continued)

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x128	SYNC± Status 1	SYNC± hold status, Register 0x128, Bits [7:4]				SYNC± setup status, Register 0x128, Bits [3:0]				Read only	
0x129	SYNC± and clock divider status	0	0	0	0	Clock divider phase when SYNC± was captured 0000 = in-phase 0001 = SYNC± is ½ cycle delayed from clock 0010 = SYNC± is 1 cycle delayed from clock 0011 = 1½ input clock cycles delayed 0100 = 2 input clock cycles delayed 0101 = 2½ input clock cycles delayed … 1111 = 7½ input clock cycles delayed				Read only	
0x12A	SYNC± counter	SYNC± counter, Bits[7:0] increments when a SYNC± signal is captured								Read only	
0x1FF	Chip sync mode							Synchronization mode 00 = normal 01 = timestamp		0x00	
0x200	Chip application mode	0	0	Chip Q ignore 0 = normal (I/Q) 1 = ignore (I only)	0	0	0	Chip operating mode 00 = full bandwidth mode 01 = DDC 0 on 10 = DDC 0 and DDC 1		0x00	
0x201	Chip decimation ratio	0	0	0	0	0	Chip decimation ratio select 000 = decimate by 1 001 = decimate by 2 010 = decimate by 4 011 = decimate by 8 100 = decimate by 16			0x00	
0x228	Customer offset	Offset adjust in LSBs from +127 to −128 (twos complement format)								0x00	
0x245	Fast detect (FD) control (local)	0	0	0	0	Force FD_A/ FD_B pins 0 = normal function 1 = force to value	Force value of FD_A/ FD_B pins if force pins is true, this value is output on FD_x pins	0	Enable fast detect output	0x00	
0x247	FD upper threshold LSB (local)	Fast detect upper threshold, Bits[7:0]								0x00	
0x248	FD upper threshold MSB (local)	0	0	0	Fast detect upper threshold, Bits[12:8]					0x00	
0x249	FD lower threshold LSB (local)	Fast detect lower threshold, Bits[7:0]								0x00	
0x24A	FD lower threshold MSB (local)	0	0	0	Fast detect lower threshold, Bits[12:8]					0x00	

MEMORY MAP

Table 29. Memory Map Registers (Continued)

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x24B	FD dwell time LSB (local)	Fast detect dwell time, Bits[7:0]								0x00	
0x24C	FD dwell time MSB (local)	Fast detect dwell time, Bits[15:8]								0x00	
0x26F	Signal monitor synchronization control	0	0	0	0	0	0	Synchronization mode 00 = disabled 01 = continuous 11 = one-shot		0x00	
0x270	Signal monitor control (local)	0	0	0	0	0	0	Peak detector 0 = disabled 1 = enabled	0	0x00	
0x271	Signal Monitor Period Register 0 (local)	Signal monitor period, Bits[7:0]								0x80	In decimated output clock cycles
0x272	Signal Monitor Period Register 1 (local)	Signal monitor period, Bits[15:8]								0x00	In decimated output clock cycles
0x273	Signal Monitor Period Register 2 (local)	Signal monitor period, Bits[23:16]								0x00	In decimated output clock cycles
0x274	Signal monitor result control (local)	0	0	0	Result update 1 = update results (self clear)	0	0	0	Result selection 0 = reserved 1 = peak detector	0x01	
0x275	Signal Monitor Result Register 0 (local)	Signal monitor result, Bits[7:0] When Register 0x0274, Bit 0 = 1, result Bits[19:7] = peak detector absolute value, Bits [12:0]; result Bits[6:0] = 0								Read only	Updated based on Reg. 0x274, Bit 4
0x276	Signal Monitor Result Register 1 (local)	Signal monitor result, Bits[15:8]								Read only	Updated based on Reg. 0x274, Bit 4
0x277	Signal Monitor Result Register 1 (local)	0	0	0	0	Signal monitor result, Bits[19:16]				Read only	Updated based on Reg. 0x274, Bit 4
0x278	Signal monitor period counter result (local)	Period count result, Bits[7:0]								Read only	Updated based on Reg. 0x274, Bit 4
Digital Downconverter (DDC) Function Registers—See the Digital Downconverters (DDCs) Section											
0x300	DDC synchronization control	0	0	0	DDC NCO soft reset 0 = normal operation 1 = reset	0	0	Synchronization mode (triggered by SYNC±) 00 = disabled 01 = continuous 11 = one-shot			

MEMORY MAP

Table 29. Memory Map Registers (Continued)

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x310	DDC 0 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = f_S/4 Hz IF mode (f_S/4 downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	
0x311	DDC 0 input selection	0	0	0	0	0	Q input select 0 = Ch. A 1 = Ch. B	0	I input select 0 = Ch. A 1 = Ch. B	0x00	
0x314	DDC 0 frequency LSB	DDC 0 NCO FTW, Bits[7:0], twos complement								0x00	
0x315	DDC 0 frequency MSB	X	X	X	X	DDC 0 NCO FTW, Bits[11:8], twos complement				0x00	
0x320	DDC 0 phase LSB	DDC 0 NCO POW, Bits[7:0], twos complement								0x00	
0x321	DDC 0 phase MSB	X	X	X	X	DDC 0 NCO POW, Bits[11:8], twos complement				0x00	
0x327	DDC 0 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Ch. B	0	I output test mode enable 0 = disabled 1 = enabled from Ch. A	0x00	
0x330	DDC 1 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = f_S/4 Hz IF mode (f_S/4 downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 (complex to real enabled) 11 = decimate by 1		0x00	
0x331	DDC 1 input selection	0	0	0	0	0	Q input select 0 = Ch. A 1 = Ch. B	0	I input select 0 = Ch. A 1 = Ch. B	0x00	
0x334	DDC 1 frequency LSB	DDC 1 NCO FTW, Bits[7:0], twos complement								0x00	
0x335	DDC 1 frequency MSB	X	X	X	X	DDC 1 NCO FTW, Bits[11:8], twos complement				0x00	

MEMORY MAP

Table 29. Memory Map Registers (Continued)

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x340	DDC 1 phase LSB	DDC 1 NCO POW, Bits[7:0], twos complement								0x00	
0x341	DDC 1 phase MSB	X	X	X	X	DDC 1 NCO POW, Bits[11:8], twos complement				0x00	
0x347	DDC 1 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Ch. B	0	I output test mode enable 0 = disabled 1 = enabled from Ch. A	0x00	
0x350	DDC 2 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0Hz IF mode (mixer bypassed, NCO disabled) 10 = f_S/4 Hz IF mode (f_S/4 downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	
0x351	DDC 2 input selection	0	0	0		0	Q input select 0 = Ch. A 1 = Ch. B	0	I input select 0 = Ch. A 1 = Ch. B	0x00	
0x354	DDC 2 frequency LSB	DDC 2 NCO FTW, Bits[7:0], twos complement								0x00	
0x355	DDC 2 frequency MSB	X	X	X	X	DDC 2 NCO FTW, Bits[11:8], twos complement				0x00	
0x360	DDC 2 phase LSB	DDC 2 NCOPOW, Bits[7:0], twos complement								0x00	
0x361	DDC 2 phase MSB	X	X	X	X	DDC 2 NCO POW, Bits[11:8], twos complement				0x00	
0x367	DDC 2 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Ch. B	0	I output test mode enable 0 = disabled 1 = enabled from Ch. A	0x00	
0x370	DDC 3 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = f_S/4 Hz IF mode (f_S/4 downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	

MEMORY MAP

Table 29. Memory Map Registers (Continued)

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x371	DDC 3 input selection	0	0	0	0	0	Q input select 0 = Ch. A 1 = Ch. B	0	I input select 0 = Ch. A 1 = Ch. B	0x05	
0x374	DDC 3 frequency LSB	DDC 3 NCO FTW, Bits[7:0] twos complement								0x00	
0x375	DDC 3 frequency MSB	X	X	X	X	DDC 3 NCO FTW, Bits[11:8] twos complement				0x00	
0x380	DDC 3 phase LSB	DDC 3 NCO POW, Bits[7:0] twos complement								0x00	
0x381	DDC 3 phase MSB	X	X	X	X	DDC 3 NCO POW, Bits[11:8] twos complement				0x00	
0x387	DDC 3 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Ch. B	0	I output test mode enable 0 = disabled 1 = enabled from Ch. A	0x00	
Digital Outputs and Test Modes											
0x550	ADC test modes (local)	User pattern selection 0 = continuous repeat 1 = single pattern	0	Reset PN long gen 0 = long PN enable 1 = long PN reset	Reset PN short gen 0 = short PN enable 1 = short PN reset	Test mode selection 0000 = off (normal operation) 0001 = midscale short 0010 = positive full scale 0011 = negative full scale 0100 = alternating checker board 0101 = PN sequence, long 0110 = PN sequence, short 0111 = one/zero word toggle 1000 = the user pattern test mode (used with Register 0x550, Bit 7 and User Pattern 1 to User Pattern 4 registers) 1111 = ramp output				0x00	
0x551	User Pattern 1 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x552	User Pattern 1 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x553	User Pattern 2 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x554	User Pattern 2 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573

MEMORY MAP

Table 29. Memory Map Registers (Continued)

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x555	User Pattern 3 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x556	User Pattern 3 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x557	User Pattern 4 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x558	User Pattern 4 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x559	Output Mode Control 1	0	0	0	0	0	Status bit selection 000 = tie low (1'b0) 001 = overrange bit 010 = signal monitor bit 011 = fast detect (FD) bit 100 = not applicable 101 = system reference			0x00	
0x561	Output mode	0	0	0	0	0	Sample invert 0 = normal 1 = sample invert	Data format select 00 = offset binary 01 = twos complement		0x01	
0x562	Output overrange (OR) clear	Virtual Converter 7 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 6 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 5 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 4 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 3 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 2 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 1 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 0 OR 0 = OR bit enabled 1 = OR bit cleared	0x00	
0x563	Output OR status	Virtual Converter 7 OR 0 = no OR 1 = OR occurred	Virtual Converter 6 OR 0 = no OR 1 = OR occurred	Virtual Converter 5 OR 0 = no OR 1 = OR occurred	Virtual Converter 4 OR 0 = no OR 1 = OR occurred	Virtual Converter 3 OR 0 = no OR 1 = OR occurred	Virtual Converter 2 OR 0 = no OR 1 = OR occurred	Virtual Converter 1 OR 0 = no OR 1 = OR occurred	Virtual Converter 0 OR 0 = no OR 1 = OR occurred	0x00	Read only
0x564	Output channel select	0	0	0	0	0	0	0	Converter channel swap 0 = normal channel ordering 1 = channel swap enabled	0x00	

MEMORY MAP

Table 29. Memory Map Registers (Continued)

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x568	LVDS output mode	0	0	Frame clock mode (only used when in output data mode is in byte mode) 00 = frame clock always off 01 = frame clock always on 10 = reserved 11 = frame clock conditionally on based on PN23 sequence		0	Output data mode 000 = parallel mode (one converter) 001 = parallel interleaved mode (two converters) 010 = parallel channel multiplexed (even/odd) mode (one converter) 011 = parallel channel multiplexed (even/odd) mode (two converters) 100 = byte mode (one converter) 101 = byte mode (two converters) 110 = byte mode (four converters) Others = reserved			0x01	
0x569	Digital clock output adjust	0	0	0	0	0	0	DCO phase adjustment 0x0: 0° 0x1: 90° 0x2: 180° 0x3: 270°		0x01	
0x56A	Output Parallel Driver Adjust 1	0	1	0	0	LVDS output drive current adjust 000 = 2 mA 001 = 2.25 mA 010 = 2.5 mA 011 = 2.75 mA 100 = 3.0 mA 101 = 3.25 mA 110 = 3.5 mA (default) 111 = 3.75 mA			0	0x4C	
0x56B	Output Parallel Driver Adjust 2	0	0	0	0	0	0	Output slew rate control of LVDS driver Interface 00 = 80 ps 01 = 150 ps 10 = 200 ps 11 = 250 ps		0x00	

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

The AD9684 must be powered by the following six supplies: AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, and SPIVDD = 1.8 V. For applications requiring an optimal high power efficiency and low noise performance, it is recommended that the ADP2164 and ADP2370 switching regulators be used to convert the 3.3 V, 5.0 V, or 12 V input rails to an intermediate rail (1.8 V and 3.8 V). These intermediate rails are then postregulated by very low noise, low dropout (LDO) regulators (ADP1741, ADP1740, and ADP125). Figure 70 shows the recommended power supply scheme for the AD9684.

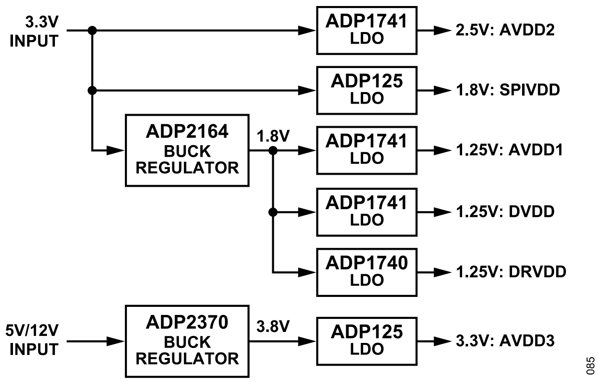


Figure 70. High Efficiency, Low Noise Power Solution for the AD9684

It is not necessary to split all of these power domains in all cases. The recommended solution shown in Figure 70 provides the lowest noise, highest efficiency power delivery system for the AD9684. If only one 1.25 V supply is available, route to AVDD1 first and then tap it off and isolate it with a ferrite bead or a filter choke, preceded by decoupling capacitors for SPIVDD, DVDD, and DRVDD, in that order. The user can employ several different decoupling capacitors to cover both high and low frequencies. These capacitors must be located close to the point of entry at the PCB level and close to the devices, with minimal trace lengths.

OUTLINE DIMENSIONS

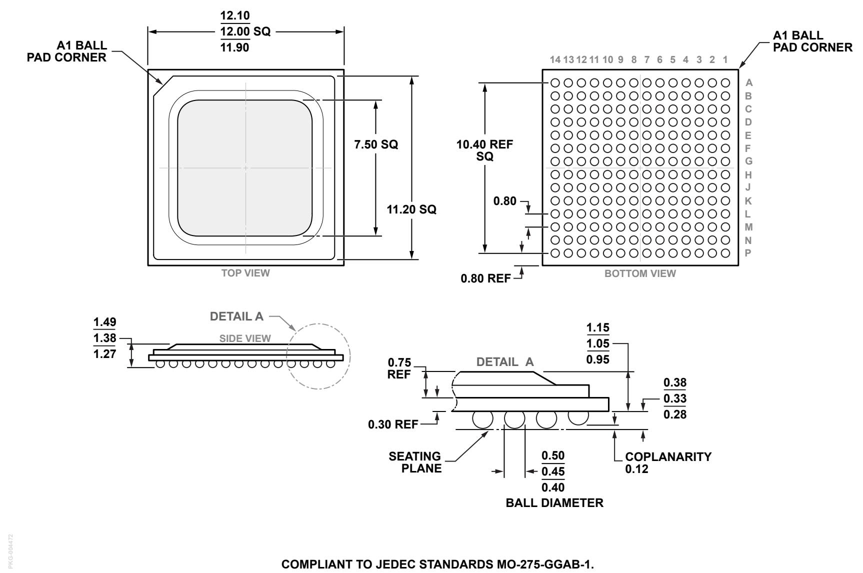


Figure 71. 196-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]
(BP-196-3)
Dimensions shown in millimeters

Updated: June 07, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD9684BBPZ-500	-40°C to +85°C	196-Ball BGA (12mm x 12mm x 1.38mm w/ EP)		BP-196-3
AD9684BBPZRL-500	-40°C to +85°C	196-Ball BGA (12mm x 12mm x 1.38mm w/ EP)	Reel, 1500	BP-196-3

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
AD9684-500EBZ	Evaluation Board for AD9684-500

[1] Z = RoHS Compliant Part.