Rev. 5 — 27 July 2021

**Product data sheet** 

# 1. General description

The 74ALVC02 is a quad 2-input NOR gate.

Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall times.

#### 2. Features and benefits

- Wide supply voltage range from 1.65 V to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- · Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF; R = 0 Ω)
- Multiple package options
- Specified from -40 °C to +85 °C



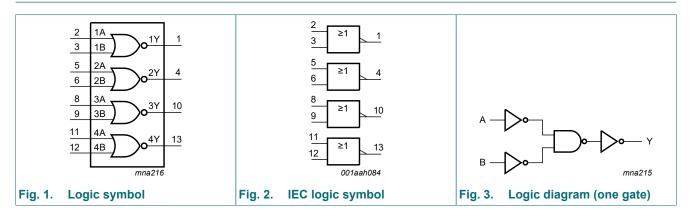
**Quad 2-input NOR gate** 

# 3. Ordering information

**Table 1. Ordering information** 

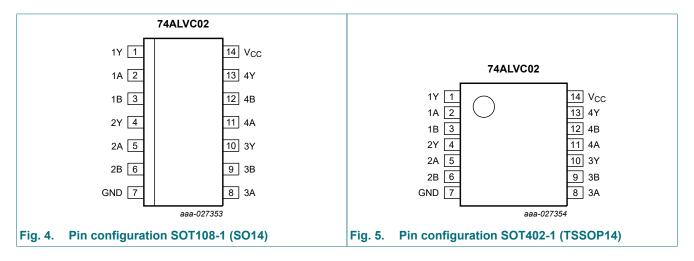
Type number	Package								
	Temperature range	Name	Description	Version					
74ALVC02D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1					
74ALVC02PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1					
74ALVC02BQ -40 °C to +85 °C DHVQFN14		DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1					

# 4. Functional diagram

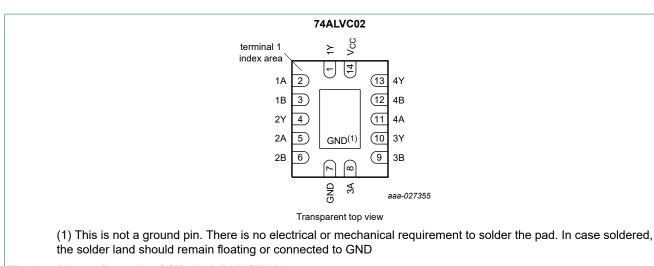


# 5. Pinning information

#### 5.1. Pinning



#### **Quad 2-input NOR gate**



# Fig. 6. Pin configuration SOT762-1 (DHVQFN14)

# 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description	
1Y, 2Y, 3Y, 4Y	1, 4, 10, 13	data output	
1A, 2A, 3A, 4A	2, 5, 8, 11	data input	
1B, 2B, 3B, 4B	3, 6, 9,12	data input	
GND	7	ground (0 V)	
V <sub>CC</sub>	14	supply voltage	

# 6. Functional description

#### **Table 3. Function table**

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level.$ 

Input	Output	
nA	nB	nY
L	L	Н
L	Н	L
Н	L	L
Н	Н	L

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**Quad 2-input NOR gate** 

# 7. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
VI	input voltage	[1]	-0.5	+4.6	V
Vo	output voltage	output HIGH or LOW state [1]	-0.5	V <sub>CC</sub> + 0.5	V
		power-down mode; V <sub>CC</sub> = 0 V	-0.5	+4.6	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mΑ
Io	output current	$V_O = 0 V \text{ to } V_{CC}$	-	±50	mΑ
I <sub>CC</sub>	supply current		-	100	mΑ
I <sub>GND</sub>	ground current		-100	-	mΑ
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C}$ [2]	-	500	mW

The input and output voltage ratings may be exceeded if the input and output current ratings are observed. For SOT402-1 (TSSOP14) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 81 °C.

# 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	V <sub>CC</sub> = 1.65 to 3.6 V	0	V <sub>CC</sub>	V
		power-down mode; $V_{CC} = 0 V$	0	3.6	V
T <sub>amb</sub>	ambient temperature		-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.65 V to 2.7 V	0	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	10	ns/V

**Quad 2-input NOR gate** 

# 9. Static characteristics

**Table 6. Static characteristics** 

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> =	-40 °C to	+85 °C	Unit
			Min	Typ[1]	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 1.65 V	1.25	1.51	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.3 V	1.8	2.10	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 2.3 V	1.7	2.01	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	2.53	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	2.76	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.2	2.68	-	V
V <sub>OL</sub>	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 1.65 V	-	0.11	0.3	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.3 V	-	0.17	0.4	V
		I <sub>O</sub> = 18 mA; V <sub>CC</sub> = 2.3 V	-	0.25	0.6	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	0.16	0.4	V
		I <sub>O</sub> = 18 mA; V <sub>CC</sub> = 3.0 V	-	0.23	0.4	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	0.30	0.55	V
l <sub>l</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 3.6 V or GND	-	±0.1	±5	μΑ
I <sub>OFF</sub>	power-off leakage current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} = 0 \text{ V to } 3.6 \text{ V}$	-	±0.1	±10	μΑ
I <sub>CC</sub>	supply current	$V_{CC} = 3.6 \text{ V}; V_{I} = V_{CC} \text{ or GND}; I_{O} = 0 \text{ A}$	-	0.2	20	μΑ
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 3.0 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	750	μA
Cı	input capacitance		-	3.5	-	pF

<sup>[1]</sup> All typical values are measured at  $V_{CC}$  = 3.3 V (unless stated otherwise) and  $T_{amb}$  = 25 °C.

**Quad 2-input NOR gate** 

# 10. Dynamic characteristics

#### **Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit, see Fig. 8.

Symbol	Parameter	Conditions	T <sub>amb</sub>	Unit		
			Min	Typ[1]	Max	
t <sub>pd</sub>	propagation delay	nA, nB to nY; see Fig. 7 [2]				
	V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	2.8	4.7	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.0	3.1	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.5	3.1	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.2	2.8	ns
C <sub>PD</sub>	power dissipation capacitance	per gate; $V_I$ = GND to $V_{CC}$ ; [3] $V_{CC}$ = 3.3 V	-	32	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

Typical values for  $V_{CC}$  = 1.65 V to 1.95 V are measured at  $V_{CC}$  = 1.8 V.

Typical values for  $V_{CC}$  = 2.3 V to 2.7 V are measured at  $V_{CC}$  = 2.5 V.

Typical values for  $V_{CC}$  = 3.0 V to 3.6 V are measured at  $V_{CC}$  = 3.3 V.

[2]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

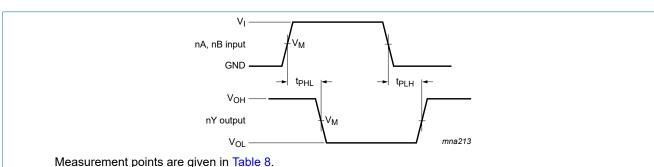
C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs

#### 10.1. Waveforms and test circuit



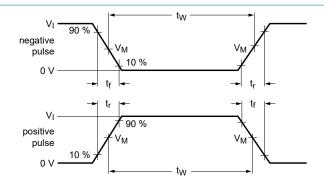
V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

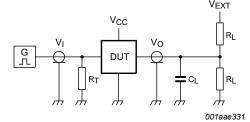
Fig. 7. Input (nA, nB) to output (nY) propagation delays

**Table 8. Measurement points** 

Supply voltage V <sub>CC</sub>	Input V <sub>I</sub>	V <sub>M</sub>
1.65 V to 1.95 V	V <sub>CC</sub>	0.5 x V <sub>CC</sub>
2.3 V to 2.7 V	Vcc	0.5 x V <sub>CC</sub>
2.7 V	2.7 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V

#### **Quad 2-input NOR gate**





Test data is given in Table 9.

Definitions test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

 $C_L$  = Load capacitance including jig and probe capacitance.

R<sub>L</sub> = Load resistance.

 $V_{EXT}$  = Test voltage for switching times.

Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V <sub>EXT</sub>			
V <sub>CC</sub>	VI	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub> R <sub>L</sub>		t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>	
1.65 V to 1.95 V	V <sub>CC</sub>	≤ 2.0 ns	30 pF	1 kΩ	open	2 × V <sub>CC</sub>	GND	
2.3 V to 2.7 V	V <sub>CC</sub>	≤ 2.0 ns	30 pF	500 Ω	open	2 × V <sub>CC</sub>	GND	
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND	
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND	

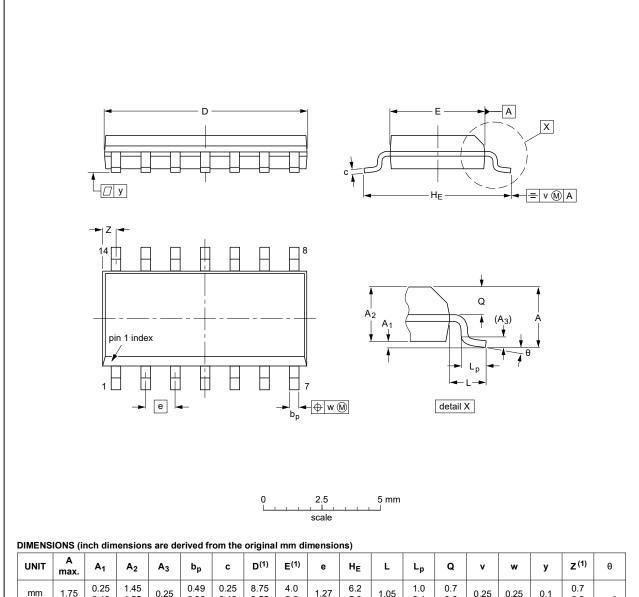
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**Quad 2-input NOR gate** 

# 11. Package outline

#### SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

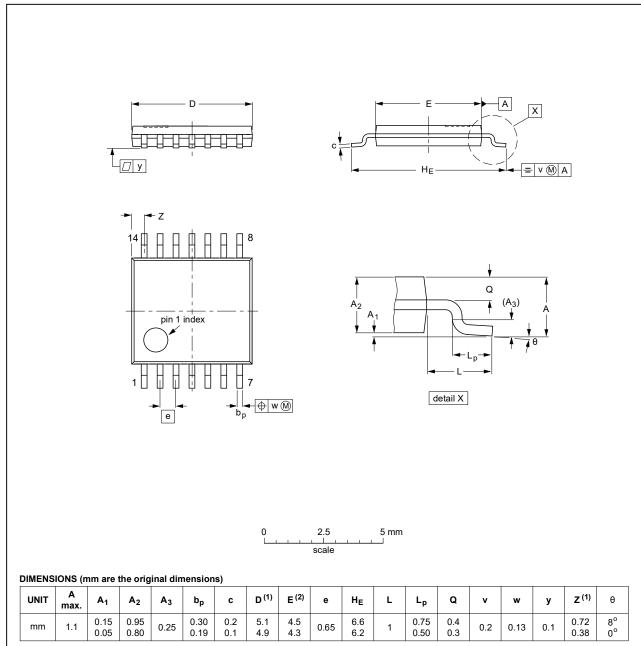
OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012				<del>99-12-27</del> 03-02-19

Fig. 9. Package outline SOT108-1 (SO14)

### **Quad 2-input NOR gate**

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFERENCES			EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT402-1		MO-153				<del>99-12-27</del> 03-02-18

Fig. 10. Package outline SOT402-1 (TSSOP14)

**Quad 2-input NOR gate** 

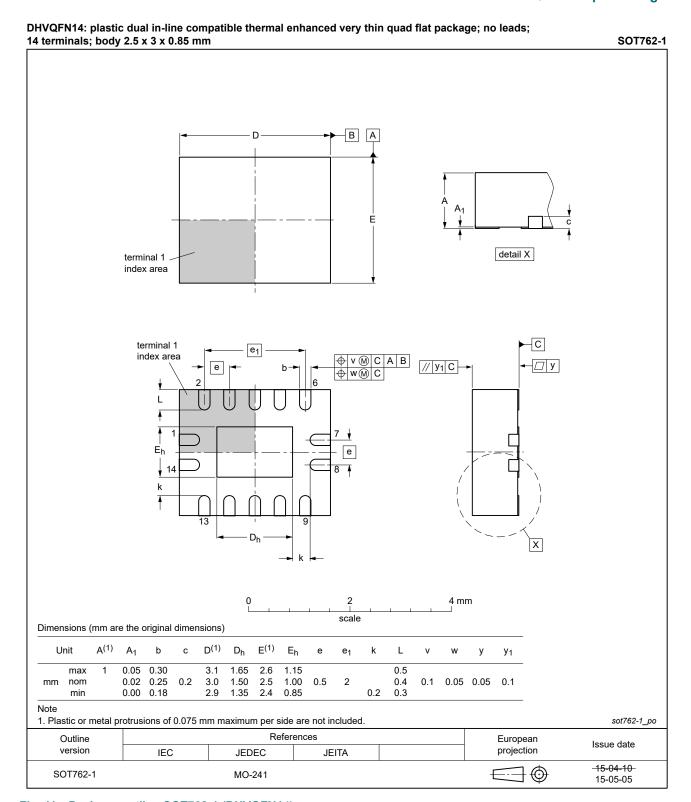


Fig. 11. Package outline SOT762-1 (DHVQFN14)

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**Quad 2-input NOR gate** 

# 12. Abbreviations

#### **Table 10. Abbreviations**

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

# 13. Revision history

#### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74ALVC02 v.5	20210714	Product data sheet	-	74ALVC02 v.4		
Modifications:	• Section 10: Maximum propagation delay (t <sub>pd(max)</sub> ) at V <sub>CC</sub> = 2.7 V changed to 3.1 ns. (errata)					
74ALVC02 v.4	20210430	Product data sheet	-	74ALVC02 v.3		
Modifications:	<ul> <li><u>Section 2</u>: Reference to JESD36 removed.</li> <li><u>Section 7</u>: Derating values for P<sub>tot</sub> total power dissipation have been updated.</li> <li><u>Section 8</u>: Maximum output voltage (power-down mode) changed from 4.6 V to 3.6 V (errata).</li> </ul>					
74ALVC02 v.3	20170907	Product data sheet	-	74ALVC02 v.2		
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>					
74ALVC02 v.2	20030714	Product specification	-	74ALVC02 v.1		
74ALVC02 v.1	20030205	Product specification	-	-		

#### **Quad 2-input NOR gate**

### 14. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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### **Quad 2-input NOR gate**

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