DRV8881 2.5-A Dual H-Bridge Motor Driver

1 Features

- Dual H-Bridge Motor Driver
  - Bipolar Stepper Motor Driver
  - Single or Dual Brushed-DC Motor Driver
- 6.5- to 45-V Operating Supply Voltage Range
- Two Control Interface Options
  - PHASE/**E**NABLE (DRV8881**E**)
  - **P**WM (DRV8881**P**)
- Multiple Decay Modes to Support Any Motor
  - Smart tune (DRV8881E Only)
  - Mixed Decay
  - Slow Decay
  - Fast Decay
- Adaptive Blanking Time for Smooth Motion
- Parallel Mode Operation (DRV8881P Only)
- Configurable Off-Time PWM Chopping
  - 10, 20, or 30 µs Off-Time
- 3.3-V, 10-mA LDO Regulator
- Low-Current Sleep Mode (28 µA)
- Small Package and Footprint
  - 28 HTSSOP (PowerPAD)
  - 28 WQFN (PowerPAD)

- **Protection Features**
  - VM Undervoltage Lockout (UVLO)
  - Charge Pump Undervoltage (CPUV)
  - Overcurrent Protection (OCP)
  - Automatic OCP Retry
  - Thermal Shutdown (TSD)
  - Fault Condition Indication Pin (nFAULT)

2 Applications

- Automatic Teller and Money Handling Machines
- Video Security Cameras
- Multi-Function Printers and Document Scanners
- Factory Automation and Robotics
- Stage Lighting Equipment

3 Description

The DRV8881 is a bipolar stepper or brushed-DC motor driver for industrial applications. The device output stage consists of two N-channel power MOSFET H-bridge drivers. The DRV8881 is capable of driving up to 2.5-A peak current or 1.4-A rms current per H-bridge (with proper PCB ground plane for thermal dissipation and at 24 V and T_A = 25°C).

Smart tune automatically tunes motors for optimal current regulation performance and compensates for motor variation and aging effects. Smart tune is available on the DRV8881E. Additionally, slow, fast, and mixed decay modes are available.

The PH/EN (DRV8881E) or PWM (DRV8881P) pins provide a simple control interface. An internal sense amplifier allows for adjustable current control. A low-power sleep mode is provided for very-low quiescent current standby using a dedicated nSLEEP pin.

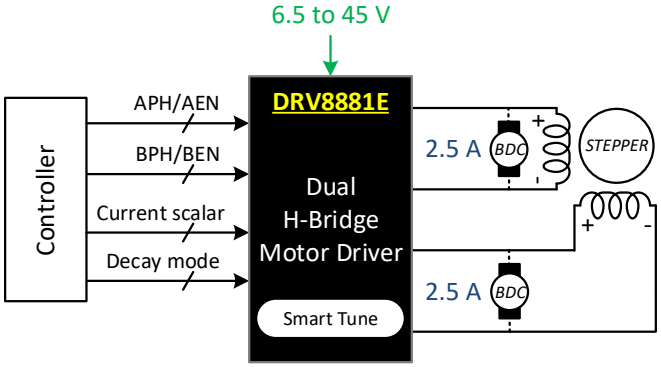
Internal protection functions are provided for undervoltage, charge pump faults, overcurrent, short-circuits, and overtemperature. Fault conditions are indicated by a nFAULT pin.

Device Information(1)

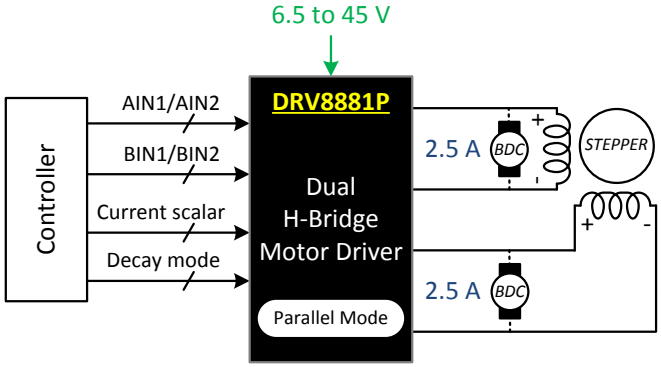
PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8881	HTSSOP (28)	9.70 mm × 6.40 mm
	WQFN (28)	5.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

DRV8881E Simplified System Diagram



DRV8881P Simplified System Diagram



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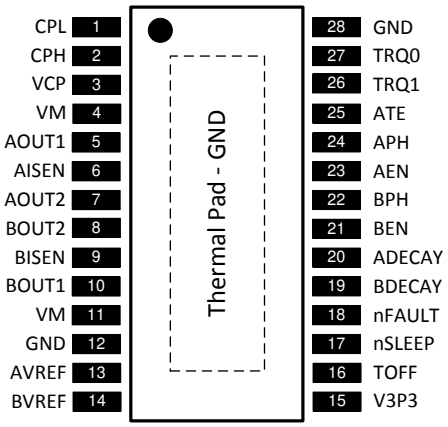
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

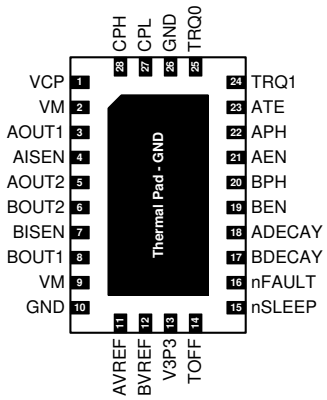
Changes from Original (June 2015) to Revision A	Page
• Updated device status to production data	1
• Updated from "PowerPAD" to "thermal pad"	4
• Corrected ATE pin number for RHR package to 23	4

5 Pin Configuration and Functions

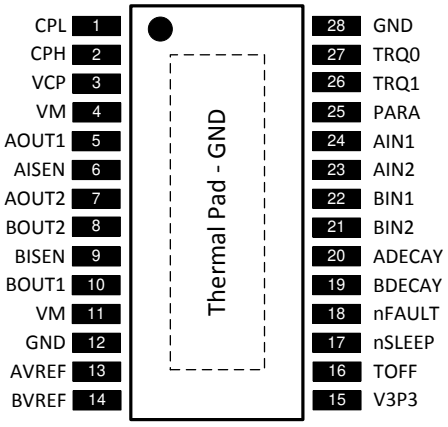
PWP Package
28-Pin HTSSOP
Top View DRV8881E



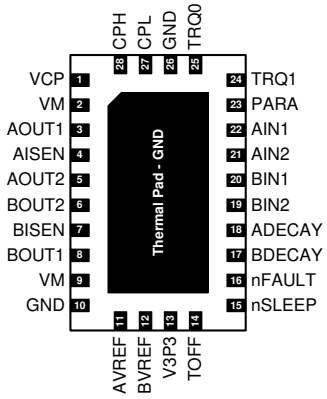
RHR Package
28-Pin WQFN
Top View DRV8881E



PWP Package
28-Pin HTSSOP
Top View DRV8881P



RHR Package
28-Pin WQFN
Top View DRV8881P



Pin Functions

PIN			TYPE	DESCRIPTION	
NAME	PWP	RHR			
CPL	1	27	PWR	Charge pump output	Connect a VM rated, 0.1-µF ceramic capacitor between CPH and CPL
CPH	2	28			
VCP	3	1	O	Charge pump output	Connect a 16-V, 0.47-µF ceramic capacitor to VM
VM	4, 11	2, 9	PWR	Power supply	Connect to motor supply voltage; bypass to GND with two 0.1 µF (for each pin) plus one bulk capacitor rated for VM
AOUT1	5	3	O	Winding A output	H-bridge outputs, drives one winding of a stepper motor
AOUT2	7	5			
AISEN	6	4	O	Winding A sense	Requires sense resistor to GND; value sets peak current in winding A
BOUT2	8	6	O	Winding B output	H-bridge outputs, drives one winding of a stepper motor
BOUT1	10	8			
BISEN	9	7	O	Winding B sense	Requires sense resistor to GND; value sets peak current in winding B
GND	12, 28	10, 26	PWR	Device ground	Must be connected to ground

Pin Functions (continued)

PIN			TYPE	DESCRIPTION	
NAME	PWP	RHR			
AVREF	13	11	I	Reference voltage input	Voltage on this pin sets the full scale chopping current in H-bridge A
BVREF	14	12			Voltage on this pin sets the full scale chopping current in H-bridge B
V3P3	15	13	—	Internal regulator	Internal supply voltage; bypass to GND with a 6.3-V, 0.47-µF ceramic capacitor; up to 10-mA external load
TOFF	16	14	I	Decay mode off time set	Sets the off-time during current chopping; tri-level pin
nSLEEP	17	15	I	Sleep mode input	Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown
nFAULT	18	16	O	Fault indication pin	Pulled logic low with fault condition; open-drain output requires an external pullup
BDECAY	19	17	I	Decay mode setting pins	Set the decay mode for bridge B; see *Decay Modes* ; tri-level pin
ADECAY	20	18			Set the decay mode for bridge A; see *Decay Modes* ; tri-level pin
TRQ1	26	24	I	Torque DAC current scalar	Scales the current by 100%, 75%, 50%, or 25%; internal pulldown
TRQ0	27	25			
PAD	PAD	PAD	PWR	Thermal pad	Must be connected to ground

DRV8881E PH/EN Pin Functions

PIN			TYPE	DESCRIPTION	
NAME	PWP	RHR			
BEN	21	19	I	Bridge B enable input	Logic high enables bridge B; logic low disables the bridge Hi-Z
BPH	22	20	I	Bridge B phase input	Logic high drives current from BOUT1 → BOUT2
AEN	23	21	I	Bridge A enable input	Logic high enables bridge A; logic low disables the bridge Hi-Z
APH	24	22	I	Bridge A phase input	Logic high drives current from AOUT1 → AOUT2
ATE	25	23	I	Smart tune enable pin	Logic high enables smart tune operation; when logic low, the decay mode is set through the DECAYx pins; smart tune must be pulled high prior to power-up or coming out of sleep, or else tied to V3P3 in order to enable smart tune; internal pulldown; see *Smart tune*

DRV8881P PWM Pin Functions

PIN			TYPE	DESCRIPTION	
NAME	PWP	RHR			
BIN2	21	19	I	Bridge B PWM input	Logic controls the state of H-bridge B; internal pulldown
BIN1	22	20			
AIN2	23	21	I	Bridge A PWM input	Logic controls the state of H-bridge A; internal pulldown
AIN1	24	22			
PARA	25	23	I	Parallel mode input	Logic high enables parallel mode

External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
CVM1	VM	GND	0.1-µF ceramic capacitor rated for VM per VM pin
CVM1	VM	GND	Bulk electrolytic capacitor rated for VM, recommended value is 100 µF, see *Bulk Capacitance Sizing*
CVCP	VCP	VM	16 V, 0.47 µF ceramic capacitor
CSW	CPH	CPL	0.1-µF X7R capacitor rated for VM
CV3P3	V3P3	GND	6.3 V, 0.47-µF ceramic capacitor
R_{nFAULT}	V_{MCU} (1)	nFAULT	> 5 kΩ
R_{AISEN}	AISEN	GND	Optional sense resistor, see *Sense Resistor*
R_{BISEN}	BISEN	GND	

(1) V_{MCU} is not a pin on the DRV8881, but a supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to V3P3

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range referenced with respect to GND (unless otherwise noted) (1)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	50	V
Power supply voltage ramp rate (VM)	0	2	V/µs
Charge pump voltage (VCP, CPH)	–0.3	VM + 12	V
Charge pump negative switching pin (CPL)	–0.3	VM	V
Internal regulator voltage (V3P3)	–0.3	3.8	V
Internal regulator current output (V3P3)	0	10	mA
Control pin voltage (APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2, nSLEEP, nFAULT, ADECAY, BDECAY, TRQ0, TRQ1, ATE, PARA)	–0.3	7.0	V
Open drain output current (nFAULT)	0	10	mA
Reference input pin voltage (AVREF, BVREF)	–0.3	V3P3 + 0.5	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–0.7	VM + 0.7	V
Continuous shunt amplifier input pin voltage (AISEN, BISEN) (2)	–0.55	0.55	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2, AISEN, BISEN)	Internally limited		A
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transients of ±1 V for less than 25 ns are acceptable

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VM	Power supply voltage range	6.5	45	V
V_{IN}	Digital pin voltage range	0	5.3	V
VREF	Reference rms voltage range (AVREF, BVREF)	0.3 (1)	V3P3	V
f_{PWM}	Applied PWM signal (APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2)	0	100	kHz
I_{V3P3}	V3P3 external load current	0	10 (2)	mA
I_{rms}	Motor rms current per H-bridge	0	1.4	A
T_A	Operating ambient temperature	–40	125	°C

(1) Operational at VREF ≈ 0 to 0.3 V, but accuracy is degraded
(2) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC (1)		DRV8881		UNIT
		PWP (HTSSOP)	RHR (WQFN)	
		28 PINS	28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.1	37.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.6	23.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	8.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.2	7.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, V3P3)						
VM	VM operating voltage		6.5		45	V
I_{VM}	VM operating supply current	nSLEEP high; ENABLE high; no motor load; VM = 24 V		8	18	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP low; VM = 24 V; T_A = 25°C		28		µA
		nSLEEP low; VM = 24 V; T_A = 125°C (1)			77	
t_{SLEEP}	Sleep time	nSLEEP low to sleep mode			100	µs
t_{WAKE}	Wake-up time	nSLEEP high to output transition			1.5	ms
t_{ON}	Turn-on time	VM > V_{UVLO} to output transition			1.5	ms
V3P3	Internal regulator voltage	External load 0 to 10 mA	2.9	3.3	3.6	V
CHARGE PUMP (VCP, CPH, CPL)						
V_{CP}	VCP operating voltage	VM > 12 V		VM + 11.5		V
		V_{UVLO} < VM < 12 V		2×VM – 1.5		
f_{VCP} (1)	Charge pump switching frequency	VM > V_{UVLO}	175		715	kHz
LOGIC-LEVEL INPUTS (APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2, nSLEEP, TRQ0, TRQ1, PARA)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage		1.6		5.3	V
V_{HYS}	Input logic hysteresis		100			mV
I_{IL}	Input logic low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic high current	V_{IN} = 5.0 V		50	100	µA
R_{PD}	Pulldown resistance	Measured between the pin and GND		100		kΩ
t_{PD}	Propagation delay	xPH, xEN, xINx input to current change		450		ns
TRI-LEVEL INPUTS (ADECAY, BDECAY, TOFF)						
V_{IL}	Tri-level input logic low voltage		0		0.6	V
V_{IZ}	Tri-level input Hi-Z voltage			1.1		V
V_{IH}	Tri-level input logic high voltage		1.6		5.3	V
V_{HYS}	Tri-level input hysteresis		100			mV
I_{IL}	Tri-level input logic low current	V_{IN} = 0 V	–55		–35	µA
I_{IZ}	Tri-level input Hi-Z current	V_{IN} = 1.3 V		15		µA
I_{IH}	Tri-level input logic high current	V_{IN} = 3.3 V		85		µA
R_{PD}	Tri-level pulldown resistance	Measured between the pin and GND		40		kΩ
R_{PU}	Tri-level pullup resistance	Measured between V3P3 and the pin		45		kΩ
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic low voltage	I_O = 4 mA			0.5	V
I_{OH}	Output logic high leakage	External pullup resistor to 3.3 V	–1		1	µA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ON)}$	High-side FET on resistance	VM = 24 V, I = 1 A, T_A = 25°C		330		mΩ
		VM = 24 V, I = 1 A, T_A = 125°C (1)		400	440	
		VM = 6.5 V, I = 1 A, T_A = 25°C		430		
		VM = 6.5 V, I = 1 A, T_A = 125°C (1)		500	560	
$R_{DS(ON)}$	Low-side FET on resistance	VM = 24 V, I = 1 A, T_A = 25°C		300		mΩ
		VM = 24 V, I = 1 A, T_A = 125°C (1)		370	400	
		VM = 6.5 V, I = 1 A, T_A = 25°C		370		
		VM = 6.5 V, I = 1 A, T_A = 125°C (1)		450	490	

(1) Specified by design and characterization data

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RISE}	Output rise time	VM = 24 V, 50 Ω load from xOUTx to GND		70		ns
t_{FALL}	Output fall time	VM = 24 V, 50 Ω load from VM to xOUTx		70		ns
t_{DEAD}	Output dead time (2)			200		ns
V_d	Body diode forward voltage	I_{OUT} = 0.5 A		0.7	1	V
PWM CURRENT CONTROL (VREF, AISEN, BISEN)						
V_{TRIP}	xISENSE trip voltage, full scale current step	TRQ at 100%, VREF = 3.3 V		500		mV
		TRQ at 75%, VREF = 3.3 V		375		
		TRQ at 50%, VREF = 3.3 V		250		
		TRQ at 25%, VREF = 3.3 V		125		
A_V	Amplifier attenuation	Torque = 100% (TRQ0 = 0, TRQ1 = 0)	6.25	6.58	6.91	V/V
		Torque = 75% (TRQ0 = 1, TRQ1 = 0)	6.2	6.56	6.92	
		Torque = 50% (TRQ0 = 0, TRQ1 = 1)	6.09	6.51	6.94	
		Torque = 25% (TRQ0 = 1, TRQ1 = 1)	5.83	6.38	6.93	
t_{OFF}	PWM off-time	TOFF logic low		20		µs
		TOFF logic high		30		
		TOFF Hi-Z		10		
t_{BLANK}	PWM blanking time	See Table 6 for details		1.8		µs
				1.5		
				1.2		
				0.9		
PROTECTION CIRCUITS						
V_{UVLO}	VM undervoltage lockout	VM falling; UVLO report		5.8	6.4	V
		VM rising; UVLO recovery		6.1	6.5	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold	100			mV
V_{CPUV}	Charge pump undervoltage	VCP falling; CPUV report		VM + 1.8		V
		VCP rising; CPUV recovery		VM + 1.9		
$V_{CPUV,HYS}$	CP undervoltage hysteresis	Rising to falling threshold	50			mV
I_{OCP}	Overcurrent protection trip level	Current through any FET	2.5	3.6		A
V_{OCP}	Sense pin overcurrent trip level	Voltage at AISEN or BISEN	0.9	1.25		V
t_{OCP}	Overcurrent deglitch time			2		µs
t_{RETRY}	Overcurrent retry time		0.5		2	ms
T_{TSD} (2)	Thermal shutdown temperature	Die temperature T_J	150			°C
T_{HYS} (2)	Thermal shutdown hysteresis	Die temperature T_J		35		°C

(2) Specified by design and characterization data

6.6 Typical Characteristics

Over recommended operating conditions (unless otherwise noted)

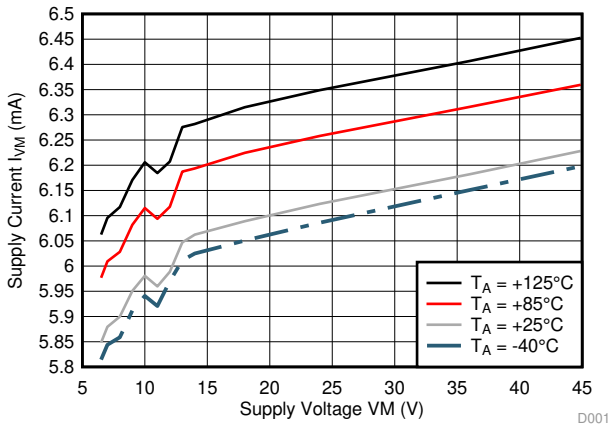


Figure 1. Supply Current over VM

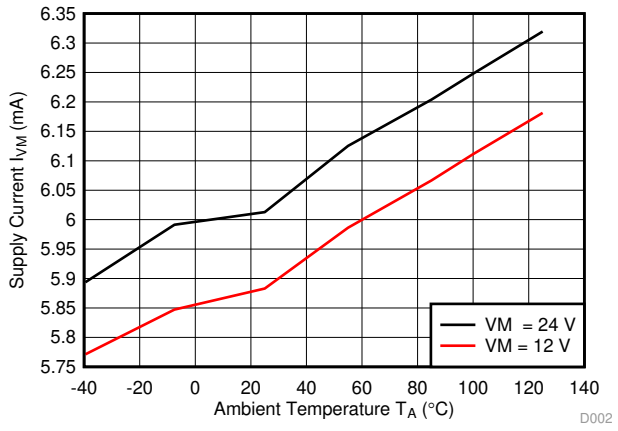


Figure 2. Supply Current over Temperature

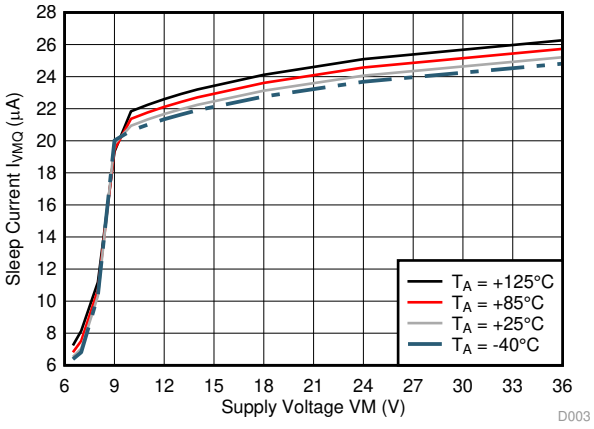


Figure 3. Sleep Current over VM

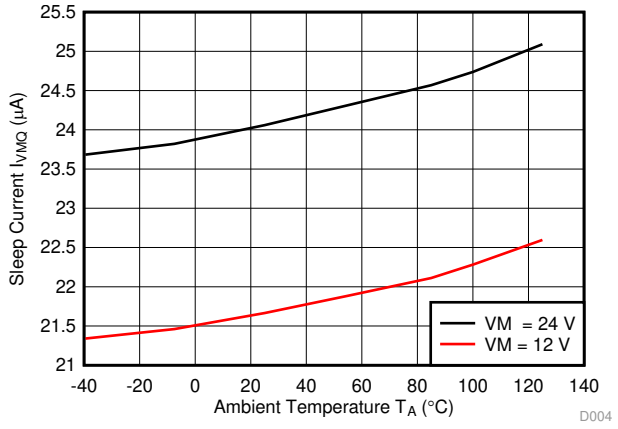


Figure 4. Sleep Current over Temperature

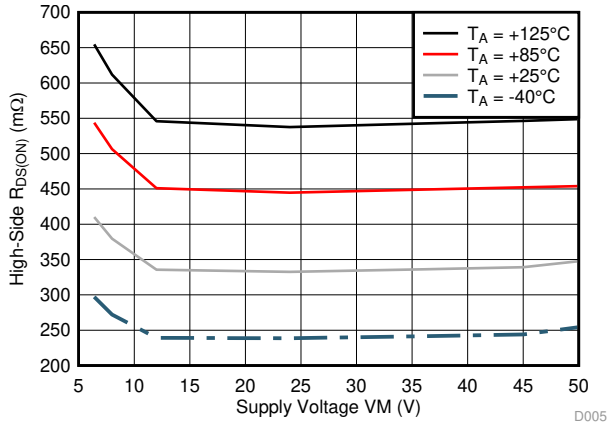


Figure 5. High-Side $R_{DS(ON)}$ over VM

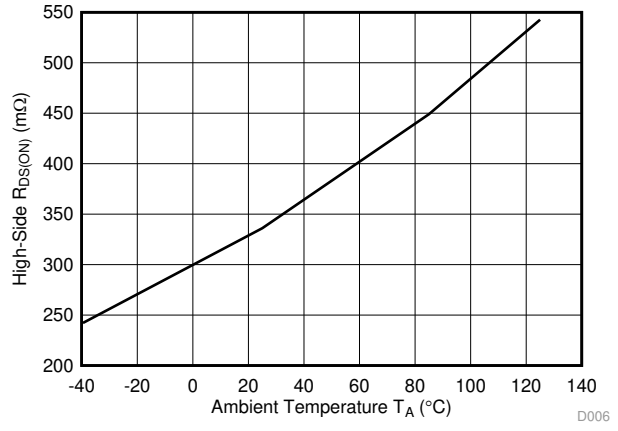


Figure 6. High-Side $R_{DS(ON)}$ over Temperature (VM = 12 V)

Typical Characteristics (continued)

Over recommended operating conditions (unless otherwise noted)

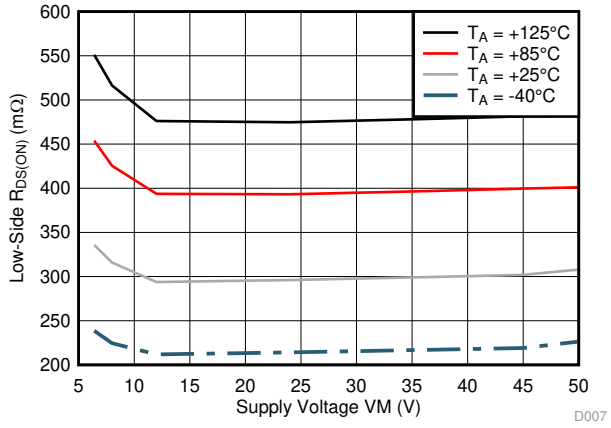


Figure 7. Low-Side $R_{DS(ON)}$ over VM

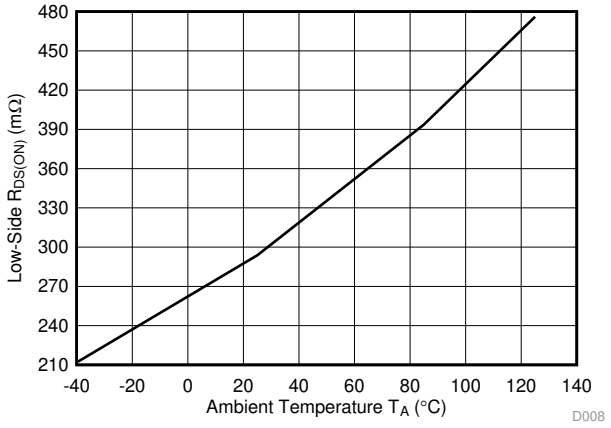


Figure 8. Low-Side $R_{DS(ON)}$ over Temperature (VM = 12 V)

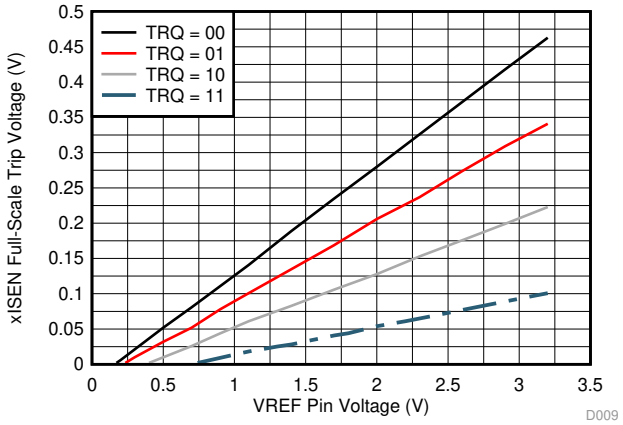


Figure 9. xISEN Trip Voltage over VREF Input

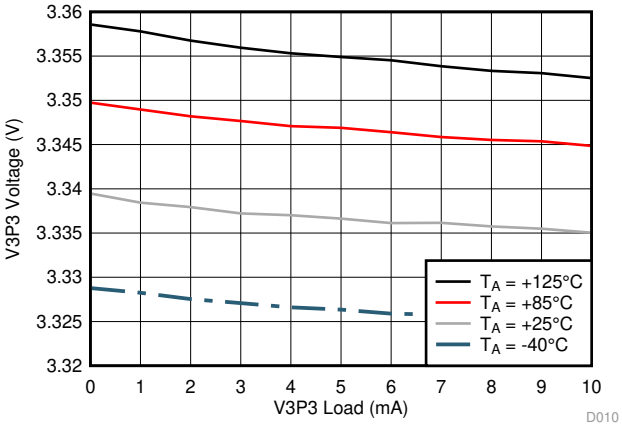


Figure 10. V3P3 Regulator over Load (VM = 24 V)

7 Detailed Description

7.1 Overview

The DRV8881 is an integrated motor driver solution for bipolar stepper motors or single/dual brushed-DC motors. The device integrates two NMOS H-bridges and current regulation circuitry. The DRV8881 can be powered with a supply voltage between 6.5 and 45 V, and is capable of providing an output current up to 2.5 A peak or 1.4 A rms per H-bridge. Actual operable rms current will depend on ambient temperature, supply voltage, and PCB ground plane size.

A simple PH/**E**N (DRV8881**E**) or **P**WM (DRV8881**P**) interface allows easy interfacing to the controller circuit.

The current regulation is highly configurable, with several decay modes of operation. The decay mode can be selected as a fixed slow, mixed, or fast decay.

In addition, an smart tune mode can be used which automatically adjusts the decay setting to minimize current ripple while still reacting quickly to step changes. This feature greatly simplifies stepper driver integration into a motor drive system. Smart tune is only available on the DRV8881E.

The PWM off-time, t_{OFF}, can be adjusted to 10, 20, or 30 μs.

An adaptive blanking time feature automatically scales the minimum drive time with output current. This helps alleviate current waveform distortion by limiting the drive time at low-currents.

A torque DAC feature allows the controller to scale the output current without needing to scale the analog reference voltage inputs AVREF and BVREF. The torque DAC is accessed using digital input pins. This allows the controller to save power by decreasing the current consumption when not required.

In the DRV8881P, a parallel mode allows the user to parallel the two H-bridge outputs in order to double the current capacity.

A low-power sleep mode is included which allows the system to save power when not driving the motor.

7.2 Functional Block Diagrams

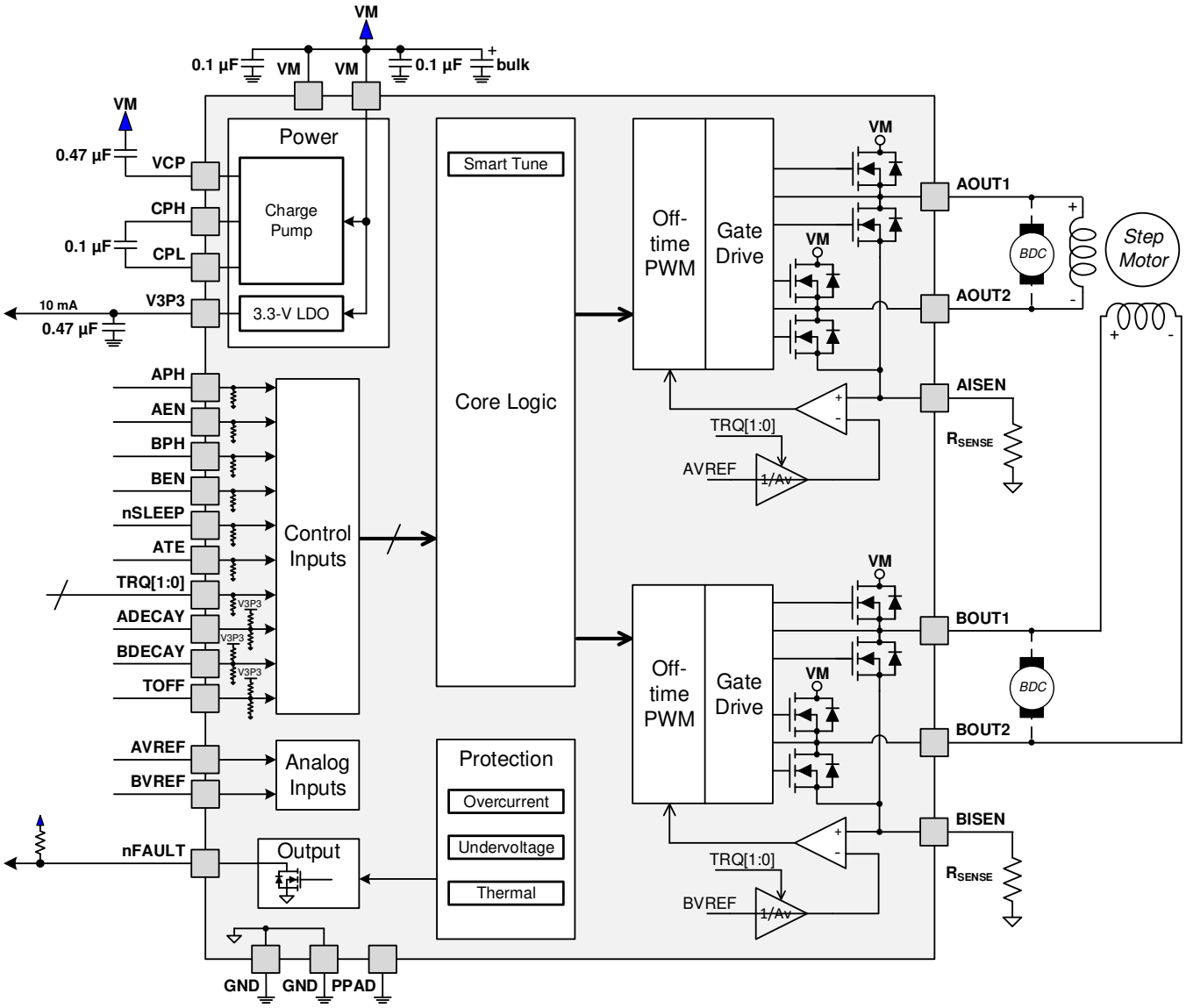


Figure 11. DRV8881E Block Diagram

Functional Block Diagrams (continued)

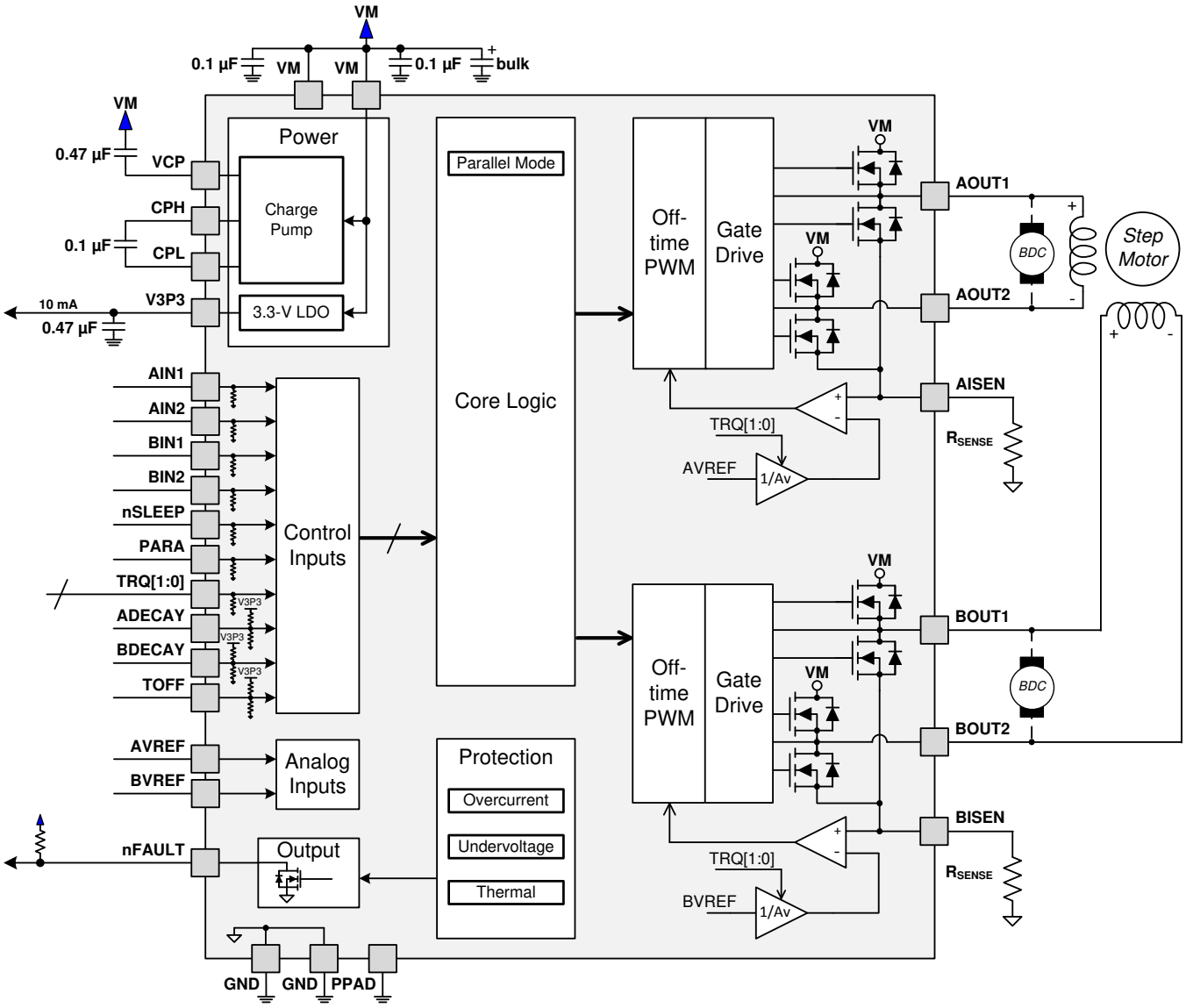


Figure 12. DRV8881P Block Diagram

7.3 Feature Description

7.3.1 Motor Driver Current Ratings

Brushed motor drivers can be classified using two different numbers to describe the output current: peak and rms. Stepper motor drivers can be described with three numbers: peak, rms, and full-scale.

7.3.1.1 Peak Current Rating

The peak current in a motor driver is limited by the overcurrent protection trip threshold I_{OCP}. The peak current describes any transient duration current pulse, for example when charging capacitance, when the overall duty cycle is very low. In general the minimum value of I_{OCP} specifies the peak current rating of the motor driver. For the DRV8881, the peak current rating is 2.5 A per bridge.

7.3.1.2 RMS Current Rating

The rms (average) current is determined by the thermal considerations of the IC. The rms current is calculated based on the $R_{DS(ON)}$, rise and fall time, PWM frequency, device quiescent current, and package thermal performance in a typical system at 25°C. The real operating rms current may be higher or lower depending on heatsinking and ambient temperature. For the DRV8881, the rms current rating is 1.4 A per bridge. In parallel mode, the DRV8881P is capable of double the rms output current, or 2.8 A.

7.3.1.3 Full-Scale Current Rating

The full-scale current for a stepper motor describes the top of the sinusoid current waveform while stepping. Since the sineusoid amplitude is related to the rms current, the full-scale current is also determined by the thermal considerations of the IC. The full-scale current rating is approximately $\sqrt{2} \times I_{rms}$. The full-scale current is set by xVREF, the sense resistor, and Torque DAC when configuring the DRV8881. For the DRV8881, the full-scale current rating is 2.0 A per bridge.

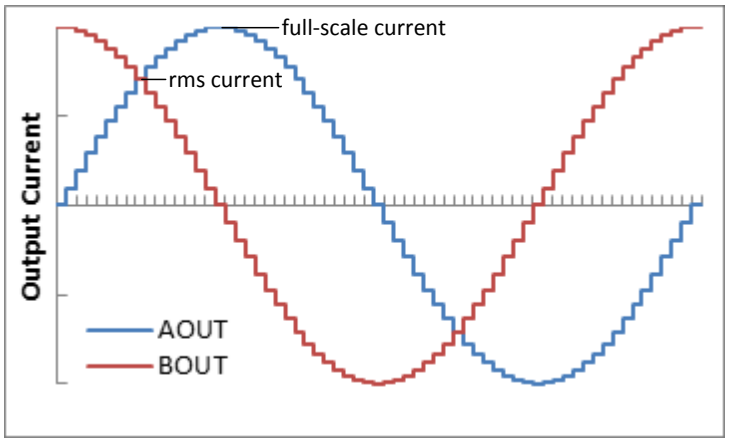


Figure 13. Full-Scale and rms Current

Feature Description (continued)

7.3.2 PWM Motor Drivers

The DRV8881 contains drivers for two full H-bridges. Figure 14 shows a block diagram of the circuitry.

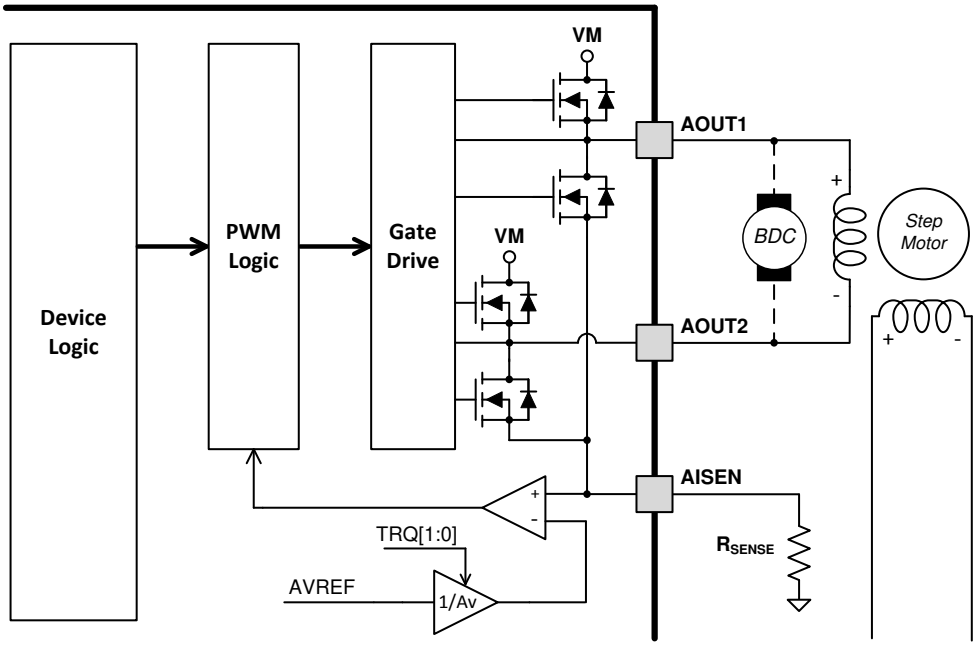


Figure 14. PWM Motor Driver Block Diagram

7.3.3 Bridge Control

The DRV8881E is controlled using a PH/EN interface. Table 1 gives the full H-bridge state. Note that this table does not take into account the current control built into the DRV8881E. Positive current is defined in the direction of xOUT1 → xOUT2.

Table 1. DRV8881E (PH/EN) Control Interface

nSLEEP	ENx	PHx	xOUT1	xOUT2	V3P3	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Disabled	Sleep mode; H-bridge disabled Hi-Z
1	0	X	Hi-Z	Hi-Z	Enabled	H-bridge disabled Hi-Z
1	1	0	L	H	Enabled	Reverse (current xOUT2 → xOUT1)
1	1	1	H	L	Enabled	Forward (current xOUT1 → xOUT2)

The DRV8881P is controlled using a PWM interface. Table 2 gives the full H-bridge state. Note that this table does not take into account the current control built into the DRV8881P. Positive current is defined in the direction of xOUT1 → xOUT2.

Table 2. DRV8881P (PWM) Control Interface

nSLEEP	xIN1	xIN2	xOUT1	xOUT2	V3P3	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Disabled	Sleep mode; H-bridge disabled Hi-Z
1	0	0	Hi-Z	Hi-Z	Enabled	Coast; H-bridge disabled Hi-Z
1	0	1	L	H	Enabled	Reverse (current xOUT2 → xOUT1)
1	1	0	H	L	Enabled	Forward (current xOUT1 → xOUT2)
1	1	1	L	L	Enabled	Brake; low-side slow decay

7.3.4 Current Regulation

The current through the motor windings is regulated by an adjustable fixed-off-time PWM current regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. Once the current hits the current chopping threshold, the bridge enters a decay mode for a fixed period of time to decrease the current, which is configurable between 10 and 30 µs through the tri-level input TOFF. After the off time expires, the bridge is re-enabled, starting another PWM cycle.

Table 3. Off-Time Settings

TOFF	OFF-TIME t_{OFF}
0	20 µs
1	30 µs
Z	10 µs

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pin with a reference voltage. To generate the reference voltage for the current chopping comparator, the xVREF input is attenuated by a factor of Av. In addition, the TRQx pins further scale the reference.

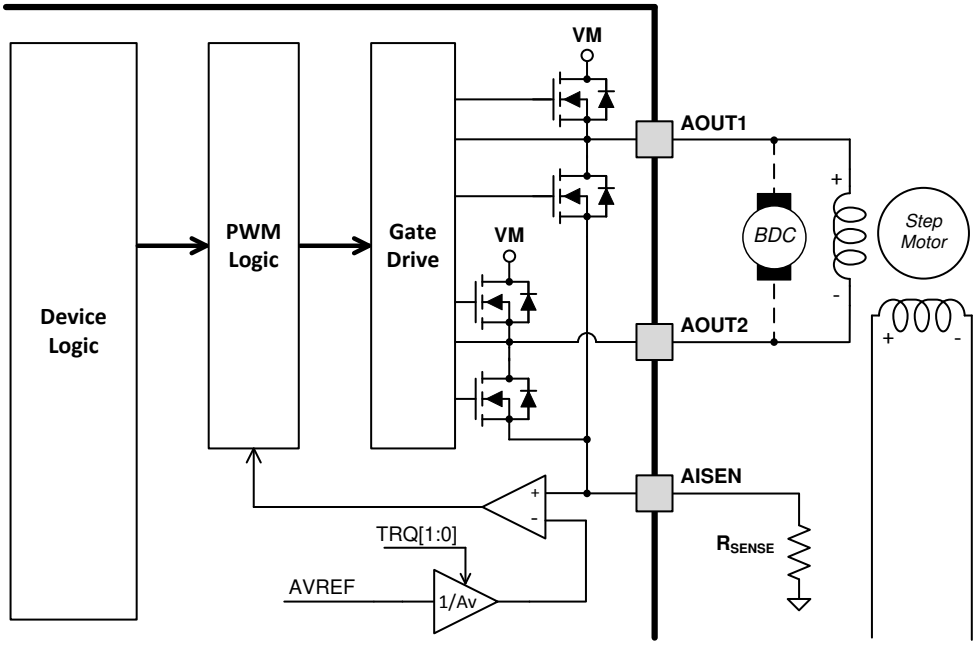


Figure 15. Current Regulation Block Diagram

The chopping current is calculated as follows:

$$I_{TRIP}\ (A) = \frac{VREF\ (V) \times TRQ\ (\%)}{A_v \times R_{SENSE}\ (\Omega)} = \frac{VREF\ (V) \times TRQ\ (\%)}{6.6 \times R_{SENSE}\ (\Omega)} \quad (1)$$

TRQ is a DAC used to scale the output current. The current scalar value for different inputs is shown in Table 4.

Table 4. Torque DAC Settings

TRQ1	TRQ0	CURRENT SCALAR (TRQ)	EFFECTIVE ATTENUATION
1	1	25%	26.4 V/V
1	0	50%	13.2 V/V
0	1	75%	8.8 V/V
0	0	100%	6.6 V/V

7.3.5 Decay Modes

A fixed decay mode is selected by setting the tri-level ADECAY and BDECAY pins as shown in Table 5. Note that if the ATE pin is logic high, the ADECAY and BDECAY pins are ignored and smart tune is used.

Table 5. Decay Mode Settings

xDECAY	DECAY MODE
0	Slow decay
Z	Fast decay
1	Mixed decay: 30% fast

The ADECAY pin sets the decay mode for H-bridge A (AOUT1, AOUT2), and the BDECAY pin sets the decay mode for H-bridge B (BOUT1, BOUT2).

7.3.5.1 Mode 1: Slow Decay

To configure the DRV8881 into this mode, pull DECAY1 and DECAY0 logic low.

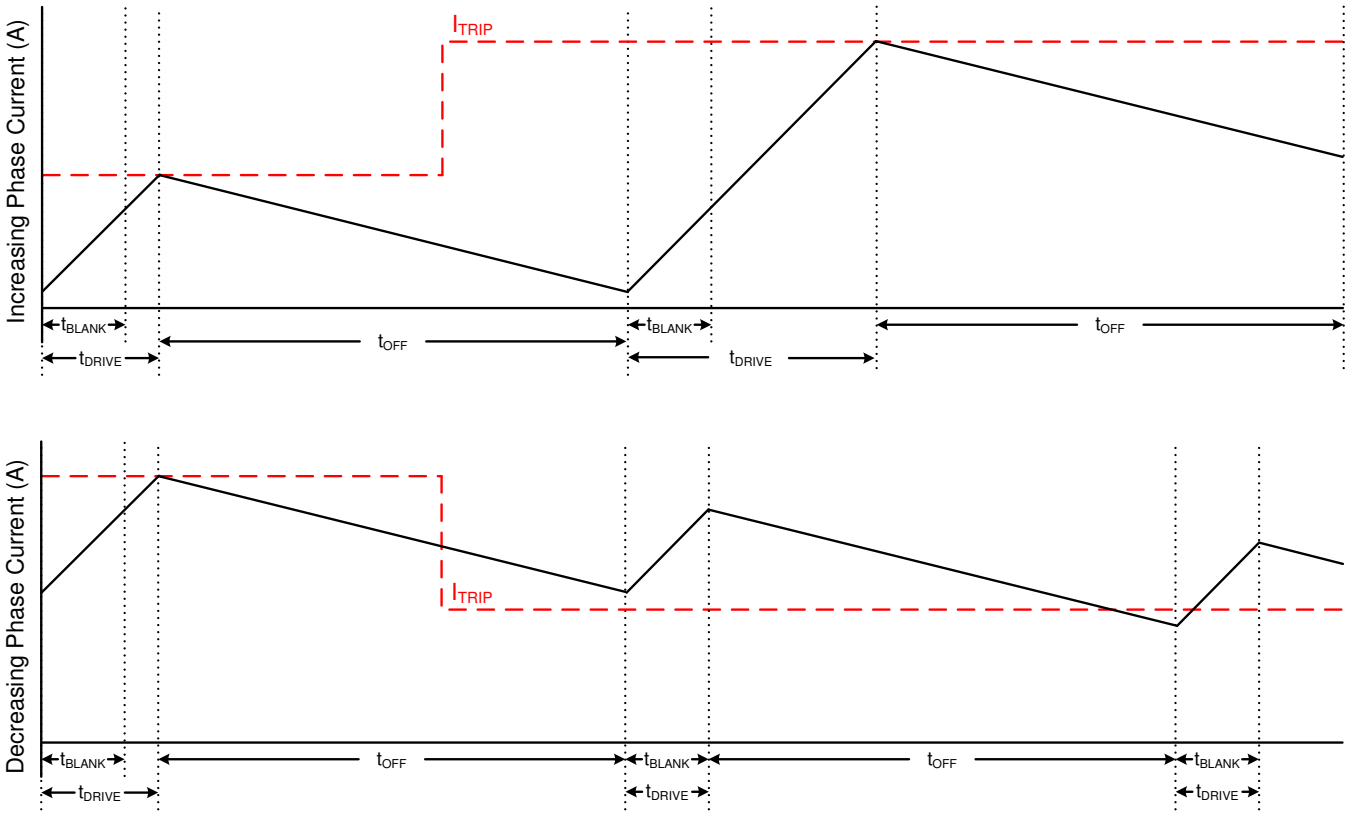


Figure 16. Slow Decay Mode

During slow decay, both of the low-side FETs of the H-bridge are turned on, allowing the current to be recirculated.

Slow decay exhibits the least current ripple of the decay modes for a given t_{OFF}. However, if the current trip level is decreasing, slow decay will take a long time to settle to the new I_{TRIP} level because the current decreases very slowly.

7.3.5.2 Mode 2: Fast Decay

To configure the DRV8881 into this mode, pull DECAY1 and DECAY0 logic high.

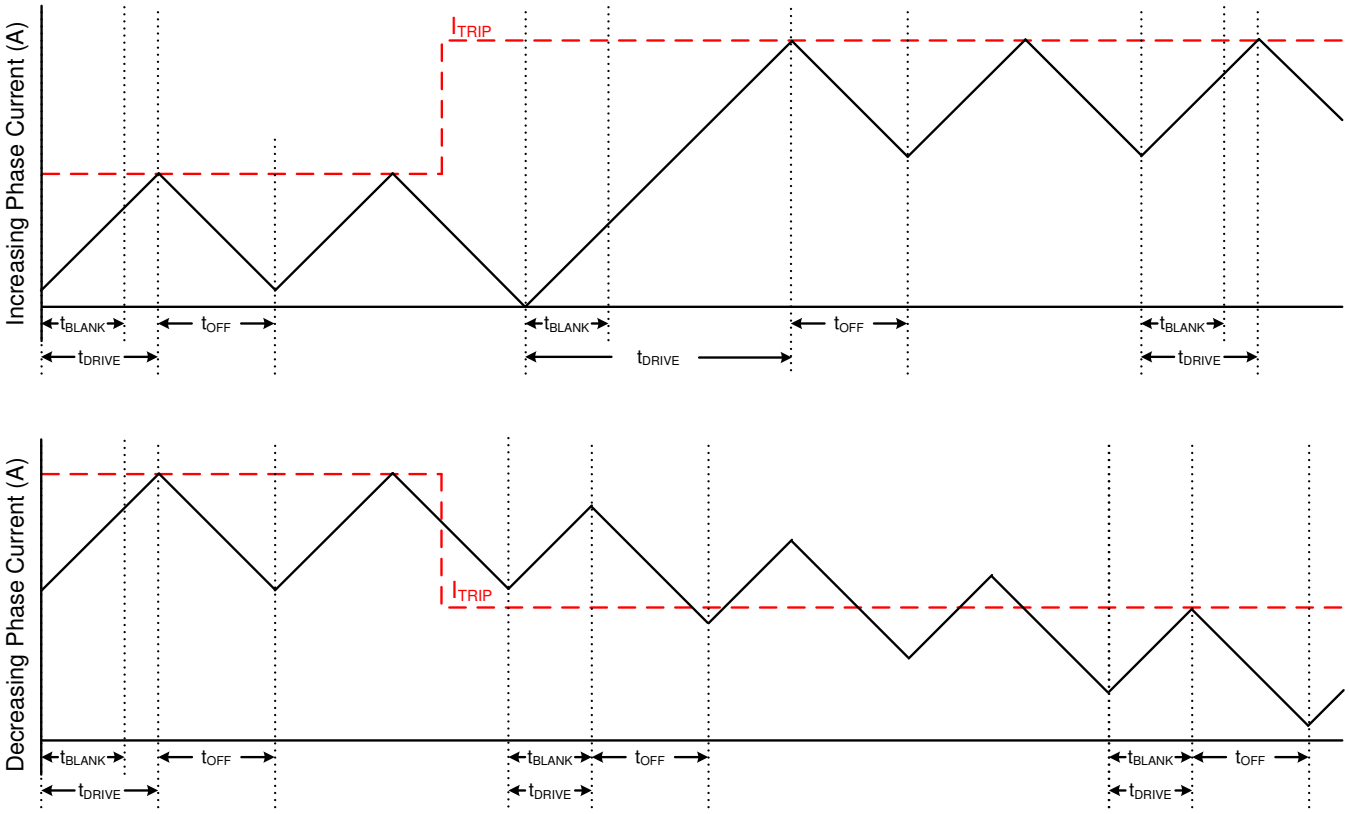


Figure 17. Fast Decay Mode

During fast decay, the polarity of the H-bridge is reversed. The H-bridge will be turned off as current approaches zero in order to prevent current flow in the reverse direction.

Fast decay exhibits the highest current ripple of the decay modes for a given t_{OFF}. Transition time on decreasing current is much faster than slow decay since the current is allowed to decrease much faster.

7.3.5.3 Mode 3: 30%/70% Mixed Decay

To configure the DRV8881 into this mode, pull DECAY1 logic high and pull DECAY0 logic low.

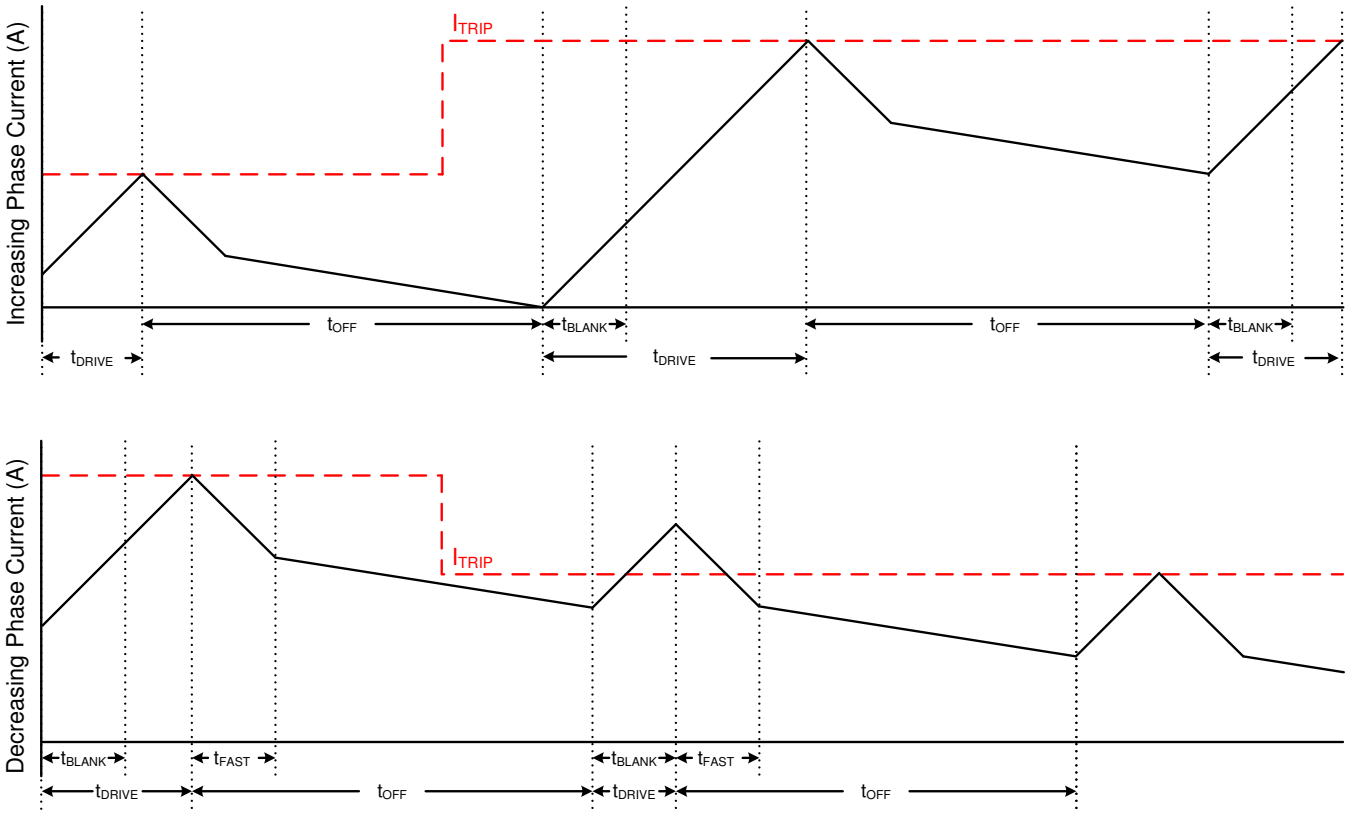


Figure 18. Mixed Decay Mode (30% Fast, 70% Slow)

Mixed decay begins as fast decay for 30% of t_{OFF}, followed by slow decay for the remainder of t_{OFF}. In this mode, mixed decay occurs for both increasing and decreasing current steps.

This mode exhibits ripple larger than slow decay, but smaller than fast decay. Mixed decay will settle to the new I_{TRIP} level faster than slow decay when dealing with decreasing current trip levels.

In cases where current is held for a long time or at very-low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and requires an excessively large off-time. Increasing/decreasing mixed decay mode allows the current level to stay in regulation when no back-EMF is present across the motor windings.

7.3.6 Smart tune

Smart tune is available on DRV8881E only.

To enable the smart tune mode, pull the ATE pin logic high. Ensure the xDECAY pins are logic low. The smart tune mode is registered internally when exiting from sleep mode or the power-up sequence. The ATE pin can be shorted to V3P3 to pull it logic high for this purpose.

Smart tune greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle in order to prevent regulation loss. If there is a long drive time to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle in order to operate with less ripple and more efficiently.

Smart tune will automatically adjust the decay scheme based on operating factors like:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Motor back-EMF difference on rising and falling steps
- Low-current vs. high-current dI/dt

7.3.7 Adaptive Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a period of time before enabling the current sense circuitry. Note that the blanking time also sets the minimum drive time of the PWM.

The time t_{BLANK} is determined by VREF and the torque DAC setting. The timing information for t_{BLANK} is given in Table 6.

Table 6. Adaptive Blanking Time Settings over Torque DAC and xVREF Input Voltage

xVREF	TORQUE DAC TRQ[1:0] SETTING			
	00 - 100%	01 - 75%	10 - 50%	11 - 25%
2.475 → 3.300 V	1.80 µs	1.50 µs	1.20 µs	0.90 µs
1.650 → 2.475 V	1.50 µs	1.20 µs	0.90 µs	0.90 µs
0.825 → 1.650 V	1.20 µs	0.90 µs	0.90 µs	0.90 µs
0.000 → 0.825 V	0.90 µs	0.90 µs	0.90 µs	0.90 µs

7.3.8 Parallel Mode

To enter parallel mode on the DRV8881P, the PARA pin must be logic high during device power-up or when exiting the sleep mode. The PARA pin can be shorted to V3P3 to pull it logic high for this purpose.

In this mode, the AIN1 and AIN2 pins control the state of the outputs and the BIN1 and BIN2 pins are ignored. Similarly, the ADECAY pin controls the decay mode of the output and AVREF is used as the analog reference voltage. The BIN1, BIN2, BDECAY, and BVREF pins can be tied to GND or left Hi-Z.

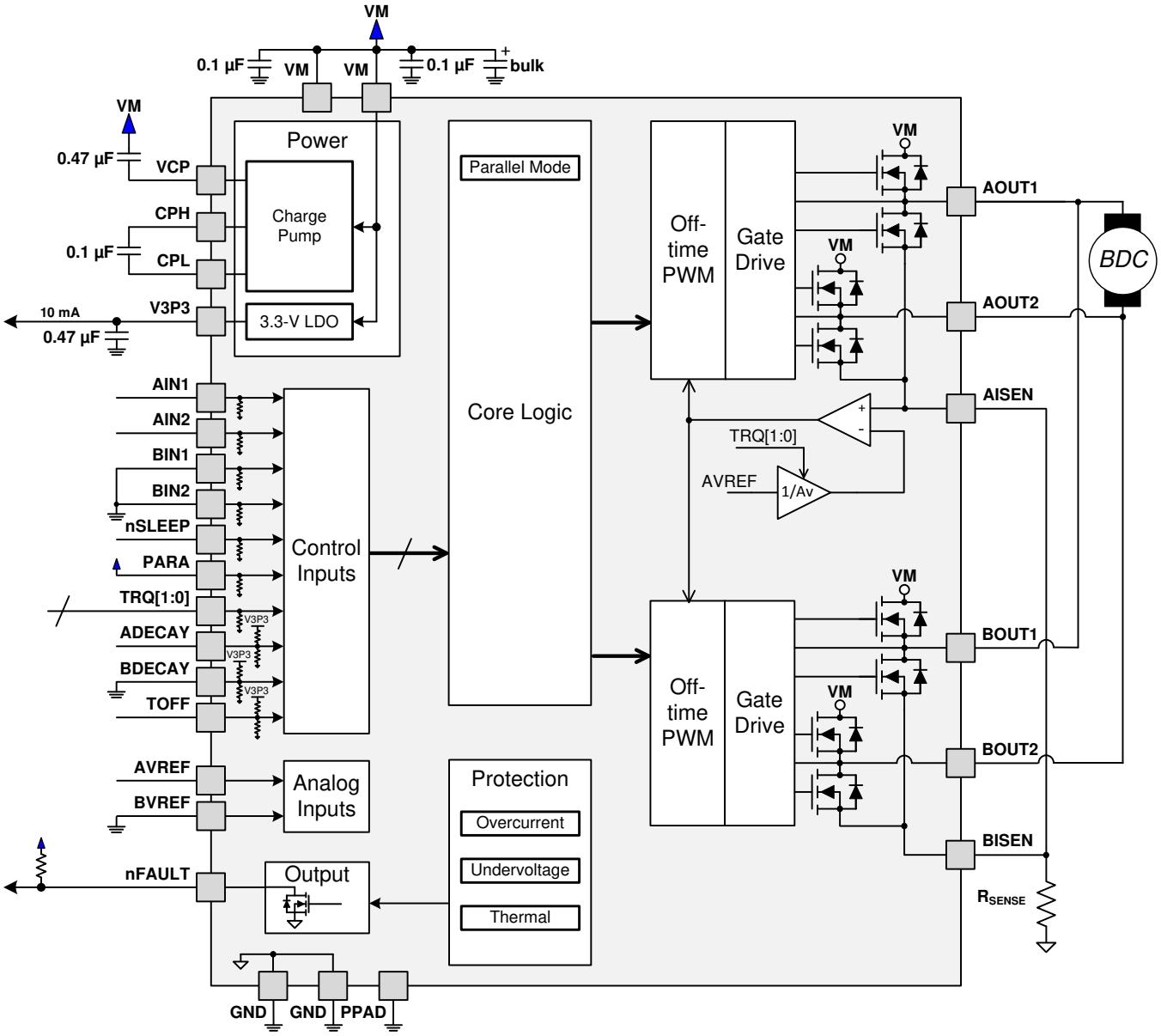


Figure 19. Parallel Mode Diagram

7.3.9 Charge Pump

A charge pump is integrated in order to supply a high-side NMOS gate drive voltage. The charge pump requires a capacitor between the VM and VCP pins. Additionally a low-ESR ceramic capacitor is required between pins CPH and CPL.

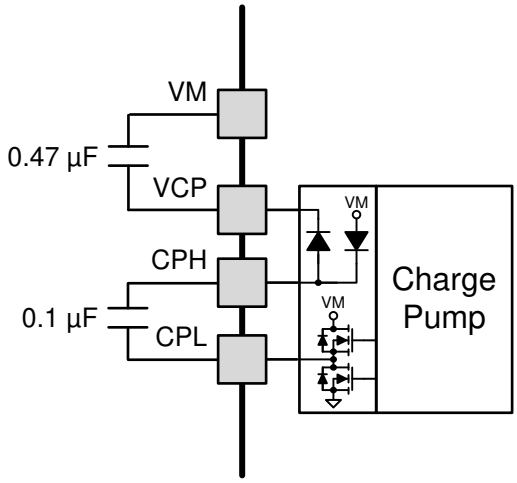


Figure 20. Charge Pump Diagram

7.3.10 LDO Voltage Regulator

An LDO regulator is integrated into the DRV8881. It can be used to provide the supply voltage for a low-power microcontroller or other low-current devices. For proper operation, bypass V3P3 to GND using a ceramic capacitor.

The V3P3 output is nominally 3.3 V. When the V3P3 LDO current load exceeds 10 mA, the LDO will behave like a constant current source. The output voltage will drop significantly with currents greater than 10 mA.

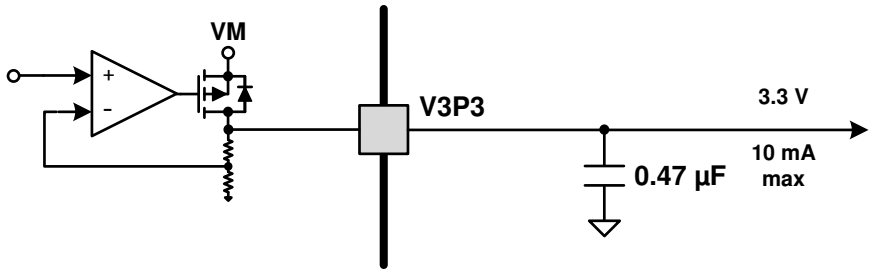


Figure 21. LDO Diagram

If a digital input needs to be tied permanently high (that is, TOFF or ADECAY), it is preferable to tie the input to V3P3 instead of an external regulator. This will save power when VM is not applied or in sleep mode: V3P3 is disabled and current will not be flowing through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 100 kΩ, and tri-level inputs have a typical pulldown of 40 kΩ.

7.3.11 Logic and Tri-Level Pin Diagrams

Figure 22 gives the input structure for logic-level pins APH/AIN1, AEN/AIN2, BPH/BIN1, BEN/BIN2, nSLEEP, ATE/PARA, TRQ0, TRQ1:

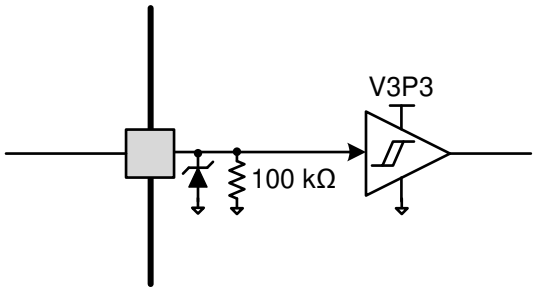


Figure 22. Logic-level Input Pin Diagram

Tri-level logic pins TOFF, ADECAY, and BDECAY have the following structure as shown in Figure 23.

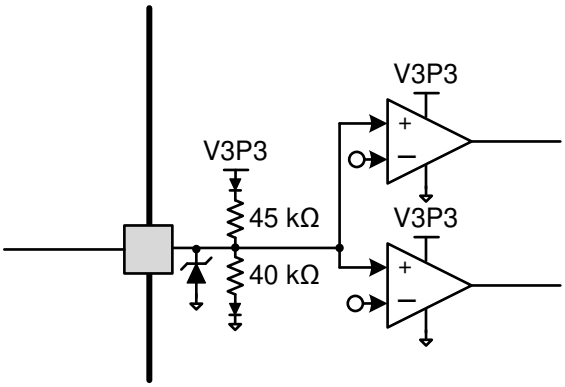


Figure 23. Tri-Level Input Pin Diagram

7.3.12 Protection Circuits

The DRV8881 is fully protected against VM undervoltage, charge pump undervoltage, overcurrent, and overtemperature events.

7.3.12.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge will be disabled, the charge pump will be disabled, and the nFAULT pin will be driven low. Operation will resume when VM rises above the UVLO threshold. The nFAULT pin will be released after operation has resumed.

7.3.12.2 VCP UVLO (CPUV)

If at any time the voltage on the VCP pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Operation will resume when VCP rises above the CPUV threshold. The nFAULT pin will be released after operation has resumed.

7.3.12.3 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{OCP}, all FETs in the H-bridge will be disabled and nFAULT will be driven low. In addition to this FET current limit, an overcurrent condition is also detected if the voltage at xISEN exceeds V_{OCP}.

For the DRV8881E (PH/EN), both H-bridges are shut down when either bridge encounters an overcurrent fault. For the DRV8881P (PWM), only the H-bridge driver experiencing the overcurrent fault is shut down, and the other bridge will remain active.

The driver will be re-enabled after the OCP retry period (t_{RETRY}) has passed. nFAULT becomes high again after the retry time. If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes and nFAULT remains deasserted.

7.3.12.4 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. After the die temperature has fallen to a safe level, operation will automatically resume. The nFAULT pin will be released after operation has resumed.

Table 7. Fault Condition Summary

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	V3P3	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO} (max 6.4 V)	nFAULT	Disabled	Disabled	Operating	VM > V_{UVLO} (max 6.5 V)
VCP undervoltage (CPUV)	VCP < V_{CPUV} (typ VM + 1.8 V)	nFAULT	Disabled	Operating	Operating	VCP > V_{CPUV} (typ VM + 1.9 V)
Thermal shutdown (TSD)	T_J > T_{TSD} (min 150°C)	nFAULT	Disabled	Operating	Operating	T_J < T_{TSD}- T_{HYS} (T_{HYS} typ 35°C)
Overcurrent (OCP)	IOUT > I_{OCP} (min 2.5 A) VxISEN > V_{OCP} (min 0.9 V)	nFAULT	Disabled	Operating	Operating	t_{RETRY}

7.4 Device Functional Modes

The DRV8881 is active unless the nSLEEP pin is brought logic low. In sleep mode the charge pump is disabled, the H-bridge FETs are disabled Hi-Z, and the V3P3 regulator is disabled. Note that t_{SLEEP} must elapse after a falling edge on the nSLEEP pin before the device is in sleep mode. The DRV8881 is brought out of sleep mode automatically if nSLEEP is brought logic high. Note that t_{WAKE} must elapse before the outputs change state after wake-up.

Table 8. Functional Modes Summary

FAULT	CONDITION	H-BRIDGE	CHARGE PUMP	V3P3
Operating	6.5 V < VM < 45 V nSLEEP pin = 1	Operating	Operating	Operating
Sleep mode	6.5 V < VM < 45 V nSLEEP pin = 0	Disabled	Disabled	Disabled
Fault encountered	VM undervoltage (UVLO)	Disabled	Disabled	Operating
	VCP undervoltage (CPUV)	Disabled	Operating	Operating
	Overcurrent (OCP)	Disabled	Operating	Operating
	Thermal shutdown (TSD)	Disabled	Operating	Operating

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8881 is used in stepper or brushed motor control.

8.2 Typical Applications

8.2.1 DRV8881P Typical Application

The following design procedure can be used to configure the DRV8881. In this application, the DRV8881P will be used to drive a stepper motor.

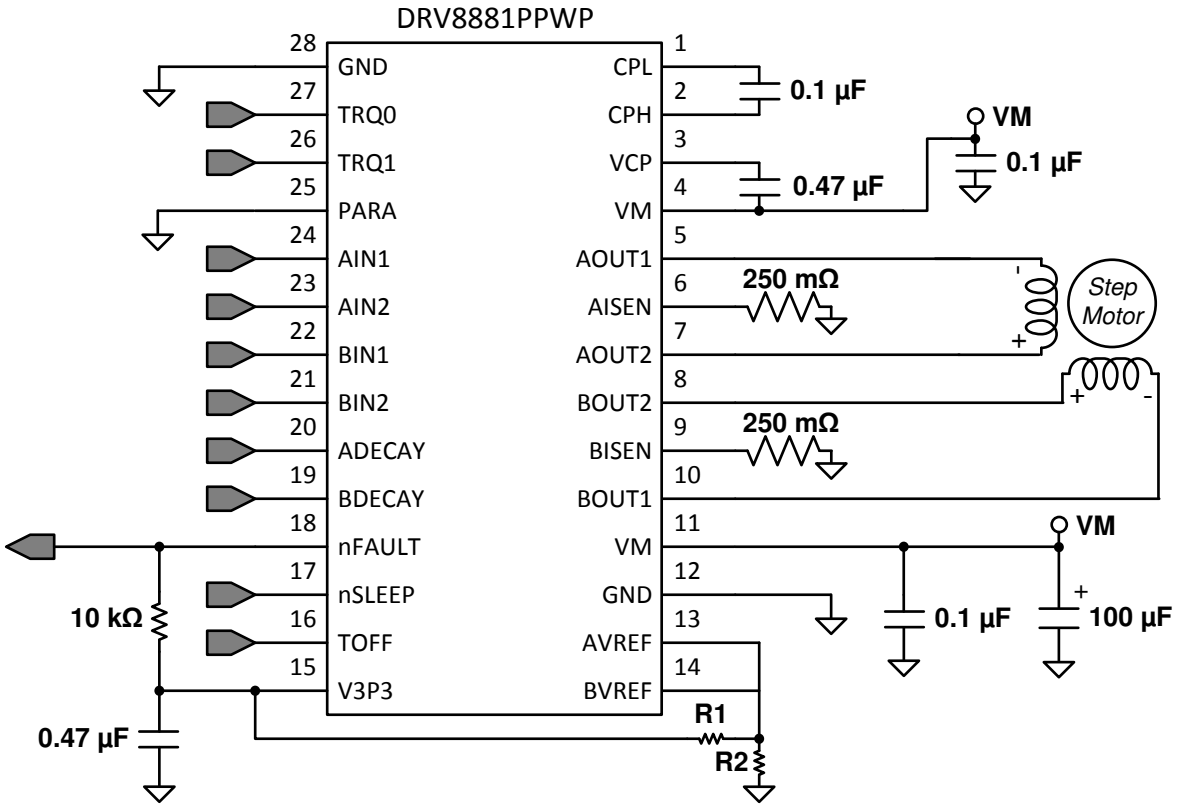


Figure 24. Typical Application Schematic

Typical Applications (continued)

8.2.1.1 Design Requirements

Table 9 gives design input parameters for system design.

Table 9. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	4.5 Ω/phase
Motor winding inductance	L_L	10.5 mH/phase
Motor full step angle	θ_{step}	1.8°/step
Target microstepping level	n_m	Non-circular 1/2 step
Target motor speed	v	120 rpm
Target full-scale current	I_{FS}	800 mA

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Current Regulation

In a stepper motor, the full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity will depend on the TRQ pins, the xVREF analog voltage, and the sense resistor value (R_{SENSE}). AVREF and BVREF can be configured to drive different currents, but in this example the same full-scale current is used in both coils.

$$I_{FS}\ (A) = \frac{xVREF\ (V) \times TRQ\ (\%)}{A_v \times R_{SENSE}\ (\Omega)} = \frac{xVREF\ (V) \times TRQ\ (\%)}{6.6 \times R_{SENSE}\ (\Omega)} \quad (2)$$

TRQ is a DAC used to scale the output current. The current scalar value for different inputs is shown in Table 10.

Table 10. Torque DAC Settings

TRQ1	TRQ0	CURRENT SCALAR (TRQ)
1	1	25%
1	0	50%
0	1	75%
0	0	100%

Example: If the desired full-scale current is 800 mA

Set R_{SENSE} = 250 mΩ, assume TRQ = 100%.

xVREF would have to be 1.32 V.

Create a resistor divider from V3P3 (3.3 V) to set AVREF and BVREF ≈ 1.32 V.

Set R2 = 10 kΩ, set R1 = 15 kΩ

Note that I_{FS} must also follow Equation 3 in order to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

$$I_{FS}\ (A) < \frac{VM\ (V)}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega) + R_{SENSE}\ (\Omega)} \quad (3)$$

8.2.1.2.2 Stepper Motor Speed

Next, the driving waveform needs to be planned. In order to command the correct speed, determine the frequency of the input waveform.

If the target motor speed is too high, the motor will not spin. Make sure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}),

$$f_{step}\ (steps/s) = \frac{v\ (rpm) \times 360\ (°/rot)}{\theta_{step}\ (°/step) \times n_m\ (steps/microstep) \times 60\ (s/min)} \quad (4)$$

θ_{step} can be found in the stepper motor data sheet or written on the motor itself.

The frequency f_{step} gives the frequency of input change on the DRV8881P. 1/ f_{step} = t_{STEP} on the diagram below.

$$f_{step}\ (steps/s) = \frac{120\ rpm \times 360°/rot}{1.8°/step \times 1/2\ steps/microstep \times 60\ s/min} = 800\,Hz \quad (5)$$

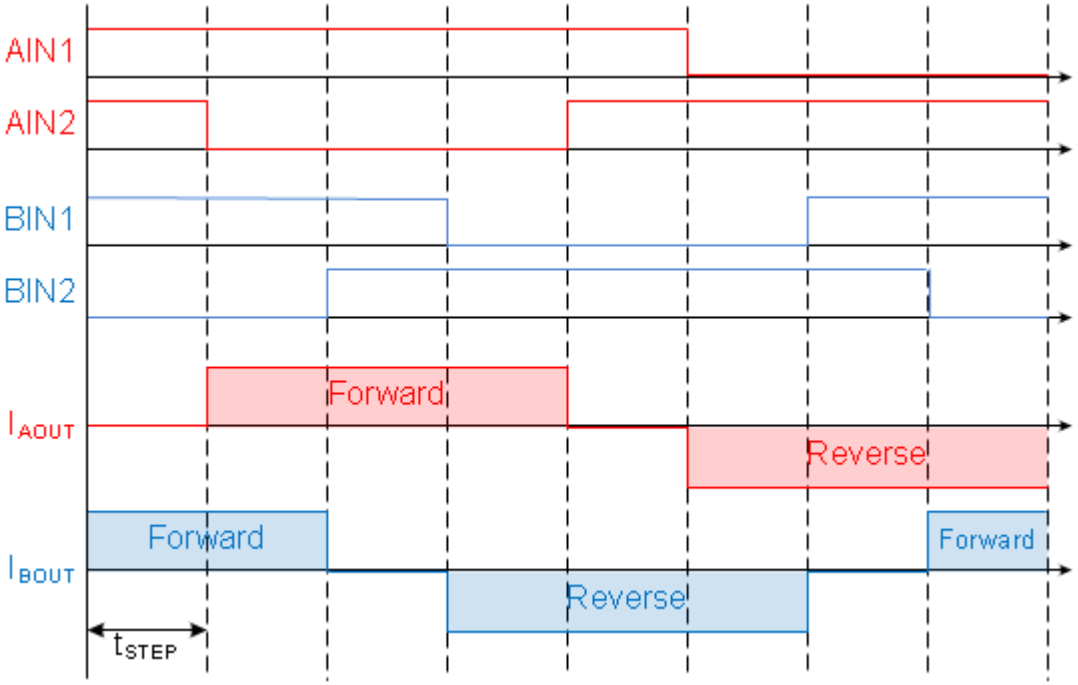


Figure 25. Example 1/2 Stepping Operation

8.2.1.2.3 Decay Modes

The DRV8881 supports several different decay modes: slow decay, fast decay, mixed decay, and smart tune (DRV8881E only). The current through the motor windings is regulated using an adjustable fixed-time-off scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8881 will place the winding in one of the decay modes for TOFF. After TOFF, a new drive phase starts.

8.2.1.2.4 Sense Resistor

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{rms}^2 \times R$. For example, if the rms motor current is 1.4 A and a 250 mΩ sense resistor is used, the resistor will dissipate 1.4 A^2 × 0.25 Ω = 0.49 W. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

8.2.1.3 Application Curve

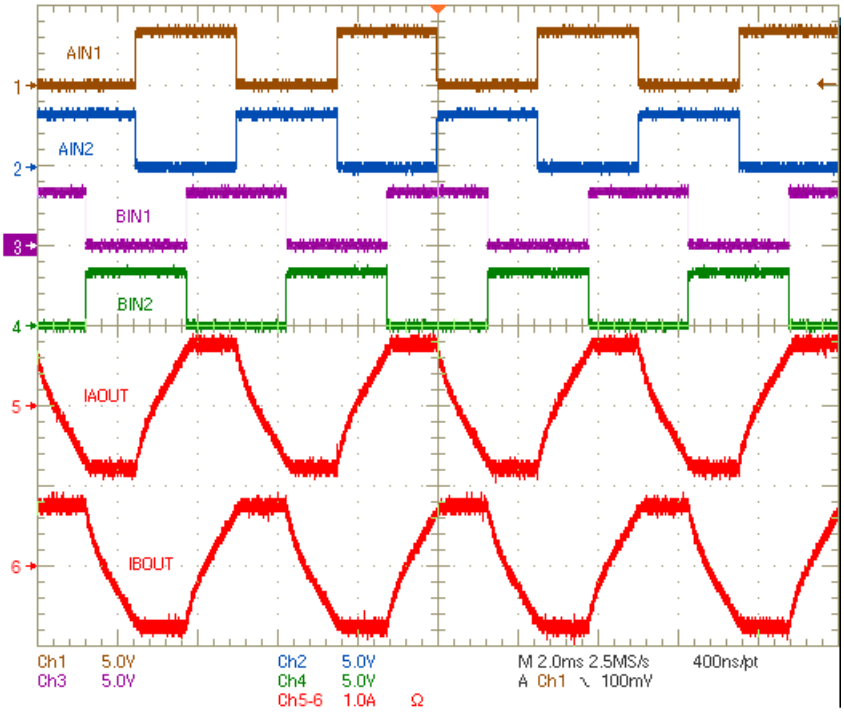


Figure 26. DRV8881P Inputs and Output Current Waveform

8.2.2 Alternate Application

In this application, the DRV8881P will be operated in parallel mode in order to drive a single brushed-DC motor.

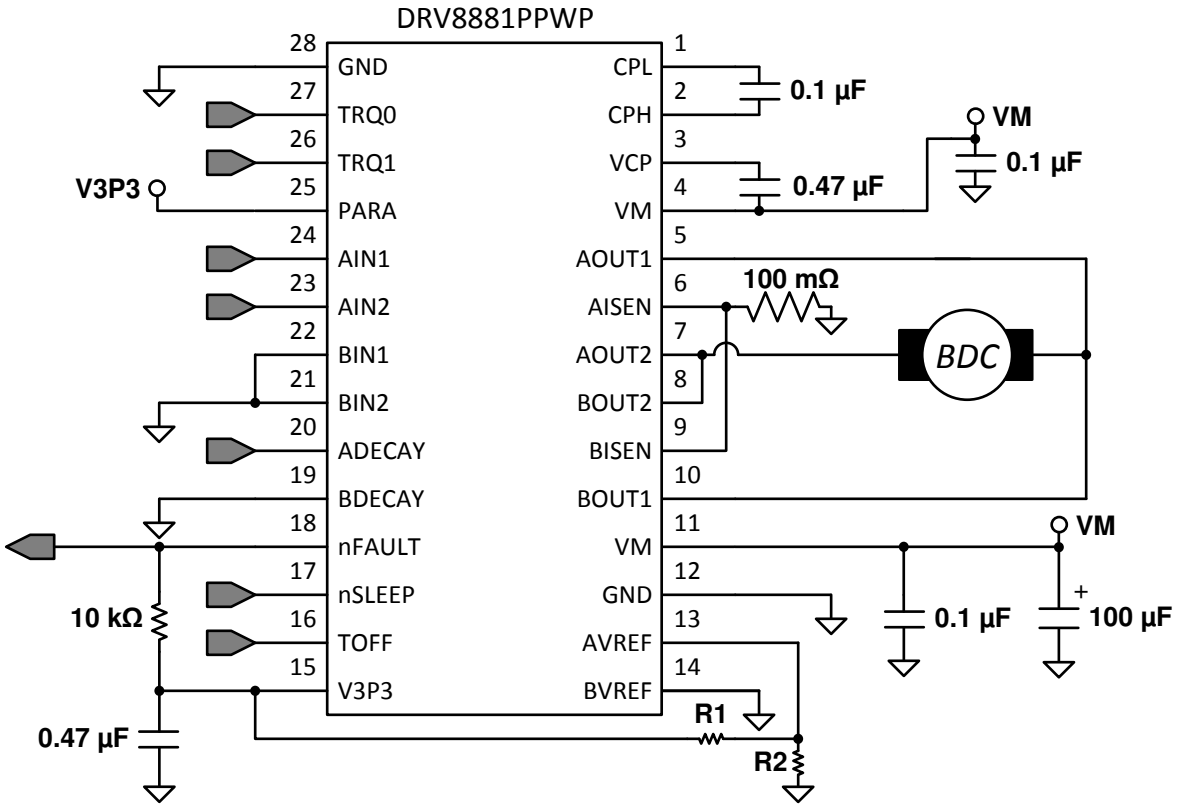


Figure 27. Typical Application Schematic

8.2.2.1 Design Requirements

Table 11 gives design input parameters for system design.

Table 11. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	6 Ω
Motor winding inductance	L_L	4.1 mH
Target maximum motor current	I_{TRIP}	2 A

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Current Regulation

The maximum current (I_{TRIP}) is set by the TRQ pins, the xVREF analog voltage, and the sense resistor value (R_{SENSE}). In parallel mode the winding current is set by AVREF only and BVREF is ignored. When starting a brushed-DC motor, a large inrush current may occur because there is no back-EMF. Current regulation will act to limit this inrush current and prevent high current on startup.

Example: If the desired regulation current is 2 A

Set R_{SENSE} = 100 mΩ, assume TRQ = 100%.

AVREF would have to be 1.32 V.

Create a resistor divider from V3P3 (3.3 V) to set AVREF ≈ 1.32 V: Set R2 = 10 kΩ, set R1 = 15 kΩ

8.2.2.3 Application Curves

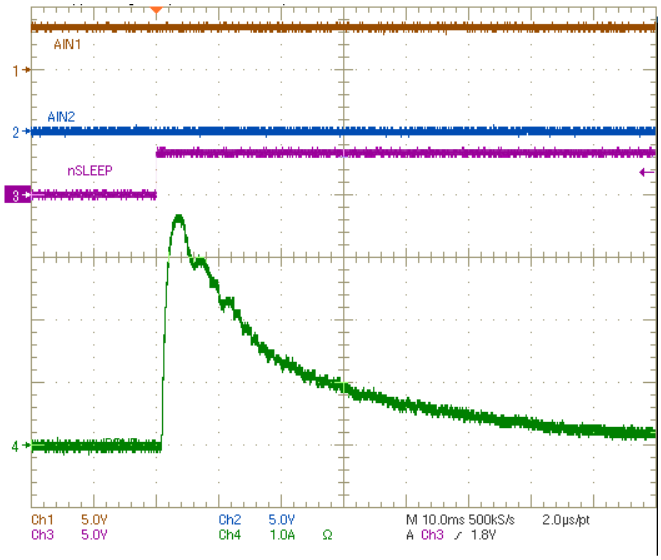


Figure 28. DRV8881P Startup Current Waveform Without Current Regulation

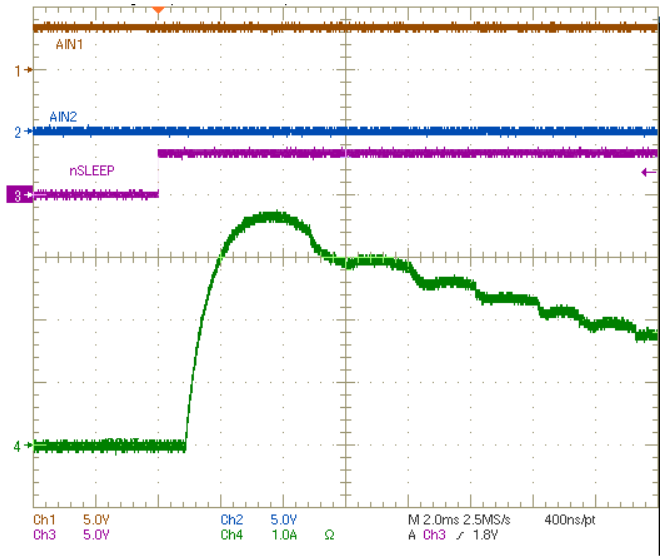


Figure 29. DRV8881P Startup Current Waveform Without Current Regulation (Zoomed In)

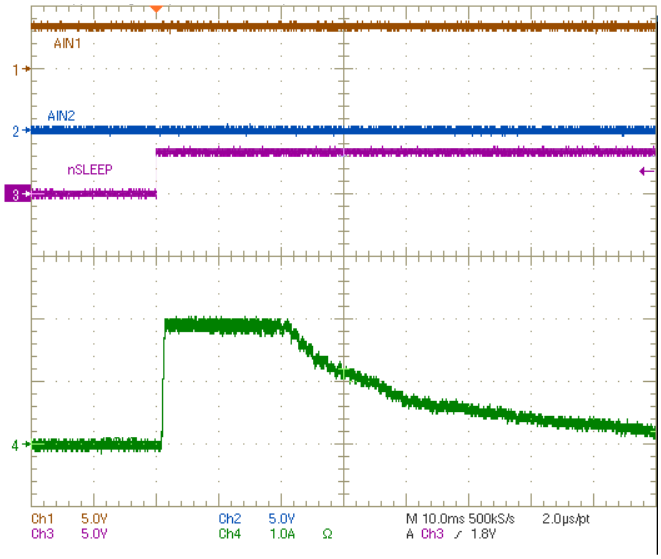


Figure 30. DRV8881P Startup Current Waveform With 2-A Current Regulation

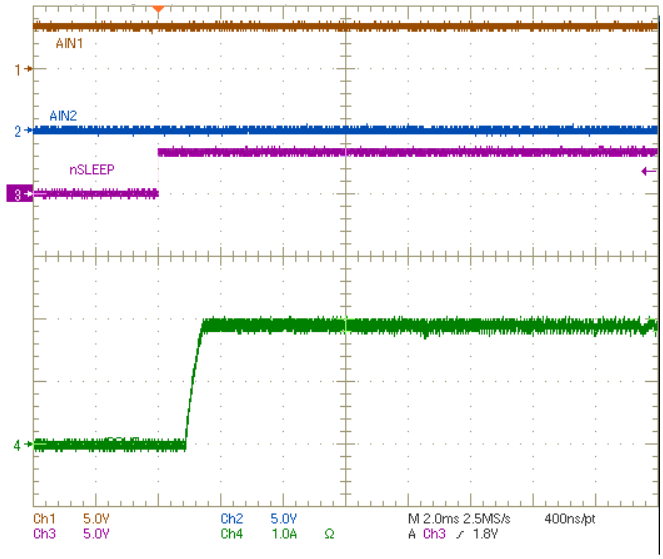


Figure 31. DRV8881P Startup Current Waveform With 2-A Current Regulation (Zoomed In)

9 Power Supply Recommendations

The DRV8881 is designed to operate from an input voltage supply (VM) range between 6.5 V and 45 V. THe device has an absolute maximum rating of 50 V. A 0.1 µF ceramic capacitor rated for VM must be placed at each VM pin as close to the DRV8881 as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

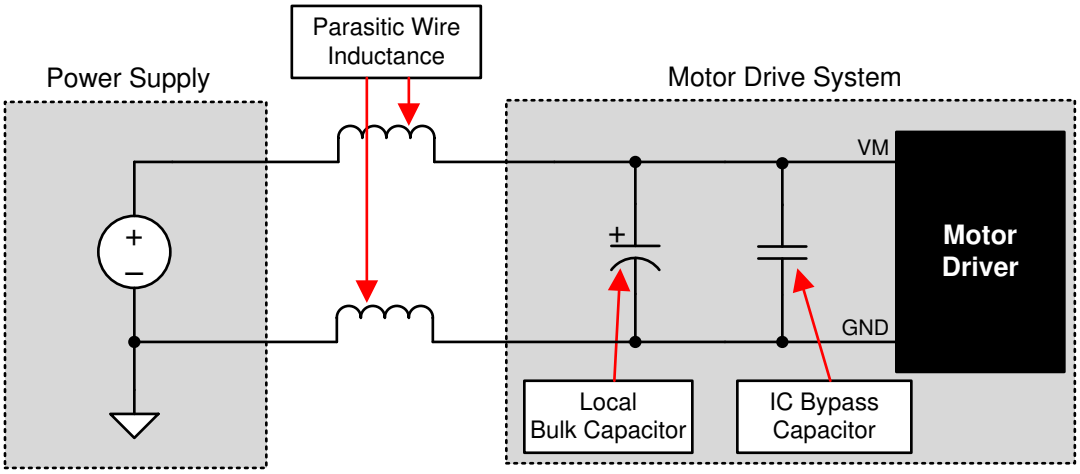


Figure 32. Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

Each VM terminal must be bypassed to GND using a low-ESR ceramic bypass capacitors with recommended values of 0.1 μF rated for VM. These capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device GND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component may be an electrolytic.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.1 μF rated for VM is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.47 μF rated for 16 V is recommended. Place this component as close to the pins as possible.

Bypass V3P3 to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

The current sense resistors should be placed as close as possible to the device pins in order to minimize trace inductance between the pin and resistor.

10.2 Layout Example

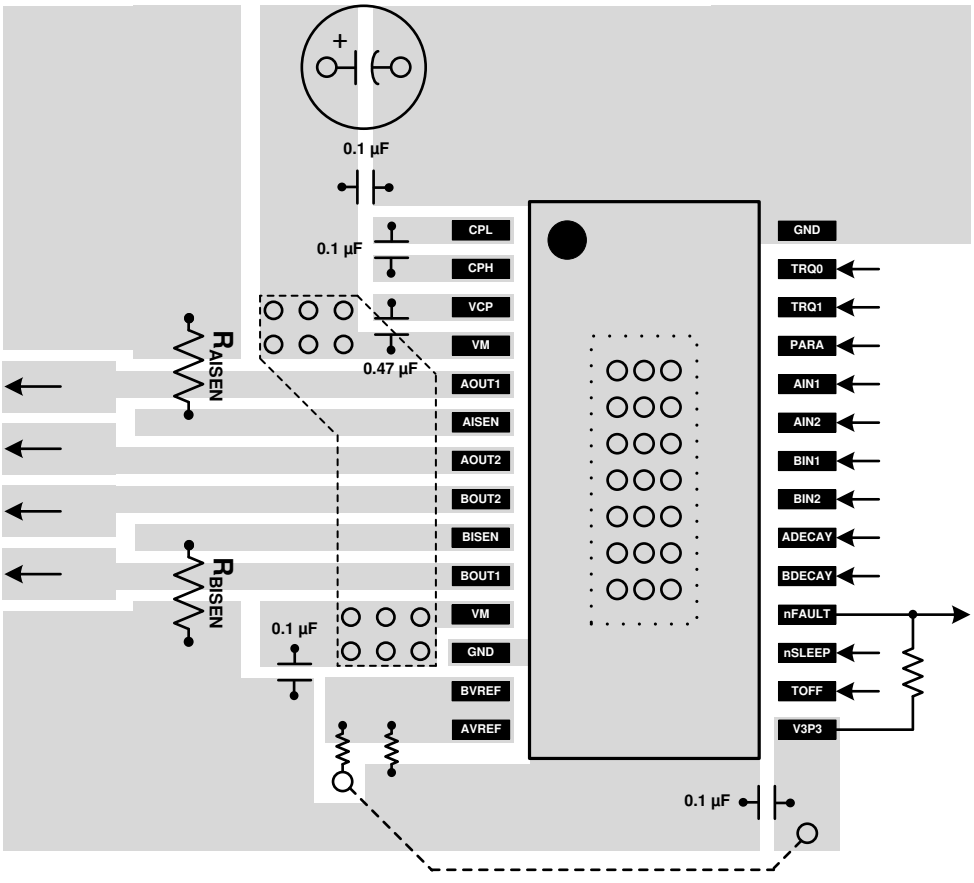


Figure 33. Layout Recommendation

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- *PowerPAD™ Thermally Enhanced Package*, SLMA002
- *PowerPAD™ Made Easy*, SLMA004
- *Current Recirculation and Decay Modes*, SLVA321
- *Calculating Motor Driver Power Dissipation*, SLVA504
- *Understanding Motor Driver Current Ratings*, SLVA505
- *High Resolution Microstepping Driver With the DRV88xx Series*, SLVA416

11.2 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8881EPWP	ACTIVE	HTSSOP	PWP	28	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8881E	Samples
DRV8881EPWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8881E	Samples
DRV8881ERHRR	ACTIVE	WQFN	RHR	28	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8881E	Samples
DRV8881ERHRT	ACTIVE	WQFN	RHR	28	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8881E	Samples
DRV8881PPWP	ACTIVE	HTSSOP	PWP	28	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8881P	Samples
DRV8881PPWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8881P	Samples
DRV8881PRHRR	ACTIVE	WQFN	RHR	28	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8881P	Samples
DRV8881PRHRT	ACTIVE	WQFN	RHR	28	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8881P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

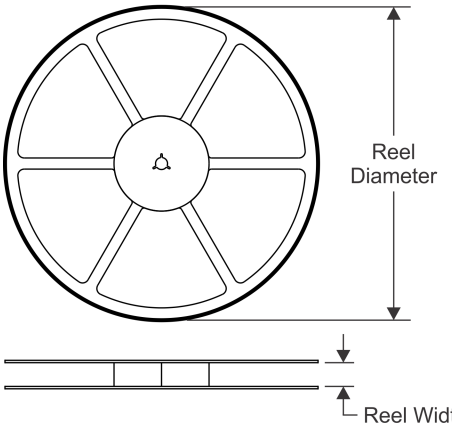
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

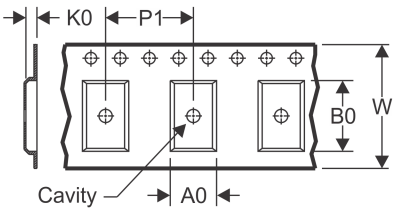
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

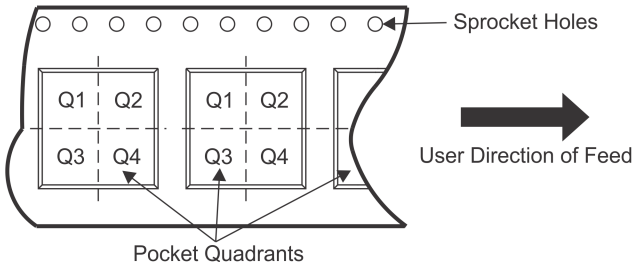


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

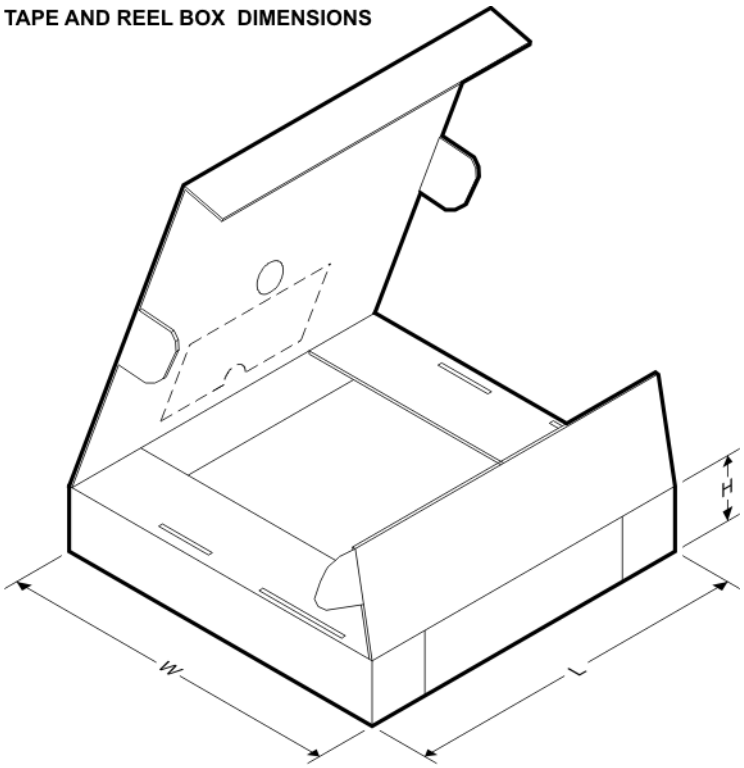
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8881EPWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
DRV8881ERHRR	WQFN	RHR	28	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
DRV8881ERHRT	WQFN	RHR	28	250	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
DRV8881PPWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
DRV8881PRHRR	WQFN	RHR	28	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
DRV8881PRHRT	WQFN	RHR	28	250	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8881EPWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0
DRV8881ERHRR	WQFN	RHR	28	3000	367.0	367.0	35.0
DRV8881ERHRT	WQFN	RHR	28	250	210.0	185.0	35.0
DRV8881PPWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0
DRV8881PRHRR	WQFN	RHR	28	3000	367.0	367.0	35.0
DRV8881PRHRT	WQFN	RHR	28	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

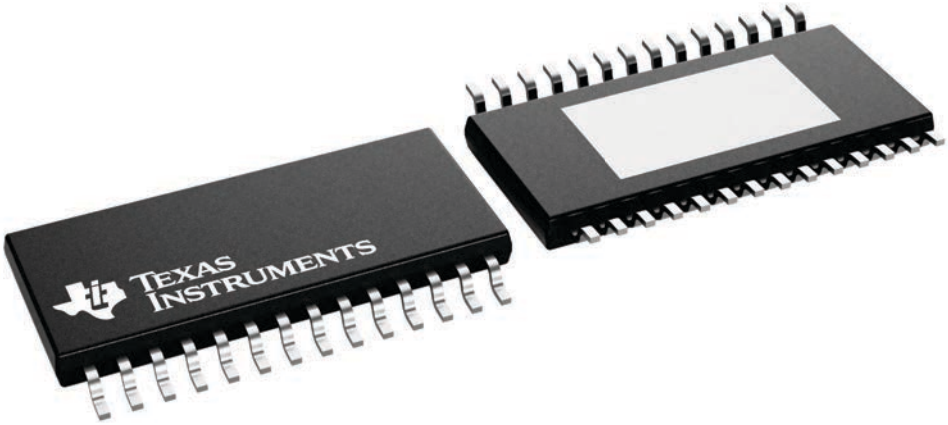
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

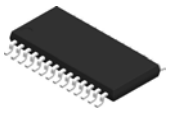
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

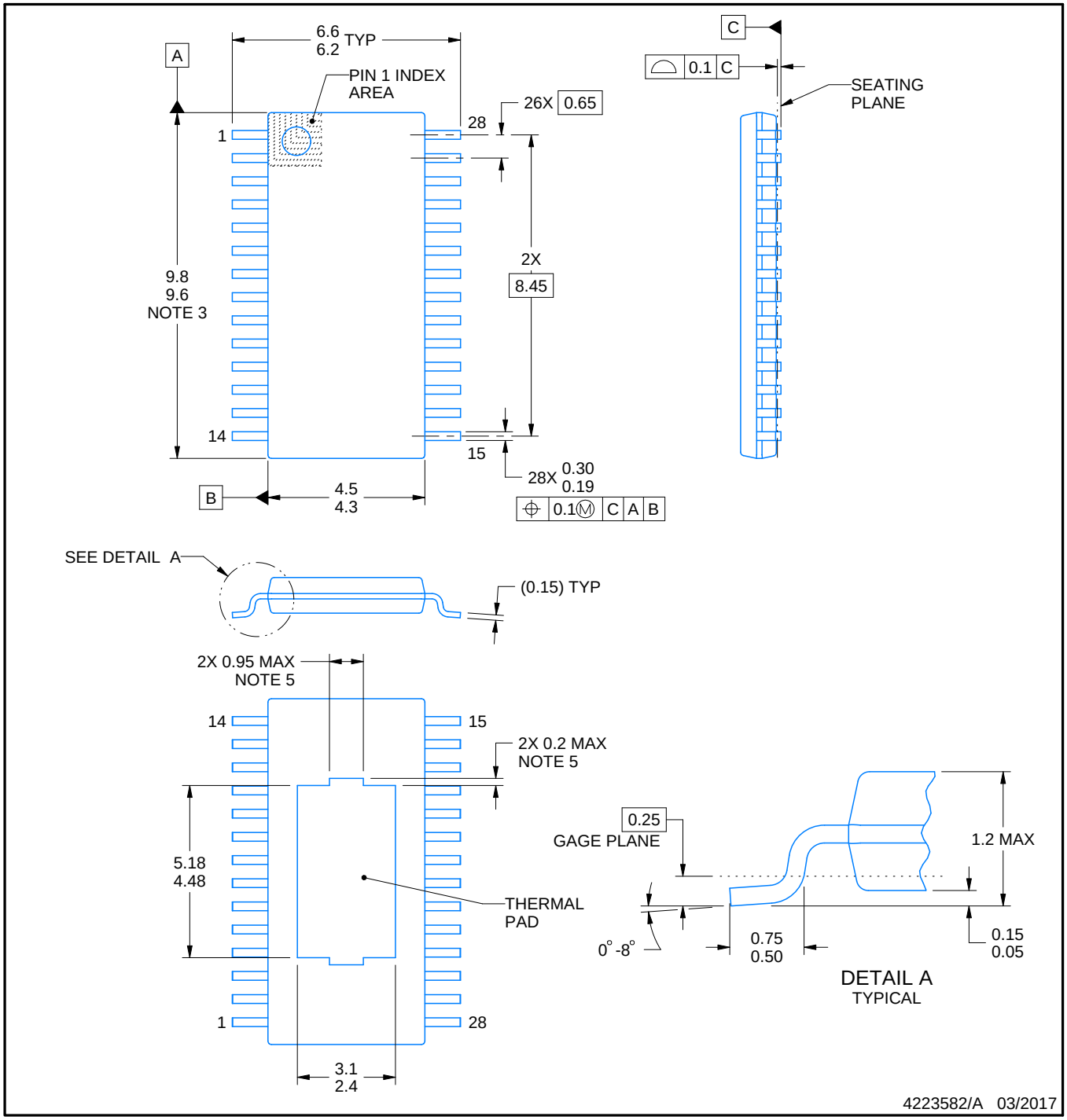
PACKAGE OUTLINE

PWP0028C



PowerPAD™ TSSOP - 1.2 mm max height

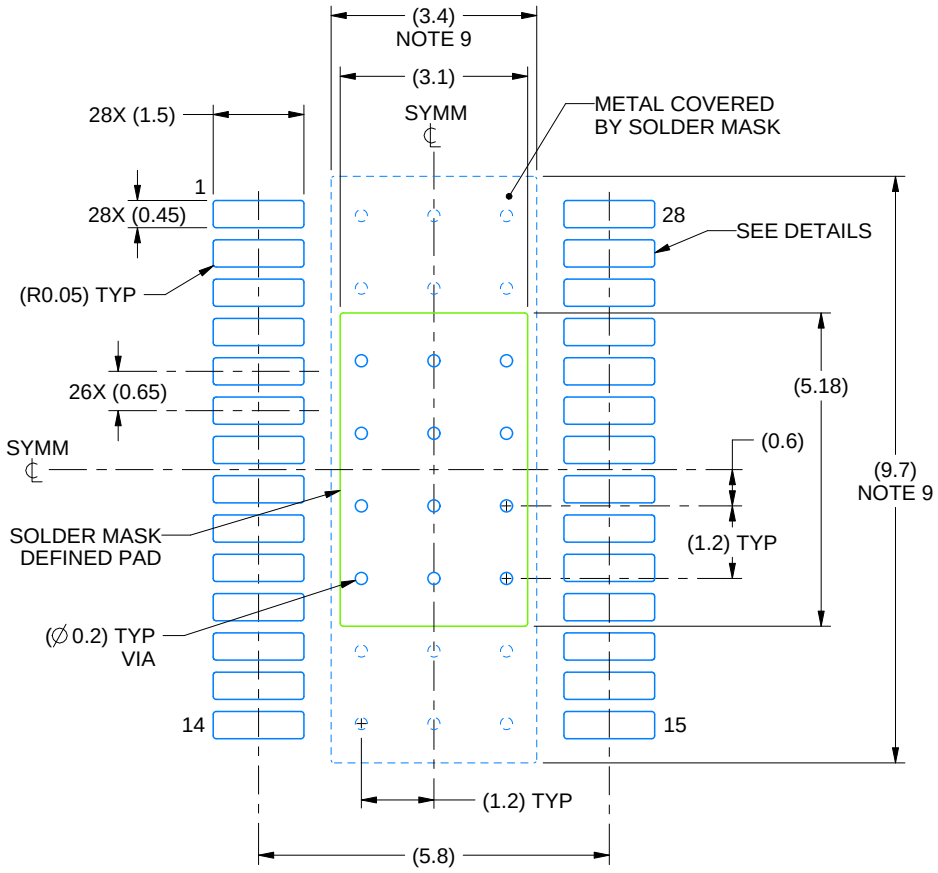
SMALL OUTLINE PACKAGE



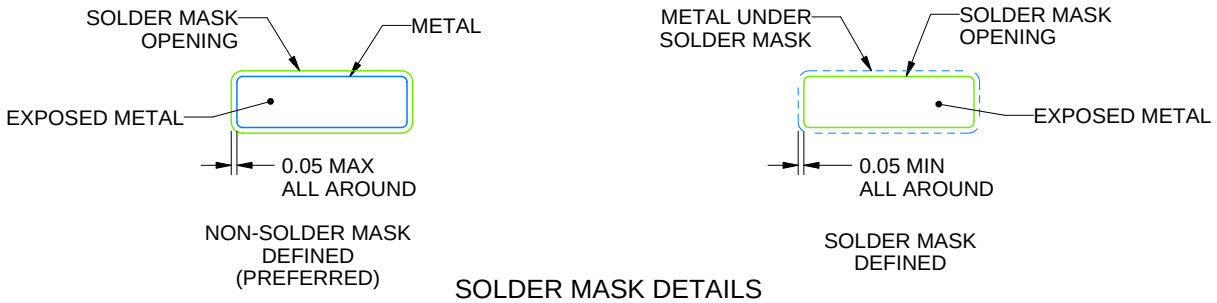
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

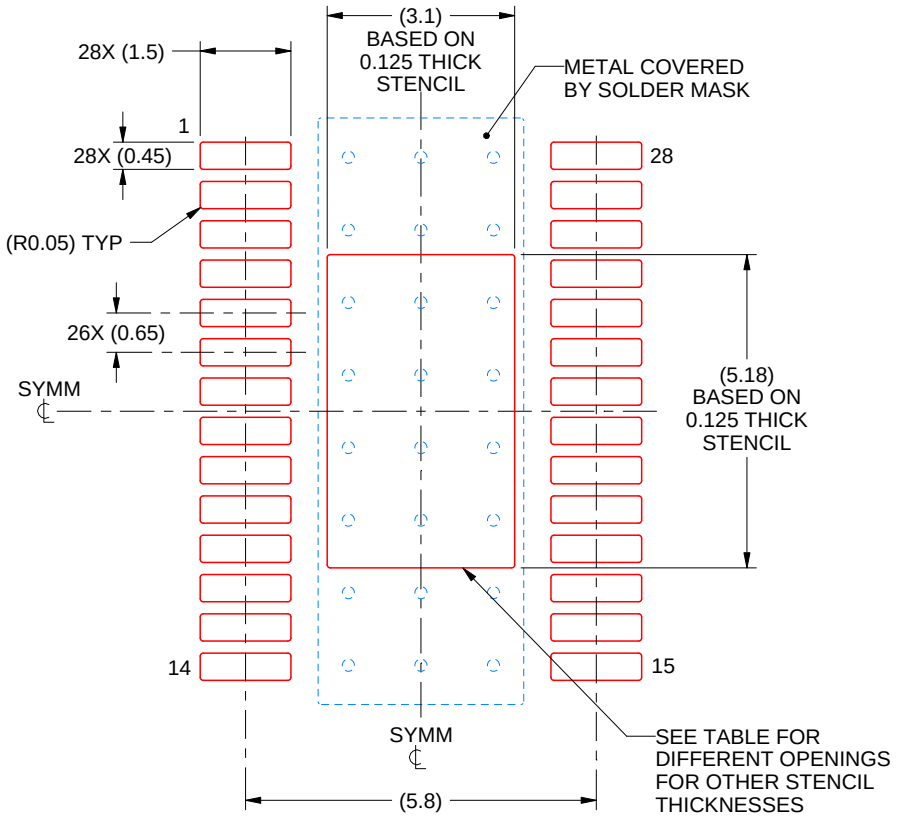


SOLDER MASK DETAILS

4223582/A 03/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 5.79
0.125	3.10 X 5.18 (SHOWN)
0.15	2.83 X 4.73
0.175	2.62 X 4.38

4223582/A 03/2017

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

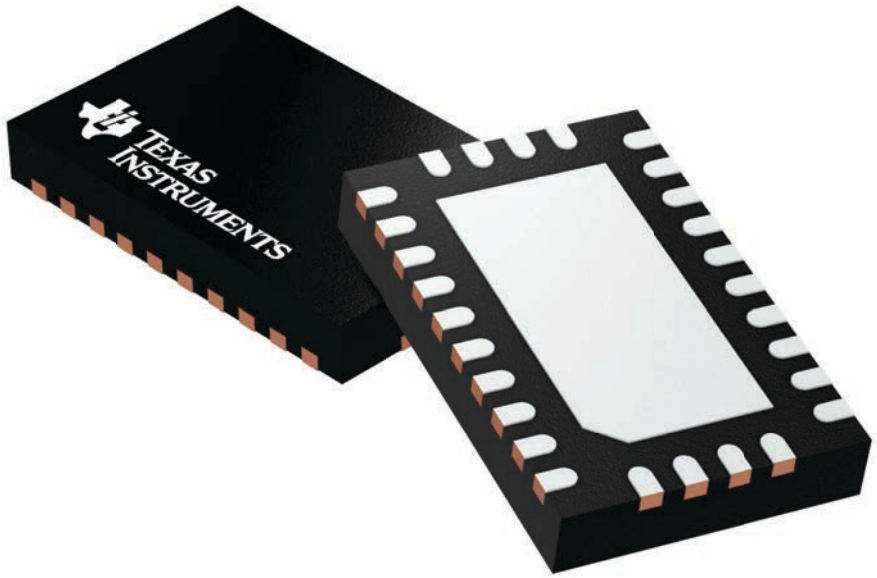
GENERIC PACKAGE VIEW

RHR 28

WQFN - 0.8 mm max height

3.5 x 5.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

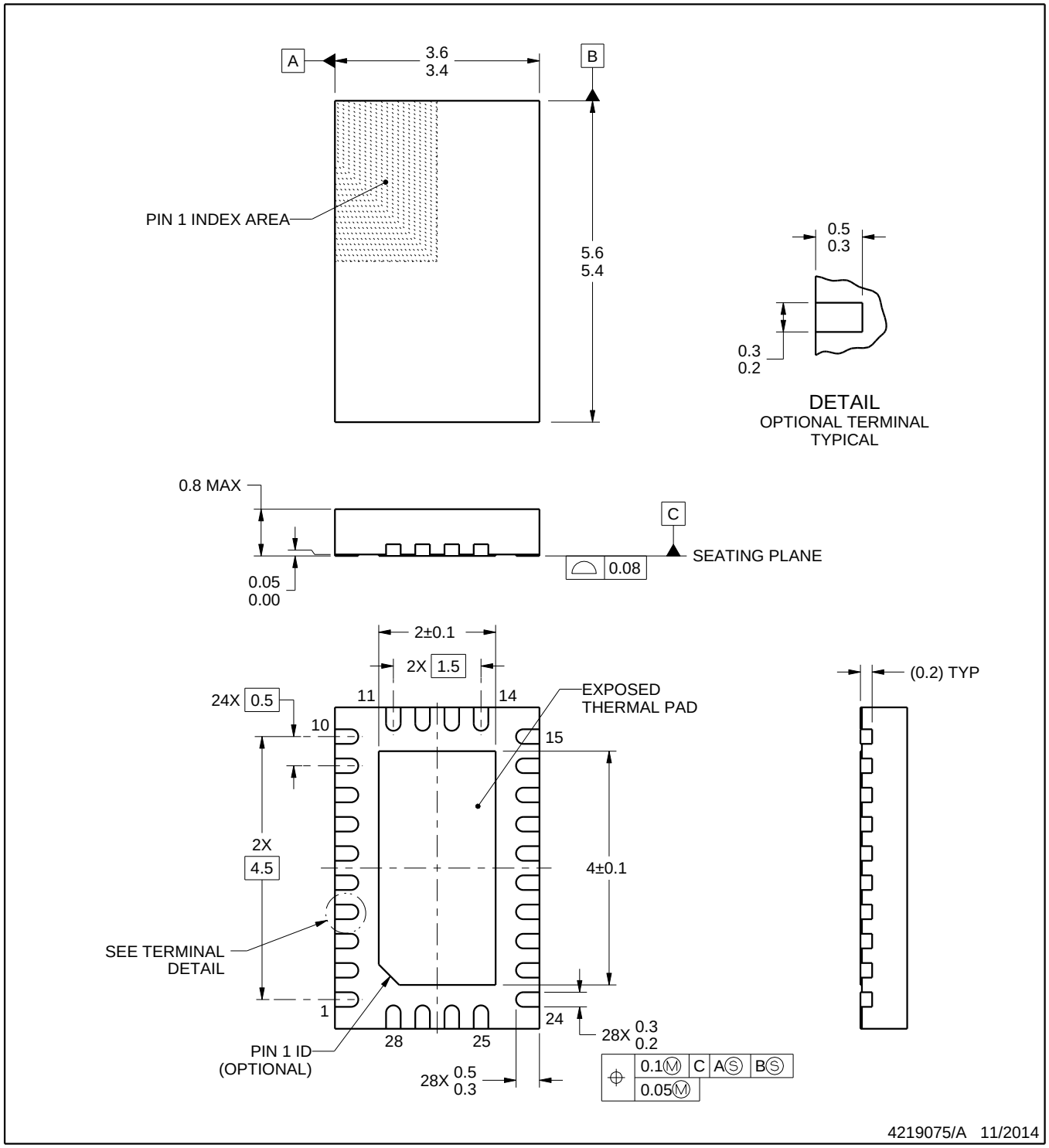
4210249/B

PACKAGE OUTLINE

RHR0028A

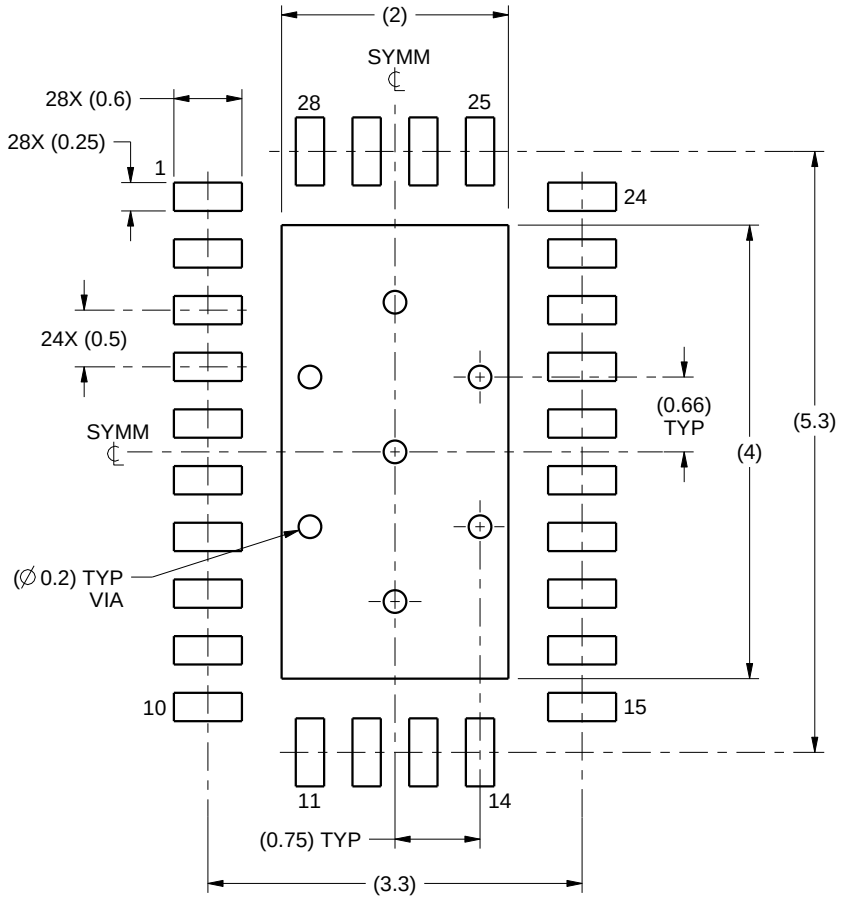
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

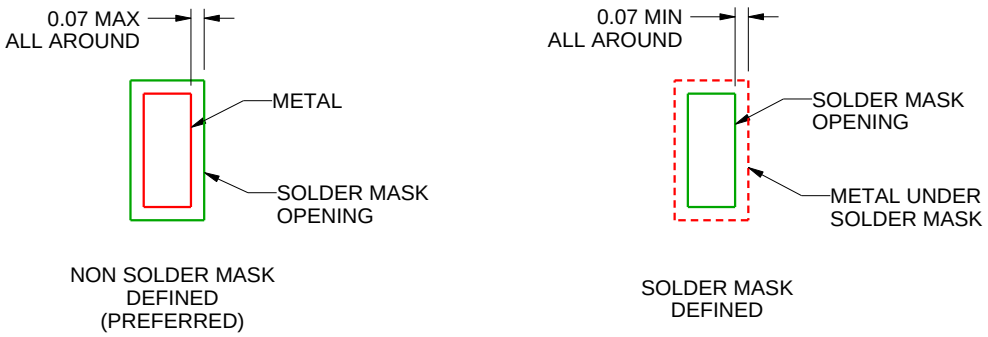


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

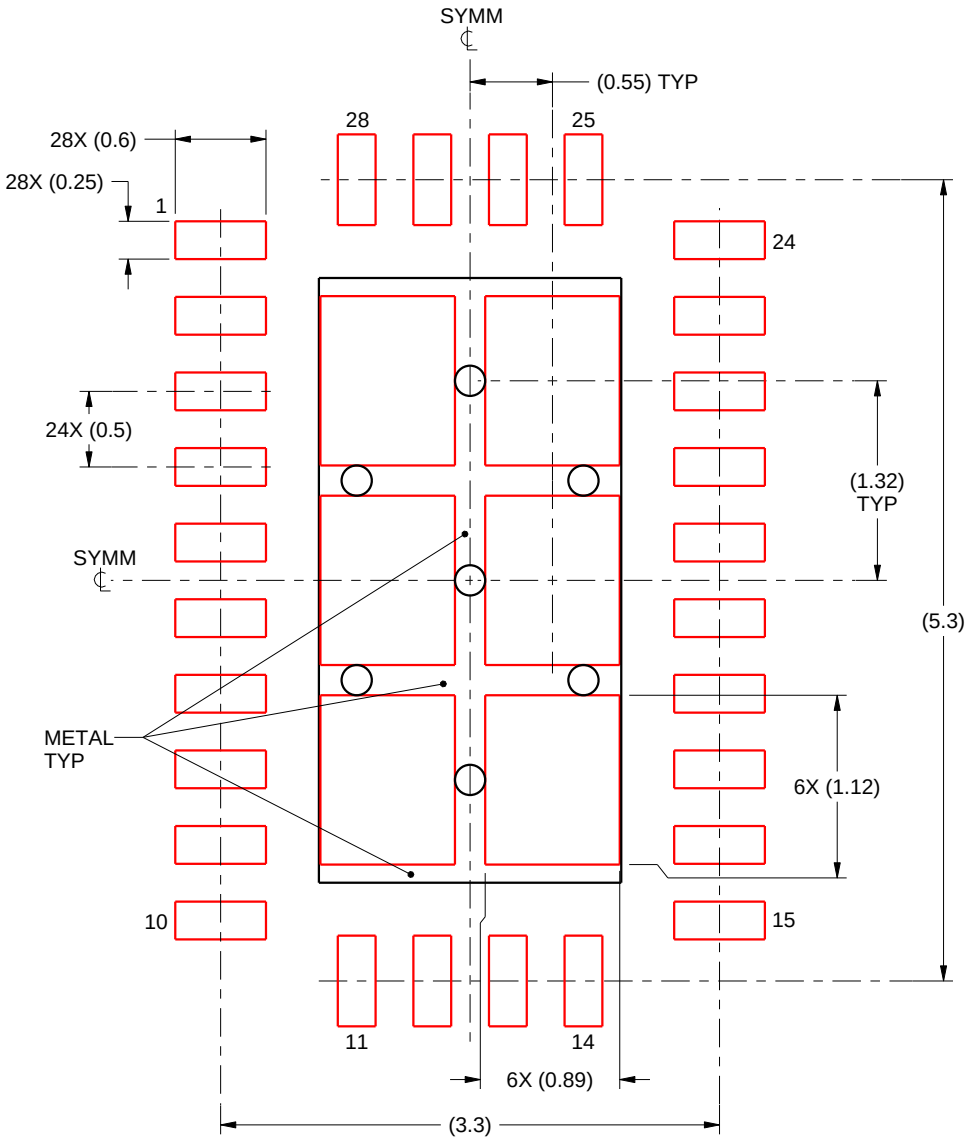


SOLDER MASK DETAILS

4219075/A 11/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219075/A 11/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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