CM1293A

2 and 4-Channel Low Capacitance ESD Protection Arrays

ON Semiconductor®

http://onsemi.com

Product Description

The CM1293A family of diode arrays has been designed to provide ESD protection for electronic components or subsystems requiring minimal capacitive loading. These devices are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series that steer the positive or negative ESD current pulse to either the positive (V_P) or negative (V_N) supply rail. A Zener diode is embedded between V_P and V_N which helps protect the V_{CC} rail against ESD strikes. The CM1293A protects against ESD pulses up to ±8 kV contact discharge) per the IEC 61000−4−2 Level 4 standard.

This device is particularly well−suited for protecting systems using high−speed ports such as USB2.0, IEEE1394 (FireWire®, i.LINK™), Serial ATA, DVI, HDMI, and corresponding ports in removable storage, digital camcorders, DVD−RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

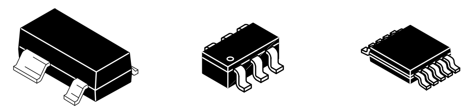
Features

- Two and Four Channels of ESD Protection
- Provides ESD Protection to IEC61000−4−2
  - ±8 kV Contact Discharge
- Low Loading Capacitance of 2.0 pF Max
- Low Clamping Voltage
- Channel I/O to I/O Capacitance 1.5 pF Typical
- Zener Diode Protects Supply Rail and Eliminates the Need for External By−Pass Capacitors
- Each I/O Pin Can Withstand over 1000 ESD Strikes*
- These Devices are Pb−Free and are RoHS Compliant

Applications

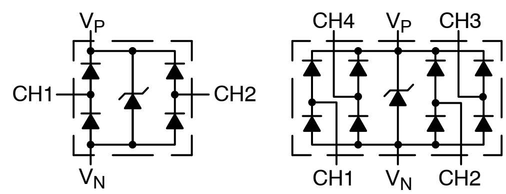
- DVI Ports, HDMI Ports in Notebooks, Set Top Boxes, Digital TVs, LCD Displays
- Serial ATA Ports in Desktop PCs and Hard Disk Drives
- PCI Express Ports
- General Purpose High−Speed Data Line ESD Protection

*Standard test condition is IEC61000−4−2 level 4 test circuit with each pin subjected to ±8 kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.



SOT−143 SR SUFFIX CASE 318A	SC−74 SO SUFFIX CASE 318F	MSOP−10 MR SUFFIX CASE 846AE

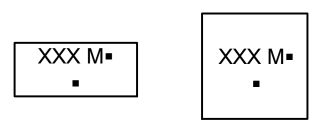
BLOCK DIAGRAM



CM1293A−02SR
CM1293A−02SO

CM1293A−04MR

MARKING DIAGRAM



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
CM1293A−02SR	SOT143−4 (Pb−Free)	3,000 / Tape & Reel
CM1293A−02SO	SC−74 (Pb−Free)	3,000 / Tape & Reel
CM1293A−04MR	MSOP−10 (Pb−Free)	4,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

July, 2012 − Rev. 8

Publication Order Number:
CM1293A/D

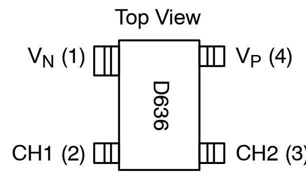
Table 1. PIN DESCRIPTIONS

2–Channel, 4–Lead SOT143–4 Package (CM1293A–02SR)			
Pin	**Name**	**Type**	**Description**
1	V_N	GND	Negative Voltage Supply Rail
2	CH1	I/O	ESD Channel
3	CH2	I/O	ESD Channel
4	V_P	PWR	Positive Voltage Supply Rail

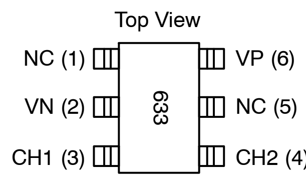
2–Channel, SC–74 Package (CM1293A–02SO)			
Pin	**Name**	**Type**	**Description**
1	NC	–	No Connect
2	VN	GND	Negative Voltage Supply Rail
3	CH1	I/O	ESD Channel
4	CH2	I/O	ESD Channel
5	NC	–	No Connect
6	VP	PWR	Positive Voltage Supply Rail

4–Channel, 10–Lead MSOP–10 Package (CM1293A–04MR)			
Pin	**Name**	**Type**	**Description**
1	CH1	I/O	ESD Channel
2	NC	–	No Connect
3	V_P	PWR	Positive Voltage Supply Rail
4	CH2	I/O	ESD Channel
5	NC	–	No Connect
6	CH3	I/O	ESD Channel
7	NC	–	No Connect
8	V_N	GND	Negative Voltage Supply Rail
9	CH4	I/O	ESD Channel
10	NC	–	No Connect

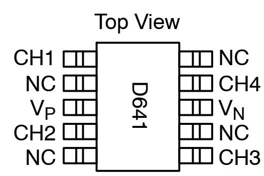
PACKAGE/PINOUT DIAGRAM



4–Lead SOT143–4



2–Channel SC–74



10–Lead MSOP–10

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Operating Supply Voltage (V_P – V_N)	6.0	V
Operating Temperature Range	–40 to +85	°C
Storage Temperature Range	–65 to +150	°C
DC Voltage at any Channel Input	(V_N – 0.5) to (V_P + 0.5)	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	–40 to +85	°C
Package Power Rating SOT143−4 Package (CM1293A−02SR) SC−74 Package (CM1293A−02SO) MSOP−10 Package (CM1293A−04MR)	 225 225 400	mW

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_P	Operating Supply Voltage (V_P–V_N)			3.3	5.5	V
I_P	Operating Supply Current	(V_P–V_N) = 3.3 V			8.0	μA
V_F	Diode Forward Voltage Top Diode Bottom Diode	I_F = 8 mA, T_A = 25°C	 0.60 0.60	 0.80 0.80	 0.95 0.95	V
I_{LEAK}	Channel Leakage Current	T_A = 25°C, V_P = 5 V, V_N = 0 V		±0.1	±1.0	μA
C_{IN}	Channel Input Capacitance	At 1 MHz, V_P = 3.3 V, V_N = 0 V, V_{IN} = 1.65 V			2.0	pF
ΔC_{IO}	Channel I/O to I/O Capacitance			1.5		pF
V_{ESD}	ESD Protection − Peak Discharge Voltage at any Channel Input, in System Contact Discharge per IEC 61000−4−2 Standard Human Body Model, MIL−STD−883, Method 3015	 T_A = 25°C (Notes 2 and 4) T_A = 25°C (Notes 3 and 4)	 ±8 ±15			kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	T_A = 25°C, I_{PP} = 1A, t_P = 8/20 μS (Note 4)		 +9.9 –1.6		V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	T_A = 25°C, I_{PP} = 1A, t_P = 8/20 μS (Note 4)		 0.96 0.5		Ω

1. All parameters specified at T_A = –40°C to +85°C unless otherwise noted.
2. Standard IEC 61000−4−2 with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330 Ω, V_P = 3.3 V, V_N grounded.
3. Human Body Model per MIL−STD−883, Method 3015, $C_{Discharge}$ = 100 pF, $R_{Discharge}$ = 1.5 kΩ, V_P = 3.3 V, V_N grounded.
4. These measurements performed with no external capacitor on V_P.

PERFORMANCE INFORMATION

Input Channel Capacitance Performance Curves

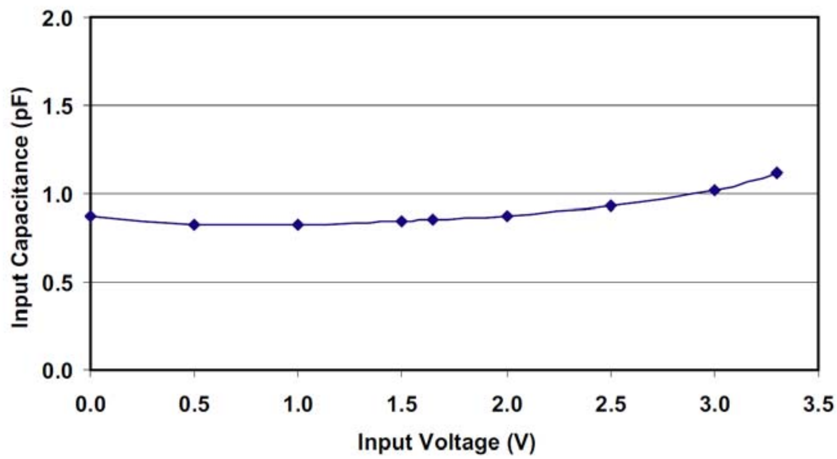


Figure 1. Typical Variation of C_{IN} vs. V_{IN}
(f = 1 MHz, V_P = 3.3 V, V_N = 0 V, 0.1 μF Chip Capacitor between V_P and V_N, 25°C)

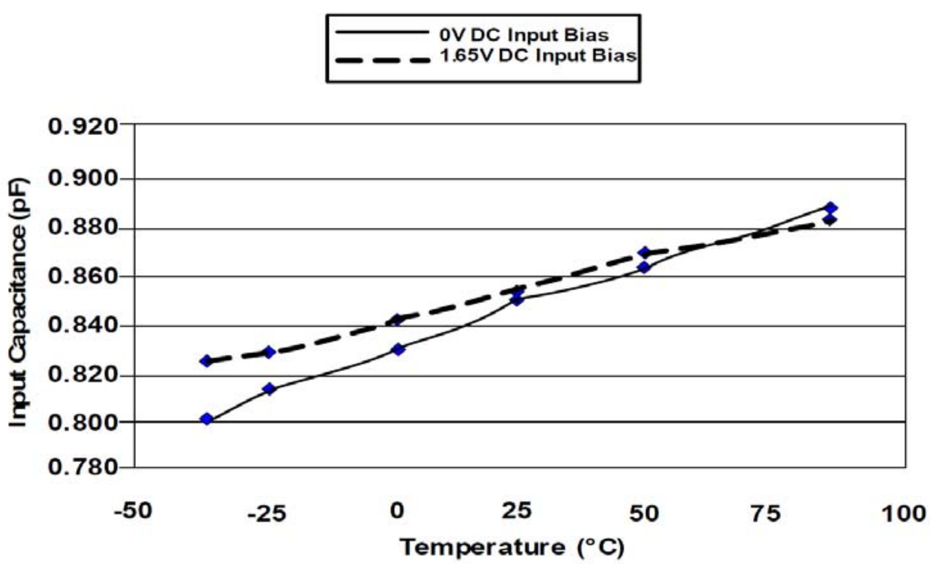


Figure 2. Typical Variation of C_{IN} vs. Temp
(f = 1 MHz, V_{IN} = 30 mV, V_P = 3.3 V, V_N = 0 V, 0.1 μF Chip Capacitor between V_P and V_N)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ω Environment)

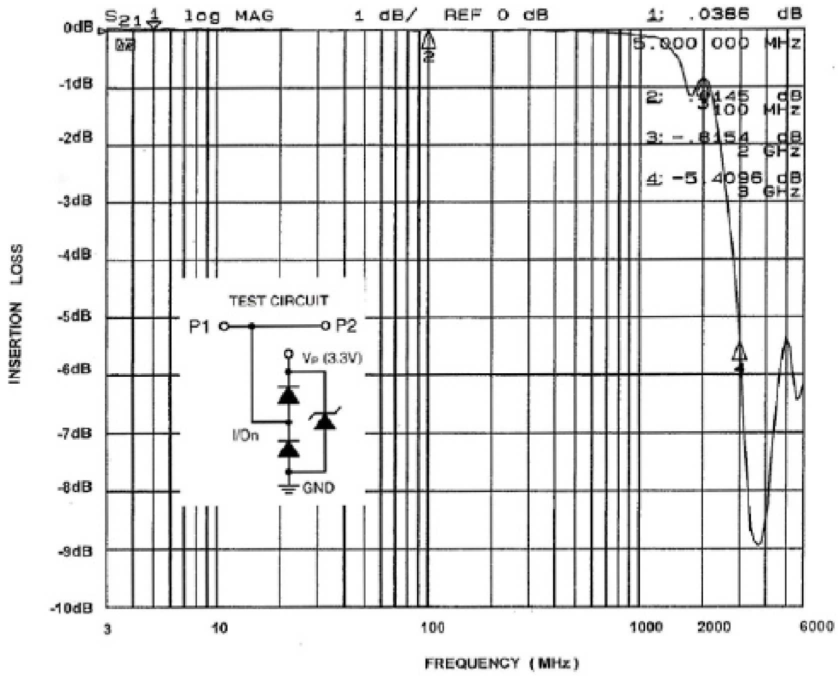


Figure 3. Insertion Loss (S21) vs. Frequency (0 V DC Bias, V_P = 3.3 V)

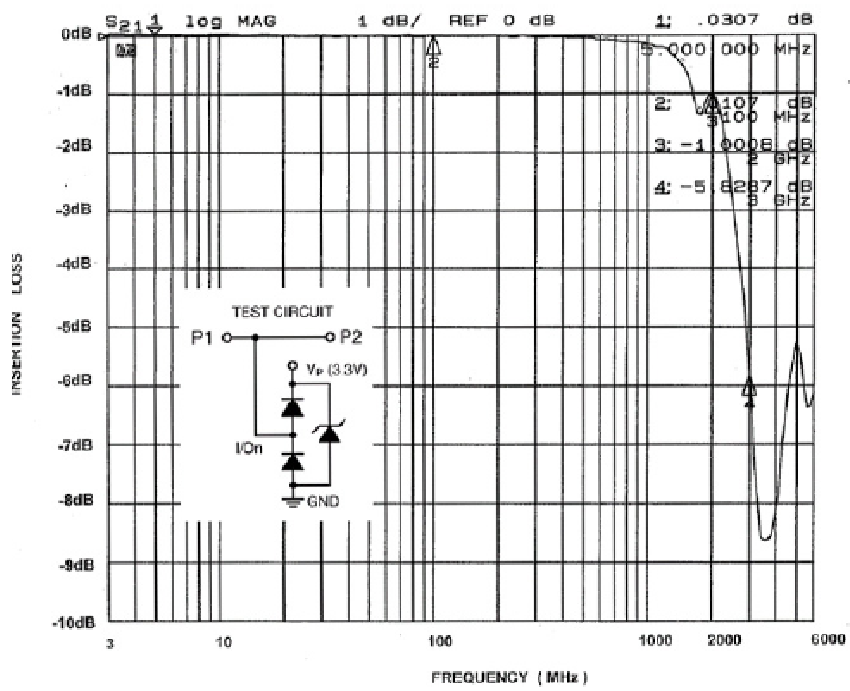


Figure 4. Insertion Loss (S21) vs. Frequency (2.5 V DC Bias, V_P = 3.3 V)

APPLICATION INFORMATION

Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Figure 5, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by L_1 and L_2. The voltage V_{CL} on the line being protected is:

$$V_{CL} = \text{Fwd voltage drop of } D_1 + V_{SUPPLY} + L_1 \times d(I_{ESD}) / dt + L_2 \times d(I_{ESD}) / dt$$

where I_{ESD} is the ESD current pulse, and V_{SUPPLY} is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000−4−2 standard results in a current pulse that rises from zero to 30 Amps in 1 ns. Here $d(I_{ESD})/dt$ can be approximated by $\Delta I_{ESD}/\Delta t$, or $30/(1 \times 10^{-9})$. So just 10 nH of series inductance (L_1 and L_2 combined) will lead to a 300 V increment in V_{CL}!

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

The CM1293 has an integrated Zener diode between V_P and V_N. This greatly reduces the effect of supply rail inductance L_2 on V_{CL} by clamping V_P at the breakdown voltage of the Zener diode. However, for the lowest possible V_{CL}, especially when V_P is biased at a voltage significantly below the Zener breakdown voltage, it is recommended that a 0.22 µF ceramic chip capacitor be connected between V_P and the ground plane.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

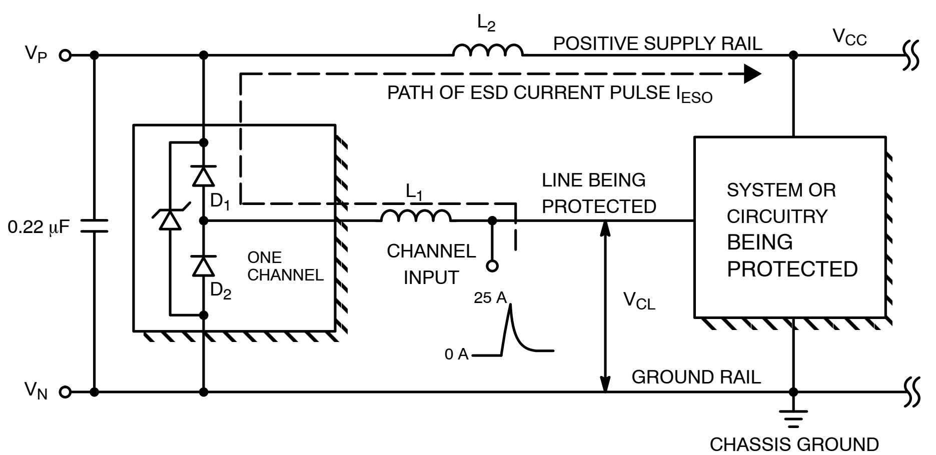
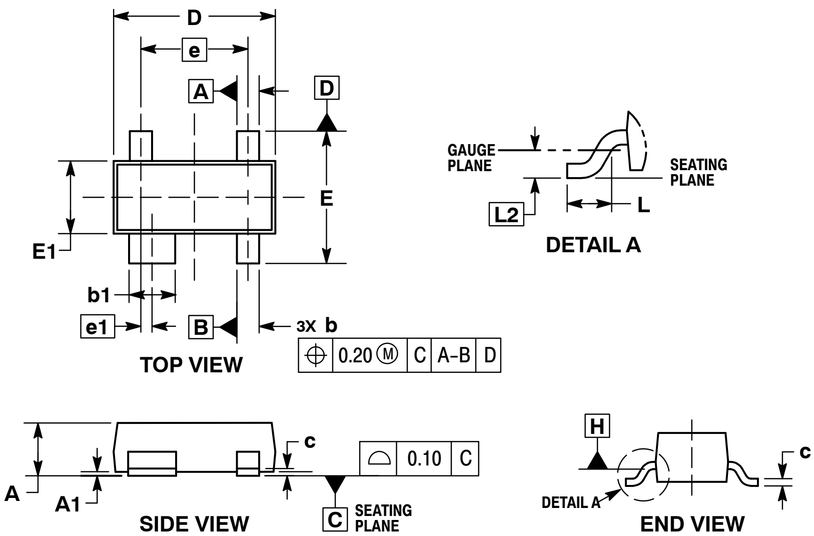


Figure 5. Application of Positive ESD Pulse between Input Channel and Ground

PACKAGE DIMENSIONS

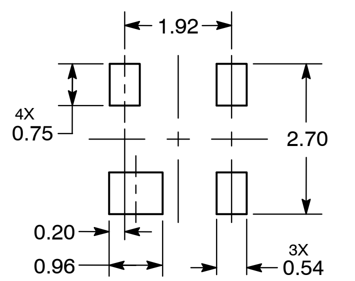
SOT−143
CASE 318A−06
ISSUE U



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, AND GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
6. DATUMS A AND B ARE DETERMINED AT DATUM H.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.12
A1	0.01	0.15
b	0.30	0.51
b1	0.76	0.94
c	0.08	0.20
D	2.80	3.05
E	2.10	2.64
E1	1.20	1.40
e	1.92 BSC	
e1	0.20 BSC	
L	0.35	0.70
L2	0.25 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



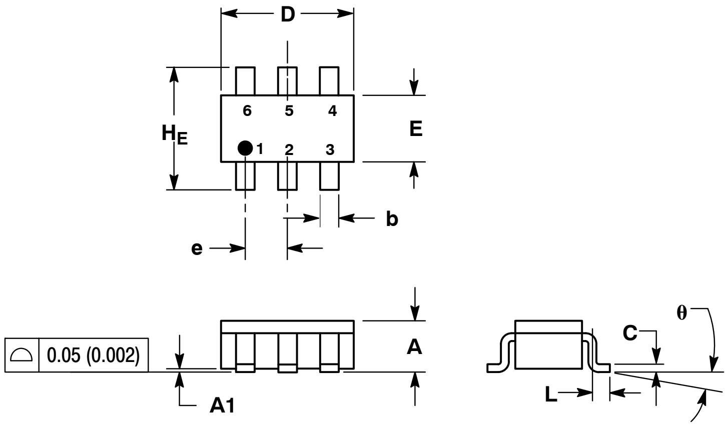
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SC−74
CASE 318F−05
ISSUE N

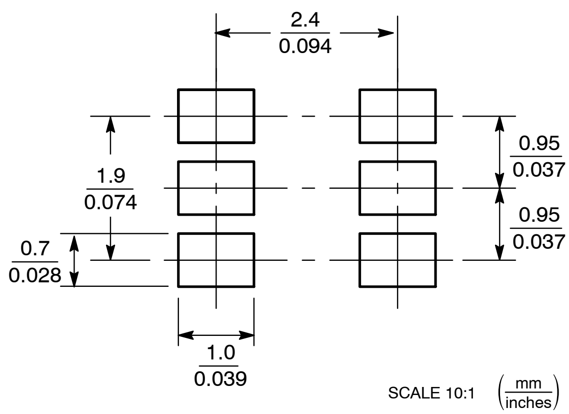
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F−01, −02, −03, −04 OBSOLETE. NEW STANDARD 318F−05.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	–	10°	0°	–	10°

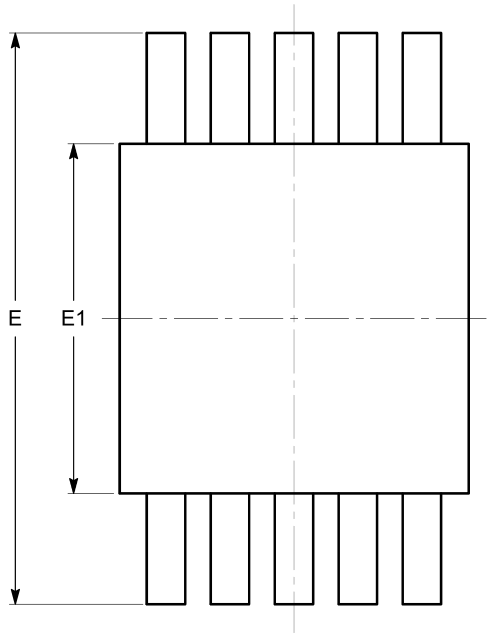
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

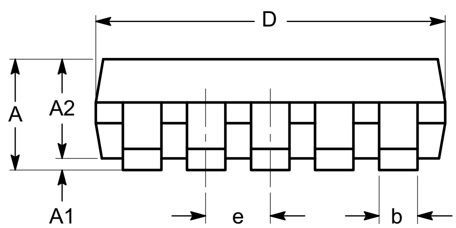
PACKAGE DIMENSIONS

MSOP 10, 3x3
CASE 846AE−01
ISSUE O

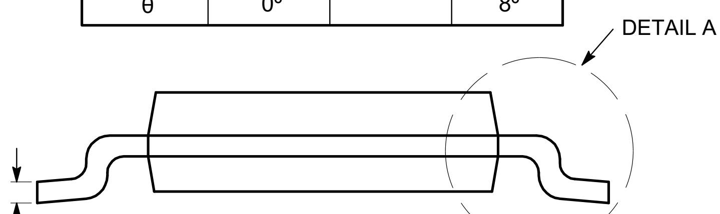


TOP VIEW

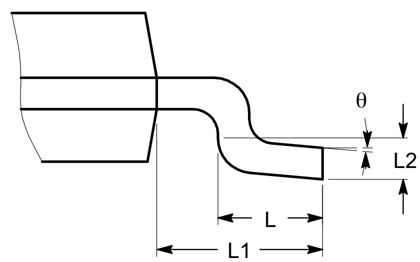
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.00	0.05	0.15
A2	0.75	0.85	0.95
b	0.17		0.27
c	0.13		0.23
D	2.90	3.00	3.10
E	4.75	4.90	5.05
E1	2.90	3.00	3.10
e	0.50 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
θ	0º		8º



SIDE VIEW



END VIEW



DETAIL A

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-187.

FireWire is a registered trademark of Apple Computer, Inc.
i.LINK is a trademark of Sony Corporation.

PUBLICATION ORDERING INFORMATION

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