ROHM GROUP
LAPIS
SEMICONDUCTOR

FEBL22Q62xRB-03

RB-S22Q62xTB32
User's Manual

Issue Date: March 26, 2020

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Table of Contents

1. Overview

This instruction manual is for the RB-S22Q62xTB32 which is the ML22Q623/ML22Q624/ML22Q625/ML22Q626 reference board.

Combining the board with a Sound Device Control Board 3 (hereinafter referred to as "SDCB3") enables the following functions to be implemented:

- Voice playback by ML22Q623/ML22Q624/ML22Q625/ML22Q626.
- Writing voice data into ML22Q623/ML22Q624/ML22Q625/ML22Q626.

2. Operational notes

The following describes the precautions to follow when handling the RB-S22Q62xTB32.

- Turn off the power when attaching the RB-S22Q62xTB32 to the SDCB3.
- Turn off the power when loading devices into the RB-S22Q62xTB32. Be sure to orient the device correctly. Pin 1 direction is toward the lower left side when the lid is opened. The Figure 1 shows the setting directions of devices.
- The ML22Q623/ML22Q624/ML22Q625/ML22Q626 supply voltages are 2.7 to 3 6V / 3.3 to 5 5V. Use the RB-S22Q62xTB32 with a power supply voltage of 3. 0V.
- RB-S22Q62xTB32 is a device used only by experts in R&D facilities for research and development purposes. RB-S22Q62xTB32 is not intended to be used in mass-produced products or parts thereof.
- The information in this document is subject to change without notice due to product improvement and technological improvement. Prior to use, please ensure that the information is up to date.
- LAPIS Semiconductor does not provide any RB-S22Q62xTB32 support. Replace only in case of initial failure.

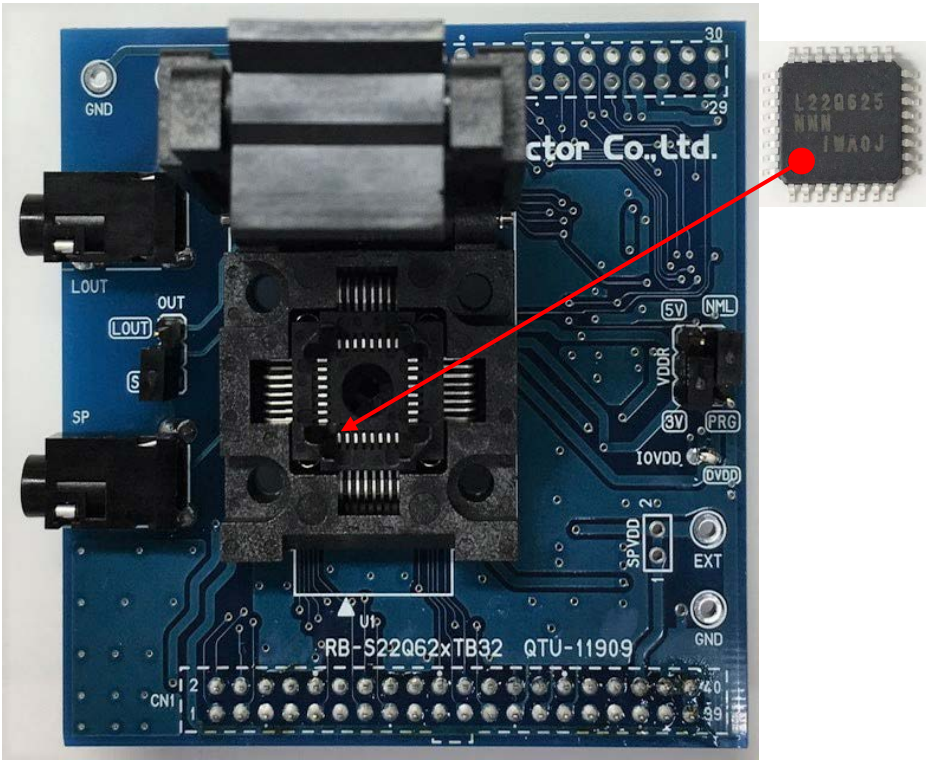


Figure 1 Outline Diagram

3. Specification

3.1. Jumper Pin Setting

Table 1 shows the RB-S22Q62xTB32 jumper pin settings.

Table 1

Jumper Pin Name	Setting
VDDR	Fixed on the 3V side
IRON	Fixed on the NML side

Table 2

Jumper Pin Name	LINE output	Speaker amplifier output
OUT	Fixed on the LOUT side	Fixed on the SP side

3.2. PCB layout

Figure 2 shows the RB-S22Q62xTB32 PCB layout.

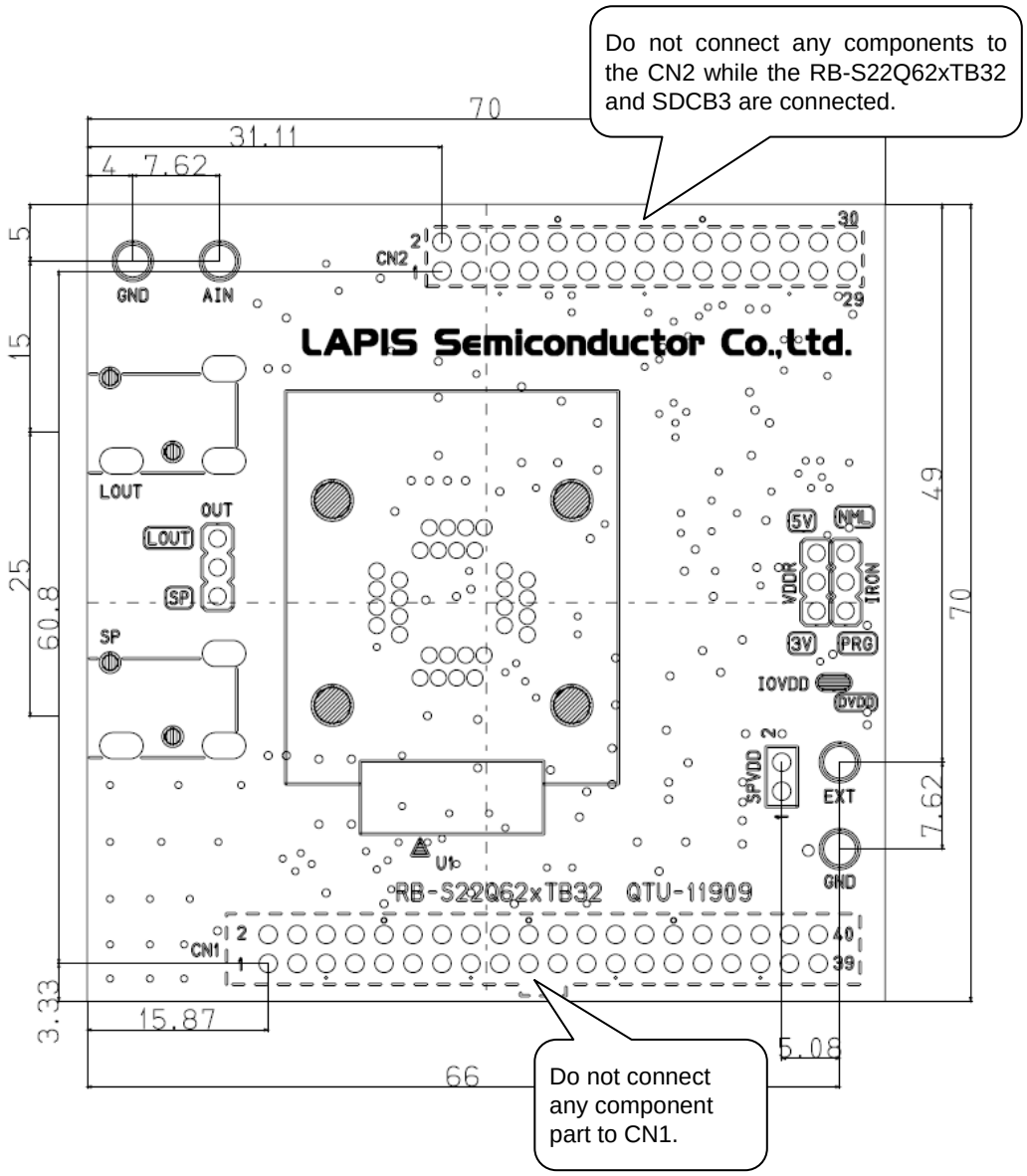
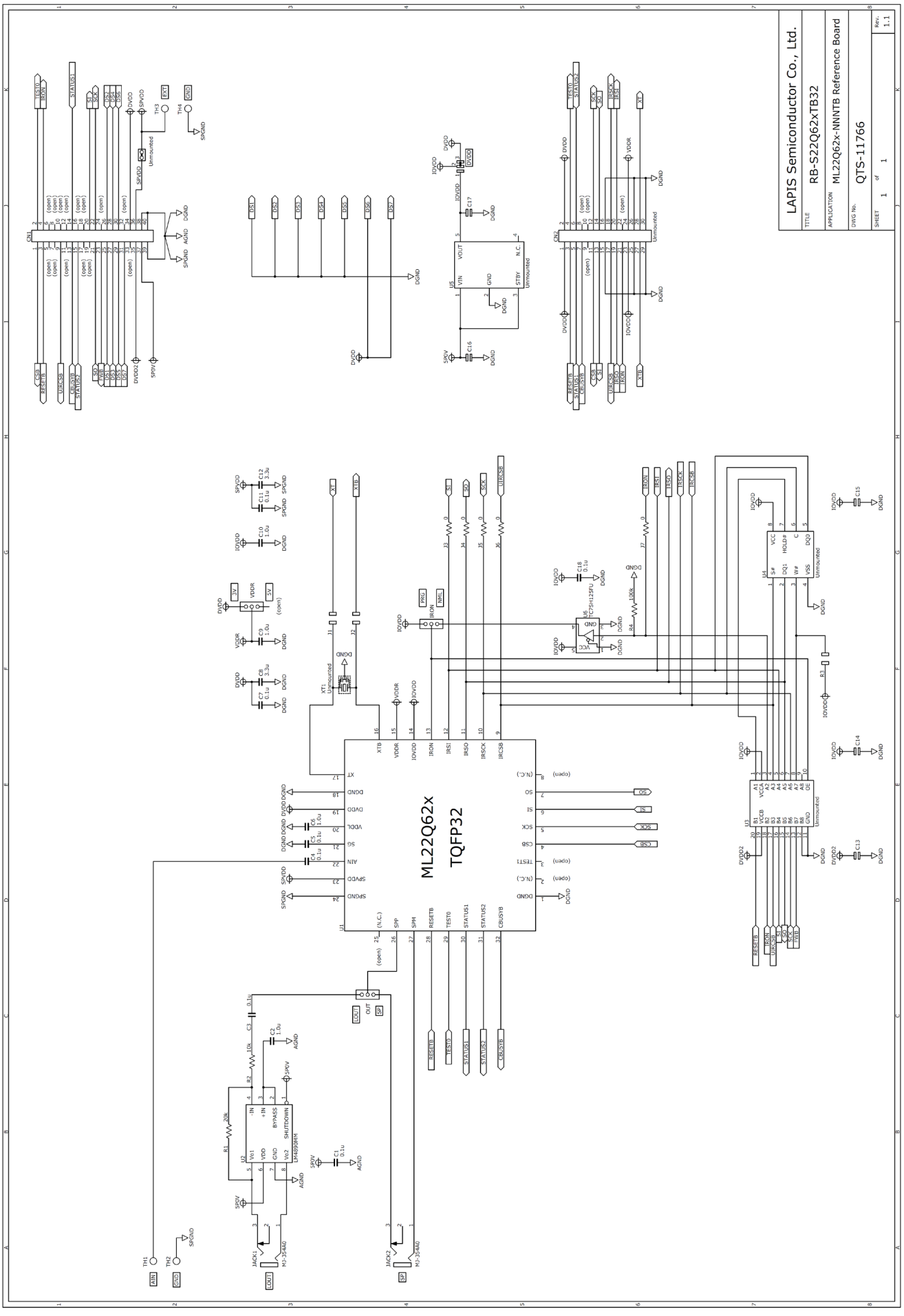


Figure 2 PCB layout

3.3. BOM list, Schematic

	Parts Number	Symbol	Contents	Qty.	Vendor
1	QTU-11909	RB-S22Q62xTB32	PCB	1	LAPIS Semiconductor Co., Ltd.
2	CGA3E2X7R1E104K080AA	C1,C3,C4,C5, C7,C11,C18	Ceramic Capacitor 0.1μF/25V X7R	7	TDK Corporation
3	CGA3E1X7R1C105K080AC	C2,C6,C9,C10	Ceramic Capacitor 1.0μF/16V X7R	4	TDK Corporation
4	C1608X5R1C335K080AC	C8,C12	Ceramic Capacitor 3.3μF/16V X5R	2	TDK Corporation
5	HIF3FB-40DA-2.54DSA(71)	CN1	40pin Receptacle	1	Hirose Electric Co., Ltd.
6	A2-3PA-2.54DSA	IRON,VDDR,OUT	3pin Pin Header	3	Hirose Electric Co., Ltd.
7	MCR03EZPJ000	J3,J4,J5,J6, J7	Resistor 0Ω	5	Rohm Co., Ltd.
8	-	IOVDD	Select pad	1	-
9	MJ-354A0	JACK1,JACK2	2-Conductor Miniature Jack	2	MARUSHIN ELECTRIC MFG. CO., LTD.
10	MCR03EZPJ203	R1	Resistor 20kΩ ±5%	1	Rohm Co., Ltd.
11	MCR03EZPJ103	R2	Resistor 10kΩ ±5%	1	Rohm Co., Ltd.
12	MCR03EZPJ104	R4	Resistor 100kΩ ±5%	1	Rohm Co., Ltd.
13	FPQ-32-0.8-007S-00	U1	QFP P0.80 32P Socket	1	Enplas Corporation
14	LM4890MM/NOPB	U2	Audio Power Amplifier	1	Texas Instruments Incorporated
15	TC7SH125FU	U6	Bus Buffer with 3-State Output	1	Toshiba Corporation
16	HIF3GA-2.54SP	-	Short Pin	3	Hirose Electric Co., Ltd.
17	-	C13,C14,C15,C16, C17	Unmounted	5	-
18	-	CN2	Unmounted	1	-
19	-	J1,J2	Unmounted	2	-
20	-	SPVDD	Unmounted	1	-
21	-	R3	Unmounted	1	-
22	-	TH1,TH2,TH3,TH4	Unmounted	4	-
23	-	U3	Unmounted	1	-
24	-	U4	Unmounted	1	-
25	-	U5	Unmounted	1	-
26	-	XT1	Unmounted	1	-


LAPIS Semiconductor Co., Ltd.
TITLE
RB-S22Q62xTB32
APPLICATION
ML22Q62x-NNNTB Reference Board
DWG No.
QTS-11766
SHEET
1 of 1
Rev.
1.1
ML22Q62x
TQFP32

3.4. CN1

CN1 is a 40-pin connector that is used to connect to the SDCB3.

3.5. CN2

CN2 is a 30-pin connector to which ML22Q623/ML22Q624/ML22Q625/ML22Q626 terminals are connected.

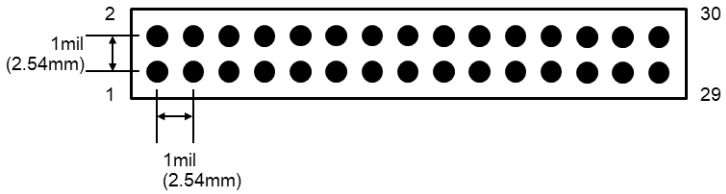


Figure 3 CN2 connectors hole pattern

Table 3 CN2 connector pin connections

CN2 Pin No		Connect LSI	LSI Pin No	LSI Pin Name
1	VDD (3V)	ML22Q623/ML22Q624/ML22Q625/ML22Q626	19	DVDD
2	VDD (3V)	ML22Q623/ML22Q624/ML22Q625/ML22Q626	19	DVDD
3	I/O	ML22Q623/ML22Q624/ML22Q625/ML22Q626	28	RESTB
4	I/O	ML22Q623/ML22Q624/ML22Q625/ML22Q626	29	TEST0
5	I/O	ML22Q623/ML22Q624/ML22Q625/ML22Q626	30	STATUS1
6	I/O	ML22Q623/ML22Q624/ML22Q625/ML22Q626	31	STATUS2
7	I/O	ML22Q623/ML22Q624/ML22Q625/ML22Q626	32	CBUSYB
8	I/O	-	-	-
9	I/O	-	-	-
10	I/O	-	-	-
11	I/O	ML22Q623/ML22Q624/ML22Q625/ML22Q626	4	CSB
12	I/O	ML22Q623/ML22Q624/ML22Q625/ML22Q626	5	SCK
13	I/O	ML22Q623/ML22Q624/ML22Q625/ML22Q626	6	SI
14	I/O	ML22Q623/ML22Q624/ML22Q625/ML22Q626	7	SO
15	GND	ML22Q623/ML22Q624/ML22Q625/ML22Q626	1, 18	DGND
16	GND	ML22Q623/ML22Q624/ML22Q625/ML22Q626	1, 18	DGND
17	I/O	ML22Q623/ML22Q624/ML22Q625/ML22Q626	9	IRCSB
18	I/O	ML22Q623/ML22Q624/ML22Q625/ML22Q626	10	IRSCK
19	I/O	ML22Q623/ML22Q624/ML22Q625/ML22Q626	11	IRSO
20	I/O	ML22Q623/ML22Q624/ML22Q625/ML22Q626	12	IRSI
21	I/O	ML22Q623/ML22Q624/ML22Q625/ML22Q626	13	IRON
22	I/O	-	-	-
23	IOVDD	ML22Q623/ML22Q624/ML22Q625/ML22Q626	14	IOVDD
24	VDDR	ML22Q623/ML22Q624/ML22Q625/ML22Q626	15	VDDR
25	GND	ML22Q623/ML22Q624/ML22Q625/ML22Q626	1, 18	DGND
26	GND	ML22Q623/ML22Q624/ML22Q625/ML22Q626	1, 18	DGND
27	I/O	ML22Q623/ML22Q624/ML22Q625/ML22Q626	16	XTB
28	I/O	ML22Q623/ML22Q624/ML22Q625/ML22Q626	17	XT
29	GND	ML22Q623/ML22Q624/ML22Q625/ML22Q626	1, 18	DGND
30	GND	ML22Q623/ML22Q624/ML22Q625/ML22Q626	1, 18	DGND

3.6. LOUT jack

LOUT is a jack to which the ML22Q623/ML22Q624/ML22Q625/ML22Q626 line-amp outputs are connected via a speaker amplifier.

3.7. SP jack

SP is the jack to which ML22Q623/ML22Q624/ML22Q625/ML22Q626 speaker amplifier outputs are connected.

3.8. AIN, GND terminal

This terminal is connected to the ML22Q623/ML22Q624/ML22Q625/ML22Q626 speaker amplifier input terminal. Input a speaker amplifier input signal between the AIN pin and GND pin.

3.9. Ceramic resonator, External Clock

Ceramic resonator can be mounted on a XT1. Table 4 table shows the ceramic resonators used.

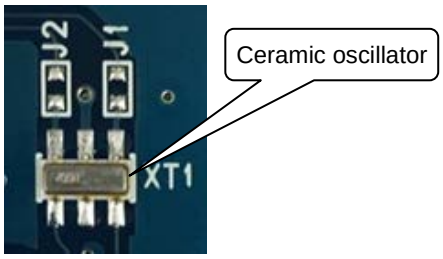


Figure 4 Ceramic resonator

Table 4 Ceramic resonator

Vendor	Frequency[Hz]	Parts Number
Murata Manufacturing Co., Ltd.	4M	CSTCR4M00G55B-R0
Murata Manufacturing Co., Ltd.	4.096M	CSTCR4M09G55B-R0

External clocks can be entered from the CN2's 28 pins. Connect between J1 terminals.

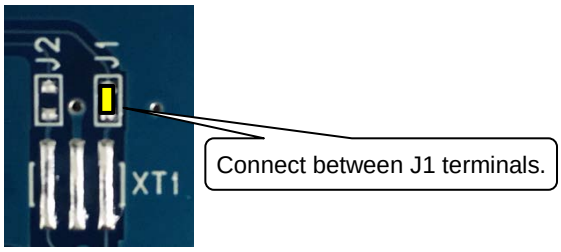


Figure 5 External clock

Revision History

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
FEBL22Q62xRB-01	October 31, 2019	–	–	First edition.
FEBL22Q62xRB-03	March 26, 2020	1	1	Figure 1 Outline Diagram
		2	2	Figure 2 PCB layout
		3	3	3.3. BOM list, Schematic