

DATA SHEET

AS183-92/AS183-92LF: 300 kHz-2.5 GHz pHEMT GaAs SPDT Switch

Applications

- General purpose medium-power switches in telecommunication applications
- Transmit/receive switches in 802.11 b/g WLAN Bluetooth™ systems

Features

- IP1dB: +30 dBm typical @ 3 V
- IP3: +43 dBm typical @ 3 V
- \bullet Low insertion loss: 0.3 dB @ 0.9 GHz
- Low DC power consumption
- Ultra-miniature, SC-70 (6-pin, 2.00 x 1.25 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

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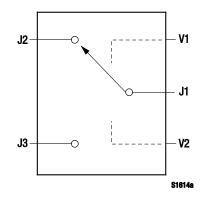


Figure 1. AS183-92/AS183-92LF Block Diagram

Description

The AS183-92/AS183-92LF is a pHEMT GaAs FET Single Pole Double Throw (SPDT) switch. The device features low insertion loss and positive voltage operation with very low DC power consumption. The AS183-92/AS183-92LF is manufactured in a compact, low-cost 2.00 x 1.25 mm, 6-pin SC-70 package.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

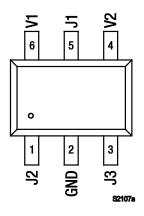


Figure 2. AS183-92/AS183-92LF Pinout –6-Pin SC-70 (Top View)

Pin #	Pin # Name Description		Pin #	Name	Description
1	J2	RF input/output 2 (Note 1)	4	V2	DC control voltage
2	GND	Ground	5	J1	RF input/output 1 (Note 1)
3	J3	RF input/output 3 (Note 1)	6	V1	DC control voltage

Table 1. AS183-92/AS183-92LF Signal Descriptions

Note 1: A 100 pF blocking capacitor is required for >500 MHz operation. Use larger value capacitors for lower frequency operation.

Table 2. AS183-92/AS183-92LF Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Control voltage	VCTL	-0.2	+8.0	V
RF input power (VcrL = 0 to 7 V) @ >500 MHz	Pin		6	W
Operating temperature	Тор	-40	+85	°C
Storage temperature	Тята	-65	+150	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value.

CAUTION: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Electrical and Mechanical Specifications

The absolute maximum ratings of the AS183-92/AS183-92LF are provided in Table 2. Electrical specifications are provided in Table 3.

Performance characteristics for the AS183-92/AS183-92LF are illustrated in Figures 3 through 5.

The state of the AS183-92/AS183-92LF is determined by the logic provided in Table 4.

Parameter	Symbol	Test Condition	Min	Typical	Мах	Units
Insertion loss (Note 2)		300 kHz to 1.0 GHz 300 kHz to 2.0 GHz 300 kHz to 2.5 GHz		0.30 0.30 0.55	0.40 0.40 0.60	dB dB dB
Isolation		300 kHz to 1.0 GHz 300 kHz to 2.0 GHz 300 kHz to 2.5 GHz	18 12 11	20 14 13		dB dB dB
Voltage Standing Wave Ratio (Note 3)	VSWR	300 kHz to 2.5 GHz		1.2:1	1.6:1	-
Switching characteristics: Rise/fall On/off		10/90% or 90/10% RF 50% control to 90/10%		10		ns
Video feedthrough		RF T _{RISE} = 1 ns, bandwidth = 500 MHz		20 25		ns mV
1 dB Input Compression Point	IP1dB	@ 0.5 to 2.5 GHz				
		$ \begin{array}{l} V_{CTL} = 0 \text{ to } 3 \text{ V} \\ V_{CTL} = 0 \text{ to } 5 \text{ V} \end{array} $		+30 +34		dBm dBm
3 rd Order Intercept Point	IP3	@ 0.5 to 2.5 GHz, for two- tone $P_{IN} = +15 \text{ dBm}$				
		$ \begin{array}{l} V_{CTL} = 0 \text{ to } 3 \text{ V} \\ V_{CTL} = 0 \text{ to } 5 \text{ V} \end{array} $		+43 +50		dBm dBm
Thermal resistance				25		°C/W
Control voltage: Low (@ 20 μA max) High (@ 100 μA max) High (@ 200 μA max)	Vctl_l Vctl_h Vctl_h		0		0.2 3.0 5.0	V V V

Table 3. AS183-92/AS183-92LF Electrical Specifications (Note 1) (Vcn = 0 to 3 V, Top = +25 °C, Characteristic Impedance = 50 Ω , Unless Otherwise Noted)

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Note 2: Insertion loss changes by 0.003 dB/°C.

Note 3: Insertion loss state.

Typical Performance Characteristics

(VcrL = 0 to-3 V, ToP = +25 °C, Characteristic Impedance [Zo] = 50 Ω , Unless Otherwise Noted)

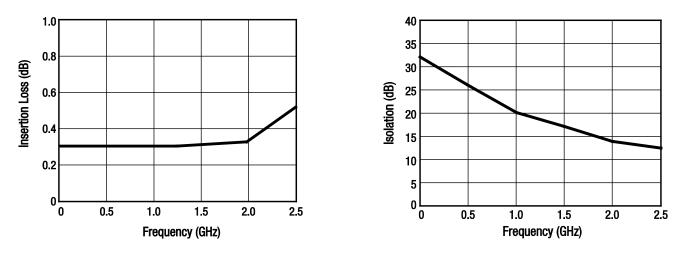


Figure 3. Insertion Loss vs Frequency

Figure 4. Isolation vs Frequency

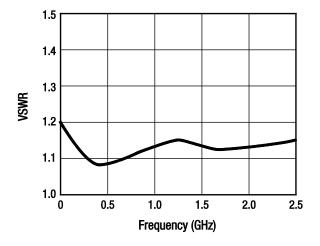


Figure 5. VSWR vs Frequency

Table 4. Truth Table (VHIGH = 3 to 5 V)

V1	V2	J1-J2	J1-J3
Vhigh	0	Insertion loss	Isolation
0	Vhigh	Isolation	Insertion loss

Note: Any state other than described in this Table places the device in an undefined state and is not recommended.

Evaluation Board Description

The AS183-92/AS183-92LF Evaluation Board is used to test the performance of the AS183-92/AS183-92LF SPDT switch. An Evaluation Board schematic diagram is provided in Figure 6. An assembly drawing for the Evaluation Board is shown in Figure 7.

Package Dimensions

The PCB layout footprint for the AS183-92/AS183-92LF is provided in Figure 8. Typical case markings are shown in Figure 9. Package dimensions for the 6-pin SC-70 are shown in Figure 10, and tape and reel dimensions are provided in Figure 11.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The AS183-92/AS183-92LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

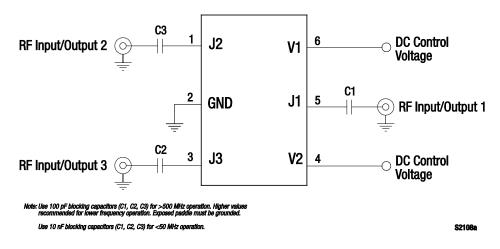


Figure 6. AS183-92/AS183-92LF Evaluation Board Schematic

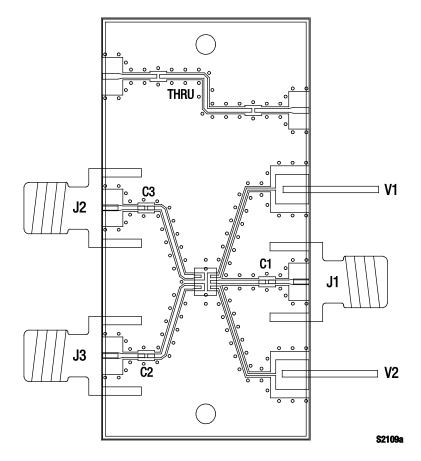


Figure 7. AS183-92/AS183-92LF Evaluation Board Assembly Diagram

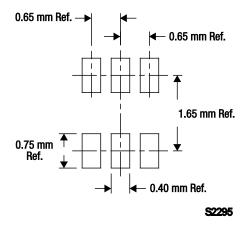


Figure 8. AS183-92/AS183-92LF PCB Layout Footprint (Top View)

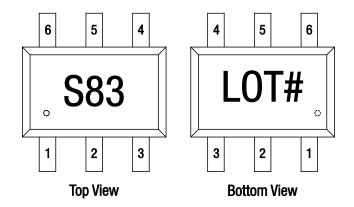
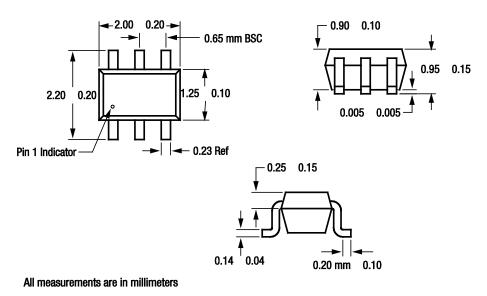


Figure 9. Typical Case Markings



Dimensioning and tolerancing according to ASME Y14.5M-1994

S1479

Figure 10. AS183-92/AS183-92LF 6-Pin SC-70 Package Dimensions

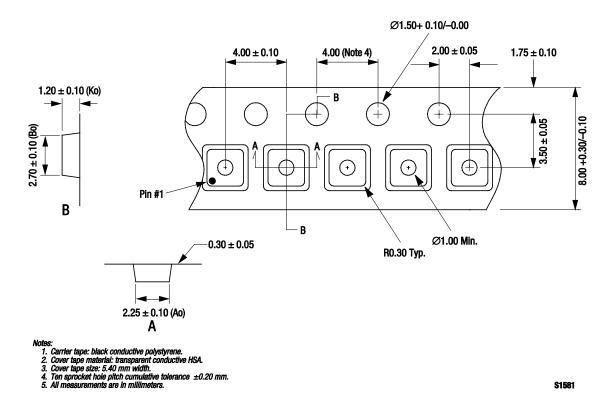


Figure 11. AS183-92/AS183-92LF Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
AS183-92/AS183-92LF SPDT Switch	AS183-92/AS183-92LF	AS183-92/AS183-92LF-EVB

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