

1. General description

Planar passivated high commutation three quadrant triac in a SOT78D (IITO-220) internally insulated plastic package with selfprotective clamping capabilities against low and high energy transients. This triac will commute the full RMS current at the maximum rated junction temperature ($T_{j(max)} = 150\text{ °C}$) without the aid of a snubber. It is used in circuits where high static and dynamic dV/dt and high dI/dt can occur and in applications where "high junction operating temperature capability" is required.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- High junction operating temperature capability ($T_{j(max)} = 150\text{ °C}$)
- High minimum I_{GT} for guaranteed immunity to gate noise
- Full cycle AC conduction
- Over-voltage withstand capability to IEC 61000-4-5
- Internally insulated package
- Isolated mounting base with 2500 V (RMS) isolation
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Less sensitive gate for high noise immunity
- Triggering in three quadrants only
- Planar passivated for voltage ruggedness and reliability

3. Applications

- Applications subject to high temperature ($T_{j(max)} = 150\text{ °C}$)
- Electronic thermostats (heating and cooling)
- High power motor controls e.g washing machine and vacuum cleaners
- Rectifier-fed DC inductive loads e.g DC motors and solenoids
- Refrigeration and air conditioning compressors

4. Quick reference data

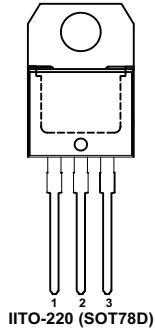
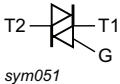
Table 1. Quick reference data

Symbol	Parameter	Conditions	Values	Unit
Absolute maximum rating				
V_{DRM}	repetitive peak off-state voltage		800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 112\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	16	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $t_p = 20\text{ ms}$; $T_{j(init)} = 25\text{ °C}$; Fig. 4 ; Fig. 5	160	A
		full sine wave; $t_p = 16.7\text{ ms}$; $T_{j(init)} = 25\text{ °C}$	176	A
T_j	junction temperature		150	°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2+ G+$ $T_j = 25\text{ }^\circ\text{C}; \text{Fig. 7}$	-	-	35	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2+ G-$ $T_j = 25\text{ }^\circ\text{C}; \text{Fig. 7}$	-	-	35	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2- G-$ $T_j = 25\text{ }^\circ\text{C}; \text{Fig. 7}$	-	-	35	mA
I_H	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 9}$	-	-	40	mA
V_T	on-state voltage	$I_T = 20\text{ A}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 10}$	-	-	1.5	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}; T_j = 125\text{ }^\circ\text{C}; (V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	1000	-	-	V/ μ s
		$V_{DM} = 536\text{ V}; T_j = 150\text{ }^\circ\text{C}; (V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	500	-	-	V/ μ s
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}; T_j = 150\text{ }^\circ\text{C}; I_{T(RMS)} = 16\text{ A};$ $dV_{com}/dt = 20\text{ V}/\mu\text{s};$ gate open circuit; snubberless condition	12	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>IITO-220 (SOT78D)</p>	 <p>sym051</p>
2	T2	main terminal 2		
3	G	gate		
mb	n.c	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BTA316Y-800CT	IITO-220	Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 leads TO-220	IITO-220E

7. Marking

Table 4. Marking codes

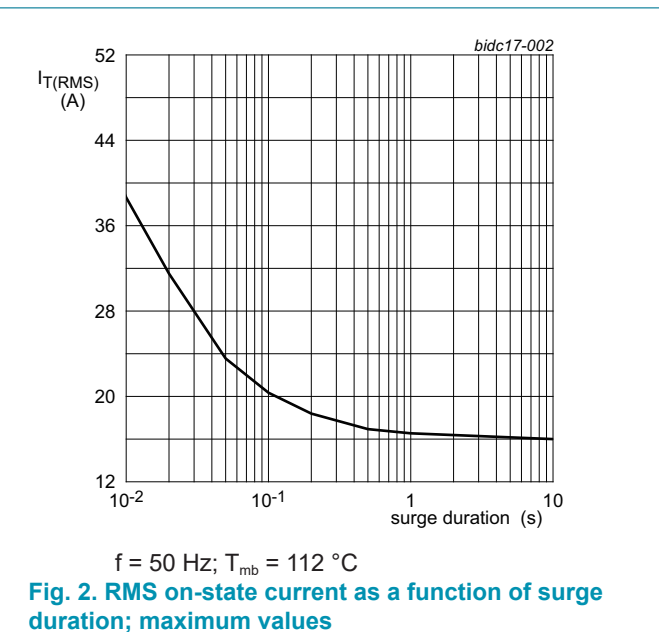
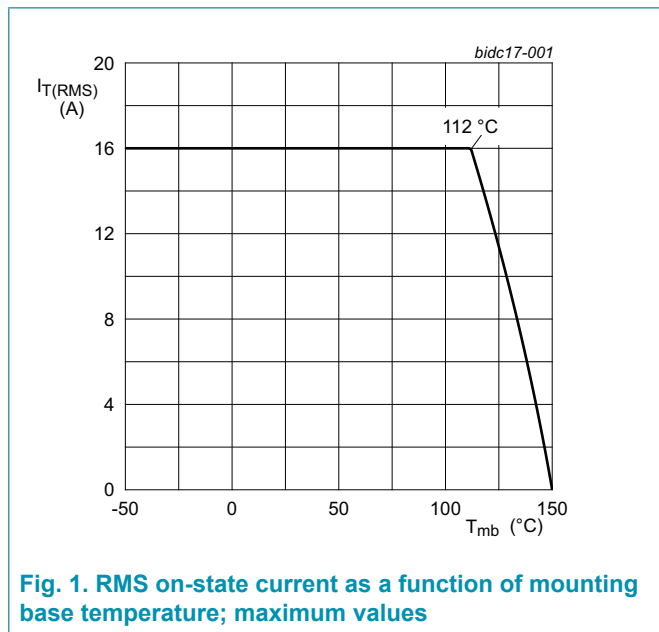
Type number	Marking codes
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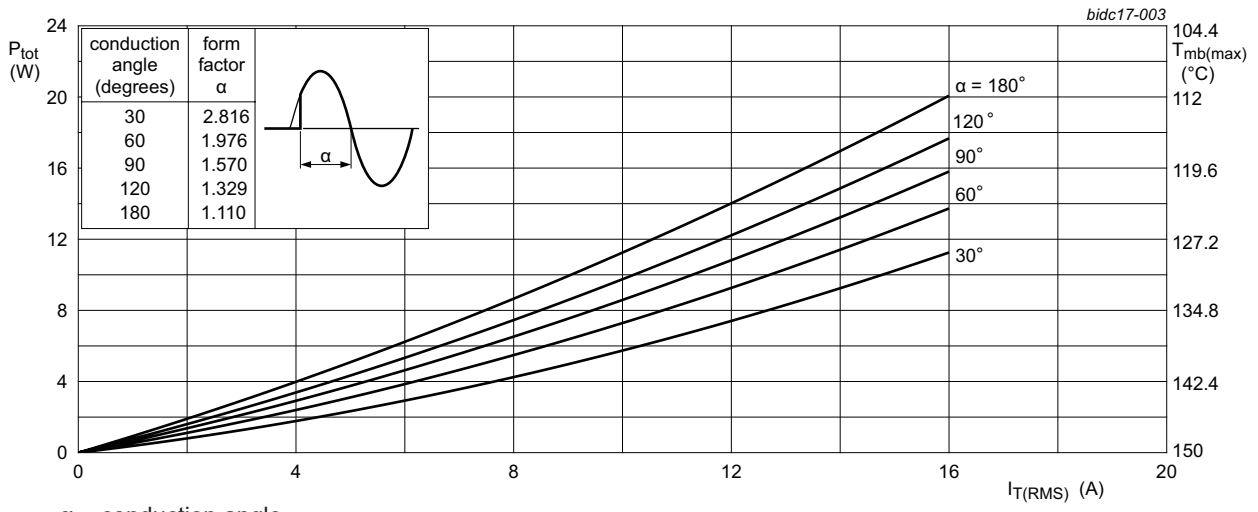
8. Limiting values

Table 4. Limiting values

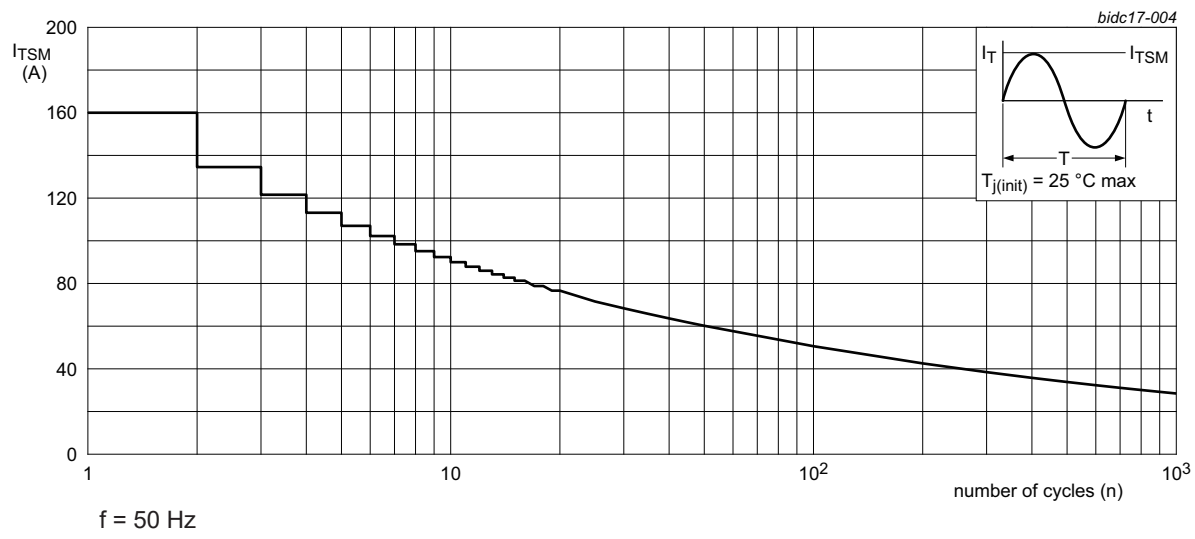
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Values	Unit
V_{DRM}	repetitive peak off-state voltage		800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 112^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	16	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $t_p = 20\text{ ms}$; $T_{j(\text{init})} = 25^\circ\text{C}$; Fig. 4 ; Fig. 5	160	A
		full sine wave; $t_p = 16.7\text{ ms}$; $T_{j(\text{init})} = 25^\circ\text{C}$	176	A
I^2t	I^2t for fusing	$t_p = 10\text{ms}$; sine wave	128	A^2s
dI_T/dt	rate of rise of on-state current	$I_G = 150\text{mA}$	100	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		2	A
P_{GM}	peak gate power		5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	0.5	W
T_{stg}	storage temperature		-40 to 150	$^\circ\text{C}$
T_j	junction temperature		150	$^\circ\text{C}$

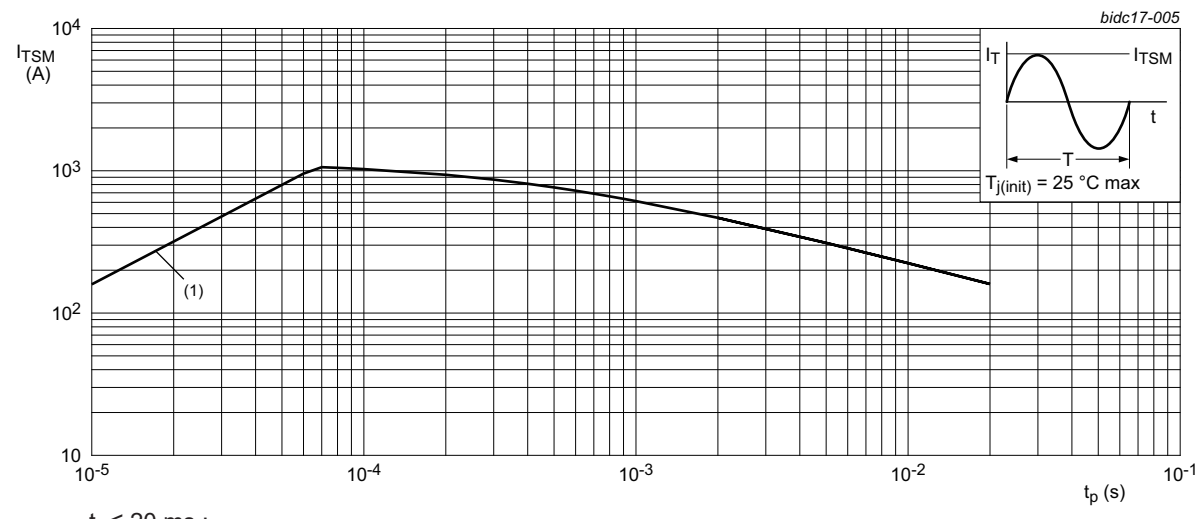




α = conduction angle
 a = form factor = $I_{T(RMS)} / I_{T(AV)}$
Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



$f = 50 \text{ Hz}$
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20 \text{ ms}$;
 (1) dI_T/dt limit
Fig. 5. Total power dissipation as a function of RMS on-state current; maximum values

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6	-	-	1.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air	-	60	-	K/W

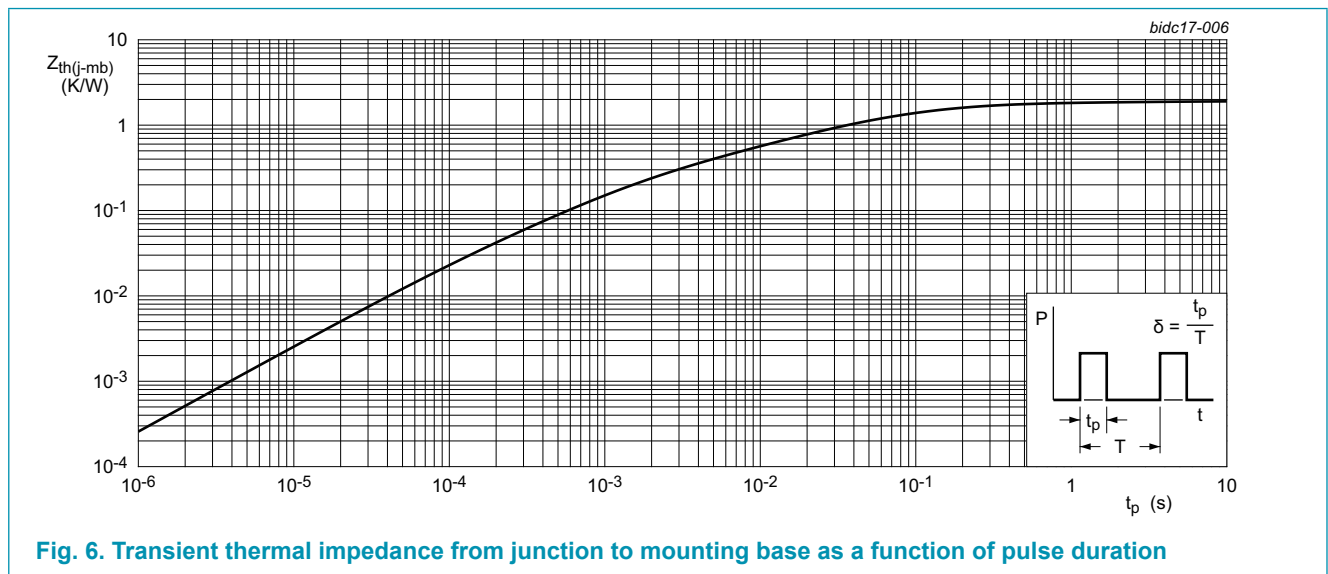


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Isolation characteristics

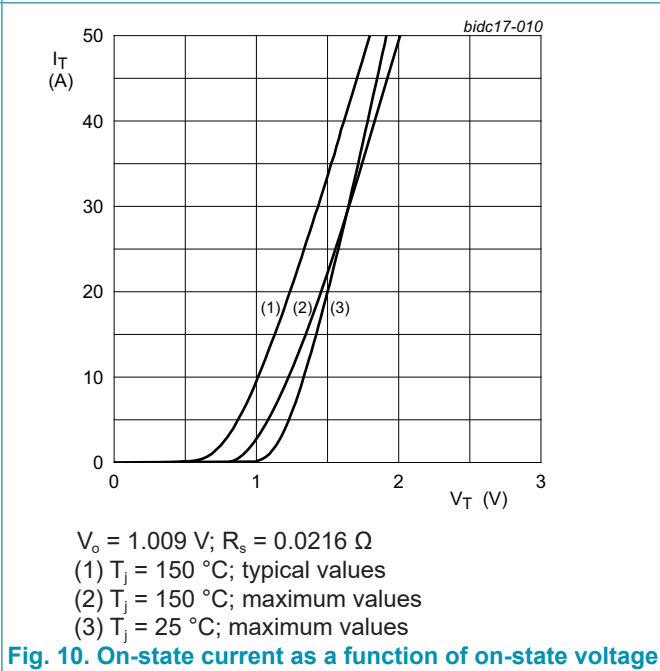
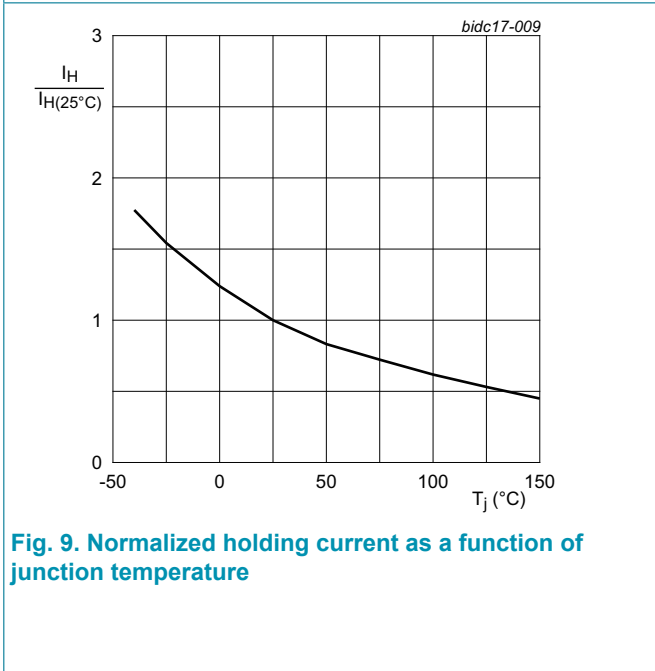
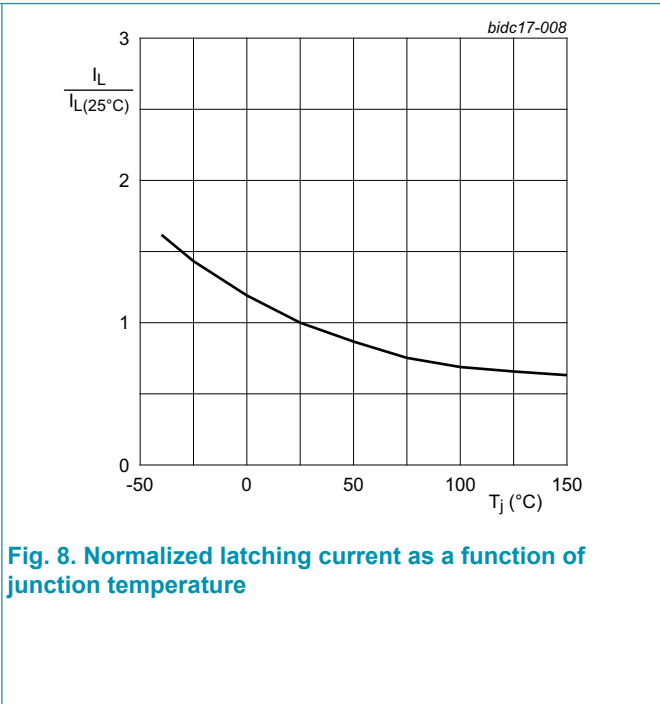
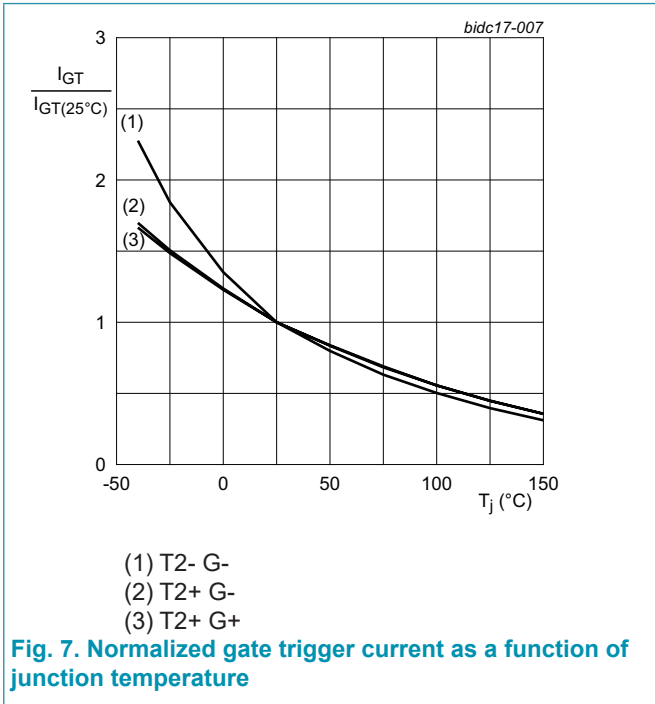
Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; from all pins to external heatsink; sinusoidal waveform; clean and dust free	-	-	2500	V
C_{isol}	isolation capacitance	from cathode to external heatsink	-	10	-	PF

11. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_J = 25\text{ °C}$; Fig. 7	-	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_J = 25\text{ °C}$; Fig. 7	-	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_J = 25\text{ °C}$; Fig. 7	-	-	35	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_J = 25\text{ °C}$; Fig. 8	-	-	50	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_J = 25\text{ °C}$; Fig. 8	-	-	70	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_J = 25\text{ °C}$; Fig. 8	-	-	50	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_J = 25\text{ °C}$; Fig. 9	-	-	40	mA
V_T	on-state voltage	$I_T = 20\text{ A}$; $T_J = 25\text{ °C}$; Fig. 10	-	-	1.5	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_J = 25\text{ °C}$; Fig. 11	-	0.8	1	V
		$V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_J = 150\text{ °C}$; Fig. 11	0.2	0.45	-	V
I_D	off-state current	$V_D = 800\text{ V}$; $T_J = 25\text{ °C}$	-	-	5	μA
		$V_D = 800\text{ V}$; $T_J = 150\text{ °C}$	-	-	2	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_J = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	1000	-	-	V/ μs
		$V_{DM} = 536\text{ V}$; $T_J = 150\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	500	-	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_J = 150\text{ °C}$; $I_{T(RMS)} = 16\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; gate open circuit; snubberless condition	12	-	-	A/ms
		$V_D = 400\text{ V}$; $T_J = 150\text{ °C}$; $I_{T(RMS)} = 16\text{ A}$; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$; gate open circuit; snubberless condition	15	-	-	A/ms
		$V_D = 400\text{ V}$; $T_J = 150\text{ °C}$; $I_{T(RMS)} = 16\text{ A}$; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$; gate open circuit; snubberless condition	20	-	-	A/ms



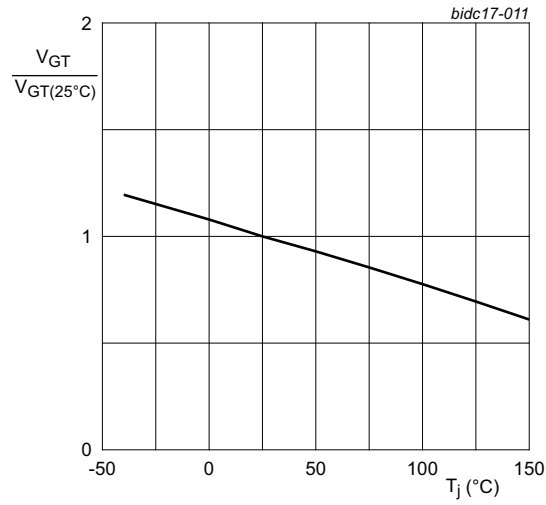
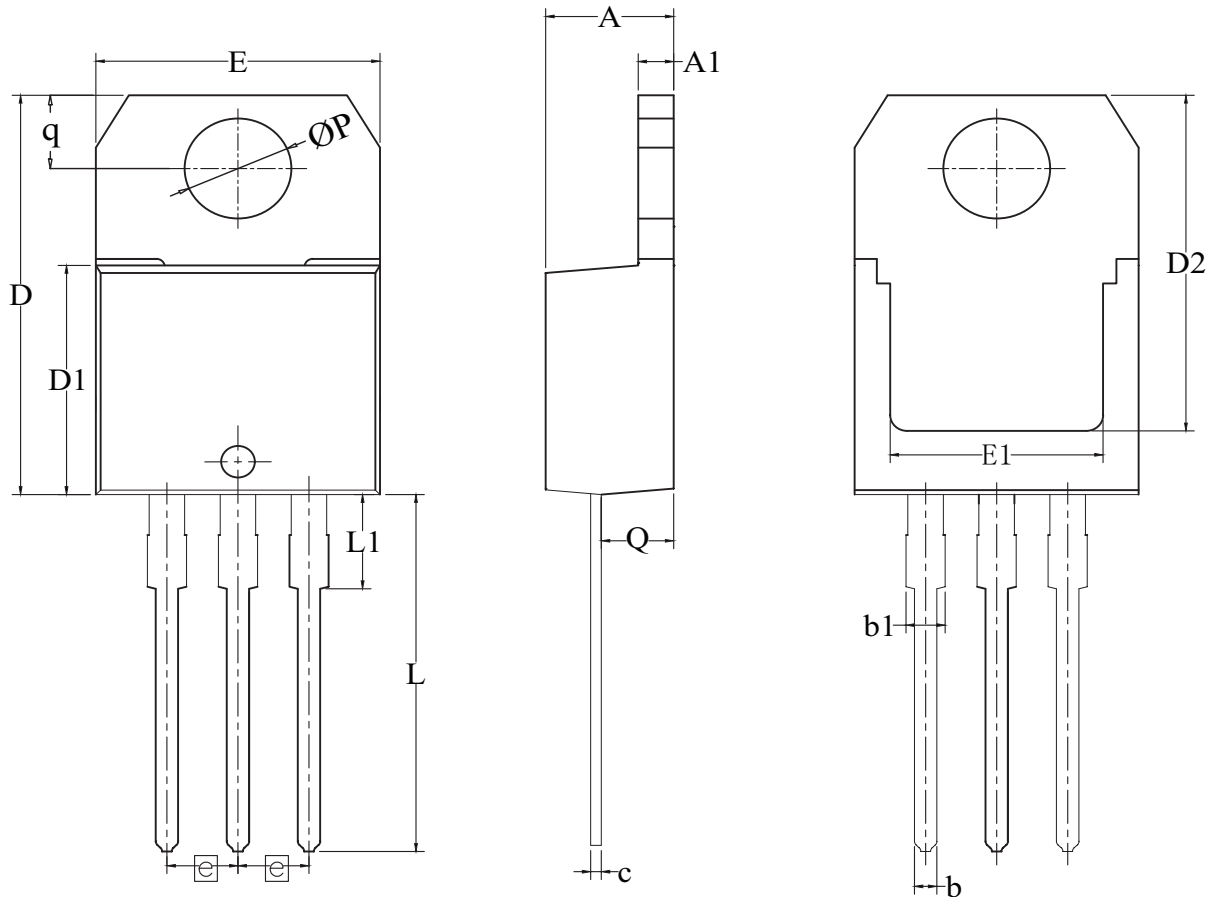


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

12. Package outline

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 leads TO-220

IITO220



Unit	A	A1	b	b1	c	D	D1	D2	E	E1	e	L	L1	P	Q	q
MM	min	4.30	1.25	0.69	1.20	0.40	15.20	8.50	12.20	10.00	6.86	12.80	2.70	3.70	2.40	2.70
	max	4.70	1.40	0.90	1.72	0.60	16.00	9.02	12.88	10.40	8.89	14.00	3.30	3.95	2.80	3.00

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 26 June 2018

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