

AK5



ESD Sensitive



5.0 x 3.2 x 1.3 mm
RoHS/RoHS II Compliant
MSL = 1

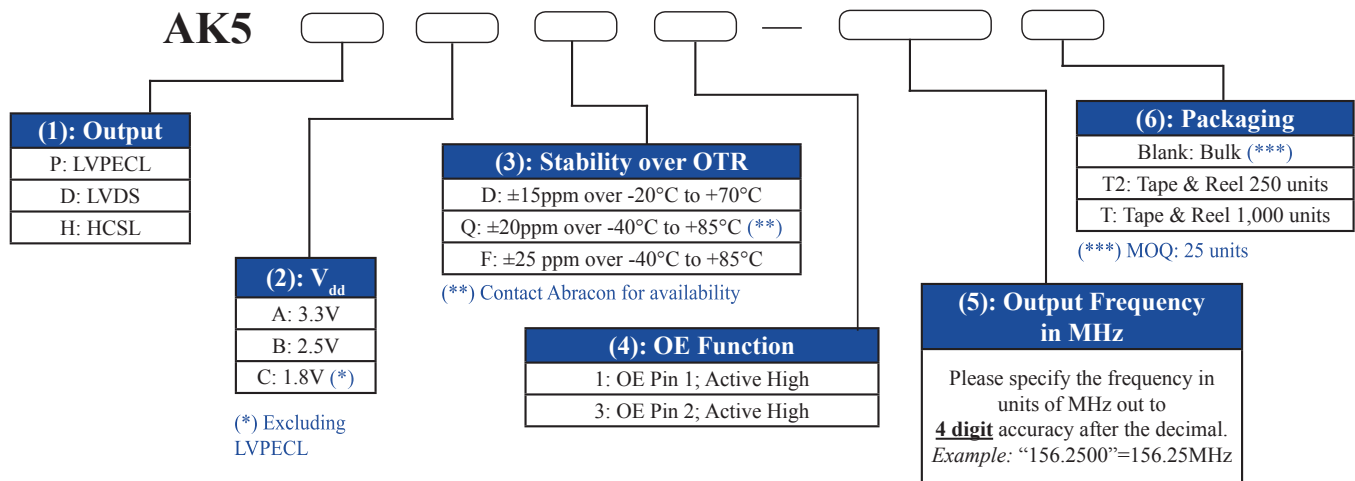
Features

- 3rd overtone solution
- Ultra-Low jitter: 70 fs typ RMS (100fs MAX, F= 156.25MHz LVPECL); spurs included
- Frequency range: 100MHz to 200MHz
- Lowest in-class power consumption (16mA Typ LVDS)
- ± 20 ppm & ± 25 ppm stability (-40 to +85°C) options available (dependent on frequency)
- 3.3V, 2.5V, 1.8V V_{dd} supply
- LVPECL, LVDS, & HCSL differential output options
- Output enable standard

Applications

- Networking and communications
- Gigabit Ethernet
- Fibre Channel
- SONET/SDH
- RF systems, base stations (BTS)
- Datacenter
- PCI Express
- Test & measurement

Options and Part Identification [Note 1]



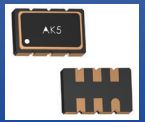
Part Number Example:

AK5PAF1-156.2500

AK5PAF1-156.2500T2

AK5PAF1-156.2500T

Note 1: Contact Abracon for non-standard part number configurations and/or requests with carrier frequency callouts up to 5 & 6 digit accuracy after the decimal.



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Electrical Characteristics

Parameters		Min.	Typ.	Max.	Unit	Notes		
Frequency Range		100		200	MHz			
Standard Available Frequencies		100 148.5	122.88 156.25	125 200	MHz	Contact Abracon for availability of frequencies not listed		
Supply Voltage (V_{dd}) ^[Note 2]		2.97 2.37 1.71	3.3 2.5 1.8	3.63 2.62 1.89	V	Option "A" Option "B" Option "C"		
Supply Current (I_{dd})	LVPECL		30	50	mA	@ 200MHz; @ $V_{dd} = 3.3V$		
	LVDS		16	27		@ 200MHz; @ $V_{dd} = 3.3V$		
	HCSL		17	30		@ 200MHz; @ $V_{dd} = 3.3V$		
Operating Temperature Range		-20 -40		+70 +85	°C	Option "D" Option "F" or "Q"		
Storage Temperature		-55		+150	°C			
Frequency Accuracy (Initial Set-Tolerance) ^[Note 3] at time of shipment (Pre-Reflow) @ +25°C		-10	< ±5	+10	ppm	Relative to carrier frequency		
Frequency Stability over ^[Note 4] Operating Temperature Range		-15 -20 -25		+15 +20 +25	ppm	Option "D" (-20°C to +70°C) Option "Q" (-40°C to +85°C) Option "F" (-40°C to +85°C)		
Aging over 20 Year Product Life ^[Note 5]		-15		+15	ppm			
All-Inclusive Frequency Accuracy (Total Stability) over 20 Year Product Life ^[Note 5, 6]		-40 -45 -50		+40 +45 +50	ppm	Option "D" (-20°C to +70°C) Option "Q" (-40°C to +85°C) Option "F" (-40°C to +85°C)		
Rise (Tr) / Fall (Tf) Time 20% to 80% $V_{peak\ to\ peak}$	LVPECL		0.2 0.3	0.4 0.6	ns	@ $V_{dd} = 3.3V, R_L = 50\Omega$ @ $V_{dd} = 2.5V, R_L = 50\Omega$		
			0.15 0.15	0.4 0.4		@ $V_{dd} = 3.3V, R_L = 100\Omega$ @ $V_{dd} = 2.5V, R_L = 100\Omega$		
	LVDS		0.3 0.3	0.5 0.5		@ $V_{dd} = 1.8V, R_L = 100\Omega$ @ $V_{dd} = 3.3V, R_L = 50\Omega$ to GND		
			0.3 0.3	0.5 0.5		@ $V_{dd} = 2.5V, R_L = 50\Omega$ to GND @ $V_{dd} = 1.8V, R_L = 50\Omega$ to GND		
	HCSL		0.3 0.3	0.5 0.6				
	Duty Cycle		45			55	%	
	Start-up Time ^[Note 3]			< 2		5.0	ms	

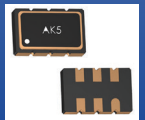
Note 2: Supply Voltage (V_{dd}) = 1.8V option not available with LVPECL output

Note 3: Relative to initial measured frequency @ +25°C

Note 4: Option Q only available in select frequencies. Please contact Abracon for availability

Note 5: Relative to post-reflow frequency

Note 6: Includes temperature stability, initial frequency accuracy, load pulling, power supply variation, and 20-year aging



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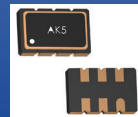


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Electrical Characteristics Cont.

Parameters		Min.	Typ.	Max.	Unit	Notes		
Differential Output High Voltage (V_{OH}) Output Low Voltage (V_{OL})	LVPECL	V_{OH}	$V_{dd}-1.03$		$V_{dd}-0.88$	V $R_L=50\Omega$ to $V_{dd}-2.0V$ $R_L=100\Omega$ between both outputs $R_L=50\Omega$ to ground on each output		
		V_{OL}	$V_{dd}-1.85$		$V_{dd}-1.60$			
	LVDS	V_{OH}		1.40	1.60			
		V_{OL}	0.90	1.10				
	HCSL	V_{OH}	0.40	0.74	0.85			
		V_{OL}	-0.15	0.00	0.15			
Output Voltage Swing		0.595	0.75	0.93	V	LVPECL		
		0.25	0.35	0.45	V	LVDS		
		0.620	0.70	0.78	V	HCSL		
Output Enable & Disable Control		$0.7*(V_{dd})$			V	Output Enable; or No Connect		
				$0.3*(V_{dd})$	V	Output Disable; High Impedance		
Output Enable Time			< 1	5.0	ms			
Output Disable Time				0.2	μs			
Output Disable Current Consumption				< 10	μA	$OE \leq 0.3V$		
RMS Phase Jitter [Note 7, 8, 9] @ +25°C (12kHz-20MHz BW)	@ 200 MHz	LVPECL		115	140	fsec	@ $V_{dd}=3.3V$	
				115	140		@ $V_{dd}=2.5V$	
		LVDS		125	150		@ $V_{dd}=3.3V$	
				65	90		@ $V_{dd}=2.5V$	
		HCSL		120	145		@ $V_{dd}=3.3V$	
				125	150		@ $V_{dd}=2.5V$	
	@ 156.25 MHz	LVPECL		75	100		fsec	@ $V_{dd}=3.3V$
				80	105			@ $V_{dd}=2.5V$
		LVDS		75	100			@ $V_{dd}=3.3V$
				100	125			@ $V_{dd}=2.5V$
		HCSL		120	145			@ $V_{dd}=3.3V$
				120	145			@ $V_{dd}=2.5V$

Note 7: Guaranteed by characterization; RMS Phase Jitter specifications are inclusive of any spurs
 Note 8: Phase jitter measured with Keysight E5052B Signal Source Analyzer
 Note 9: Refer to the next section for phase noise test setup and representative phase noise plots



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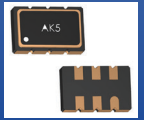
5.0 x 3.2 x 1.3 mm
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Electrical Characteristics Cont.

Parameters		Min.	Typ.	Max.	Unit	Notes
RMS Phase Jitter ^[Note 7, 8, 9] @ +25°C (12kHz-20MHz BW)	@ 148.5 MHz	LVPECL	75	100	fsec	@ V _{dd} =3.3V
			80	105		@ V _{dd} =2.5V
		LVDS	125	150		@ V _{dd} =3.3V
			120	145		@ V _{dd} =2.5V
		HCSL	115	140		@ V _{dd} =3.3V
			115	140		@ V _{dd} =2.5V
	@ 125 MHz	LVPECL	95	120	fsec	@ V _{dd} =3.3V
			125	150		@ V _{dd} =2.5V
		LVDS	185	210		@ V _{dd} =3.3V
			175	300		@ V _{dd} =2.5V
		HCSL	145	170		@ V _{dd} =1.8V
			135	160		@ V _{dd} =3.3V
	@ 122.88 MHz	LVPECL	105	130	fsec	@ V _{dd} =3.3V
			115	140		@ V _{dd} =2.5V
		LVDS	195	220		@ V _{dd} =3.3V
			180	205		@ V _{dd} =2.5V
		HCSL	145	170		@ V _{dd} =1.8V
			125	150		@ V _{dd} =3.3V
	@ 100 MHz	LVPECL	180	205	fsec	@ V _{dd} =2.5V
			180	205		@ V _{dd} =1.8V
		LVDS	185	210		@ V _{dd} =3.3V
			160	185		@ V _{dd} =2.5V
		HCSL	305	330		@ V _{dd} =3.3V
			300	325		@ V _{dd} =2.5V
	LVDS	195	220	fsec	@ V _{dd} =1.8V	
		170	195		@ V _{dd} =3.3V	
	HCSL	180	205		@ V _{dd} =2.5V	
		175	200		@ V _{dd} =1.8V	

Note 7: Guaranteed by characterization; RMS Phase Jitter specifications are inclusive of any spurs
 Note 8: Phase jitter measured with Keysight E5052B Signal Source Analyzer
 Note 9: Refer to the next section for phase noise test setup and representative phase noise plots

ClearClock™ | Ultra-Low Jitter 5.0 x 3.2mm XO



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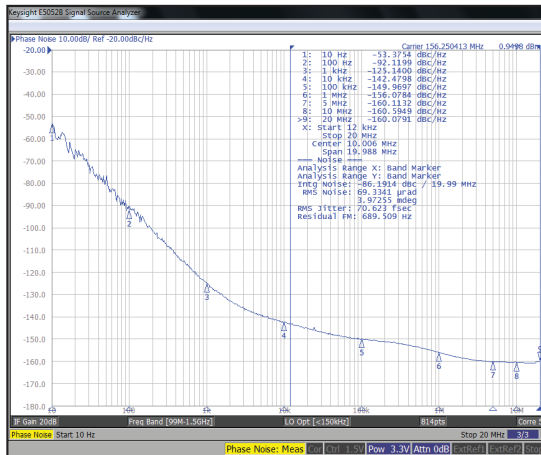


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MSL = 1

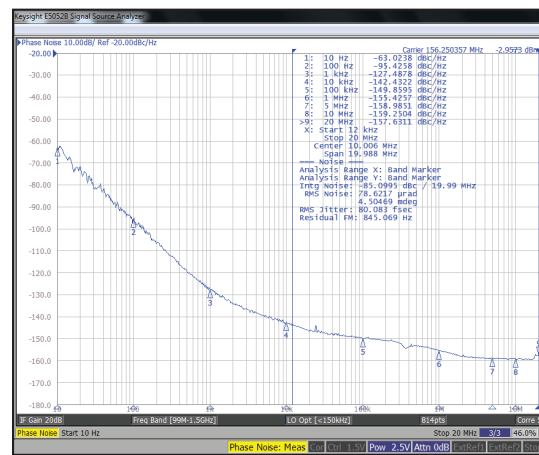
Phase Noise Test Setup ^[Note 10]

- Keysight E5052B Signal Source Analyzer
- Integration Bandwidth = 12kHz to 20MHz
- Spurious Activity (entire plot trace) = NOT Omitted (Normalized in dBc/Hz)
- Specified Spur Omission Function = NOT Enabled
- IF Gain = 20dB
- Correlation = 5
- Average = 3

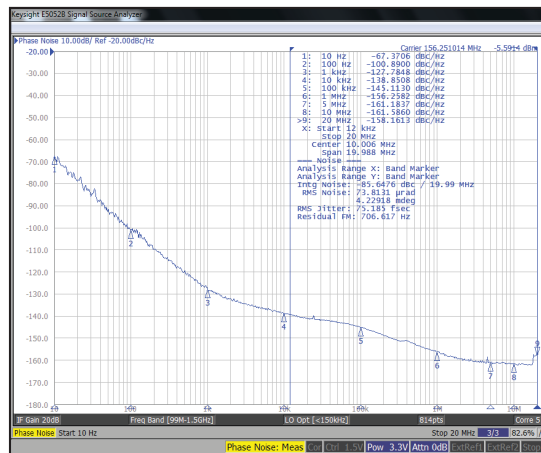
F=156.2500MHz | V_{dd}=3.3V | LVPECL
RMS Phase Jitter = 70 fsec



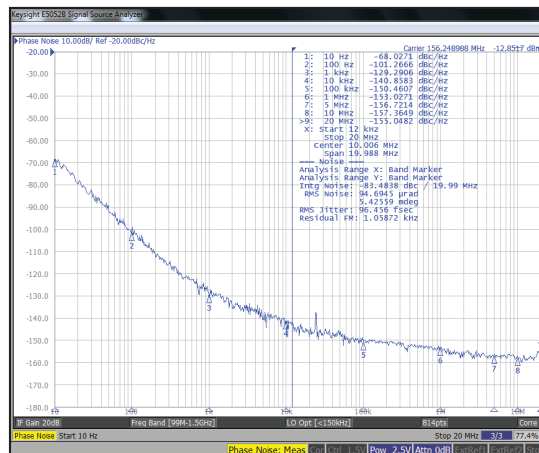
F=156.2500MHz | V_{dd}=2.5V | LVPECL
RMS Phase Jitter = 80 fsec



F=156.2500MHz | V_{dd}=3.3V | LVDS
RMS Phase Jitter = 75 fsec



F=156.2500MHz | V_{dd}=2.5V | LVDS
RMS Phase Jitter = 96 fsec



Note 10: Contact Abracon for phase noise plots at alternative supply voltage (V_{dd}) & differential output formats.

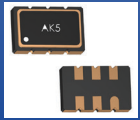


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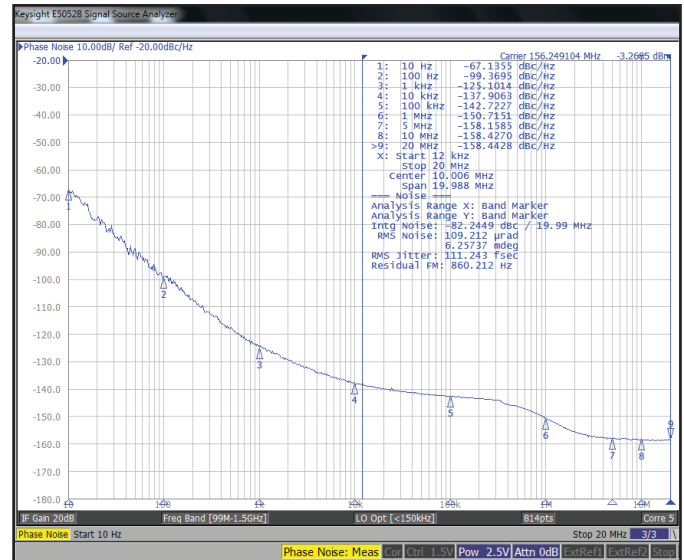
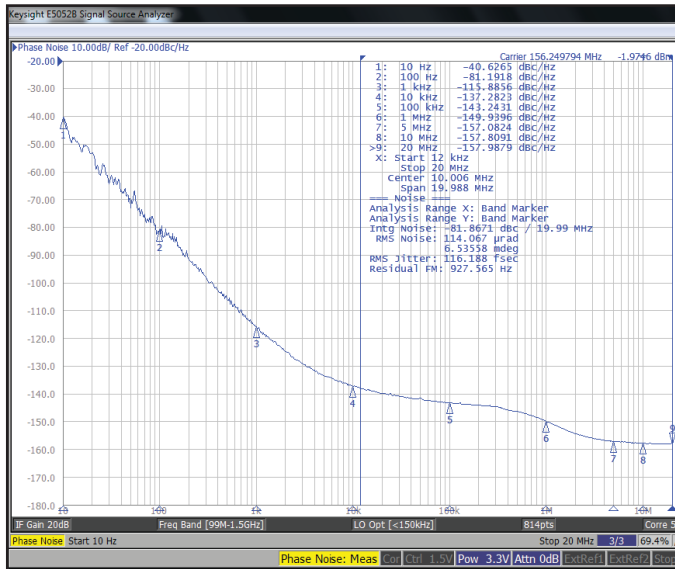


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Representative Phase Noise Plots @ +25°C [Note 10]

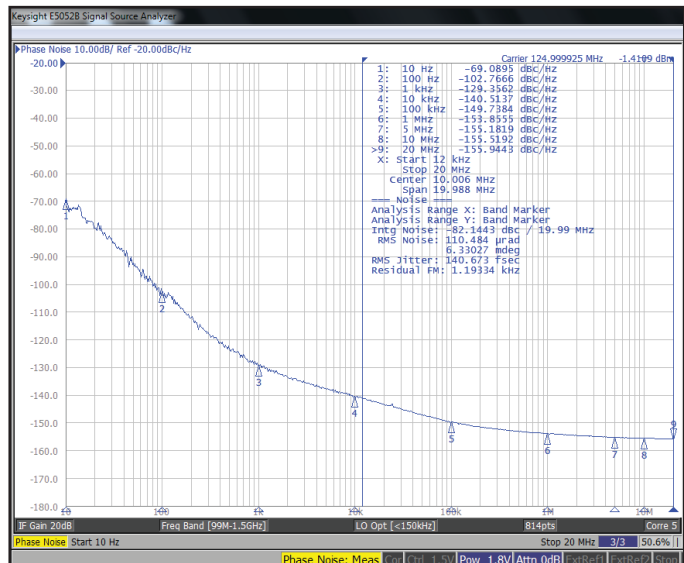
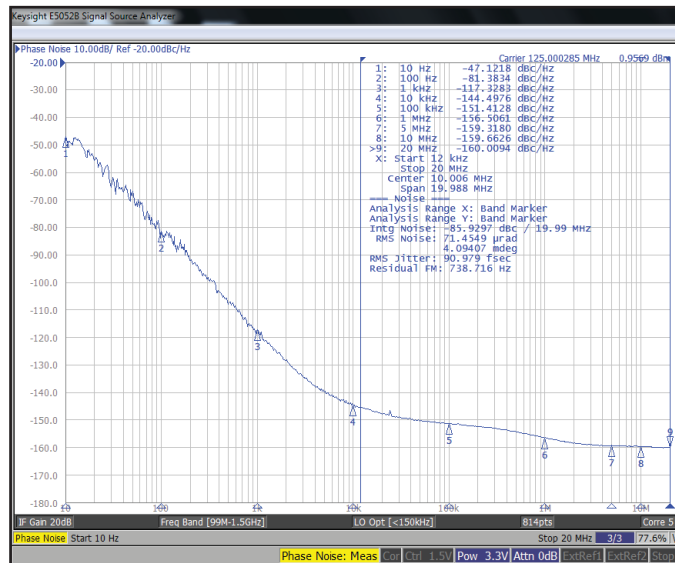
F= 156.2500MHz | V_{dd}=3.3V | HCSL
RMS Phase Jitter = 116 fsec

F=156.2500MHz | V_{dd}=2.5V | HCSL
RMS Phase Jitter = 111 fsec



F=125.0000MHz | V_{dd}=3.3V | LVPECL
RMS Phase Jitter = 90 fsec

F= 125.0000MHz | V_{dd}=1.8V | LVDS
RMS Phase Jitter = 140 fsec



Note 10: Contact Abracon for phase noise plots at alternative supply voltage (V_{dd}) & differential output formats.

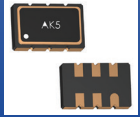


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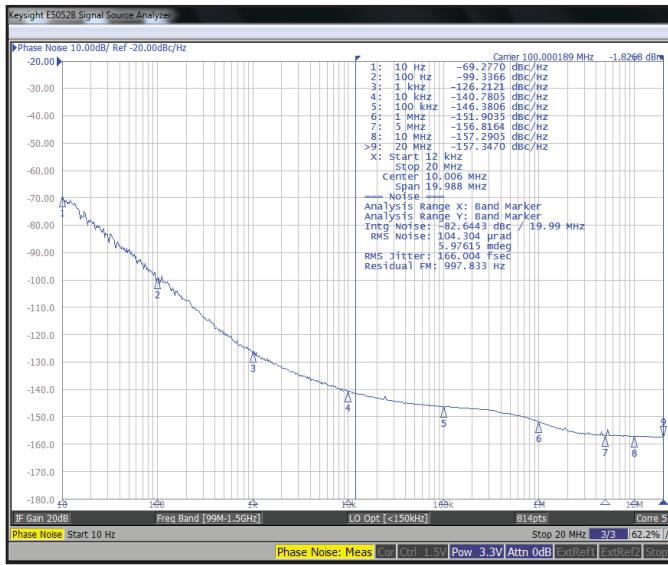
ESD Sensitive



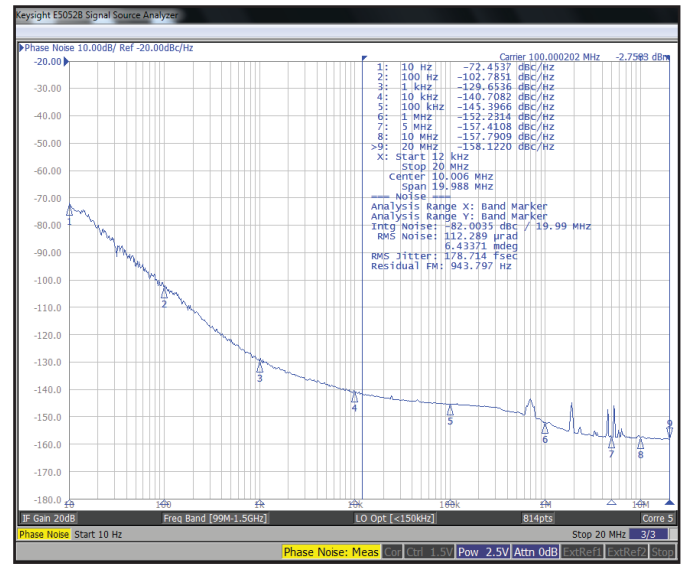
5.0 x 3.2 x 1.3 mm
RoHS/RoHS II Compliant
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Representative Phase Noise Plots @ +25°C Cont. [Note 10]

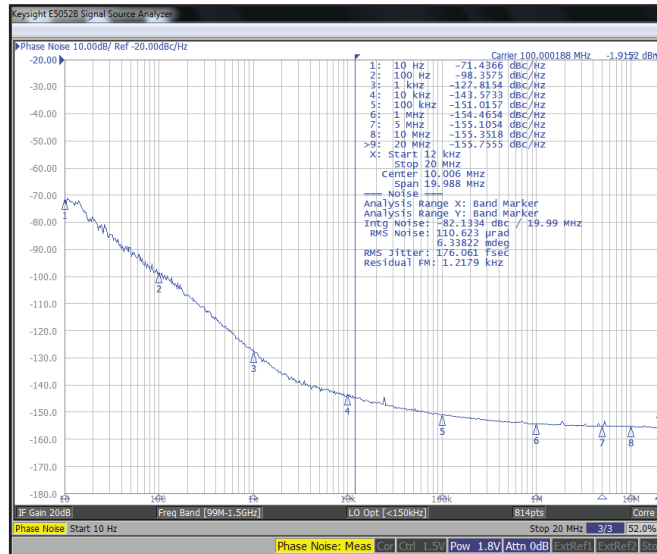
F= 100.000MHz | V_{dd}=3.3V | HCSSL
RMS Phase Jitter = 166 fsec



F=100.000MHz | V_{dd}=2.5V | HCSSL
RMS Phase Jitter = 178 fsec



F=100.000MHz | V_{dd}=1.8V | HCSSL
RMS Phase Jitter = 176 fsec



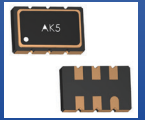
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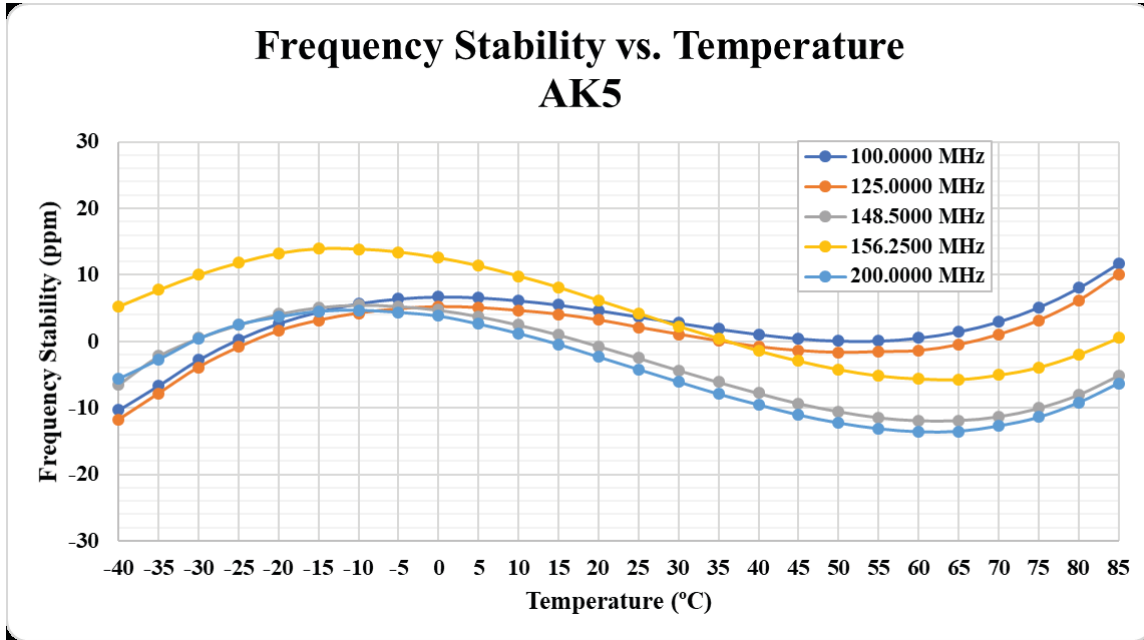


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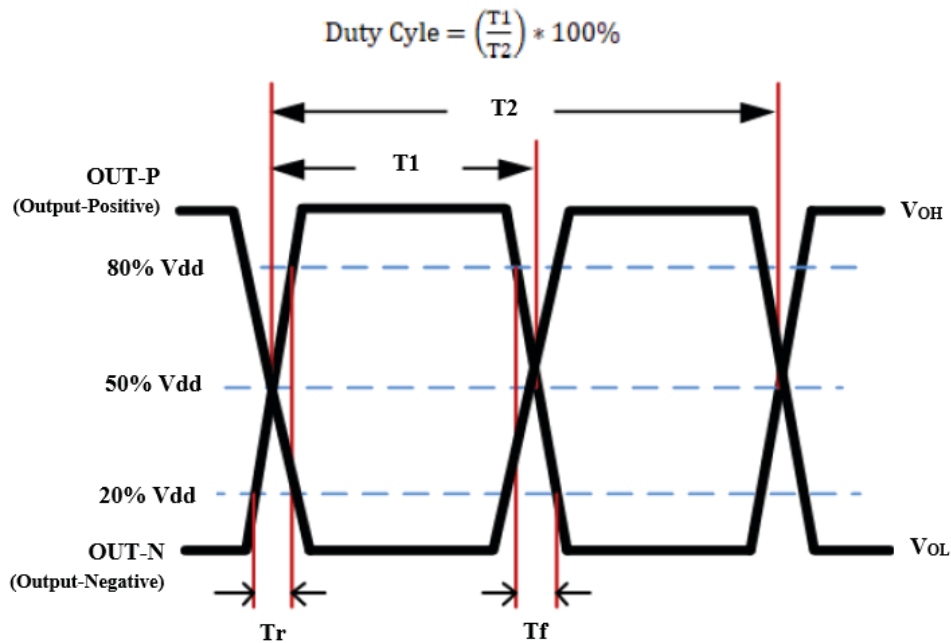


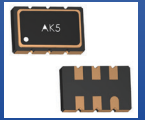
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Typical Frequency vs. Temperature Characteristics



Differential Output Waveform





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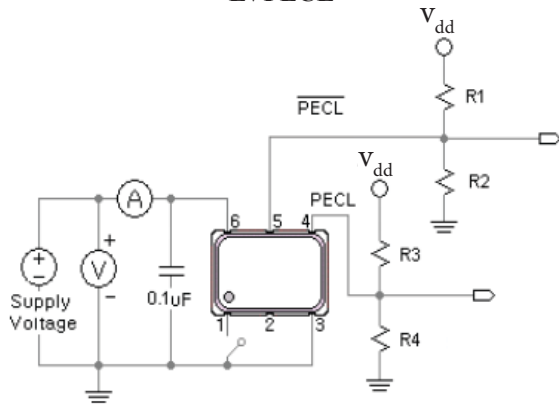
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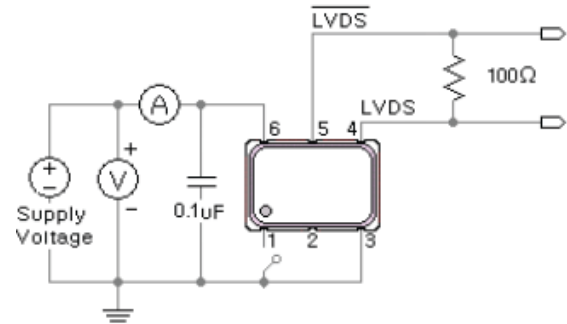
Recommended Test Circuit ^[Note 11]

LVPECL

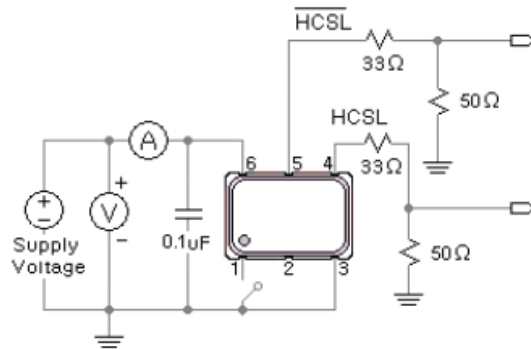


$V_{dd}=3.3V$: $R1=R3=127\Omega$; $R2=R4=82.5\Omega$
 $V_{dd}=2.5V$: $R1=R3=250\Omega$; $R2=R4=62.5\Omega$

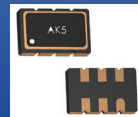
LVDS



HCSL



Note 11: Recommended test circuit images are representative of when the OE Function is located on Pin 1; when the OE Function is located on Pin 2, then Pin 1=No Connect & Pin 2=OE or No Connect.



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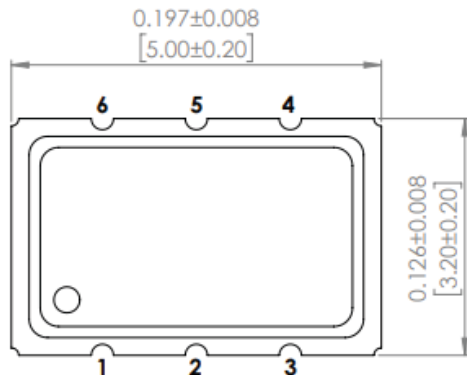


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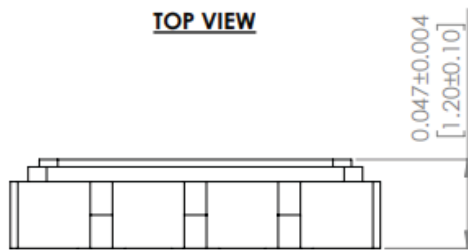


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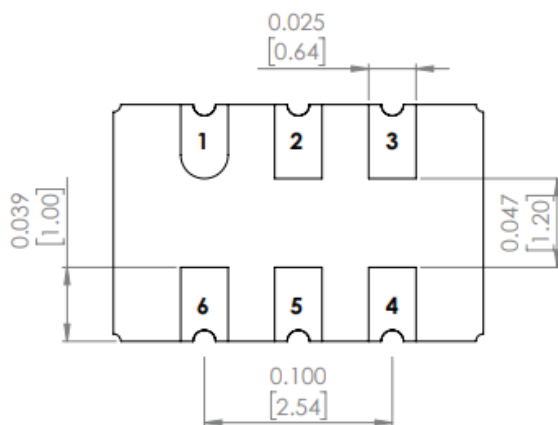
Mechanical Dimensions



TOP VIEW

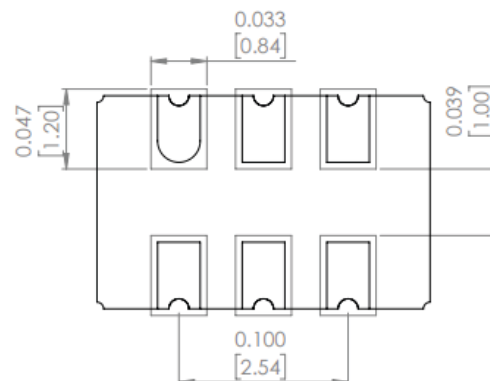


SIDE VIEW



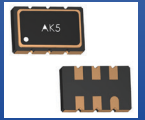
BOTTOM VIEW

Recommended Land Pattern



Case 1 Pin #1=Output Enable/Disable Function where OE is Active HIGH		Case 2 Pin #2=Output Enable/Disable Function where OE is Active HIGH	
Pin	Description	Pin	Description
# 1	Output Enable = Logic High, "1", V _{dd}	# 2	Output Enable = Logic High, "1", V _{dd}
	Output Disable = Logic Low, "0", GND		Output Enable = Logic Low, "0", GND
# 2	No Connect	# 3	GND
# 3	GND	# 4	Output
# 4	Output	# 5	Complementary output
# 5	Complementary output	# 6	Supply Voltage (V _{dd})
# 6	Supply Voltage (V _{dd})		

Dimensions: inches [mm]



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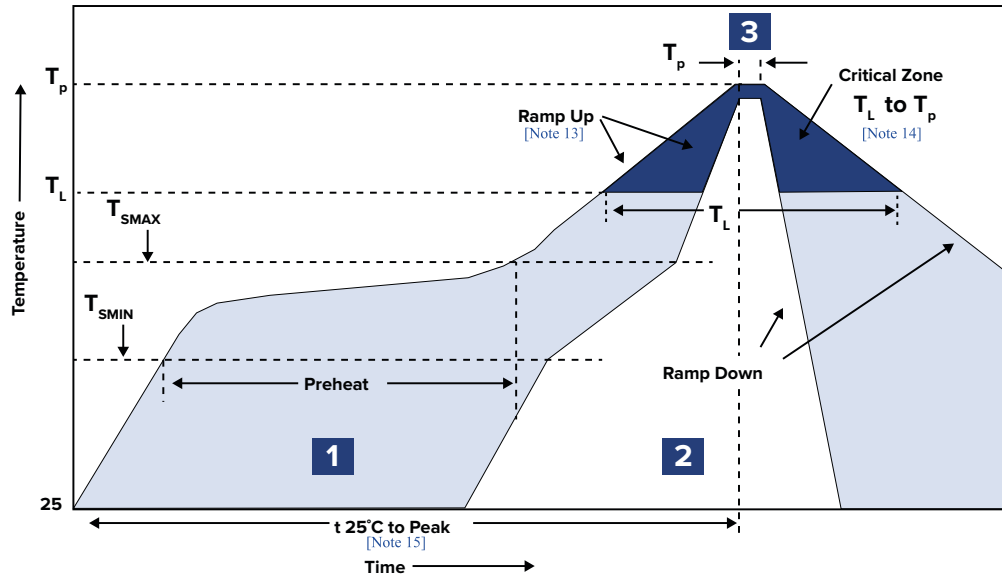


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Recommended Reflow Profile [Note 12]



Zone	Description	Temperature	Time
1	Preheat / Soak	$T_{SMIN} \sim T_{SMAX}$ 150°C ~ 200°C	60 ~ 180 sec.
2	Reflow	T_L 217°C	60 ~ 150 sec.
3	Peak heat	T_P 260°C±5°C	20 ~ 40 sec.

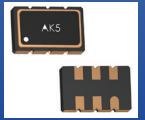
Note 12: Can withstand: 2 reflows

Note 13: Ramp Up Rate ($T_L \rightarrow T_P$) = 3°C / sec. MAX

Note 14: Ramp Down Rate ($T_P \rightarrow T_L$) = 6°C / sec. MAX

Note 15: Time 25°C to Peak Temperature (25°C → T_P) = 8 minutes MAX

All temperatures refer to topside of the package, measured on the package body surface.



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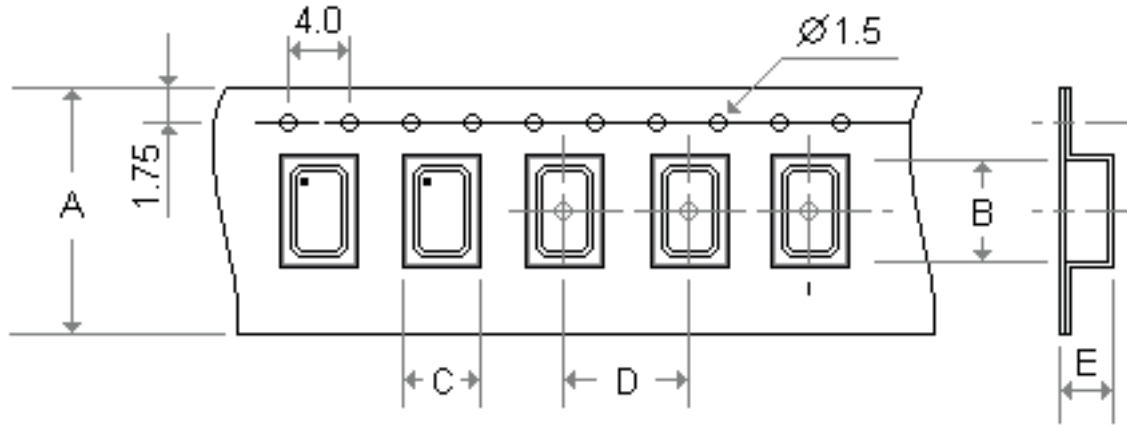


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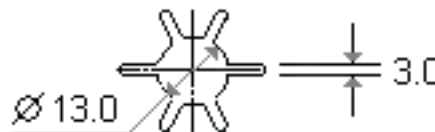
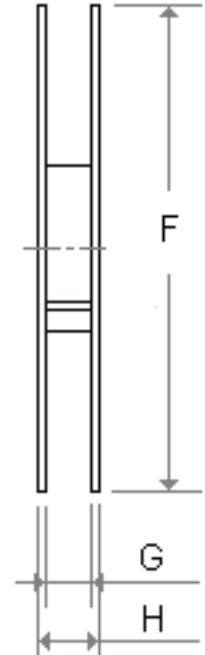
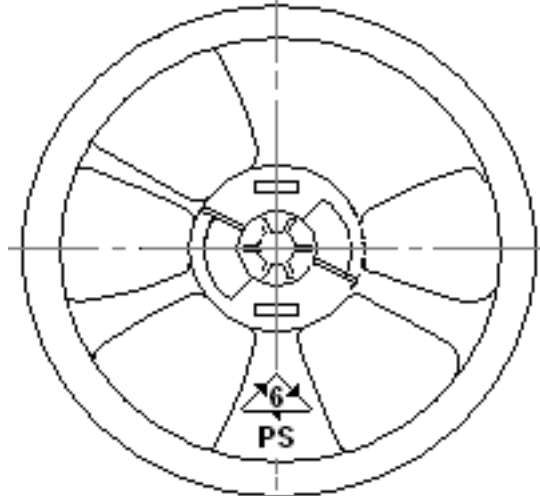
Packaging

Bulk (MOQ = 25 units)
T2 = Tape & Reel 250 units/reel
T = Tape & Reel 1,000 units/reel

Feeding (PULL) Direction →



Tape Dimensions	
A	12.0
B	5.30
C	3.60
D	8.00
E	1.40
Reel Dimensions	
F	180.00
G	13.00
H	16.00



Dimensions: mm

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