720MHz, 3.5mA Power Efficient Rail-to-Rail I/O Op Amps

FEATURES

- **Gain Bandwidth Product: 720MHz**
- **–3dB Frequency (A_V = 1): 400MHz**
- **Low Quiescent Current: 3.5mA Max**
- **High Slew Rate: 280V/µs**
- **Input Common Mode Range Includes Both Rails**
- **Output Swings Rail-to-Rail**
- Low Broadband Voltage Noise: 2.75nV/$\sqrt{Hz}$
- Power-Down Mode: 42µA
- Fast Output Recovery
- Supply Voltage Range: 2.5V to 5.25V
- Input Offset Voltage: 350µV Max
- Large Output Current: 90mA
- CMRR: 105dB
- Open Loop Gain: 60V/mV
- Operating Temperature Range: –40°C to 125°C
- Single in 6-Pin TSOT-23
- Dual in MS8, 2mm × 2mm DFN, 8-Pin TSOT-23, MS10
- Quad in MS16

APPLICATIONS

- Low Voltage, High Frequency Signal Processing
- Driving A/D Converters
- Rail-to-Rail Buffer Amplifiers
- Active Filters
- Battery Powered Equipment

DESCRIPTION

The LTC®6252/LTC6253/LTC6254 are single/dual/quad low power, high speed unity gain stable rail-to-rail input/output operational amplifiers. On only 3.5mA of supply current they feature a 720MHz gain-bandwidth product, 280V/µs slew rate and a low 2.75nV/$\sqrt{Hz}$ of input-referred noise. The combination of high bandwidth, high slew rate, low power consumption and low broadband noise makes the LTC6252 family unique among rail-to-rail input/output op amps with similar supply currents. They are ideal for lower supply voltage high speed signal conditioning systems.

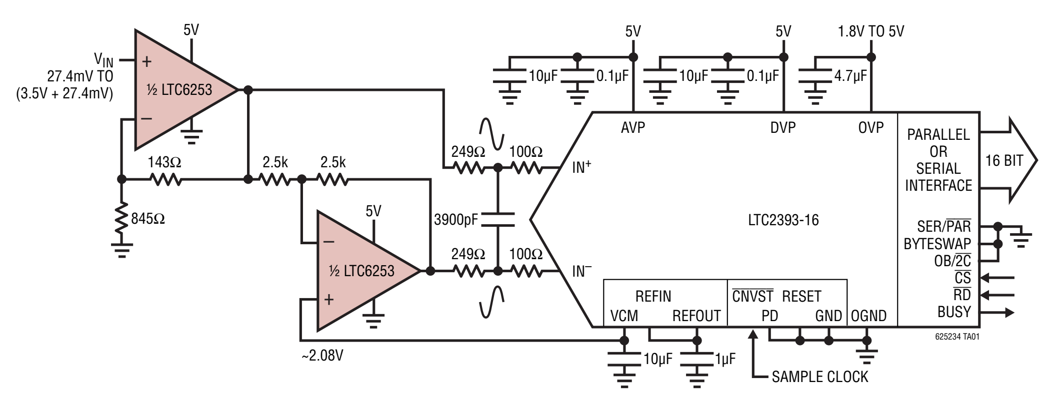
The LTC6252 family maintains high efficiency performance from supply voltage levels of 2.5V to 5.25V and is fully specified at supplies of 2.7V and 5.0V.

For applications that require power-down, the LTC6252 and the LTC6253 in MS10 offer a shutdown pin which disables the amplifier and reduces current consumption to 42µA.

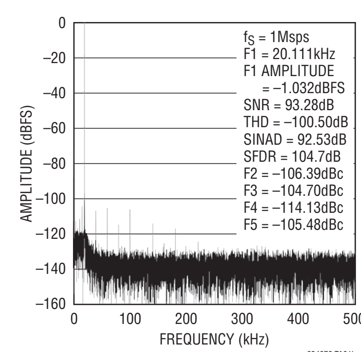
The LTC6252 family can be used as a plug-in replacement for many commercially available op amps to reduce power or to improve input/output range and performance.

TYPICAL APPLICATION

5V Single-Supply 16-Bit ADC Driver



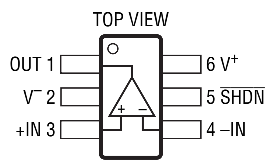
LTC6253 Driving LTC2393-16 16-Bit ADC 5V Single-Supply Performance



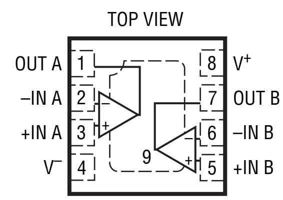
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-)................................5.5V
Input Current (+IN, –IN, $\overline{SHDN}$) (Note 2)............. ±10mA
Output Current (Note 3) .... ±100mA
Operating Temperature Range (Note 4).. –40°C to 125°C
Specified Temperature Range (Note 5) .. –40°C to 125°C
Storage Temperature Range .... –65°C to 150°C
Junction Temperature .... 150°C
Lead Temperature (Soldering, 10 sec)
MSOP, TSOT Packages Only .... 300°C

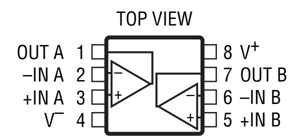
PIN CONFIGURATION



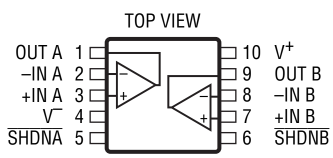
S6 PACKAGE
6-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 192°C/W (NOTE 9)



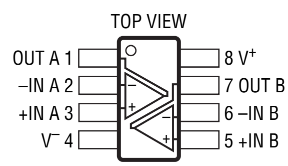
DC PACKAGE
8-LEAD (2mm × 2mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 102°C/W (NOTE 9)
EXPOSED PAD (PIN 9) IS V^-, MUST BE SOLDERED TO PCB



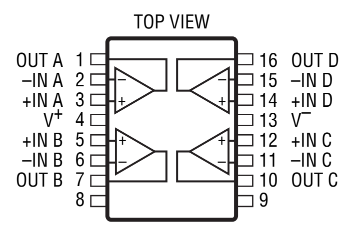
MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 163°C/W (NOTE 9)



MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 160°C/W (NOTE 9)



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 195°C/W (NOTE 9)



MS PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 125°C/W (NOTE 9)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6252CS6#TRMPBF	LTC6252CS6#TRPBF	LTFRW	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6252IS6#TRMPBF	LTC6252IS6#TRPBF	LTFRW	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6252HS6#TRMPBF	LTC6252HS6#TRPBF	LTFRW	6-Lead Plastic TSOT-23	–40°C to 125°C
LTC6253CDC#TRMPBF	LTC6253CDC#TRPBF	LFRZ	8-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LTC6253IDC#TRMPBF	LTC6253IDC#TRPBF	LFRZ	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LTC6253CMS8#PBF	LTC6253CMS8#TRPBF	LTFRX	8-Lead Plastic MSOP	0°C to 70°C
LTC6253IMS8#PBF	LTC6253IMS8#TRPBF	LTFRX	8-Lead Plastic MSOP	–40°C to 85°C
LTC6253HMS8#PBF	LTC6253HMS8#TRPBF	LTFRX	8-Lead Plastic MSOP	–40°C to 125°C
LTC6253CTS8#TRMPBF	LTC6253CTS8#TRPBF	LTFRY	8-Lead Plastic TSOT-23	0°C to 70°C
LTC6253ITS8#TRMPBF	LTC6253ITS8#TRPBF	LTFRY	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC6253HTS8#TRMPBF	LTC6253HTS8#TRPBF	LTFRY	8-Lead Plastic TSOT-23	–40°C to 125°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6253CMS#PBF	LTC6253CMS#TRPBF	LTFSB	10-Lead Plastic MSOP	0°C to 70°C
LTC6253IMS#PBF	LTC6253IMS#TRPBF	LTFSB	10-Lead Plastic MSOP	–40°C to 85°C
LTC6254CMS#PBF	LTC6254CMS#TRPBF	6254	16-Lead Plastic MSOP	0°C to 70°C
LTC6254IMS#PBF	LTC6254IMS#TRPBF	6254	16-Lead Plastic MSOP	–40°C to 85°C
LTC6254HMS#PBF	LTC6254HMS#TRPBF	6254	16-Lead Plastic MSOP	–40°C to 125°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS (V_S = 5V)

The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at T_A = 25°C. For each amplifier V_S = 5V, 0V; $V_{\overline{SHDN}}$ = 2V; V_{CM} = V_{OUT} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = Half Supply		–350	50	350	µV
			●	–1000		1000	µV
		V_{CM} = V^+ – 0.5V, NPN Mode		–2.2	0.1	2.2	mV
			●	–3.3		–3.3	mV
ΔV_{OS}	Input Offset Voltage Match (Channel-to-Channel) (Note 8)	V_{CM} = Half Supply		–350	50	350	µV
			●	–550		550	µV
		V_{CM} = V^+ – 0.5V, NPN Mode		–2.75	0.1	2.75	mV
			●	–4		4	mV
V_{OS} T_C	Input Offset Voltage Drift		●		–3.5		µV/°C
I_B	Input Bias Current (Note 7)	V_{CM} = Half Supply		–0.75	–0.1	0.75	µA
			●	–1.15		1.15	µA
		V_{CM} = V^+ – 0.5V, NPN Mode		0.8	1.4	3.0	µA
			●	0.4		5.0	µA
I_{OS}	Input Offset Current	V_{CM} = Half Supply		–0.5	–0.03	0.5	µA
			●	–0.6		0.6	µA
		V_{CM} = V^+ – 0.5V, NPN Mode		–0.5	–0.03	0.5	µA
			●	–0.6		0.6	µA
e_n	Input Noise Voltage Density	f = 1MHz			2.75		nV/√Hz
	Input 1/f Noise Voltage	f = 0.1Hz to 10Hz			2		μV_{P-P}
i_n	Input Noise Current Density	f = 1MHz			4		pA/√Hz
C_{IN}	Input Capacitance	Differential Mode			2.5		pF
		Common Mode			0.8		pF
R_{IN}	Input Resistance	Differential Mode			7.2		kΩ
		Common Mode			3		MΩ
A_{VOL}	Large Signal Voltage Gain	R_L = 1k to Half Supply (Note 10)		35	60		V/mV
			●	16			V/mV
		R_L = 100Ω to Half Supply (Note 10)		5	13		V/mV
			●	2.4			V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 3.5V		85	105		dB
			●	82			dB

ELECTRICAL CHARACTERISTICS (V_S = 5V)

The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at T_A = 25°C. For each amplifier V_S = 5V, 0V; $V_{\overline{SHDN}}$ = 2V; V_{CM} = V_{OUT} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CMR}	Input Common Mode Range		●	0		V_S	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 5.25V V_{CM} = 1V	 ●	66.5 62	70		dB dB
	Supply Voltage Range (Note 6)		●	2.5		5.25	V
V_{OL}	Output Swing Low (V_{OUT} – V^-)	No Load	 ●		25	40 65	mV mV
		I_{SINK} = 5mA	 ●		60	90 120	mV mV
		I_{SINK} = 25mA	 ●		150	200 320	mV mV
V_{OH}	Output Swing High (V^+ – V_{OUT})	No Load	 ●		65	100 120	mV mV
		I_{SOURCE} = 5mA	 ●		115	170 210	mV mV
		I_{SOURCE} = 25mA	 ●		270	330 450	mV mV
I_{SC}	Output Short-Circuit Current	Sourcing	 ●		–90	–40 –32	mA mA
		Sinking	 ●	60 40	100		mA mA
I_S	Supply Current per Amplifier	V_{CM} = Half Supply	 ●		3.3	3.5 4.8	mA mA
		V_{CM} = V^+ – 0.5V	 ●		4.25	4.85 5.9	mA mA
I_{SD}	Disable Supply Current	$V_{\overline{SHDN}}$ = 0.8V	 ●		42	55 75	µA µA
$I_{\overline{SHDNL}}$	$\overline{SHDN}$ Pin Current Low	$V_{\overline{SHDN}}$ = 0.8V	 ●	–3 –4	–1.6	0 0	µA µA
$I_{\overline{SHDNH}}$	$\overline{SHDN}$ Pin Current High	$V_{\overline{SHDN}}$ = 2V	 ●	–300 –600	35	300 600	nA nA
V_L	$\overline{SHDN}$ Pin Input Voltage Low		●			0.8	V
V_H	$\overline{SHDN}$ Pin Input Voltage High		●	2			V
I_{OSD}	Output Leakage Current in Shutdown	$V_{\overline{SHDN}}$ = 0.8V, Output Shorted to Either Supply			100		nA
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.8V to 2V			3.5		µs
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 2V to 0.8V			2		µs
BW	–3dB Closed Loop Bandwidth	A_V = 1, R_L = 1k to Half Supply			400		MHz
GBW	Gain-Bandwidth Product	f = 4MHz, R_L = 1k to Half Supply	 ●	450 320	720		MHz MHz
t_S, 0.1%	Settling Time to 0.1%	A_V = 1, V_O = 2V Step R_L = 1k			36		ns
SR	Slew Rate	A_V = –1, 4V Step (Note 11)			280		V/µs
FPBW	Full Power Bandwidth	V_{OUT} = $4V_{P-P}$ (Note 13)			9.5		MHz

ELECTRICAL CHARACTERISTICS (V_S = 5V)

The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at T_A = 25°C. For each amplifier V_S = 5V, 0V; $V_{\overline{SHDN}}$ = 2V; V_{CM} = V_{OUT} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
HD2/HD3	Harmonic Distortion R_L = 1k to Half Supply	f_C = 100kHz, V_O = $2V_{P-P}$ f_C = 1MHz, V_O = $2V_{P-P}$ f_C = 2.5MHz, V_O = $2V_{P-P}$ f_C = 4MHz, V_O = $2V_{P-P}$			99/109 97/104 83/82 77/71		dBc dBc dBc dBc
	R_L = 100Ω to Half Supply	f_C = 100kHz, V_O = $2V_{P-P}$ f_C = 1MHz, V_O = $2V_{P-P}$ f_C = 2.5MHz, V_O = $2V_{P-P}$ f_C = 4MHz, V_O = $2V_{P-P}$			97/90 95/70 87/65 78/59		dBc dBc dBc dBc
ΔG	Differential Gain (Note 14)	A_V = 2, R_L = 150Ω, V_S = ±2.5V A_V = 1, R_L = 1kΩ, V_S = ±2.5V			0.1 0.02		% %
Δθ	Differential Phase (Note 14)	A_V = 2, R_L = 150Ω, V_S = ±2.5V A_V = 1, R_L = 1kΩ, V_S = ±2.5V			0.25 0.05		Deg Deg
	Crosstalk	A_V = –1, R_L = 1k to Half Supply, V_{OUT} = $2V_{P-P}$, f = 2.5MHz			–96		dB

ELECTRICAL CHARACTERISTICS (V_S = 2.7V)

The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at T_A = 25°C. For each amplifier V_S = 2.7V, 0V; $V_{\overline{SHDN}}$ = 2V; V_{CM} = V_{OUT} = 1.35V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = Half Supply	 ●	0 –300	700	1250 1500	µV µV
		V_{CM} = V^+ – 0.5V, NPN Mode	 ●	–1.6 –2.0	0.9	3.2 3.4	mV mV
ΔV_{OS}	Input Offset Voltage Match (Channel-to-Channel) (Note 8)	V_{CM} = Half Supply	 ●	–350 –750	10	350 750	µV µV
		V_{CM} = V^+ – 0.5V, NPN Mode	 ●	–2.8 –4	0.1	2.8 4	mV mV
V_{OS} T_C	Input Offset Voltage Drift		●		2.75		µV/°C
I_B	Input Bias Current (Note 7)	V_{CM} = Half Supply	 ●	–1000 –1500	–275	600 900	nA nA
		V_{CM} = V^+ – 0.5V, NPN Mode	 ●	0.6 0	1.175	2.5 4.0	µA µA
I_{OS}	Input Offset Current	V_{CM} = Half Supply	 ●	–500 –600	–150	500 600	nA nA
		V_{CM} = V^+ – 0.5V, NPN Mode	 ●	–500 –600	–30	500 600	nA nA
e_n	Input Noise Voltage Density	f = 1MHz			2.9		nV/√Hz
	Input 1/f Noise Voltage	f = 0.1Hz to 10Hz			2		$µV_{P-P}$
i_n	Input Noise Current Density	f = 1MHz			3.6		pA/√Hz
C_{IN}	Input Capacitance	Differential Mode Common Mode			2.5 0.8		pF pF
R_{IN}	Input Resistance	Differential Mode Common Mode			7.2 3		kΩ MΩ
A_{VOL}	Large Signal Voltage Gain	R_L = 1k to Half Supply (Note 12)	 ●	16.5 7	36		V/mV V/mV
		R_L = 100Ω to Half Supply (Note 12)	 ●	2.3 1.8	6.9		V/mV V/mV

ELECTRICAL CHARACTERISTICS (V_S = 2.7V)

The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at T_A = 25°C. For each amplifier V_S = 2.7V, 0V; $V_{\overline{SHDN}}$ = 2V; V_{CM} = V_{OUT} = 1.35V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 1.2V	 ●	80 77	105		dB dB
V_{CMR}	Input Common Mode Range		●	0		V_S	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 5.25V V_{CM} = 1V	 ●	66.5 62	70		dB dB
	Supply Voltage Range (Note 6)		●	2.5		5.25	V
V_{OL}	Output Swing Low (V_{OUT} – $V^–$)	No Load	 ●		22	28 40	mV mV
		I_{SINK} = 5mA	 ●		80	100 140	mV mV
		I_{SINK} = 10mA	 ●		110	150 190	mV mV
V_{OH}	Output Swing High (V^+ – V_{OUT})	No Load	 ●		55	75 95	mV mV
		I_{SOURCE} = 5mA	 ●		125	150 200	mV mV
		I_{SOURCE} = 10mA	 ●		165	200 275	mV mV
I_{SC}	Short-Circuit Current	Sourcing	 ●		–35	–18 –14	mA mA
		Sinking	 ●	20 17	40		mA mA
I_S	Supply Current per Amplifier	V_{CM} = Half Supply	 ●		2.9	3.5 4.5	mA mA
		V_{CM} = V^+ – 0.5V	 ●		3.7	4.6 5.5	mA mA
I_{SD}	Disable Supply Current	$V_{\overline{SHDN}}$ = 0.8V	 ●		24	35 50	μA μA
$I_{\overline{SHDN}L}$	$\overline{SHDN}$ Pin Current Low	$V_{\overline{SHDN}}$ = 0.8V	 ●	–1 –1.5	–0.5	0 0	μA μA
$I_{\overline{SHDN}H}$	$\overline{SHDN}$ Pin Current High	$V_{\overline{SHDN}}$ = 2V	 ●	–300 –600	45	300 600	nA nA
V_L	$\overline{SHDN}$ Pin Input Voltage		●			0.8	V
V_H	$\overline{SHDN}$ Pin Input Voltage		●	2.0			V
I_{OSD}	Output Leakage Current Magnitude in Shutdown	$V_{\overline{SHDN}}$ = 0.8V, Output Shorted to Either Supply			100		nA
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.8V to 2V			5		μs
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 2V to 0.8V			2		μs
BW	–3dB Closed Loop Bandwidth	A_V = 1, R_L = 1k to Half Supply			350		MHz
GBW	Gain-Bandwidth Product	f = 4MHz, R_L = 1k to Half Supply			630		MHz
t_S, 0.1	Settling Time to 0.1%	A_V = +1, V_O = 2V Step R_L = 1k			34		ns
SR	Slew Rate	A_V = –1, 2V Step (Note 11)			170		V/μs
FPBW	Full Power Bandwidth	V_{OUT} = $2V_{P-P}$ (Note 13)			8.5		MHz
	Crosstalk	A_V = –1, R_L = 1k to Half Supply, V_{OUT} = $2V_{P-P}$, f = 2.5MHz			96		dB

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by back-to-back diodes. If any of the input or shutdown pins goes 300mV beyond either supply or the differential input voltage exceeds 1.4V the input current should be limited to less than 10mA. This parameter is guaranteed to meet specified performance through design and/or characterization. It is not production tested.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output current is high. This parameter is guaranteed to meet specified performance through design and/or characterization. It is not production tested.

Note 4: The LTC6252C/LTC6253C/LTC6254C and LTC6252I/LTC6253I/LTC6254I are guaranteed functional over the temperature range of –40°C to 85°C. The LTC6252H/LTC6253H/LTC6254H are guaranteed functional over the temperature range of –40°C to 125°C.

Note 5: The LTC6252C/LTC6253C/LTC6254C are guaranteed to meet specified performance from 0°C to 70°C. The LTC6252C/LTC6253C/LTC6254C are designed, characterized and expected to meet specified performance from –40°C to 85°C but are not tested or QA sampled at these temperatures. The LTC6252I/LTC6253I/LTC6254I are guaranteed to meet specified performance from –40°C to 85°C. The LTC6252H/LTC6253H/LTC6254H are guaranteed to meet specified performance from –40°C to 125°C.

Note 6: Supply voltage range is guaranteed by power supply rejection ratio test.

Note 7: The input bias current is the average of the average of the currents at the positive and negative input pins.

Note 8: Matching parameters are the difference between amplifiers A and D and between B and C on the LTC6254; between the two amplifiers on the LTC6253.

Note 9: Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are with short traces connected to the leads with minimal metal area.

Note 10: The output voltage is varied from 0.5V to 4.5V during measurement.

Note 11: Middle 2/3 of the output waveform is observed. R_L = 1k to half supply.

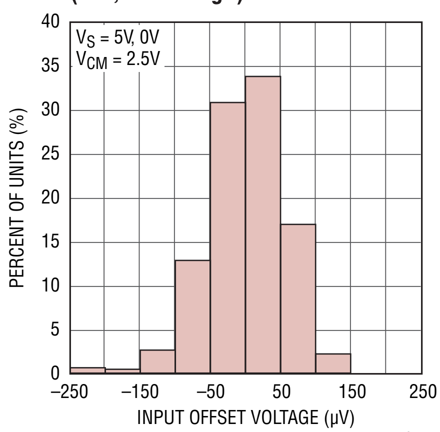
Note 12: The output voltage is varied from 0.5V to 2.2V during measurement.

Note 13: FPBW is determined from distortion performance in a gain of +2 configuration with HD2, HD3 < –40dBc as the criteria for a valid output.

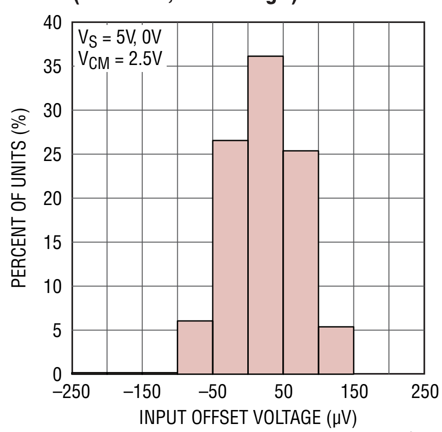
Note 14: Differential gain and phase are measured using a Tektronix TSG120YC/NTSC signal generator and a Tektronix 1780R video measurement set.

TYPICAL PERFORMANCE CHARACTERISTICS

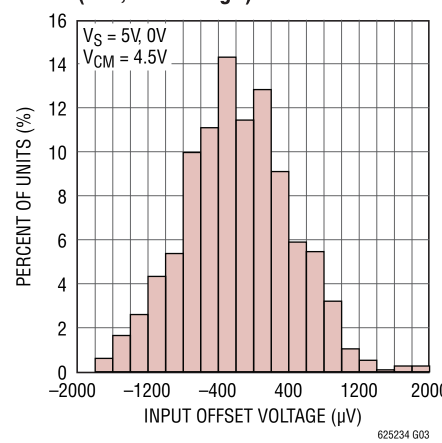
V_{OS} Distribution, V_{CM} = V_S/2 (MS, PNP Stage)



V_{OS} Distribution, V_{CM} = V_S/2 (TSOT-23, PNP Stage)

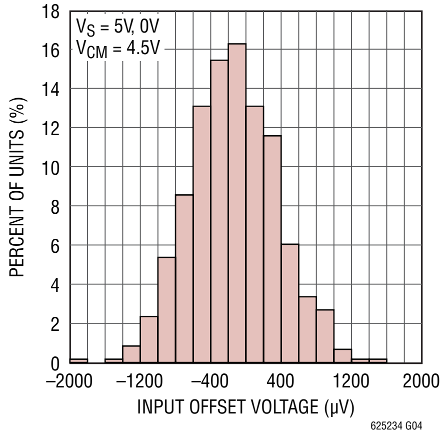


V_{OS} Distribution, V_{CM} = V^+ – 0.5V (MS, NPN Stage)

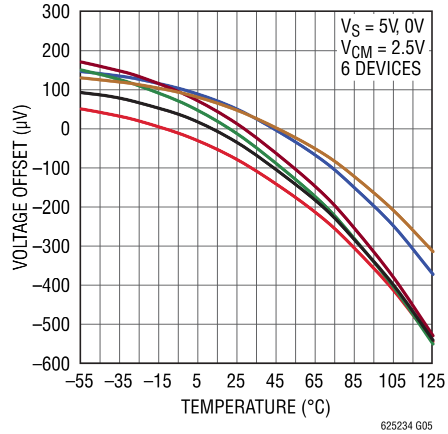


TYPICAL PERFORMANCE CHARACTERISTICS

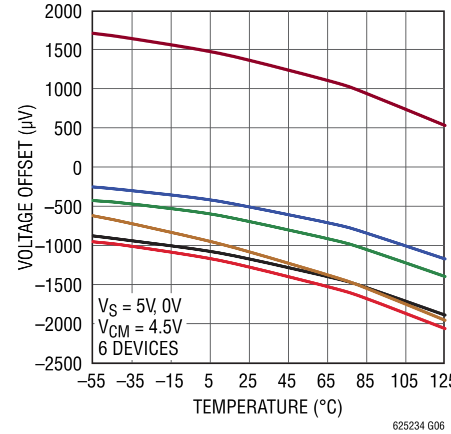
V_{OS} Distribution, $V_{CM} = V^+ – 0.5V$ (TSOT-23, NPN Stage)



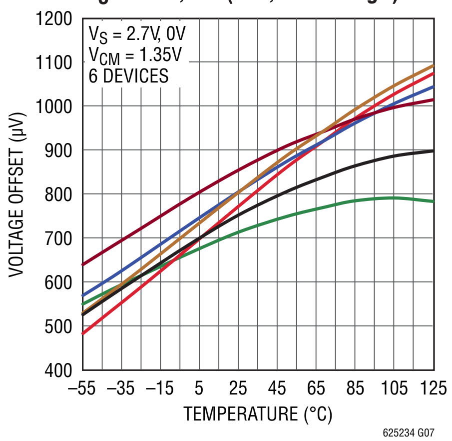
V_{OS} vs Temperature, V_S = 5V, 0V (MS, PNP Stage)



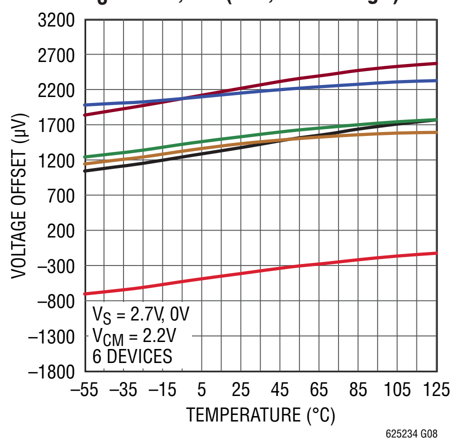
V_{OS} vs Temperature, V_S = 5V, 0V (MS, NPN Stage)



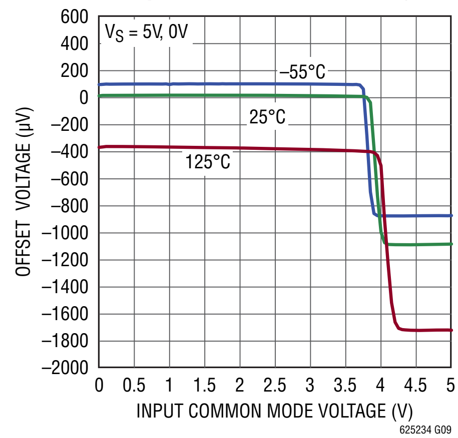
V_{OS} vs Temperature, V_S = 2.7V, 0V (MS, PNP Stage)



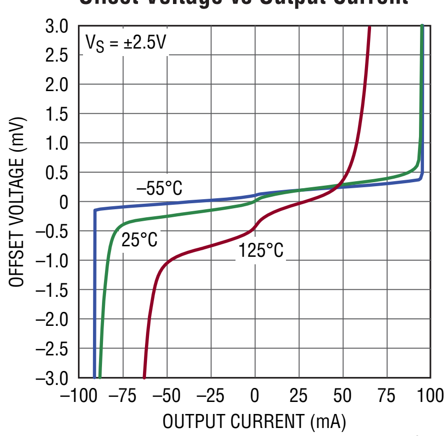
V_{OS} vs Temperature, V_S = 2.7V, 0V (MS, NPN Stage)



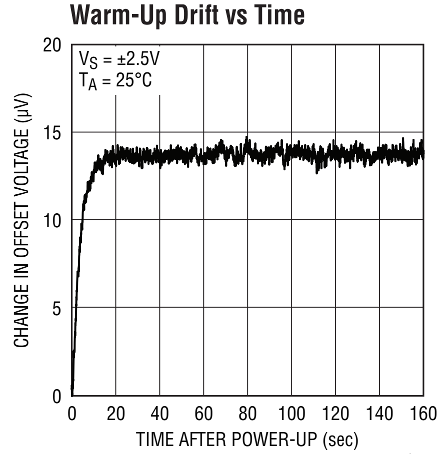
Offset Voltage vs Input Common Mode Voltage



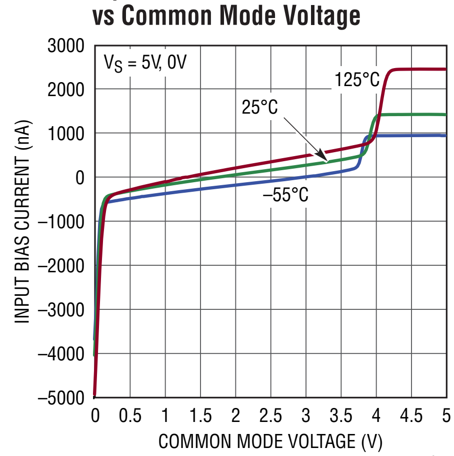
Offset Voltage vs Output Current



Warm-Up Drift vs Time

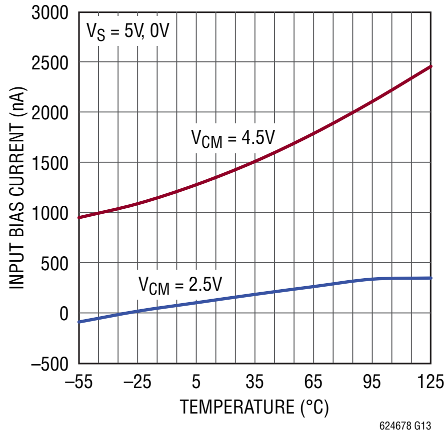


Input Bias Current vs Common Mode Voltage

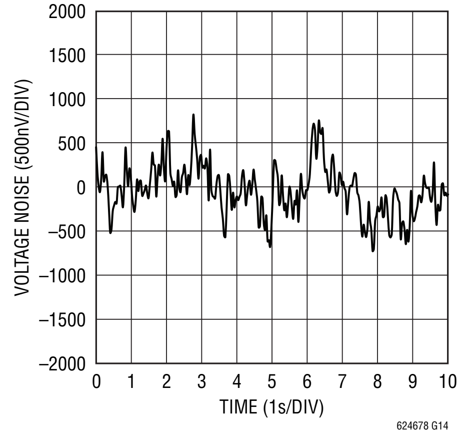


TYPICAL PERFORMANCE CHARACTERISTICS

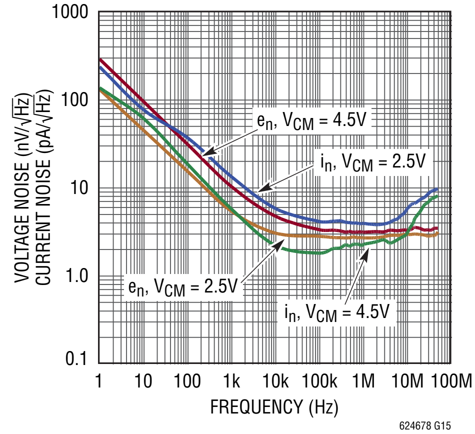
Input Bias Current vs Temperature



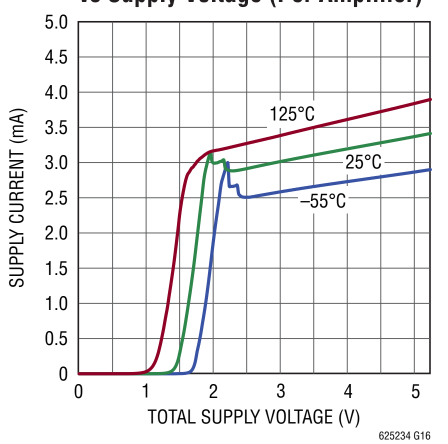
0.1Hz to 10Hz Voltage Noise



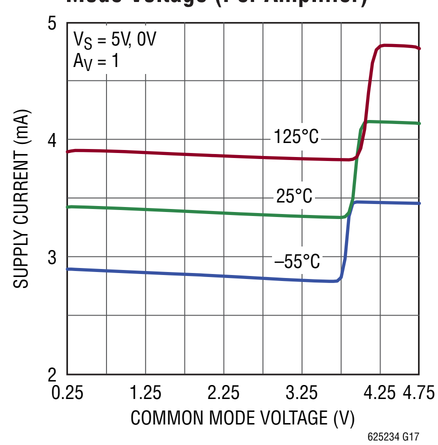
Input Noise Voltage and Noise Current vs Frequency



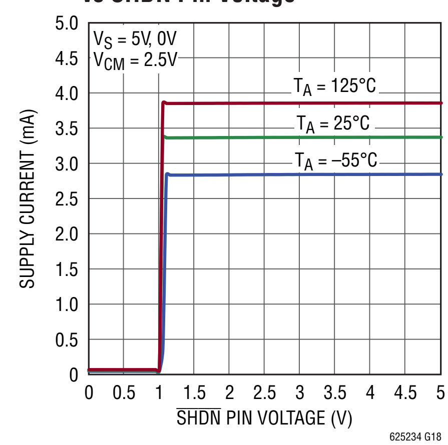
Supply Current vs Supply Voltage (Per Amplifier)



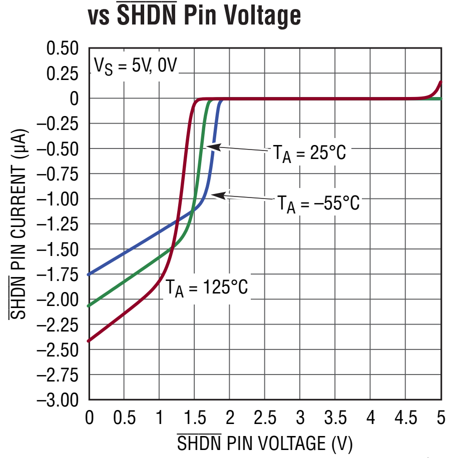
Supply Current vs Input Common Mode Voltage (Per Amplifier)



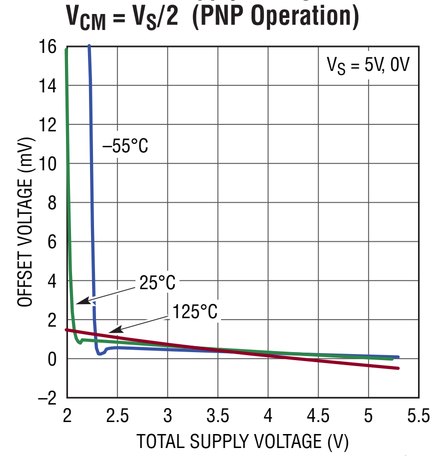
Supply Current Per Amplifier vs SHDN Pin Voltage



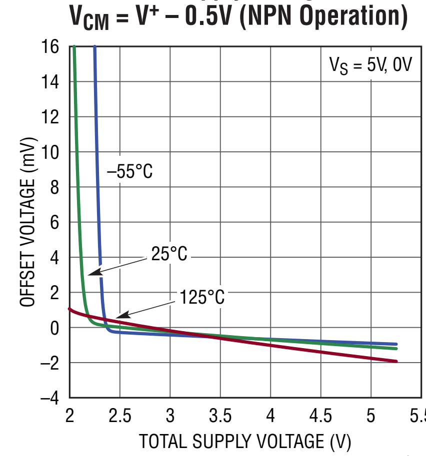
SHDN Pin Current vs SHDN Pin Voltage



Minimum Supply Voltage, $V_{CM} = V_S/2$ (PNP Operation)

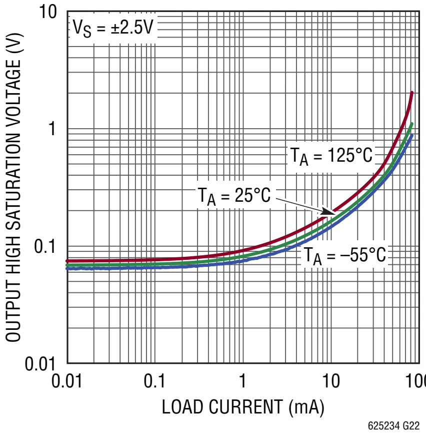


Minimum Supply Voltage, $V_{CM} = V^+ – 0.5V$ (NPN Operation)

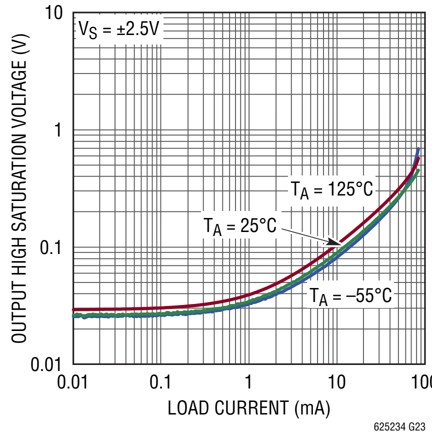


TYPICAL PERFORMANCE CHARACTERISTICS

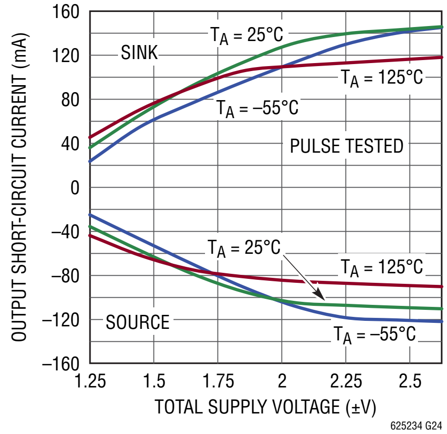
Output Saturation Voltage vs Load Current (Output High)



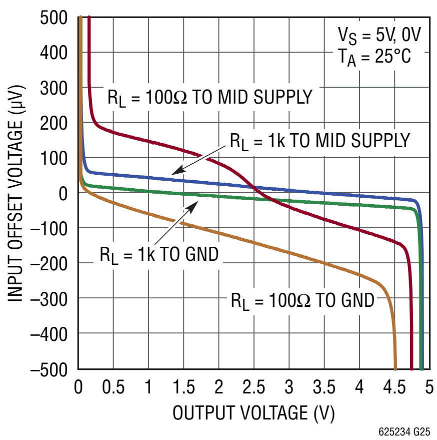
Output Saturation Voltage vs Load Current (Output Low)



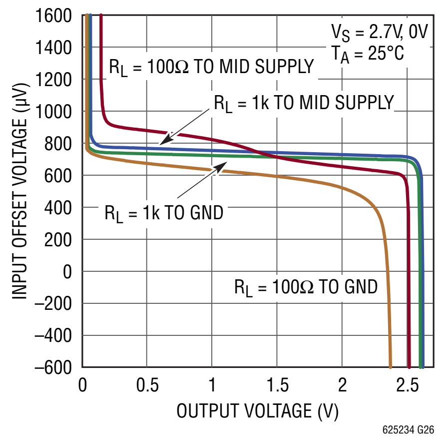
Output Short-Circuit Current vs Supply Voltage



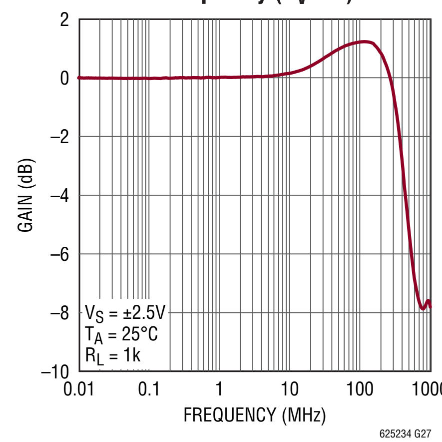
Open Loop Gain



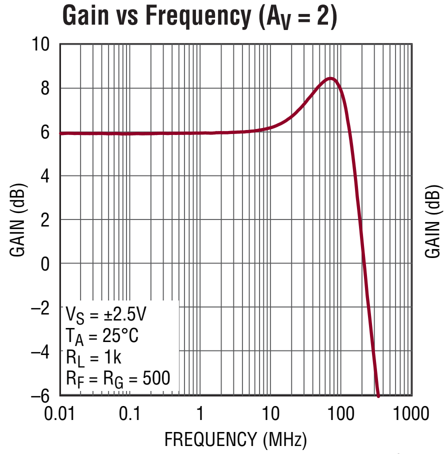
Open Loop Gain



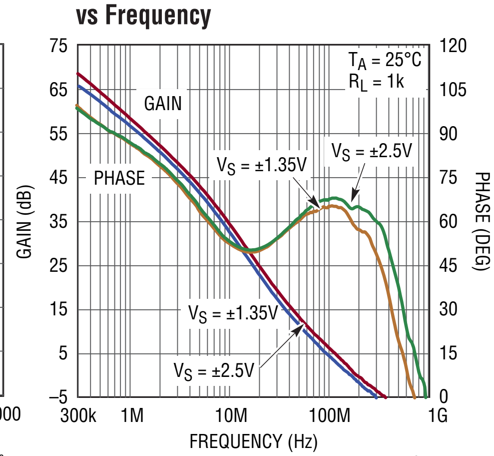
Gain vs Frequency (A_V = 1)



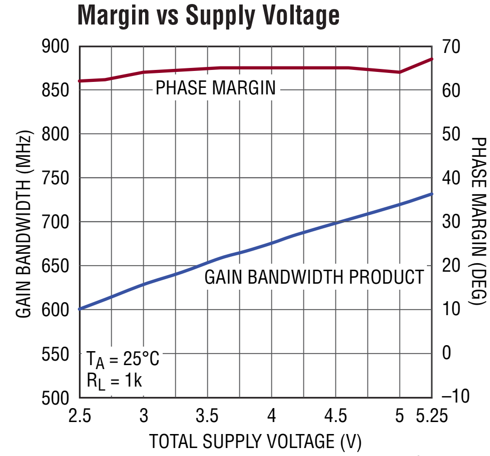
Gain vs Frequency (A_V = 2)



Open Loop Gain and Phase vs Frequency

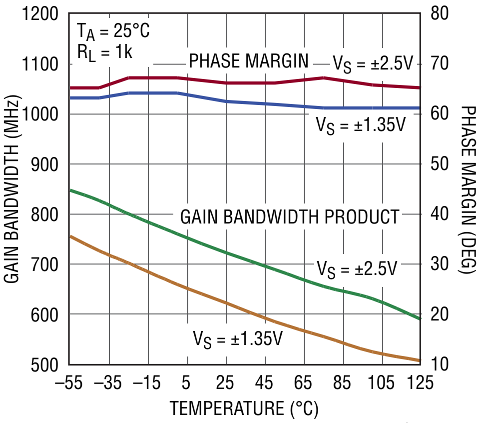


Gain Bandwidth and Phase Margin vs Supply Voltage



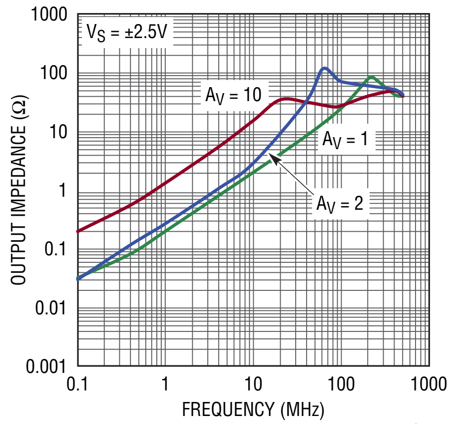
TYPICAL PERFORMANCE CHARACTERISTICS

Gain Bandwidth and Phase Margin vs Temperature



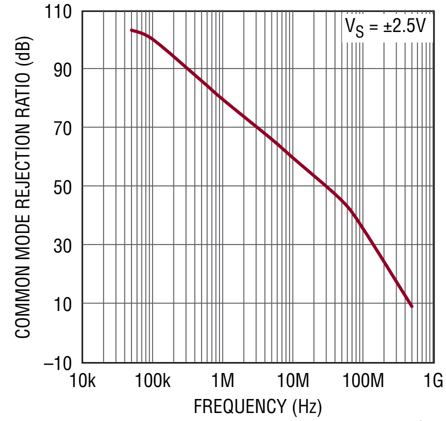
625234 G31

Output Impedance vs Frequency



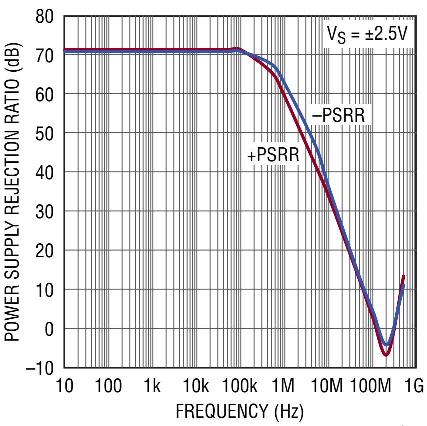
625234 G32

Common Mode Rejection Ratio vs Frequency



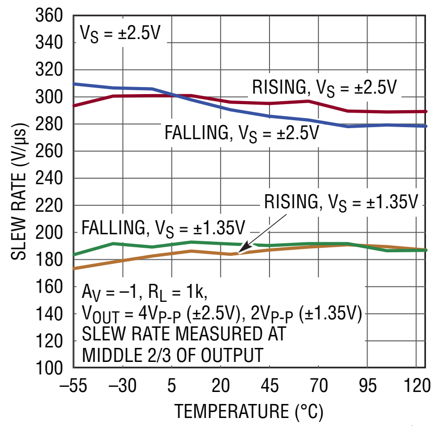
625234 G33

Power Supply Rejection Ratio vs Frequency



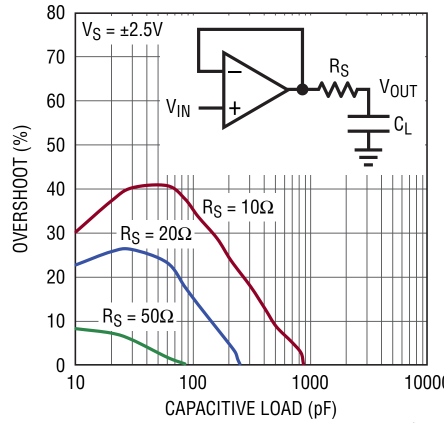
625234 G34

Slew Rate vs Temperature



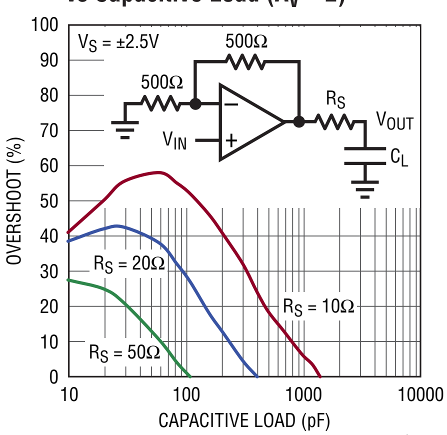
625234 G35

Series Output Resistor vs Capacitive Load ($A_V = 1$)



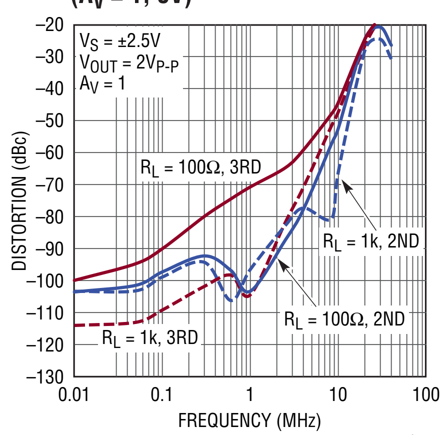
625234 G36

Series Output Resistor vs Capacitive Load ($A_V = 2$)



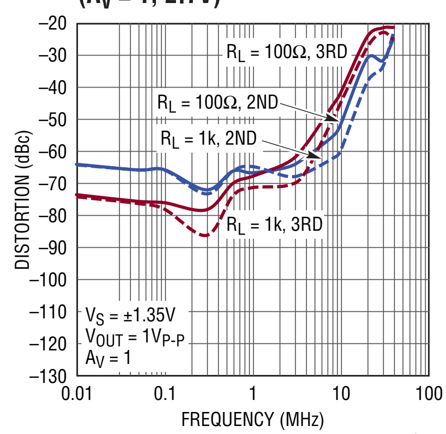
625234 G37

Distortion vs Frequency ($A_V = 1$, 5V)



625234 G38

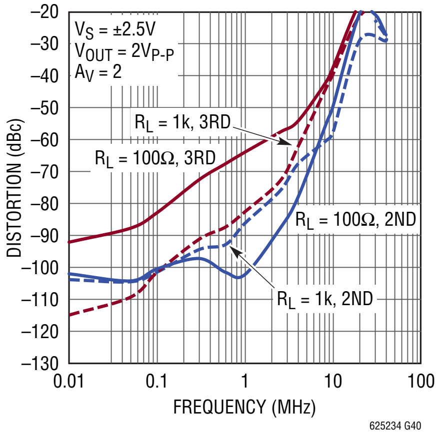
Distortion vs Frequency ($A_V = 1$, 2.7V)



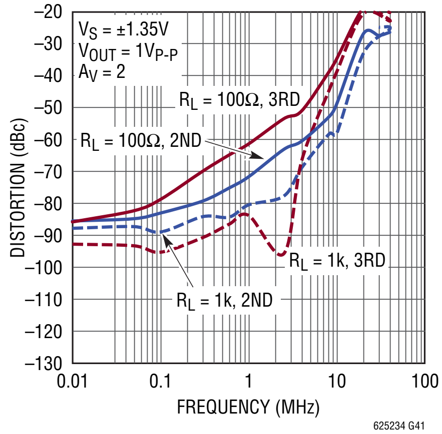
625234 G39

TYPICAL PERFORMANCE CHARACTERISTICS

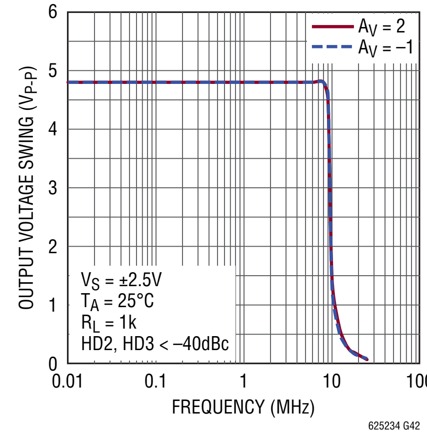
Distortion vs Frequency (A_V = 2, 5V)



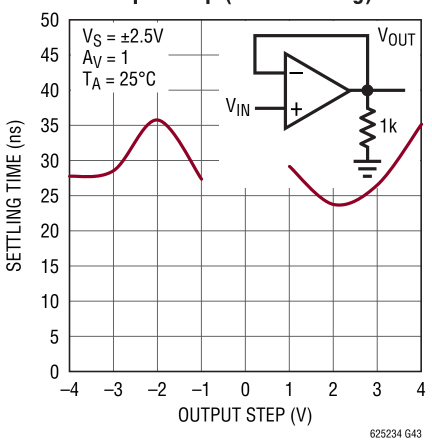
Distortion vs Frequency A_V = 2, 2.7V)



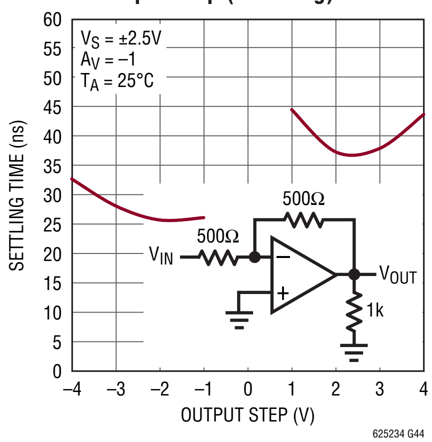
Maximum Undistorted Output Signal vs Frequency



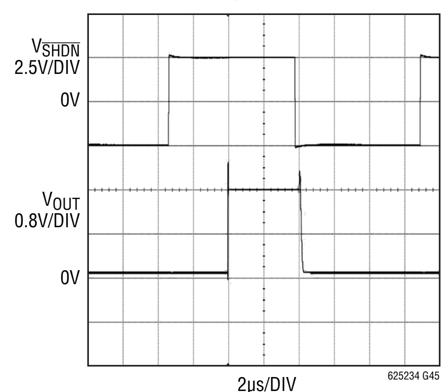
0.1% Settling Time vs Output Step (Noninverting)



0.1% Settling Time vs Output Step (Inverting)

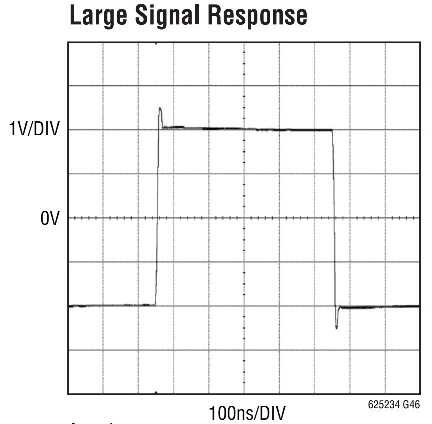


$\overline{SHDN}$ Pin Response Time



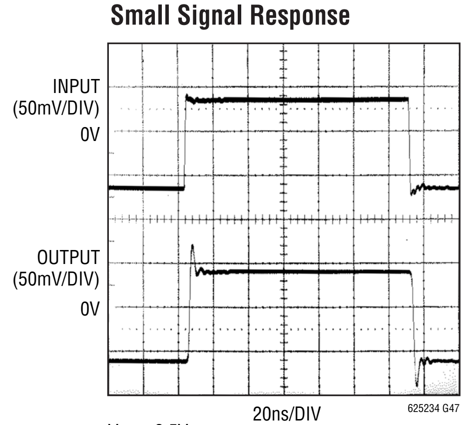
A_V = 1
V_S = ±2.5V
R_L = 1k
V_{IN} = 1.6V

Large Signal Response



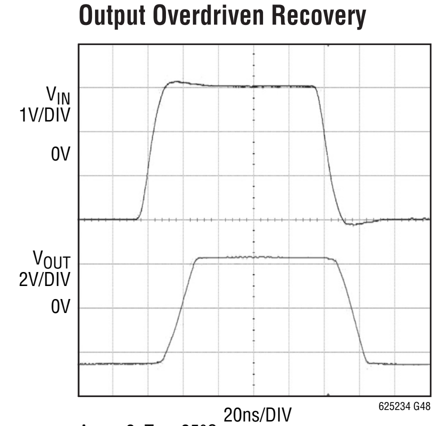
A_V = 1
V_S = ±2.5V
T_A = 25°C
R_L = 1k

Small Signal Response



V_S = ±2.5V
R_L = 1k

Output Overdriven Recovery



A_V = ±2, T_A = 25°C
V_S = ±2.5V, V_{IN} = $3V_{P-P}$
R_L = 1k, R_F = R_G = 500Ω

PIN FUNCTIONS

–IN: Inverting Input of Amplifier. Input range from V^- to V^+.

+IN: Non-Inverting Input of Amplifier. Input range from V^- to V^+.

V^+ : Positive Supply Voltage. Total supply voltage ranges from 2.5V to 5.25V.

V^- : Negative Supply Voltage. Typically 0V. This can be made a negative voltage as long as 2.5V ≤ (V^+ – V^-) ≤ 5.25V.

$\overline{\text{SHDN}}$: Active Low Shutdown. Threshold is typically 1.1V referenced to V^-. Floating this pin will turn the part on.

OUT: Amplifier Output. Swings rail-to-rail and can typically source/sink over 90mA of current at a total supply of 5V.

APPLICATIONS INFORMATION

Circuit Description

The LTC6252/LTC6253/LTC6254 have an input and output signal range that extends from the negative power supply to the positive power supply. Figure 1 depicts a simplified schematic of the amplifier. The input stage is comprised of two differential amplifiers, a PNP stage, Q1/Q2, and an NPN stage, Q3/Q4 that are active over different common mode input voltages. The PNP stage is active between the negative supply to nominally 1.2V below the positive supply. As the input voltage approaches the positive supply, the transistor Q5 will steer the tail current, I_1, to the current mirror, Q6/Q7, activating the NPN differential pair and the PNP pair becomes inactive for the remaining input common mode range. Also, at the input stage, devices Q17 to Q19 act to cancel the bias current of the PNP input pair. When Q1/Q2 are active, the current in Q16 is controlled to be the same as the current in Q1 and Q2. Thus, the base current of Q16 is nominally equal to the base current of the input devices. The base current of Q16 is then mirrored by devices Q17 to Q19 to cancel the base current of the input devices Q1/Q2. A pair of complementary common emitter stages, Q14/Q15, enable the output to swing from rail-to-rail.

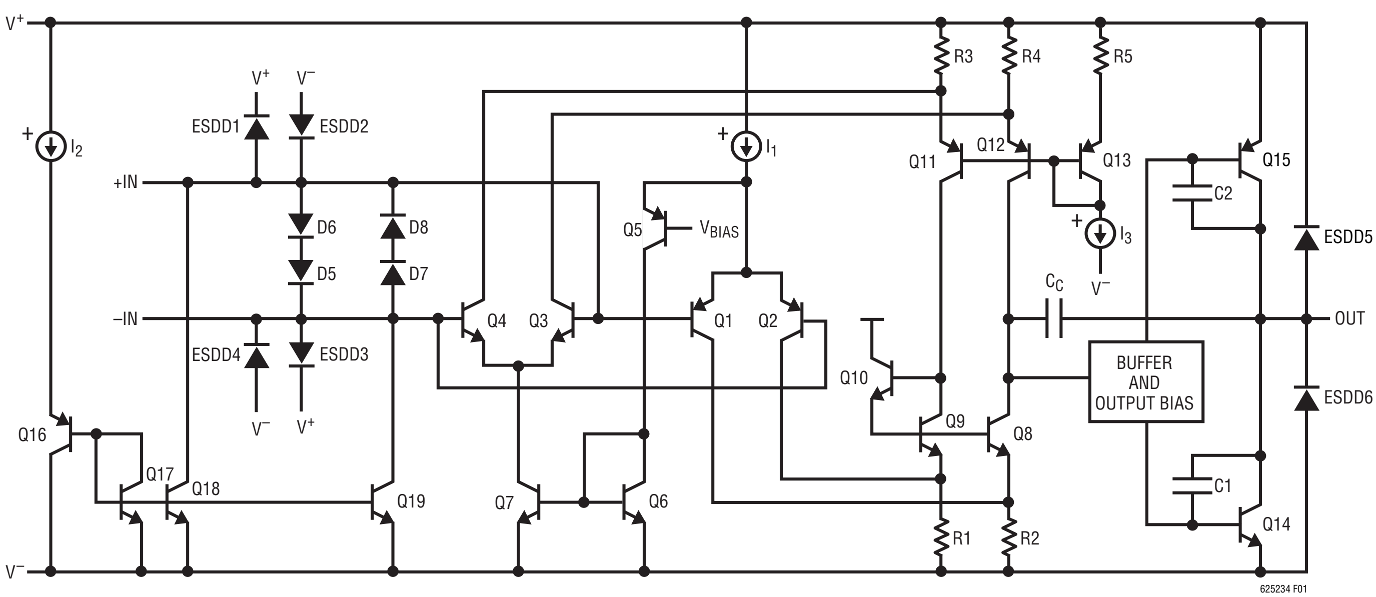


Figure 1. LTC6252/LTC6253/LTC6254 Simplified Schematic Diagram

APPLICATIONS INFORMATION

Input Offset Voltage

The offset voltage will change depending upon which input stage is active. The PNP input stage is active from the negative supply rail to approximately 1.2V below the positive supply rail, then the NPN input stage is activated for the remaining input range up to the positive supply rail with the PNP stage inactive. The offset voltage magnitude for the PNP input stage is trimmed to less than 350μV with 5V total supply at room temperature, and is typically less than 150μV. The offset voltage for the NPN input stage is less than 2.2mV with 5V total supply at room temperature.

Input Bias Current

The LTC6252 family uses a bias current cancellation circuit to compensate for the base current of the PNP input pair. This results in a typical I_B of about 100nA. When the input common mode voltage is less than 200mV, the bias cancellation circuit is no longer effective and the input bias current magnitude can reach a value above 4μA. For common mode voltages ranging from 0.2V above the negative supply to 1.2V below the positive supply, the low input bias current allows the amplifiers to be used in applications with high source resistances where errors due to voltage drops must be minimized.

Output

The LTC6252 family has excellent output drive capability. The amplifiers can typically deliver 90mA of output drive current at a total supply of 5V. The maximum output current is a function of the total supply voltage. As the supply voltage to the amplifier decreases, the output current capability also decreases. Attention must be paid to keep the junction temperature of the IC below 150°C (refer to the Power Dissipation Section) when the output is in continuous short-circuit. The output of the amplifier has reverse-biased diodes connected to each supply. If the output is forced beyond either supply, extremely high current will flow through these diodes which can result in damage to the device. Forcing the output to even 1V beyond either supply could result in several hundred milliamps of current through either diode.

Input Protection

The LTC6252/LTC6253/LTC6254 input stages are protected against a large differential input voltage of 1.4V or higher by 2 pairs of back-to-back diodes to prevent the emitter-base breakdown of the input transistors. In addition, the input and shutdown pins have reverse biased diodes connected to the supplies. The current in these diodes must be limited to less than 10mA. The amplifiers should not be used as comparators or in other open loop applications.

ESD

The LTC6252 family has reverse-biased ESD protection diodes on all inputs and outputs as shown in Figure 1.

There is an additional clamp between the positive and negative supplies that further protects the device during ESD strikes. Hot plugging of the device into a powered socket must be avoided since this can trigger the clamp resulting in larger currents flowing between the supply pins.

Capacitive Loads

The LTC6252/LTC6253/LTC6254 are optimized for high bandwidth and low power applications. Consequently they have not been designed to directly drive large capacitive loads. Increased capacitance at the output creates an additional pole in the open loop frequency response, worsening the phase margin. When driving capacitive loads, a resistor of 10Ω to 100Ω should be connected between the amplifier output and the capacitive load to avoid ringing or oscillation. The feedback should be taken directly from the amplifier output. Higher voltage gain configurations tend to have better capacitive drive capability than lower gain configurations due to lower closed loop bandwidth and hence higher phase margin. The graphs titled Series Output Resistor vs Capacitive Load demonstrate the transient response of the amplifier when driving capacitive loads with various series resistors.

APPLICATIONS INFORMATION

Feedback Components

When feedback resistors are used to set up gain, care must be taken to ensure that the pole formed by the feedback resistors and the parasitic capacitance at the inverting input does not degrade stability. For example if the amplifier is set up in a gain of +2 configuration with gain and feedback resistors of 5k, a parasitic capacitance of 5pF (device + PC board) at the amplifier's inverting input will cause the part to oscillate, due to a pole formed at 12.7MHz. An additional capacitor of 5pF across the feedback resistor as shown in Figure 2 will eliminate any ringing or oscillation. In general, if the resistive feedback network results in a pole whose frequency lies within the closed loop bandwidth of the amplifier, a capacitor can be added in parallel with the feedback resistor to introduce a zero whose frequency is close to the frequency of the pole, improving stability.

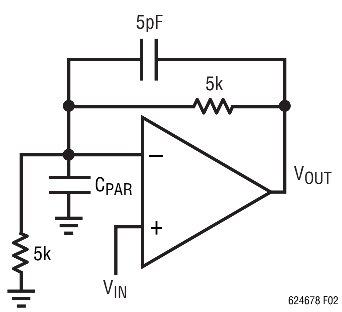


Figure 2. 5pF Feedback Cancels Parasitic Pole

Shutdown

The LTC6252 and LTC6253MS have $\overline{SHDN}$ pins that can shut down the amplifier to 42μA typical supply current. The $\overline{SHDN}$ pin needs to be taken within 0.8V of the negative supply for the amplifier to shut down. When left floating, the $\overline{SHDN}$ pin is internally pulled up to the positive supply and the amplifier remains on.

Power Dissipation

The LTC6252 and LTC6253 contain one and two amplifiers respectively. Hence the maximum on-chip power dissipation for them will be less than the maximum on-chip power dissipation for the LTC6254, which contains four amplifiers.

The LTC6254 is housed in a small 16-lead MS package and typically has a thermal resistance (θ_{JA}) of 125°C/ W. It is necessary to ensure that the die's junction temperature does not exceed 150°C. The junction temperature, T_J, is calculated from the ambient temperature, T_A, power dissipation, PD, and thermal resistance, θ_{JA}:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

The power dissipation in the IC is a function of the supply voltage, output voltage and load resistance. For a given supply voltage with output connected to ground or supply, the worst-case power dissipation $P_{D(MAX)}$ occurs when the supply current is maximum and the output voltage at half of either supply voltage for a given load resistance. $P_{D(MAX)}$ is approximately (since I_S actually changes with output load current) given by:

$$P_{D(MAX)} = (V_S \bullet I_{S(MAX)}) + \left(\frac{V_S}{2}\right)^2 / R_L$$

Example: For an LTC6254 in a 16-lead MS package operating on ±2.5V supplies and driving a 100Ω load to ground, the worst-case power dissipation is approximately given by

$$P_{D(MAX)}/\text{Amp} = (5 \bullet 4.8\text{mA}) + (1.25)^2/100 = 39.6\text{mW}$$

If all four amplifiers are loaded simultaneously then the total power dissipation is 158mW.

At the Absolute Maximum ambient operating temperature, the junction temperature under these conditions will be:

$$T_J = T_A + P_D \bullet 125°\text{C/W}$$

$$= 125 + (0.158\text{W} \bullet 125°\text{C/W}) = 145°\text{C}$$

which is less than the absolute maximum junction temperature for the LTC6254 (150°C).

Refer to the Pin Configuration section for thermal resistances of various packages.

TYPICAL APPLICATIONS

5V Single-Supply 16-Bit ADC Driver

Figure 3 shows the LTC6253 driving an LTC2393-16 16-bit A/D converter on a single 5V supply. The low wideband noise of the LTC6253 helps to achieve better than 93dB SNR. A gain of 1.17V/V is taken in the first amplifier, giving an input voltage range of $3.5V_{P-P}$ for a full-scale input to the ADC. By taking a small amount of gain, a –1dBFS output can be easily obtained without the amplifier transitioning between input regions, thus minimizing crossover distortion. Furthermore, by driving VCM with 2.08V from the ADC's VCM pin, the LTC6253 is capable of driving the LTC2393-16 to within 0.1dB of full scale. Figure 4 shows an FFT obtained with a sampling rate of 1Msps and a 20kHz input waveform. Spurious free dynamic range is an excellent 104.7dB.

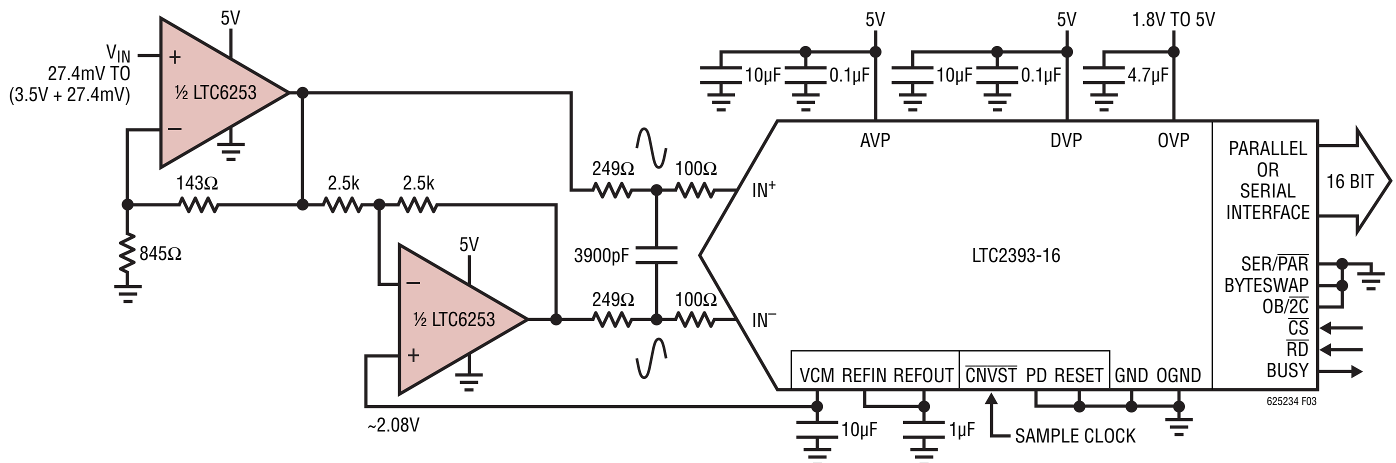


Figure 3. 5V Single Supply 16-Bit ADC Driver

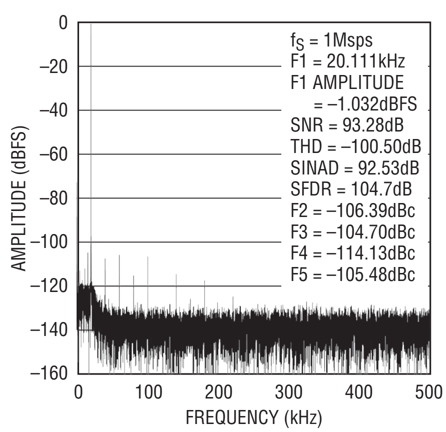


Figure 4. LTC6253 Driving LTC2393-16 16b ADC 5V Single-Supply Performance

TYPICAL APPLICATIONS

Low Noise Gain Block Using Channels in Parallel

Figure 5 shows the LTC6254 configured as a low noise gain block. By configuring each channel as a gain of 10 block and putting all four gain blocks in parallel, the input referred noise can be reduced significantly. 22Ω resistors are hooked up to the outputs of each of the channels to ensure even distribution of load currents.For a total supply current of 13.2mA, measured input referred noise density (including contributions from the resistors) between 100kHz and 10MHz was less than $1.6nV/\sqrt{Hz}$, with input referred noise density at 1 MHz being $1.5nV/\sqrt{Hz}$. The measured –3dB frequency was 37MHz for a load resistance of 1k.

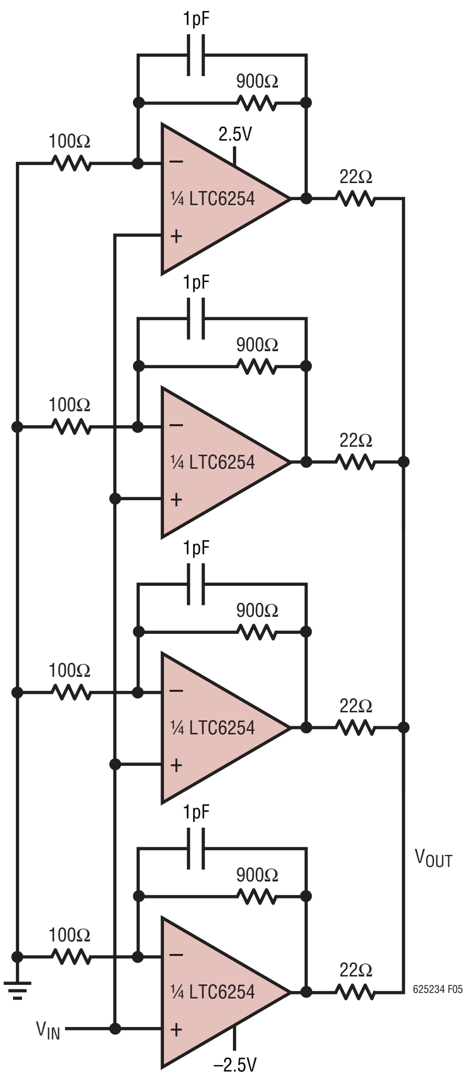


Figure 5. Low Noise Gain Block Using Parallel Channels

Multiplexing Channels

The LTC6252 and LTC6253 are available with shutdown pins in the SOT-23 and MS10 packages. While this allows for reduced power consumption, it also makes the parts suitable for high output impedance applications such as muxing. During shutdown, the bases of the amplifier's output channels are hard tied to their emitters in order to minimize leakage. Figure 6 shows the LTC6253 applied as a mux, with the outputs simply shorted together. Depending on which device is powered, either the V_A or the V_B input is buffered to V_{OUT}. The MOSFET Q1 provides a simple logic inversion, so that pulling the gate high selects the B path while the FET drain goes low shutting down the A path. R3 is provided to speed up the drain rise time. The LTC6253 turn-on time is longer than the turn-off time (3.5µs vs < 2µs) avoiding cross conduction in the output

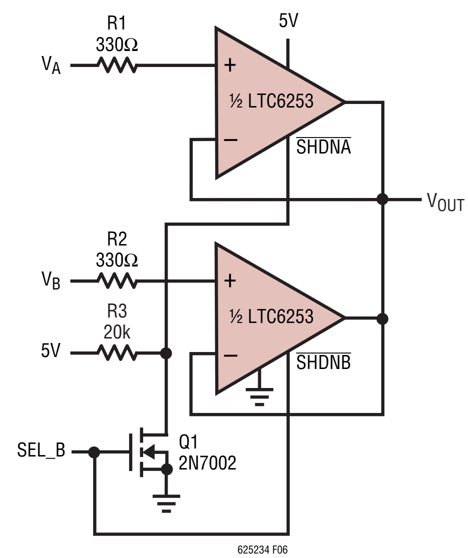


Figure 6. Multiplexing Channels

TYPICAL APPLICATIONS

stages. See the oscillograph of Figure 7, showing the inputs V_A and V_B, the SEL_B control, and the resulting output.

Note that there are protection diodes across the op amp inputs, so large signals at the output will feed back into the upstream off channel through the diodes. R1 and R2 were put in place to reduce the loading on the output, as well as to reduce the upstream feedback current and improve reverse isolation. Some reverse crosstalk can be discerned in the V_A and V_B traces during their respective off times, however, as the reverse current works back into the 50Ω source impedance of the function generators.

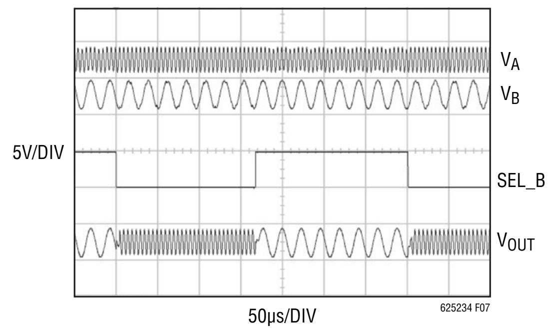


Figure 7. Oscilloscope Traces Showing Multiplexing Channels

High Speed Low Voltage Instrumentation Amplifier

Figure 8 shows a three op amp instrumentation amplifier with a gain of 41V/V which can operate on low supplies. Op amps U1 and U2 are channels from an LTC6253. Op amp U3 can be an LTC6252 or one channel of an LTC6253. Figure 9 shows the measured frequency response of the instrumentation amplifier for a load of 1kΩ. Figure 10 shows the measured CMRR of the instrumentation amplifier, and Figure 11 shows the transient response for a 50mV$_{P-P}$ input square wave applied to the positive input, with the negative input grounded.

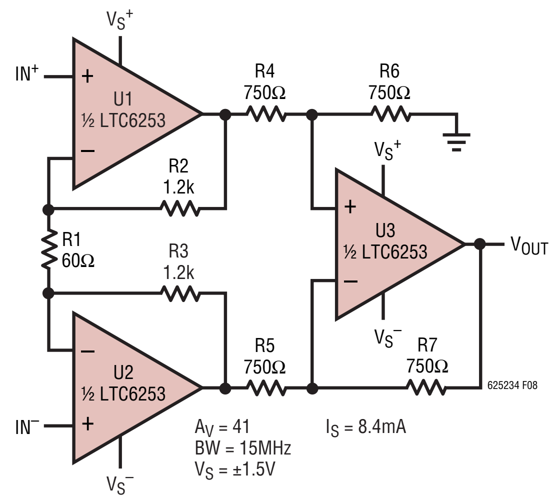


Figure 8. High Speed Low Voltage Instrumentation Amplifier

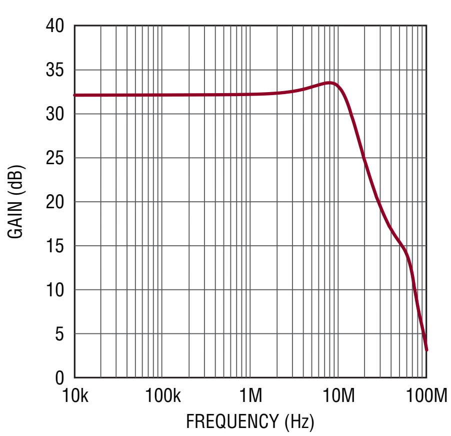


Figure 9. Instrumentation Amplifier Frequency Response

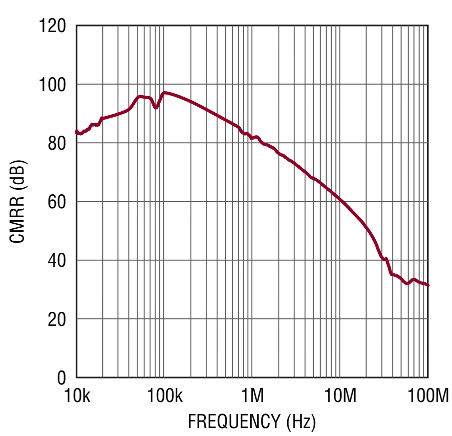


Figure 10. Instrumentation Amplifier CMRR

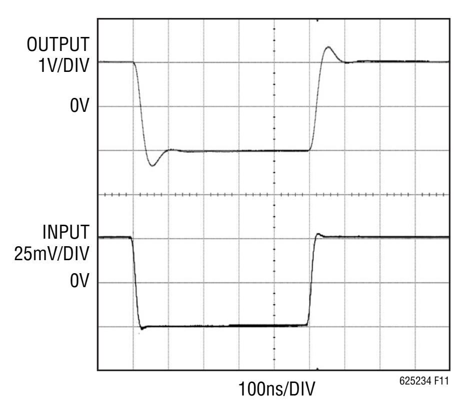
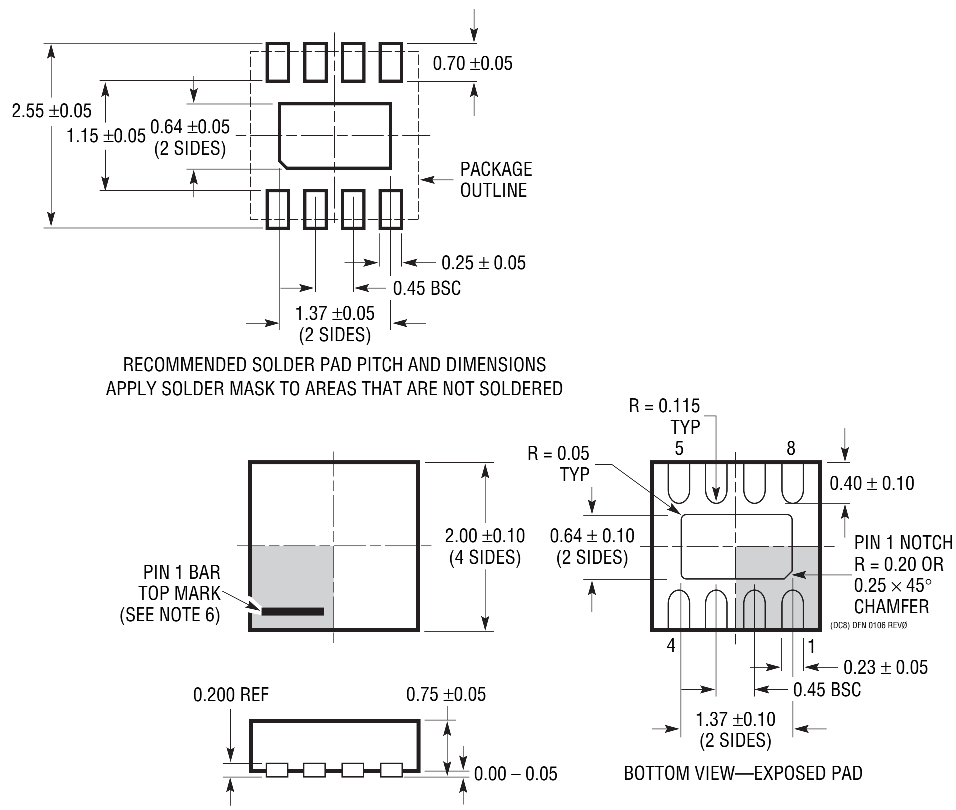


Figure 11. Transient Response, Instrumentation Amplifier

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DC8 Package
8-Lead Plastic DFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1719 Rev A)

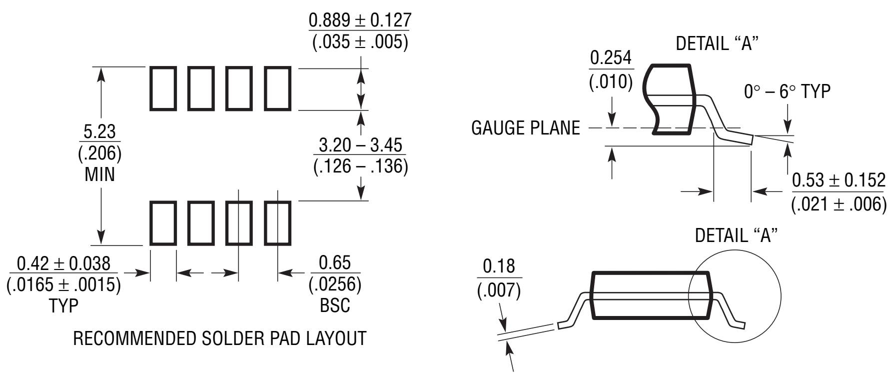


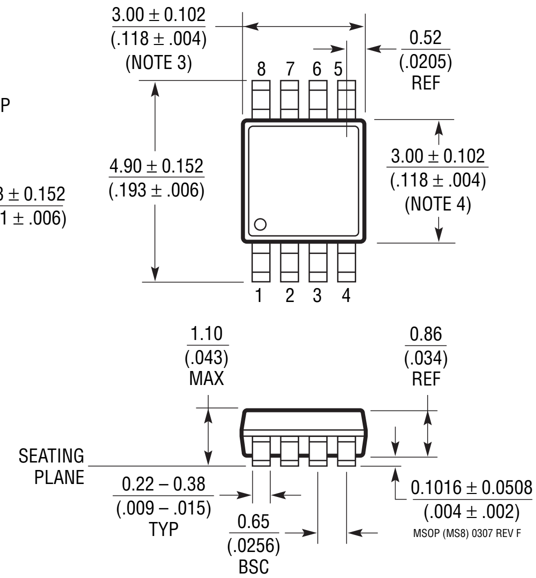
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)



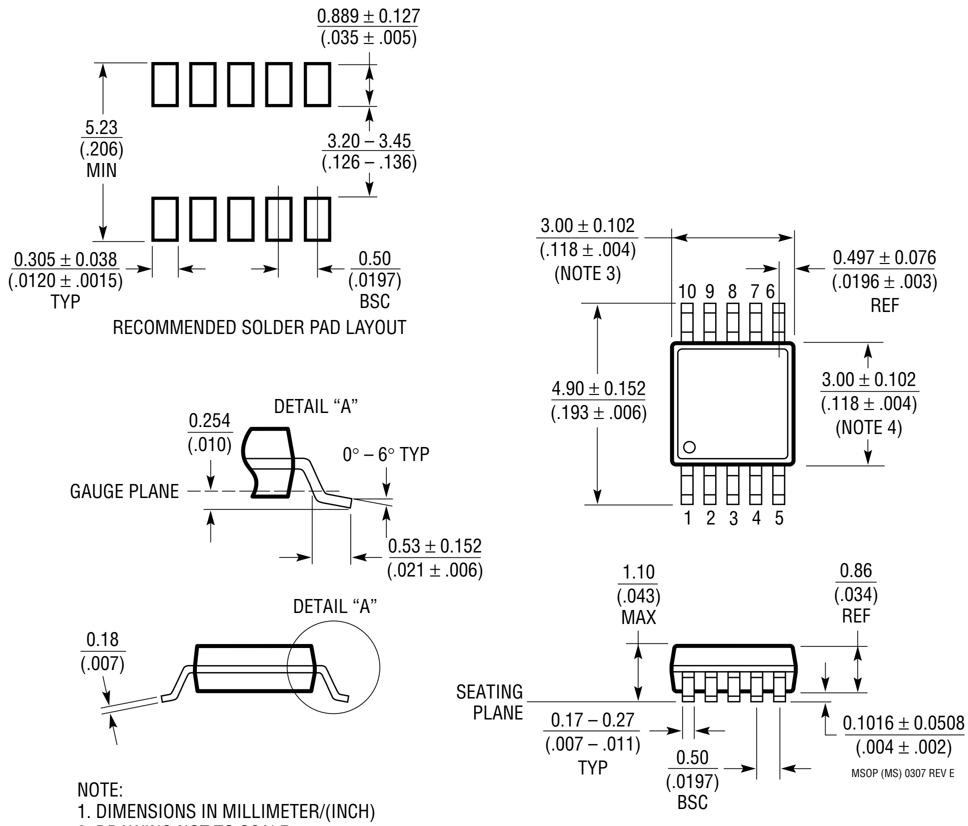


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev E)

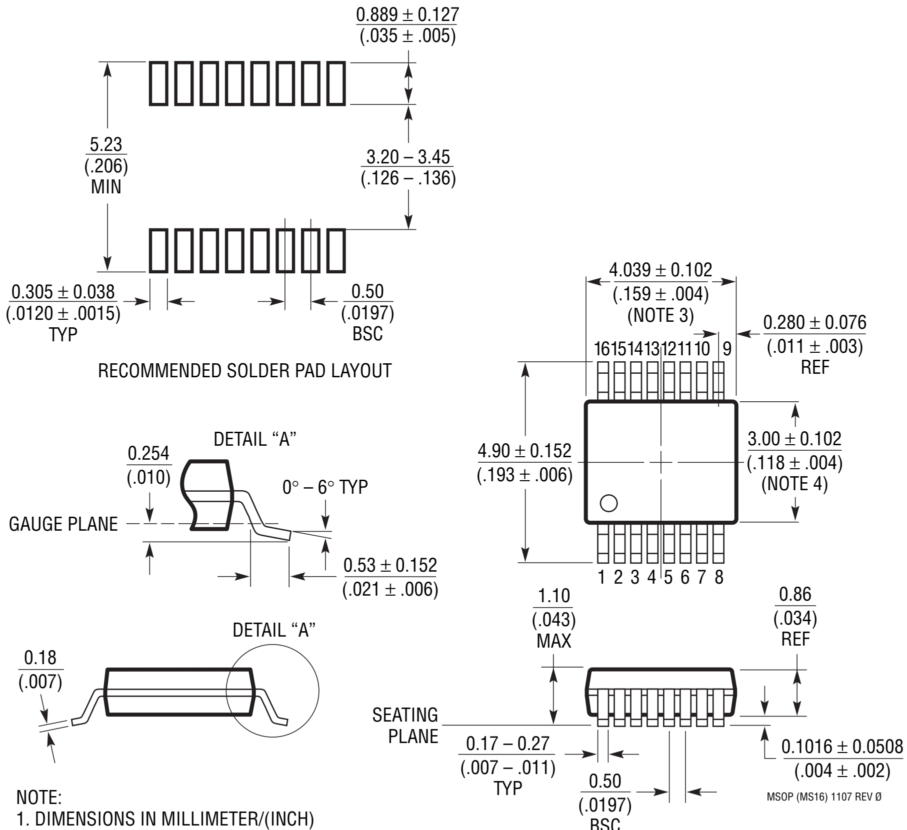


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS Package
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev Ø)

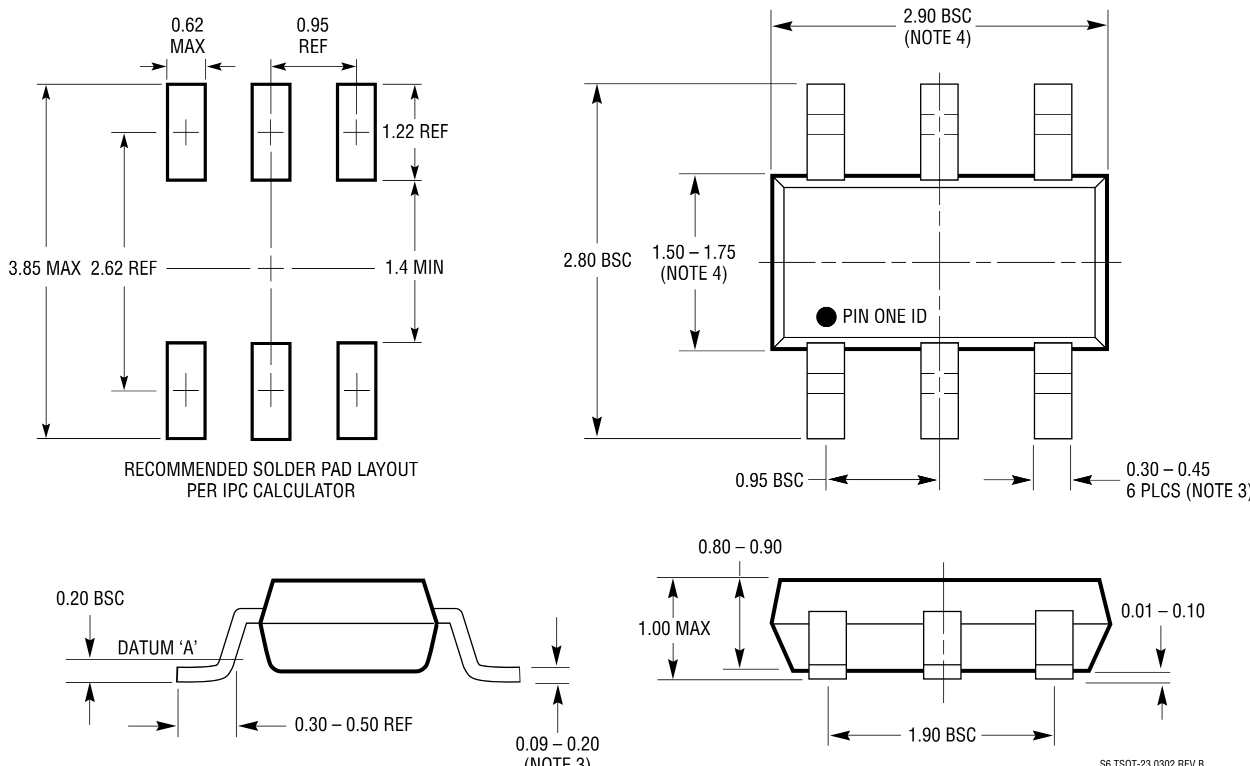


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)

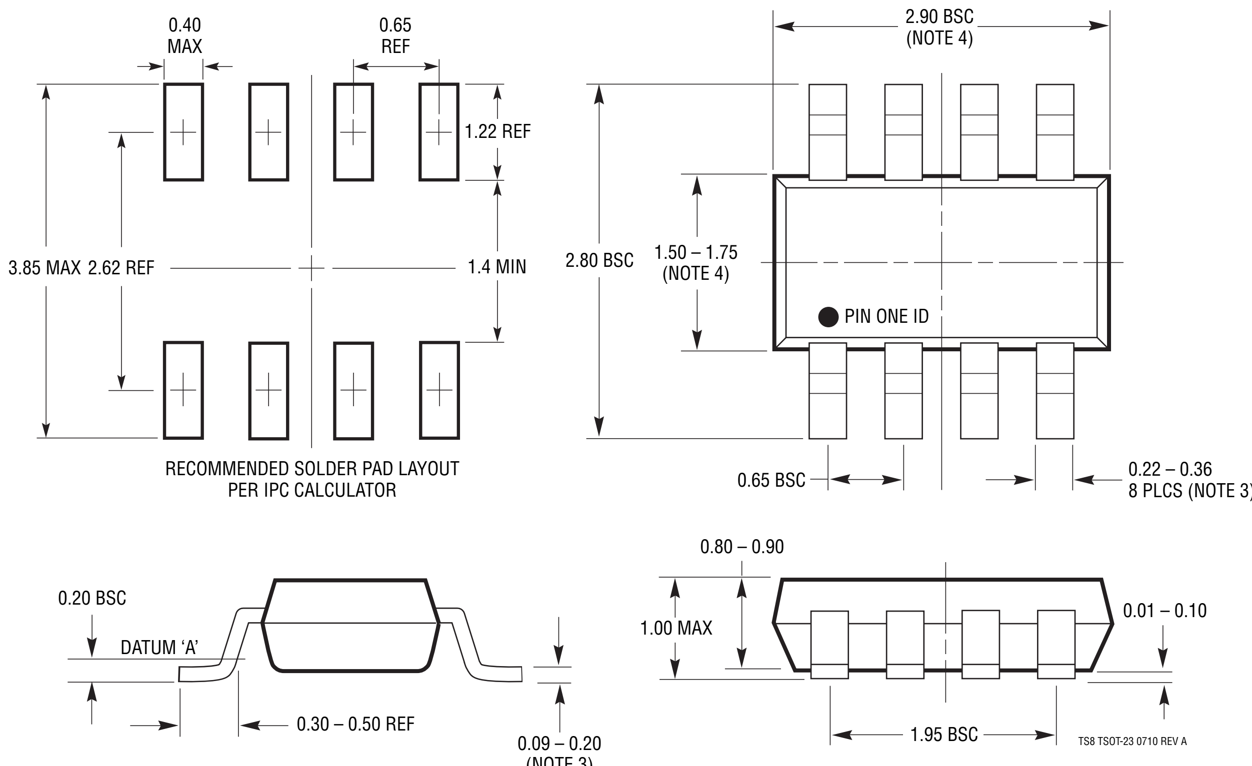


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637 Rev A)



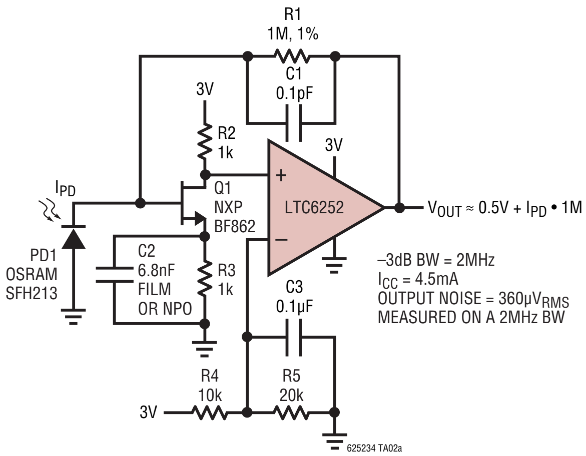
NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

REVISION HISTORY

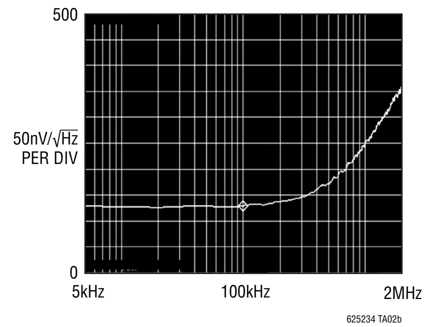
REV	DATE	DESCRIPTION	PAGE NUMBER
A	9/10	Revised I_{SD} Parameters in Electrical Characteristics section	4, 5
B	6/11	Added H-grade MS8 to Order Information section	2
C	1/12	Updated Electrical Characteristics	3 to 6

TYPICAL APPLICATION

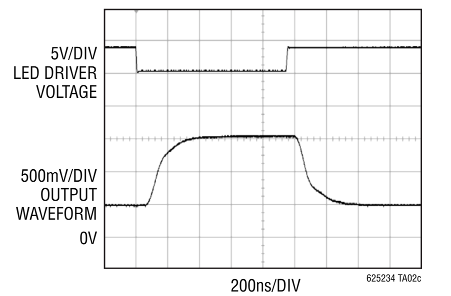
2MHz, 1MΩ Single Supply Photodiode Amplifier



Photodiode Amplifier Noise Spectrum



Photodiode Amplifier Transient Response



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Operational Amplifiers		
LT1818/LT1819	Single/Dual Wide Bandwidth, High Slew Rate Low Noise and Distortion Op Amps	400MHz, 9mA, 6nV/√Hz, 2500V/µs, 1.5mV –85dBc at 5MHz
LT1806/LT1807	Single/Dual Low Noise Rail-to-Rail Input and Output Op Amps	325MHz, 13mA, 3.5nV/√Hz, 140V/µs, 550µV, 85mA Output Drive
LTC6246/LTC6247/ LTC6248	Single/Dual/Quad High Speed Rail-to-Rail Input and Output Op Amps	180MHz, 1mA, 4.2nV/√Hz, 90V/µs, 0.5mV
LT6230/LT6231/ LT6232	Single/Dual/Quad Low Noise Rail-to-Rail Output Op Amps	215MHz, 3.5mA, 1.1nV/√Hz, 70V/µs, 350µV
LT6200/LT6201	Single/Dual Ultralow Noise Rail-to-Rail Input/Output Op Amps	165MHz, 20mA, 0.95nV/√Hz, 44V/µs, 1mV
LT6202/LT6203/ LT6204	Single/Dual/Quad Ultralow Noise Rail-to-Rail Op Amp	100MHz, 3mA, 1.9nV/√Hz, 25V/µs, 0.5mV
LT1468	16-Bit Accurate Precision High Speed Op Amp	90MHz, 3.9mA, 5nV/√Hz, 22V/µs, 175µV, –96.5dB THD at $10V_{P-P}$, 100kHz
LT1801/LT1802	Dual/Quad Low Power High Speed Rail-to-Rail Input and Output Op Amps	80MHz, 2mA, 8.5nV√Hz, 25V/µs, 350µV
LT1028	Ultralow Noise, Precision High Speed Op Amps	75MHz, 9.5mA, 0.85nV/√Hz, 11V/µs, 40µV
LTC6350	Low Noise Single-Ended to Differential Converter/ADC Driver	33MHz (–3dB), 4.8mA, 1.9nV/√Hz, 240ns Settling to 0.01% $8V_{P-P}$
ADCs		
LTC2393-16	1Msps 16-Bit SAR ADC	94dB SNR
LTC2366	3Msps, 12-Bit ADC Serial I/O	72dB SNR, 7.8mW No Data Latency TSOT-23 Package
LTC2365	1Msps, 12-Bit ADC Serial I/O	73dB SNR, 7.8mW No Data Latency TSOT-23 Package

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0112 REV C • PRINTED IN USA