

**RICOH****R1163x SERIES****3-MODE 150mA LDO REGULATOR with the Reverse Current Protection**

NO.EA-118-190320

**OUTLINE**

The R1163x Series consist of CMOS-based voltage regulator ICs with high output voltage accuracy and low supply current. These ICs perform with the chip enable function and realize a standby mode with ultra low supply current. To prevent the destruction by over current, the current limit circuit is included. The R1163x Series have 3-mode. One is standby mode with CE or standby control pin. Other two modes are realized with ECO pin. Fast Transient Mode (FT mode) and Low Power Mode (LP mode) are alternative with ECO pin. Consumption current is reduced at Low Power Mode compared with Fast Transient Mode. The output voltage is maintained between FT mode and LP mode.

Further, the reverse current protection circuit is built-in. Therefore, if a higher voltage than  $V_{DD}$  pin is forced to the output pin, the reverse current to  $V_{DD}$  pin is very small (Max.  $0.1\mu\text{A}$ ), so it is suitable for backup circuit.

Since the packages for these ICs are SOT-23-5, SON-6, and DFN(PLP)1616-6 packages, high density mounting of the ICs on boards is possible.

**FEATURES**

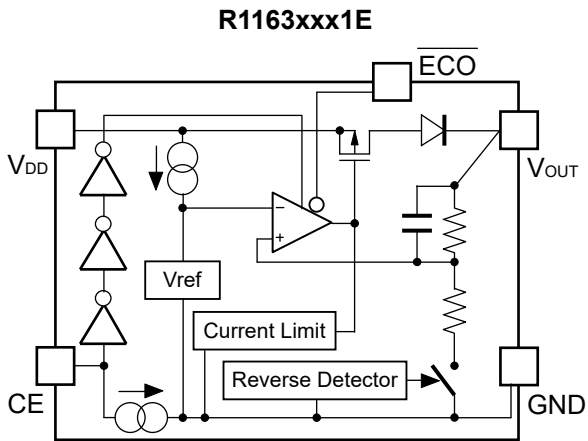
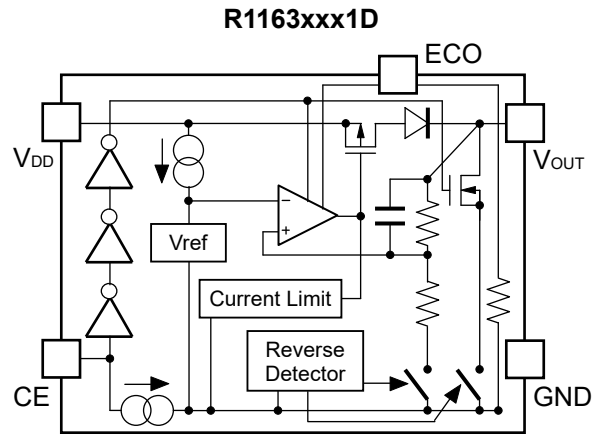
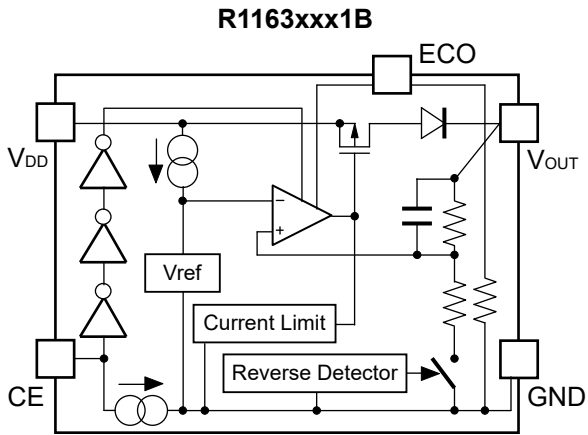
- Supply Current ..... Typ.  $6.0\mu\text{A}$  (Low Power Mode),  
Typ.  $70\mu\text{A}$  (Fast Transient Mode)
- Standby Mode ..... Typ.  $0.6\mu\text{A}$
- Reverse Current..... Max.  $0.1\mu\text{A}$
- Input Voltage Range .....  $2.0\text{V}$  to  $6.0\text{V}$
- Output Voltage Range.....  $1.5\text{V}$  to  $5.0\text{V}$  ( $0.1\text{V}$  steps)  
(For other voltages, please refer to MARK INFORMATIONS.)
- Output Voltage Accuracy.....  $\pm 1.5\%$  ( $\pm 2.5\%$  at Low Power Mode)
- Temperature-Drift Coefficient of Output Voltage .. Typ.  $\pm 100\text{ppm}/^\circ\text{C}$
- Dropout Voltage ..... Typ.  $0.25\text{V}$  ( $I_{\text{OUT}}=150\text{mA}$ ,  $V_{\text{OUT}}=2.8\text{V}$ )
- Ripple Rejection ..... Typ.  $70\text{dB}$  ( $f=1\text{kHz}$ , Fast Transient Mode)
- Line Regulation ..... Typ.  $0.02\%/V$  (Fast Transient Mode)
- Packages ..... DFN(PLP)1616-6, SOT-23-5, SON-6
- Built-in fold-back protection circuit ..... Typ.  $40\text{mA}$  (Current at short mode)
- Performs with Ceramic Capacitors .....  $C_{\text{IN}}=\text{Ceramic } 1.0\mu\text{F}$ ,  $C_{\text{OUT}}=\text{Ceramic } 0.47\mu\text{F}$

**APPLICATIONS**

- Precision Voltage References.
- Power source for electrical appliances such as cameras, VCRs and hand-held communication equipment.
- Power source for battery-powered equipment.

**R1163x**

**BLOCK DIAGRAM**



## SELECTION GUIDE

The output voltage, auto discharge function, and package, etc. for the ICs can be selected at the user's request.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R1163Kxx1*-TR	DFN(PLP)1616-6	5,000 pcs	Yes	Yes
R1163Nxx1*-TR-FE	SOT-23-5	3,000 pcs	Yes	Yes
R1163Dxx1*-TR-FE	SON-6	3,000 pcs	Yes	Yes

xx: The output voltage can be designated in the range from 1.5V(15) to 5.0V(50) in 0.1V steps.  
(For other voltages, please refer to MARK INFORMATIONS.)

\* : The auto discharge function at off state are options as follows.

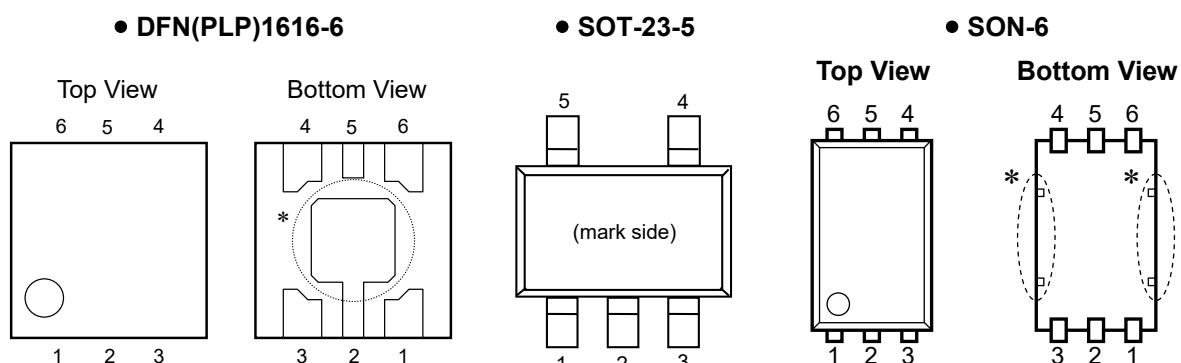
(B) without auto discharge function at off state

(D) with auto discharge function at off state

(E) without auto discharge function at off state, ECO logic reverse type (Low Power mode at ECO="H")

## R1163x

### PIN CONFIGURATIONS



### PIN DISCRIPTIONS

#### • DFN(PLP)1616-6

Pin No	Symbol	Pin Description
1	$V_{OUT}$	Output pin
2	GND	Ground Pin
3	ECO	R1163xxx1B/D: FT/LP Mode Alternative Pin ("L" LP)
	$\overline{ECO}$	R1163xxx1E: FT/LP Mode Alternative Pin ("H" LP)
4	CE	Chip Enable pin ("H" Active)
5	NC	No Connection
6	$V_{DD}$	Input Pin

\*) Tab is GND level. (They are connected to the reverse side of this IC.)

The tab is better to be connected to the GND, but leaving it open is also acceptable.

#### • SOT-23-5

Pin No	Symbol	Pin Description
1	$V_{DD}$	Input Pin
2	GND	Ground Pin
3	CE	Chip Enable Pin ("H" Active)
4	ECO	R1163xxx1B/D: FT/LP Mode Alternative Pin ("L" LP)
	$\overline{ECO}$	R1163xxx1E: FT/LP Mode Alternative Pin ("H" LP)
5	$V_{OUT}$	Output pin

#### • SON-6

Pin No	Symbol	Pin Description
1	$V_{DD}$	Input Pin
2	NC	No Connection
3	$V_{OUT}$	Output pin
4	ECO	R1163xxx1B/D: FT/LP Mode Alternative Pin ("L" LP)
	$\overline{ECO}$	R1163xxx1E: FT/LP Mode Alternative Pin ("H" LP)
5	GND	Ground Pin
6	CE	Chip Enable Pin ("H" Active)

\*) Tab suspension leads are GND level. (They are connected to the reverse side of this IC.)

The tab suspension leads should be open and do not connect to other wires or land patterns.

## ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
$V_{IN}$	Input Voltage	6.5	V
$V_{ECO}$	Input Voltage (ECO/ $\overline{ECO}$ Pin)	-0.3 ~ 6.5	V
$V_{CE}$	Input Voltage (CE Pin)	-0.3 ~ 6.5	V
$V_{OUT}$	Output Voltage	-0.3 ~ 6.5	V
$I_{OUT}$	Output Current	180	mA
$P_D$	Power Dissipation (DFN(PLP)1616-6)*	640	mW
	Power Dissipation (SOT-23-5) *	420	
	Power Dissipation (SON-6) *	500	
$T_{opt}$	Operating Temperature Range	-40 ~ 85	°C
$T_{stg}$	Storage Temperature Range	-55 ~ 125	°C

\*) For Power Dissipation, please refer to PACKAGE INFORMATION.

### ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field.

The functional operation at or over these absolute maximum ratings is not assured.

### RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

## R1163x

## ELECTRICAL CHARACTERISTICS

## R1163xxx1B/D

T<sub>opt</sub>=25°C

Symbol	Item		Conditions	Min.	Typ.	Max.	Unit	
V <sub>OUT</sub>	Output Voltage	FT Mode	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V, V <sub>ECO</sub> =V <sub>IN</sub> 1mA ≤ I <sub>OUT</sub> ≤ 30mA	×0.985		×1.015	V	
		LP Mode	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V, V <sub>ECO</sub> =GND 1mA ≤ I <sub>OUT</sub> ≤ 30mA	×0.975		×1.025		
ΔV <sub>OUT</sub>	Output Voltage Deviation between FT Mode and LP Mode		V <sub>IN</sub> =Set V <sub>OUT</sub> +1V, I <sub>OUT</sub> =30mA	V <sub>OUT</sub> > 2.0V	-1.2	0	1.2	%
				V <sub>OUT</sub> ≤ 2.0V	-24	0	24	mV
I <sub>OUT</sub>	Output Current		V <sub>IN</sub> -V <sub>OUT</sub> =1.0V	150			mA	
ΔV <sub>OUT</sub> / ΔI <sub>OUT</sub>	Load Regulation	FT Mode	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V, V <sub>ECO</sub> =V <sub>IN</sub> 1mA ≤ I <sub>OUT</sub> ≤ 150mA		20	40	mV	
		LP Mode	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V, V <sub>ECO</sub> =GND 1mA ≤ I <sub>OUT</sub> ≤ 150mA		20	45		
V <sub>DIF</sub>	Dropout Voltage		Refer to the following table					
I <sub>SS1</sub>	Supply Current (FT Mode)		V <sub>IN</sub> =Set V <sub>OUT</sub> +1V V <sub>ECO</sub> =V <sub>IN</sub>		70	100	μA	
I <sub>SS2</sub>	Supply Current (LP Mode)		V <sub>IN</sub> =Set V <sub>OUT</sub> +1V V <sub>ECO</sub> =GND		6.0	10.0	μA	
I <sub>standby</sub>	Supply Current (Standby)		V <sub>IN</sub> =Set V <sub>OUT</sub> +1V, V <sub>CE</sub> =GND V <sub>ECO</sub> =GND or V <sub>IN</sub>		0.6	1.0	μA	
ΔV <sub>OUT</sub> / ΔV <sub>IN</sub>	Line Regulation	FT Mode	Set V <sub>OUT</sub> +0.5V ≤ V <sub>IN</sub> ≤ 6.0V I <sub>OUT</sub> =30mA, V <sub>ECO</sub> =V <sub>IN</sub> If V <sub>OUT</sub> ≤ 1.6V, then 2.2V ≤ V <sub>IN</sub> ≤ 6.0V		0.02	0.10	%V	
		LP Mode	Set V <sub>OUT</sub> +0.5V ≤ V <sub>IN</sub> ≤ 6.0V I <sub>OUT</sub> =30mA, V <sub>ECO</sub> =GND If V <sub>OUT</sub> ≤ 1.6V, then 2.2V ≤ V <sub>IN</sub> ≤ 6.0V		0.05	0.20		
RR	Ripple Rejection (FT Mode)		Ripple 0.2V <sub>p-p</sub> , V <sub>IN</sub> =Set V <sub>OUT</sub> +1V, I <sub>OUT</sub> =30mA, V <sub>ECO</sub> =V <sub>IN</sub> If V <sub>OUT</sub> ≤ 1.7V, then V <sub>IN</sub> =Set V <sub>OUT</sub> +1.2V	f=1kHz		70	dB	
				f=10kHz		60		
V <sub>IN</sub>	Input Voltage			2.0		6.0	V	
ΔV <sub>OUT</sub> / ΔT <sub>opt</sub>	Output Voltage Temperature Coefficient		I <sub>OUT</sub> =30mA -40°C ≤ T <sub>opt</sub> ≤ 85°C		±100		ppm/°C	
I <sub>SC</sub>	Short Current Limit		V <sub>OUT</sub> =0V		40		mA	
I <sub>PD</sub>	CE Pull-down Current				0.3	0.6	μA	
R <sub>PDE</sub>	ECO Pull-down Resistance			2	5	30	MΩ	
V <sub>CEH</sub>	CE, ECO Input Voltage "H"			1.0		6.0	V	
V <sub>CEL</sub>	CE, ECO Input Voltage "L"			0		0.35	V	
en	Output Noise "H" (FT Mode)		BW=10Hz to 100kHz		30		μV <sub>rms</sub>	
	Output Noise "L" (LP Mode)		BW=10Hz to 100kHz		40			
R <sub>LOW</sub>	Low Output Nch Tr. ON Resistance (of D version)		V <sub>CE</sub> =0V		60		Ω	
I <sub>REV</sub>	Reverse Current		V <sub>OUT</sub> >0.5V, 0V ≤ V <sub>IN</sub> ≤ 6V		0	0.1	μA	

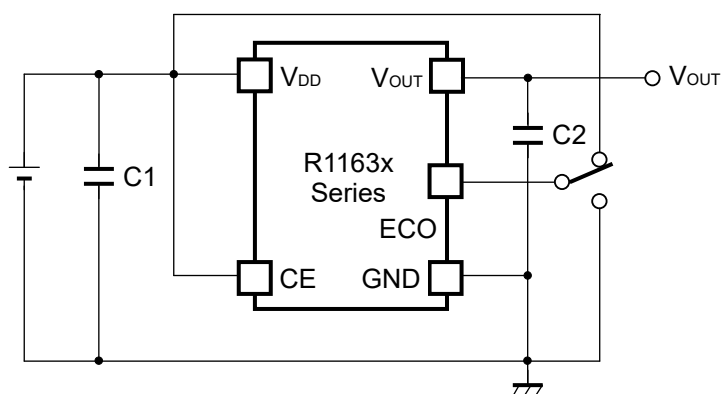
## R1163xxx1E

T<sub>opt</sub>=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	
V <sub>OUT</sub>	Output Voltage	FT Mode	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V, V <sub>ECO</sub> =GND 1mA ≤ I <sub>OUT</sub> ≤ 30mA	×0.985		×1.015	V
		LP Mode	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V, V <sub>ECO</sub> =V <sub>IN</sub> 1mA ≤ I <sub>OUT</sub> ≤ 30mA	×0.975		×1.025	
ΔV <sub>OUT</sub>	Output Voltage Deviation between FT Mode and LP Mode	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V, I <sub>OUT</sub> =30mA	V <sub>OUT</sub> > 2.0V	-1.2	0	1.2	%
			V <sub>OUT</sub> ≤ 2.0V	-24	0	24	mV
I <sub>OUT</sub>	Output Current	V <sub>IN</sub> -V <sub>OUT</sub> =1.0V	150			mA	
ΔV <sub>OUT</sub> / ΔI <sub>OUT</sub>	Load Regulation	FT Mode	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V, V <sub>ECO</sub> =GND 1mA ≤ I <sub>OUT</sub> ≤ 150mA		20	40	mV
		LP Mode	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V, V <sub>ECO</sub> =V <sub>IN</sub> 1mA ≤ I <sub>OUT</sub> ≤ 150mA		20	45	
V <sub>DIF</sub>	Dropout Voltage	Refer to the following table					
I <sub>SS1</sub>	Supply Current (FT Mode)	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V V <sub>ECO</sub> =GND		70	100	μA	
I <sub>SS2</sub>	Supply Current (LP Mode)	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V V <sub>ECO</sub> =V <sub>IN</sub>		6.0	10.0	μA	
I <sub>standby</sub>	Supply Current (Standby)	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V, V <sub>CE</sub> =GND V <sub>ECO</sub> =GND or V <sub>IN</sub>		0.6	1.0	μA	
ΔV <sub>OUT</sub> / ΔV <sub>IN</sub>	Line Regulation	FT Mode	Set V <sub>OUT</sub> +0.5V ≤ V <sub>IN</sub> ≤ 6.0V I <sub>OUT</sub> =30mA, V <sub>ECO</sub> =GND If V <sub>OUT</sub> ≤ 1.6V, then 2.2V ≤ V <sub>IN</sub> ≤ 6.0V		0.02	0.10	%V
		LP Mode	Set V <sub>OUT</sub> +0.5V ≤ V <sub>IN</sub> ≤ 6.0V I <sub>OUT</sub> =30mA, V <sub>ECO</sub> =V <sub>IN</sub> If V <sub>OUT</sub> ≤ 1.6V, then 2.2V ≤ V <sub>IN</sub> ≤ 6.0V		0.05	0.20	
RR	Ripple Rejection (FT Mode)	Ripple 0.2V <sub>p-p</sub> V <sub>IN</sub> =Set V <sub>OUT</sub> +1V, I <sub>OUT</sub> =30mA, V <sub>ECO</sub> =GND If V <sub>OUT</sub> ≤ 1.7V, then V <sub>IN</sub> =Set V <sub>OUT</sub> +1.2V	f = 1kHz		70		dB
			f = 10kHz		60		
V <sub>IN</sub>	Input Voltage		2.0		6.0	V	
ΔV <sub>OUT</sub> / ΔT <sub>opt</sub>	Output Voltage Temperature Coefficient	I <sub>OUT</sub> = 30mA -40°C ≤ T <sub>opt</sub> ≤ 85°C		±100		ppm/°C	
I <sub>SC</sub>	Short Current Limit	V <sub>OUT</sub> = 0V		40		mA	
I <sub>PD</sub>	CE Pull-down Current			0.3	0.6	μA	
V <sub>CEH</sub>	CE, $\overline{ECO}$ Input Voltage "H"		1.0		6.0	V	
V <sub>CEL</sub>	CE, $\overline{ECO}$ Input Voltage "L"		0		0.4	V	
en	Output Noise "H" (FT Mode)	BW = 10Hz to 100kHz		30		μVrms	
	Output Noise "L" (LP Mode)	BW = 10Hz to 100kHz		40			
I <sub>REV</sub>	Reverse Current	V <sub>OUT</sub> >0.5V, 0V ≤ V <sub>IN</sub> ≤ 6V		0	0.1	μA	

**R1163x****ELECTRICAL CHARACTERISTICS by OUTPUT VOLTAGE**T<sub>opt</sub>=25°C

Output Voltage V <sub>OUT</sub> (V)	Dropout Voltage (mV)				
	Condition	V <sub>DIF</sub> (FT Mode)		V <sub>DIF</sub> (LP Mode)	
		Typ.	Max.	Typ.	Max.
1.5 ≤ V <sub>OUT</sub> < 1.6	I <sub>OUT</sub> =150mA	400	680	420	680
1.6 ≤ V <sub>OUT</sub> < 1.7		380	550	390	550
1.7 ≤ V <sub>OUT</sub> < 1.8		350	520	370	520
1.8 ≤ V <sub>OUT</sub> < 2.0		340	490	350	490
2.0 ≤ V <sub>OUT</sub> < 2.8		290	425	300	430
2.8 ≤ V <sub>OUT</sub> ≤ 5.0		250	350	250	350

**TYPICAL APPLICATION**

(External Components)

Ex. C1: Ceramic Capacitor 1.0μF

C2: Ceramic Capacitor 0.47μF Murata GRM40B474K  
Kyocera CM105B474K**TECHNICAL NOTES**

When using these ICs, consider the following points:

**Phase Compensation**

In these ICs, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, be sure to use a 0.47μF or more ceramic capacitor C2.

(Test these ICs with as same external components as ones to be used on the PCB.)

When a tantalum capacitor is used with this IC, if the equivalent series resistor (ESR) of the capacitor is large, output voltage may be unstable.

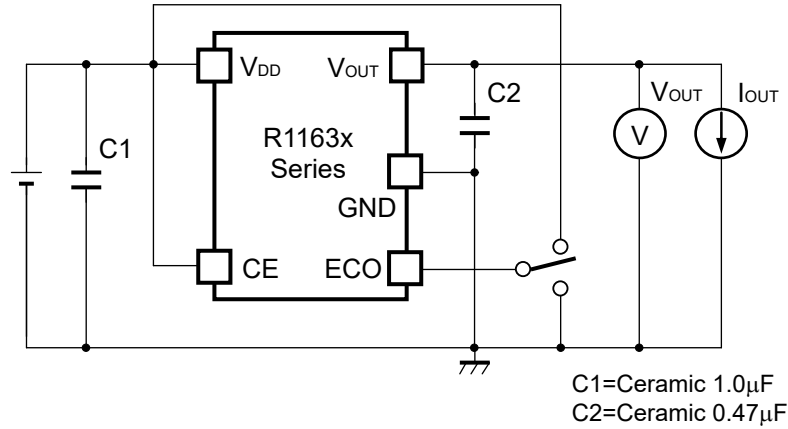
**PCB Layout**

Make V<sub>DD</sub> and GND lines sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect a capacitor C1 with as much as 1.0μF capacitor between V<sub>DD</sub> and GND pin as close as possible.

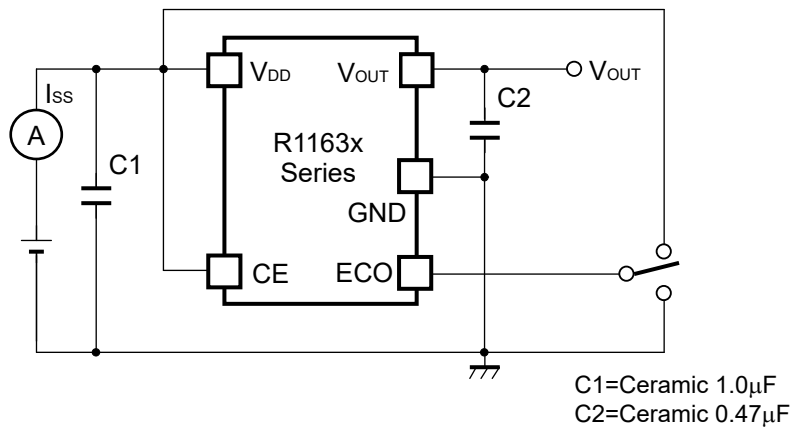
Set external components such as an output capacitor C2, as close as possible to the ICs and make wiring as short as possible.



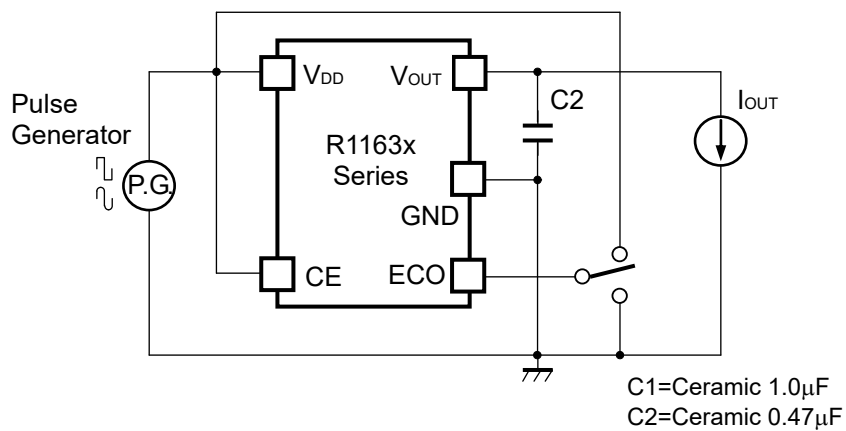
## TEST CIRCUITS



**Basic Test Circuit**

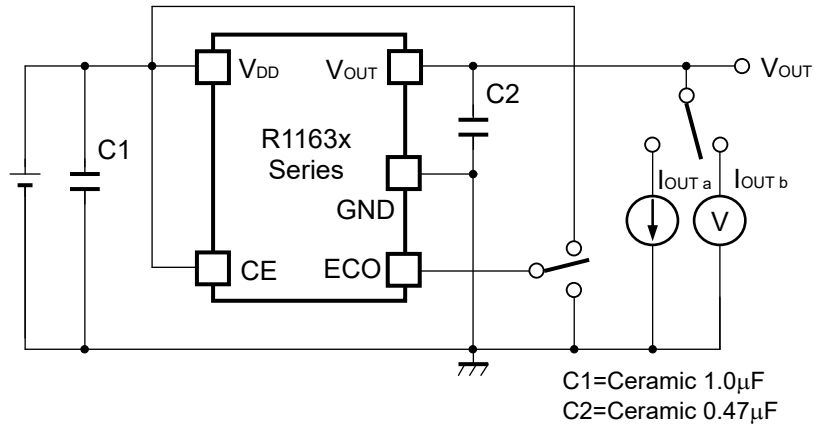


**Test Circuit for Supply Current**

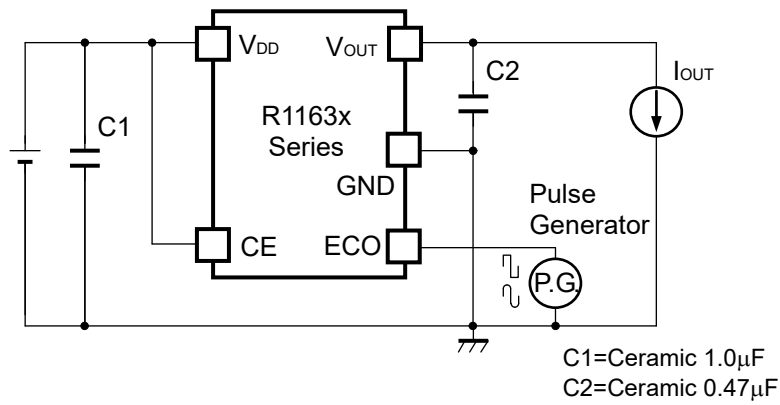


**Test Circuit for Ripple Rejection, Line Transient Response**

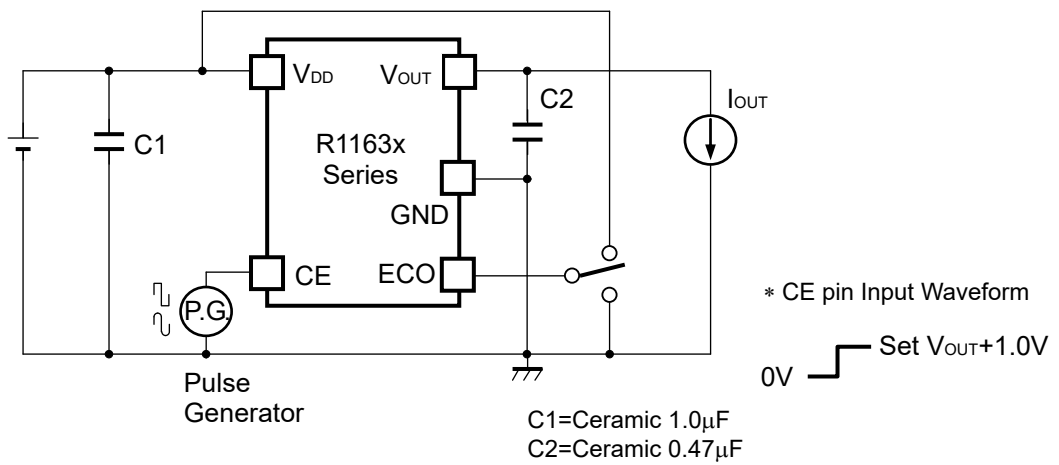
**R1163x**



**Test Circuit for Load Transient Response**



**Test Circuit for Output Voltage at Mode alternative point**



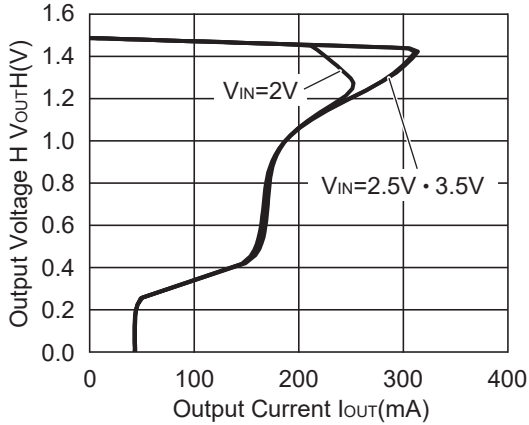
**Test Circuit for Turn On Speed with CE pin**

## TYPICAL CHARACTERISTICS

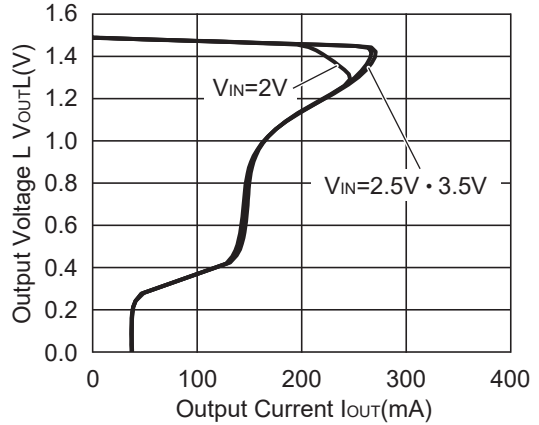
Unless otherwise provided, capacitors are ceramic type.

### 1) Output Voltage vs. Output Current

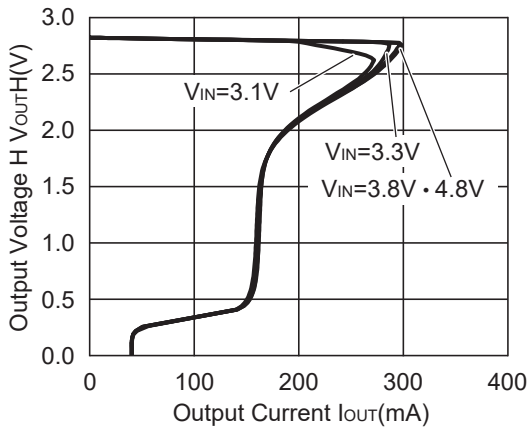
R1163x151x FT Mode



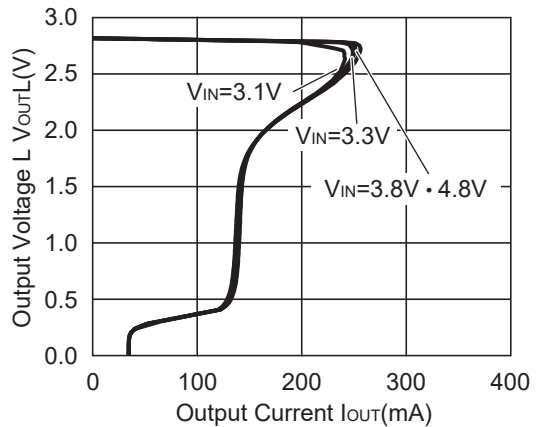
R1163x151x LP Mode



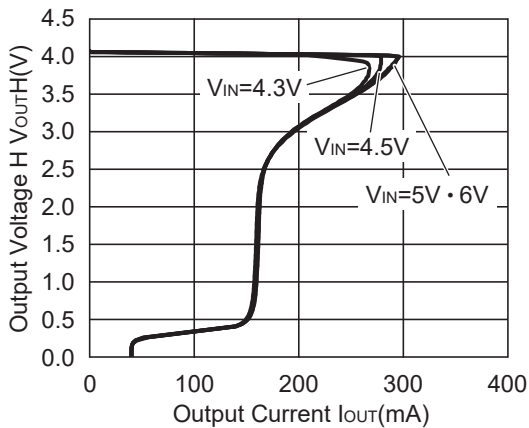
R1163x281x FT Mode



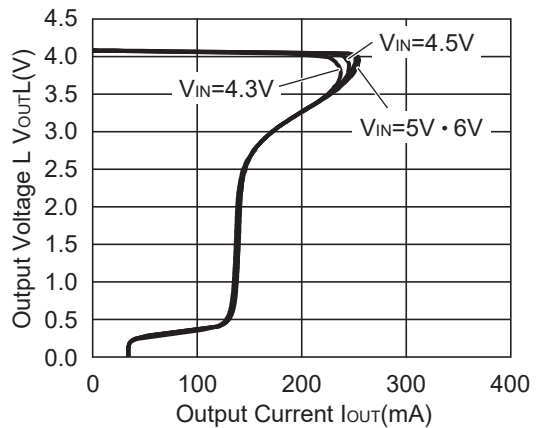
R1163x281x LP Mode



R1163x40x FT Mode



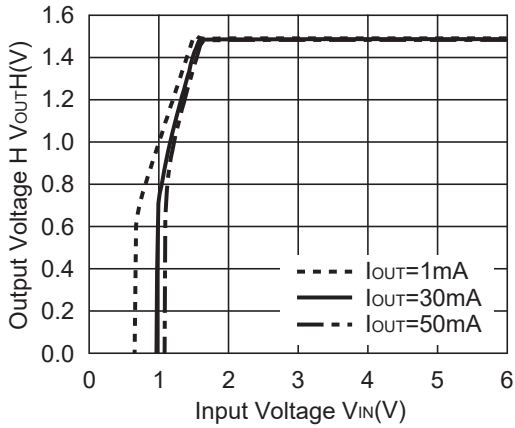
R1163x40x LP Mode



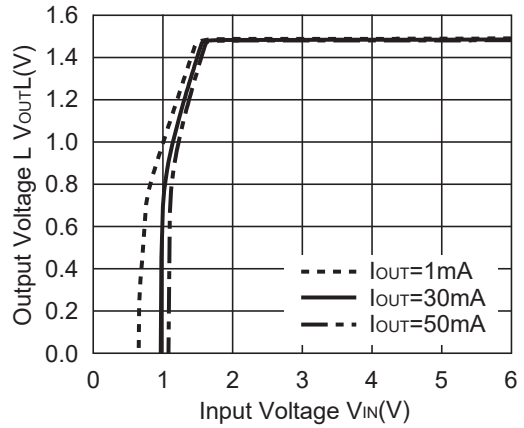
**R1163x**

**2) Output Voltage vs. Input Voltage**

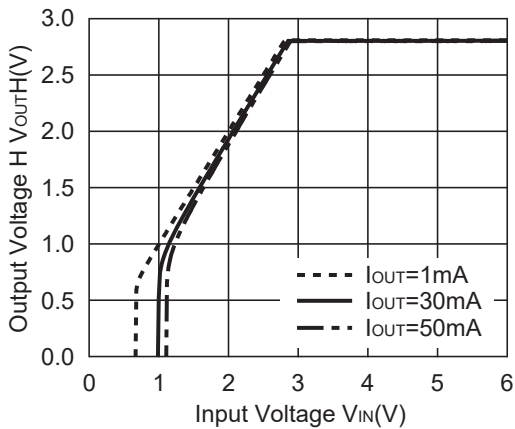
**R1163x151x FT Mode**



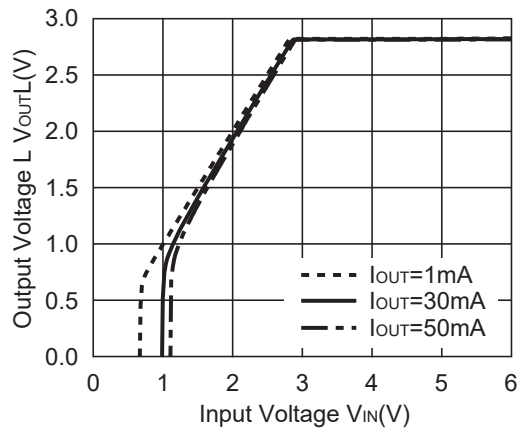
**R1163x15x LP Mode**



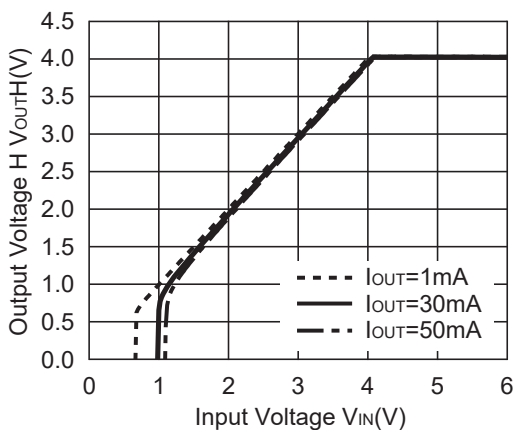
**R1163x28x FT Mode**



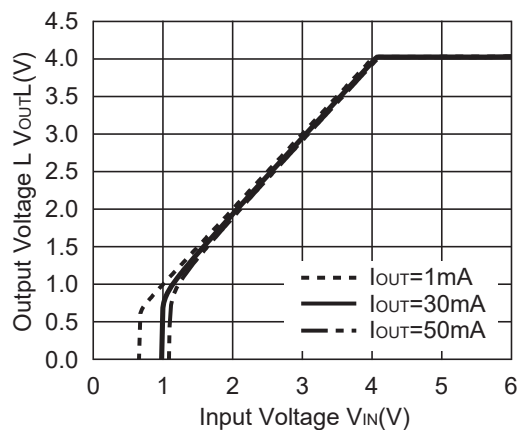
**R1163x28x LP Mode**



**R1163x40x FT Mode**

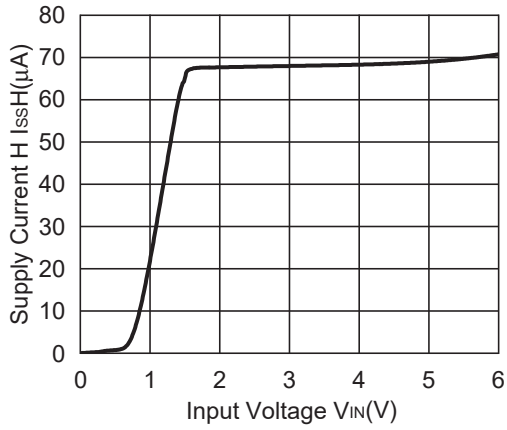


**R1163x40x LP Mode**

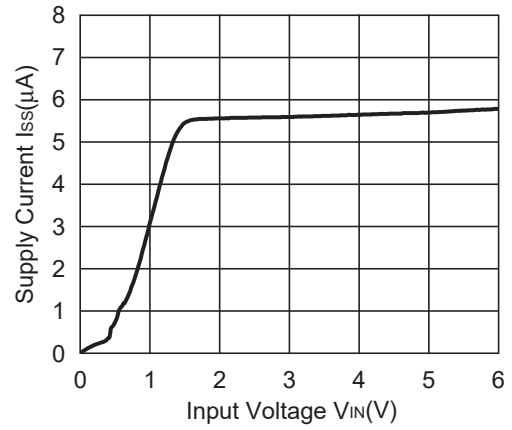


3) Supply Current vs. Input Voltage

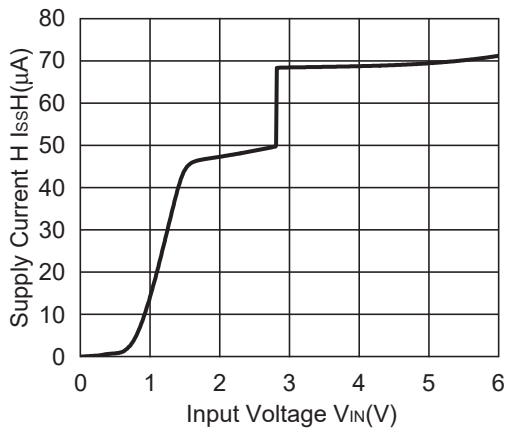
R1163x151x FT Mode



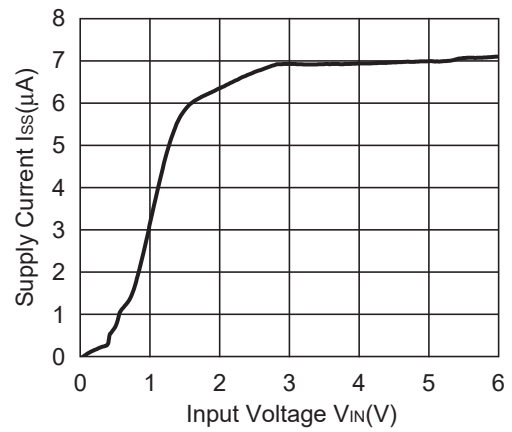
R1163x151x LP Mode



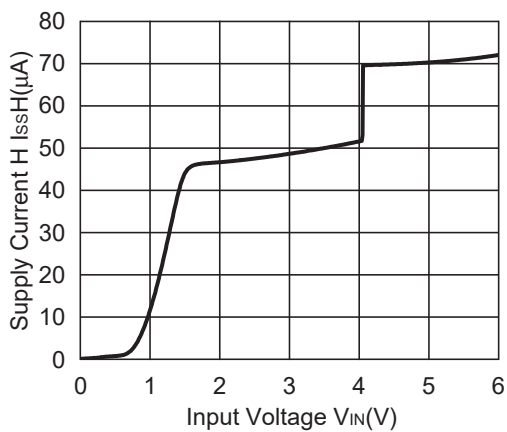
R1163x281x FT Mode



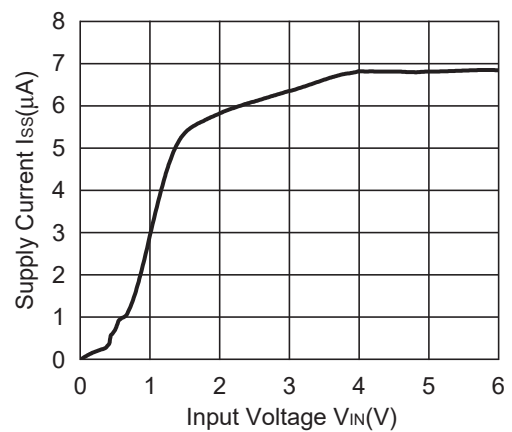
R1163x281x LP Mode



R1163x401x FT Mode



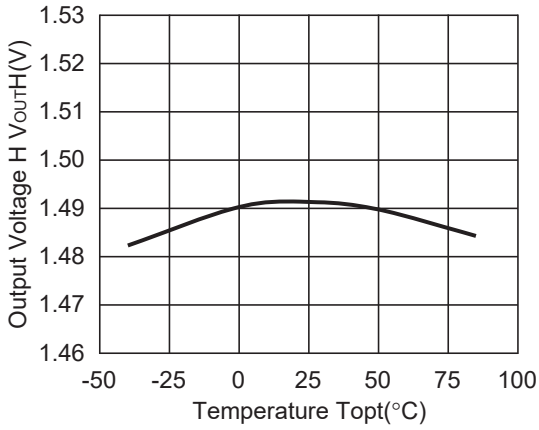
R1163x401x LP Mode



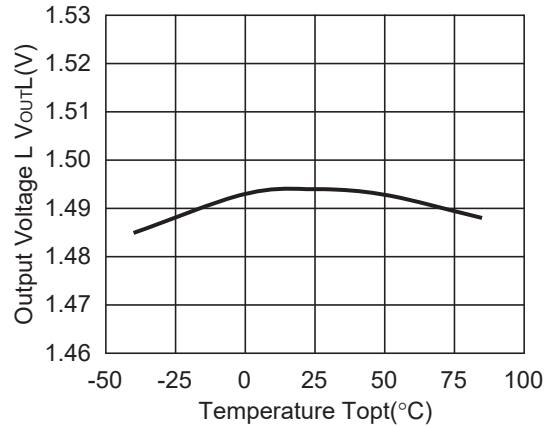
**R1163x**

**4) Output Voltage vs. Temperature**

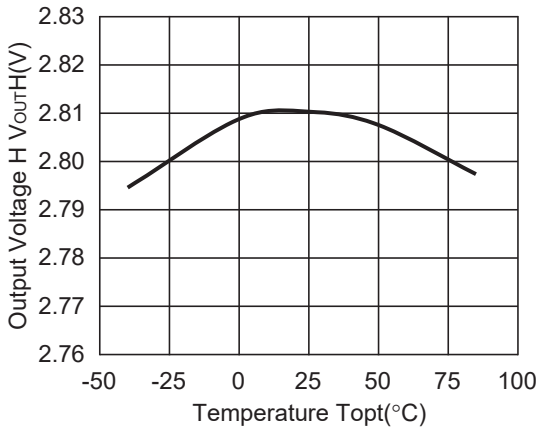
**R1163x151x FT Mode**



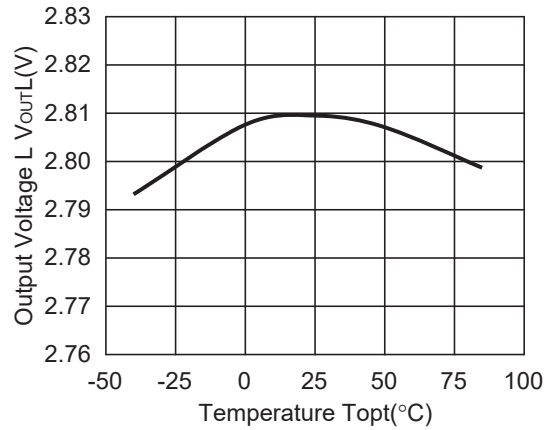
**R1163x151x LP Mode**



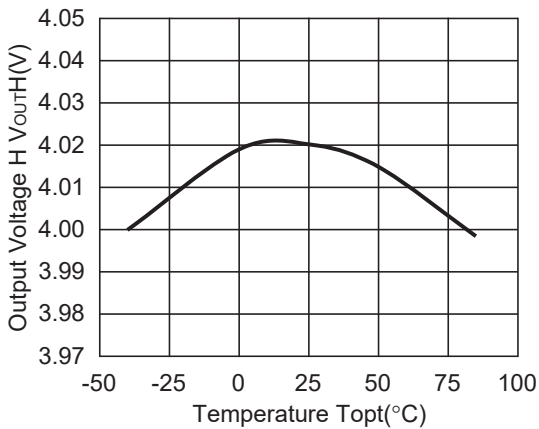
**R1163x281x FT Mode**



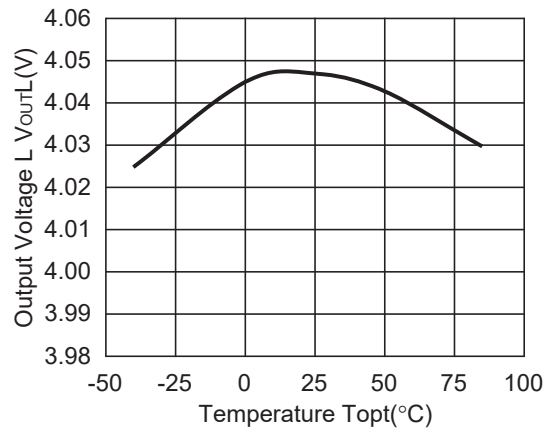
**R1163x281x LP Mode**



**R1163x401x FT Mode**

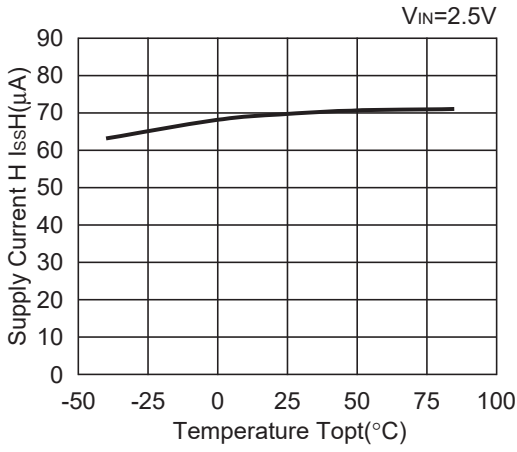


**R1163x401x LP Mode**

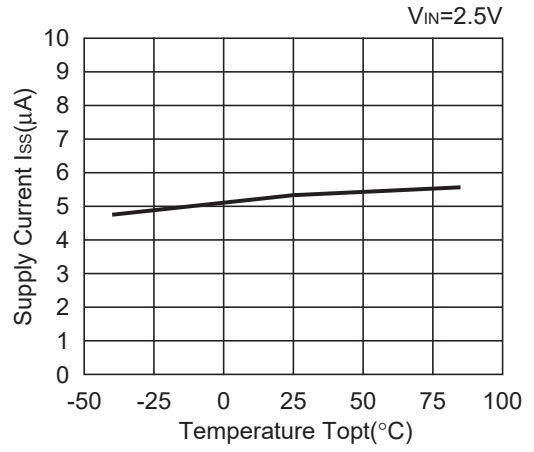


5) Supply Current vs. Temperature

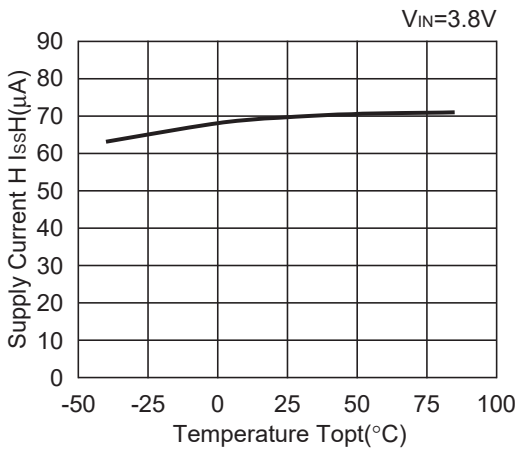
R1163x151x FT Mode



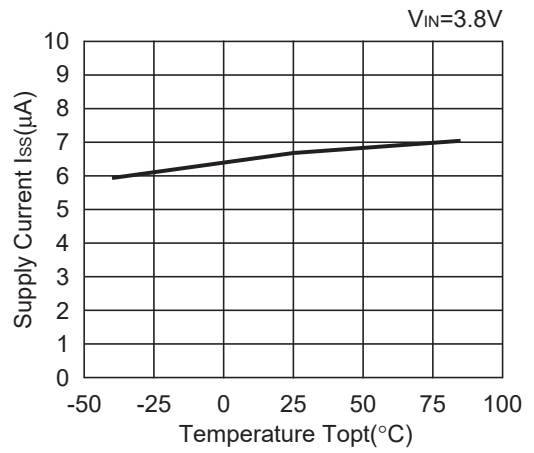
R1163x151x LP Mode



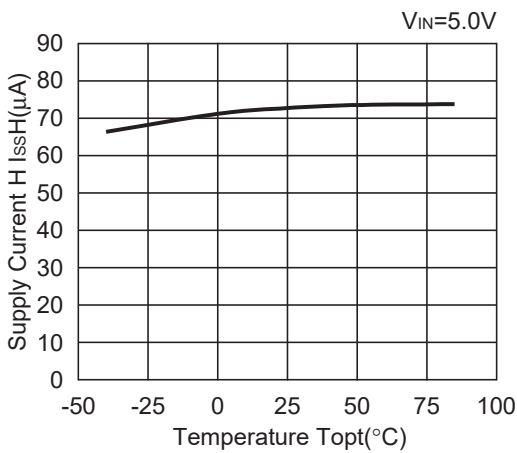
R1163x281x FT Mode



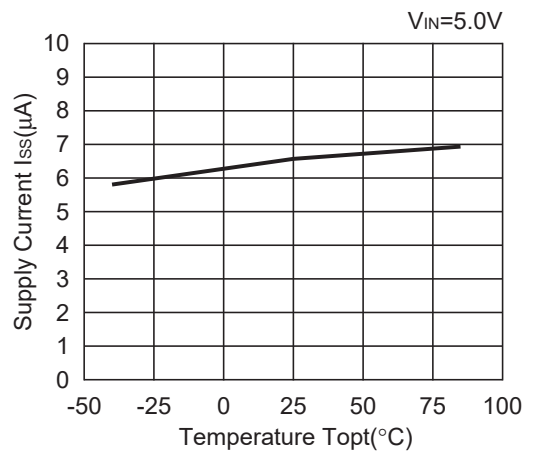
R1163x281x LP Mode



R1163x401x FT Mode

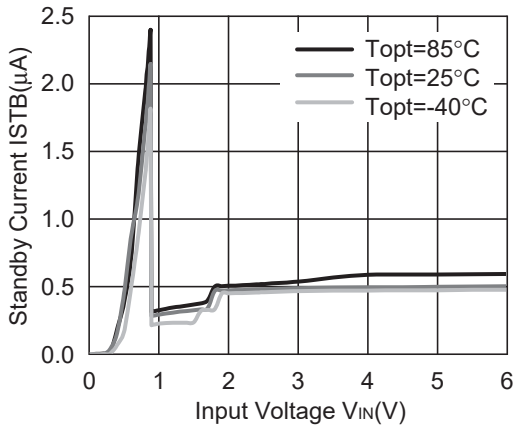


R1163x401x LP Mode

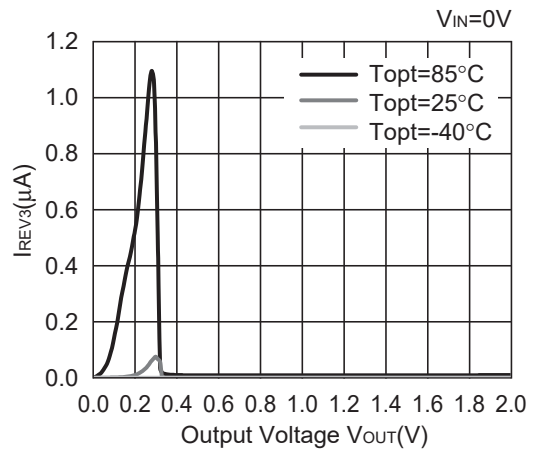
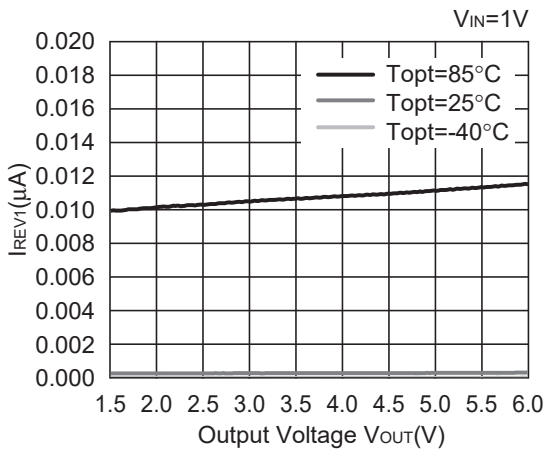


**R1163x**

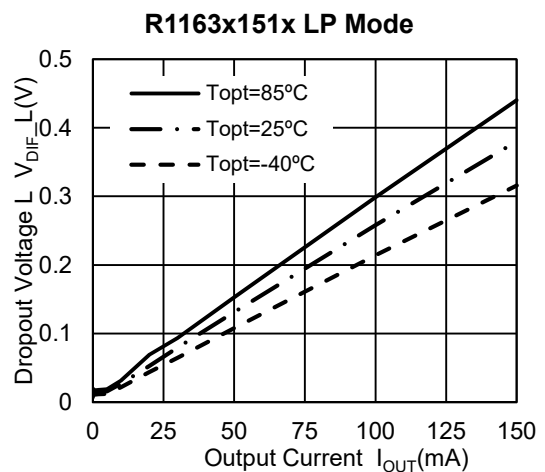
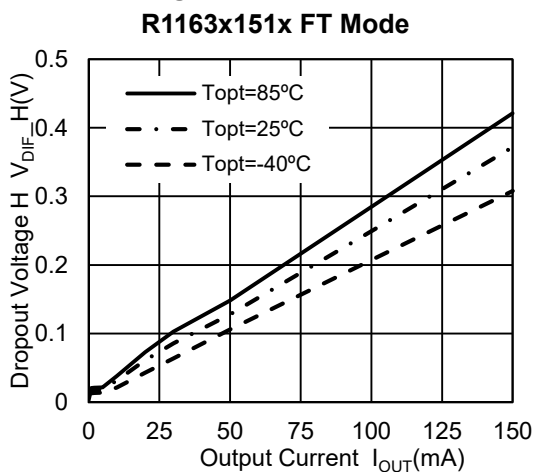
**6) Standby Current vs. Input Voltage**



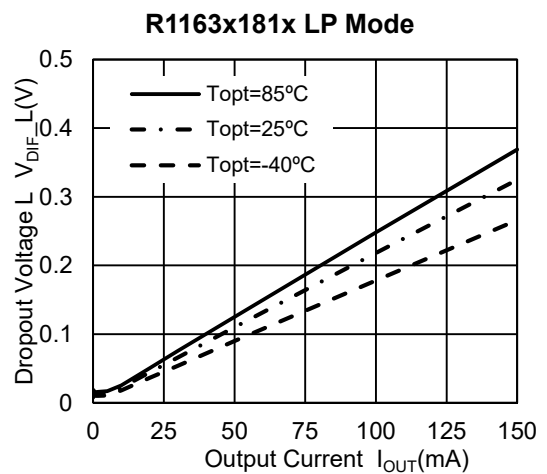
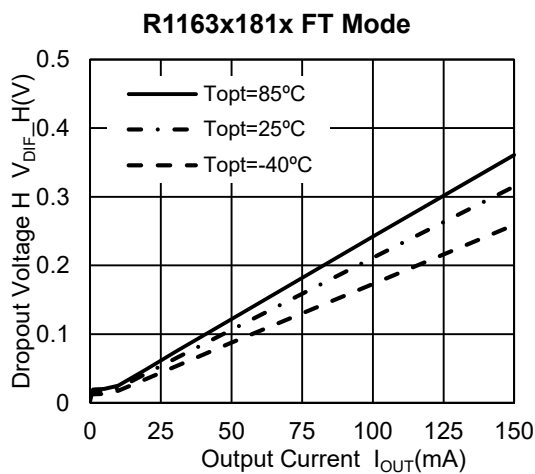
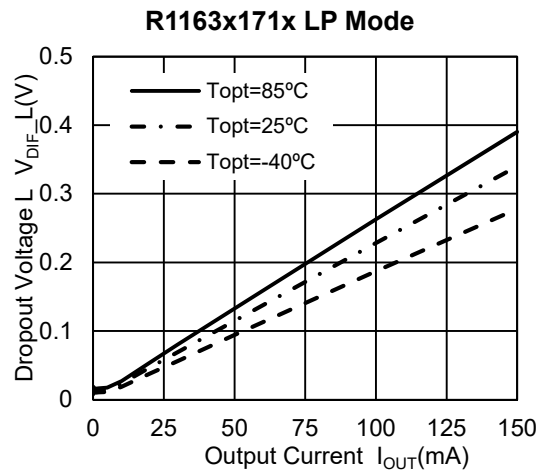
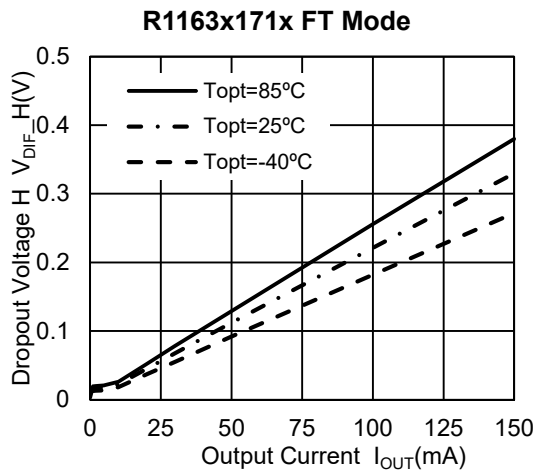
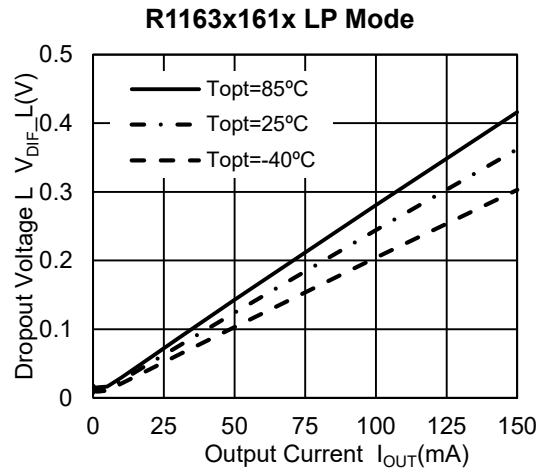
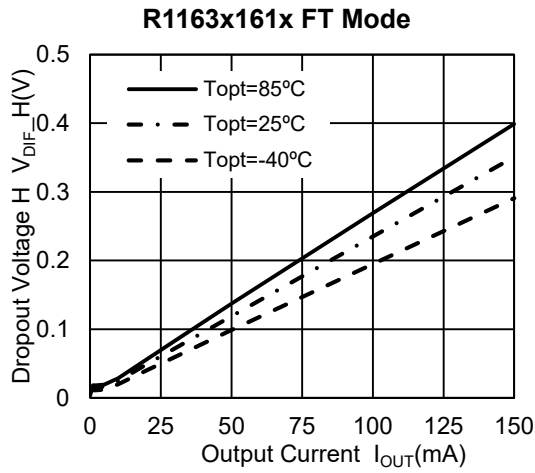
**7) Reverse Current vs. Output Voltage**



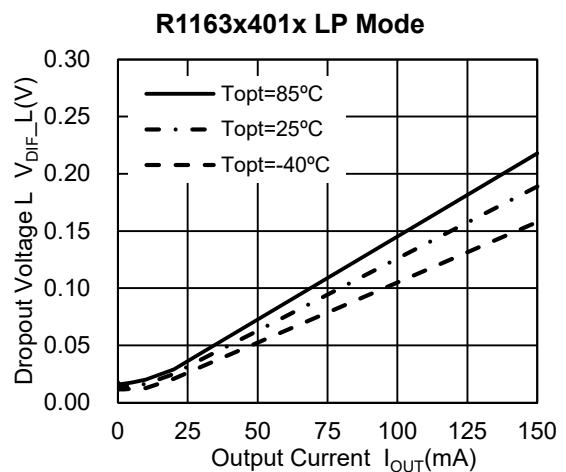
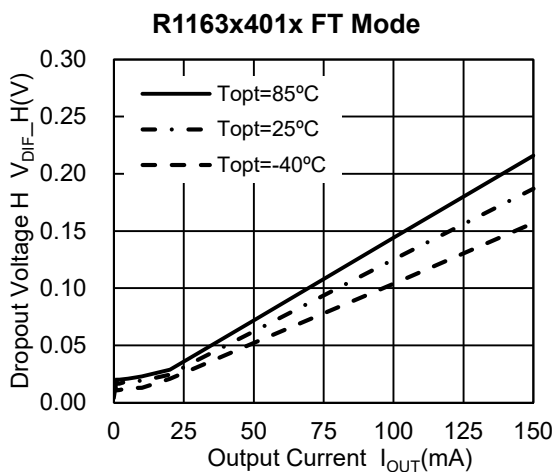
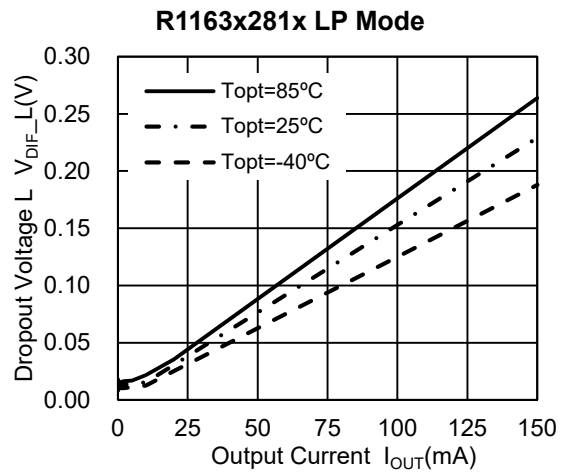
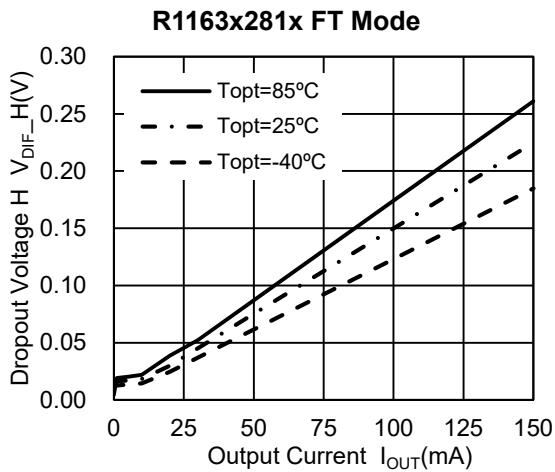
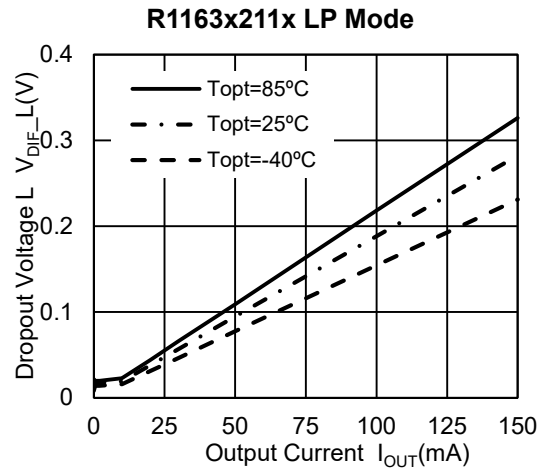
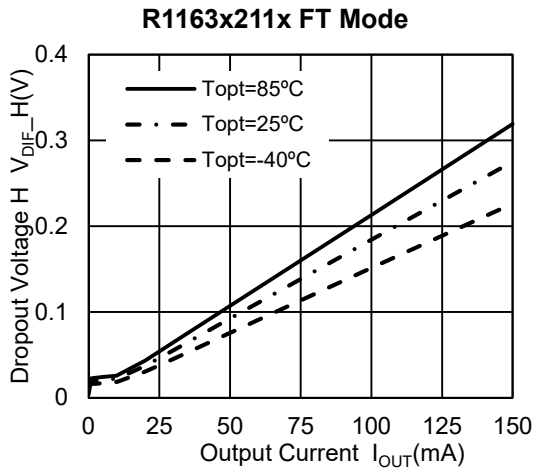
**8) Dropout Voltage vs. Output Current**



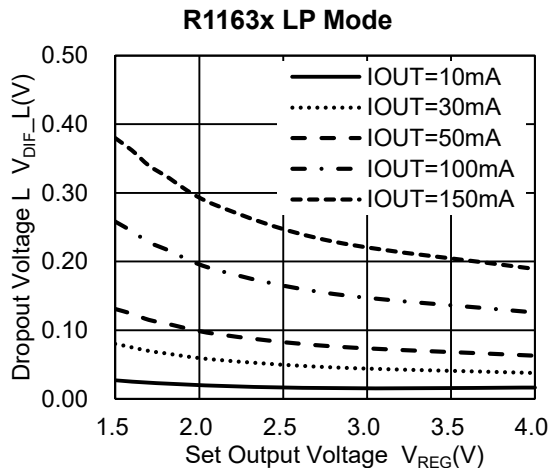
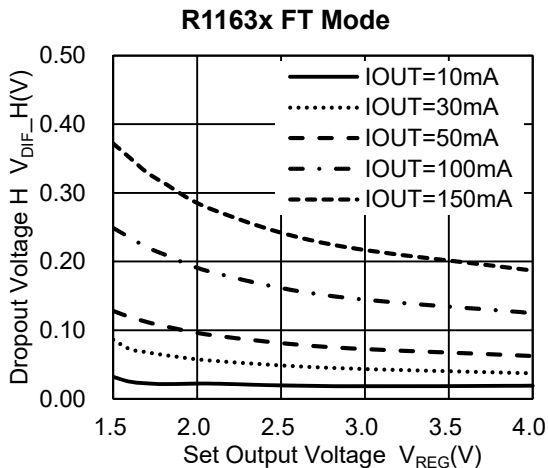




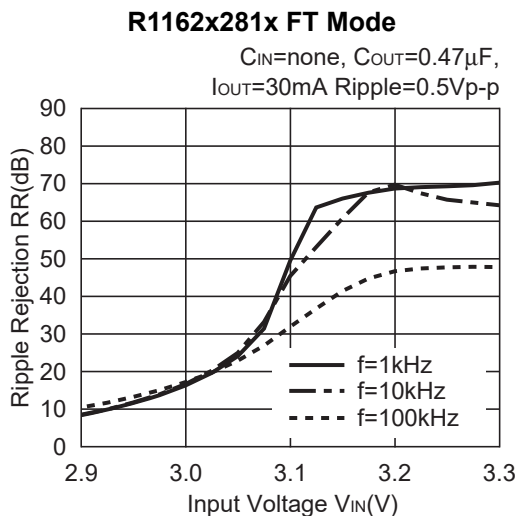
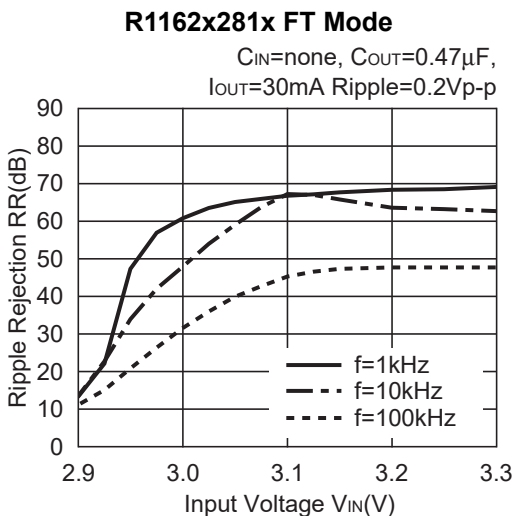
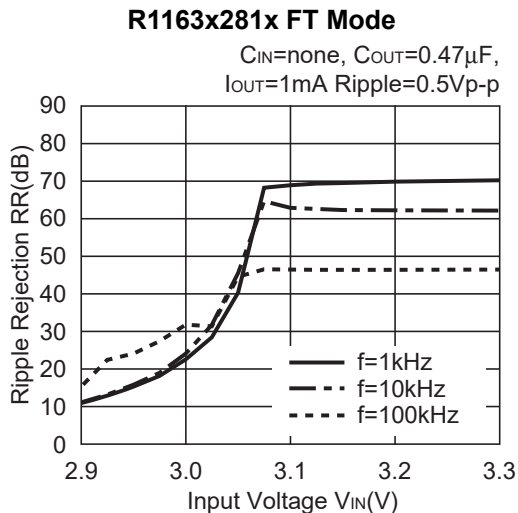
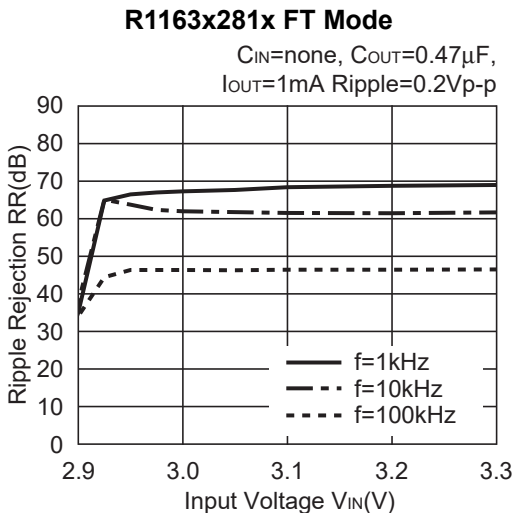
**R1163x**



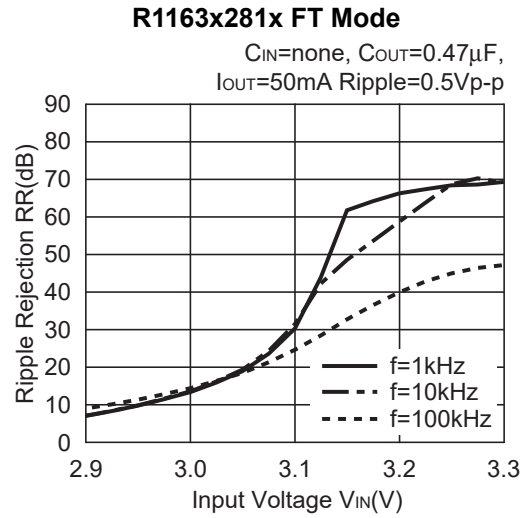
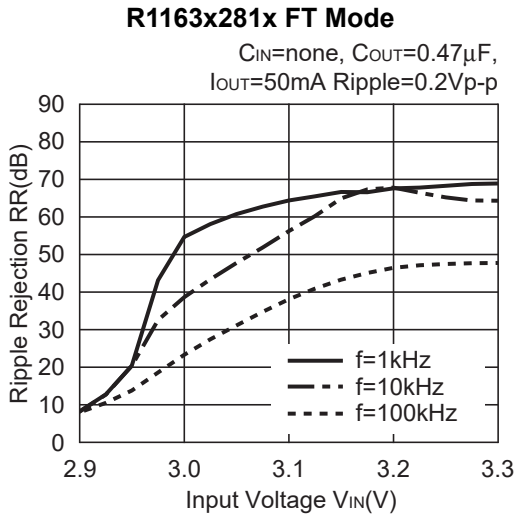
9) Dropout Voltage vs. Set Output Voltage



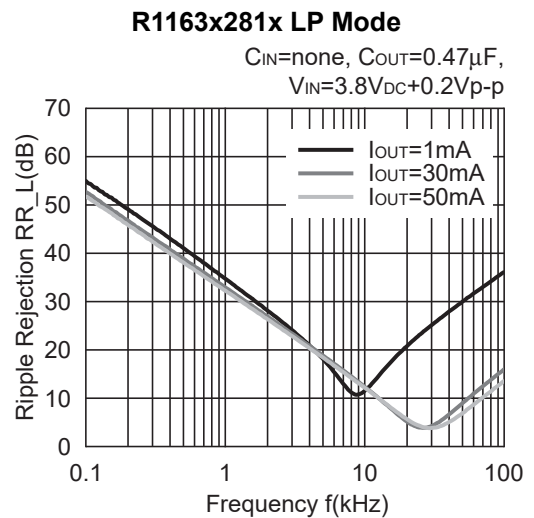
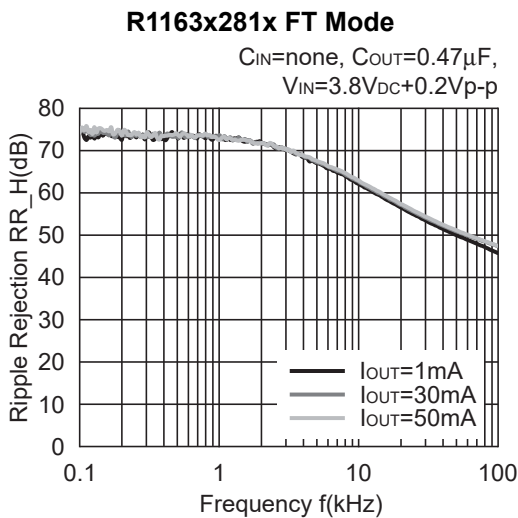
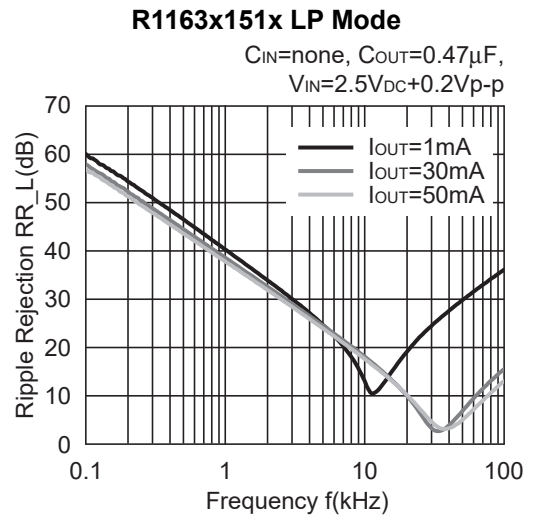
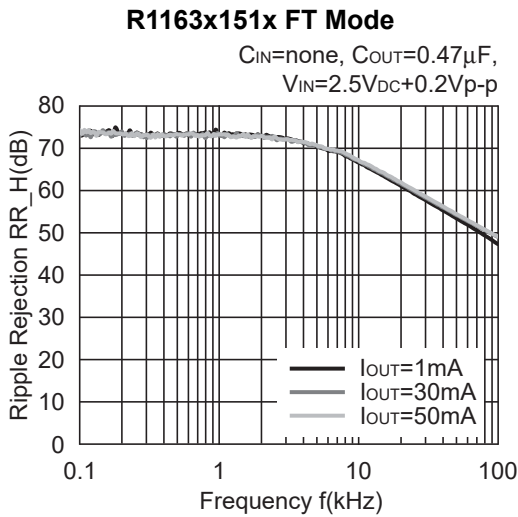
10) Ripple Rejection vs. Input Bias Voltage



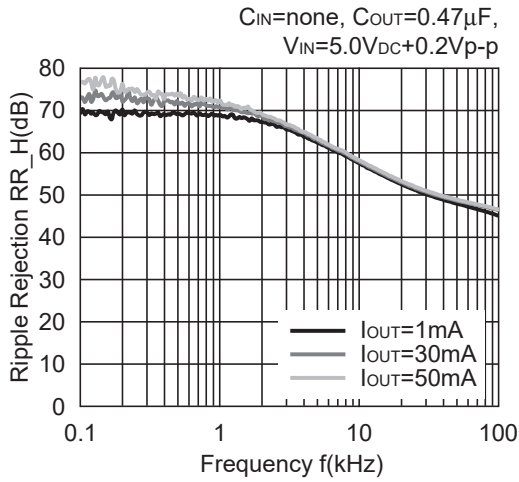
**R1163x**



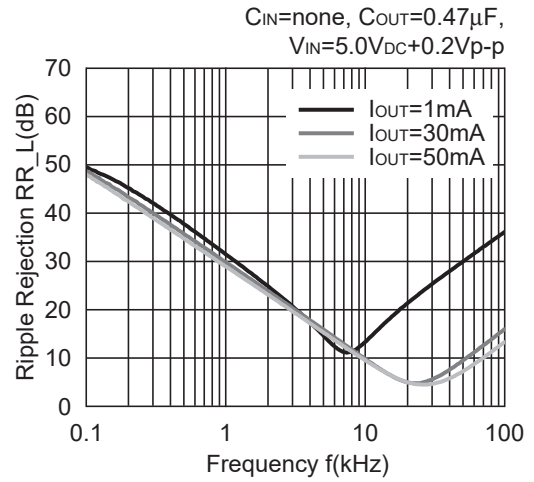
**11) Ripple Rejection vs. Frequency**



**R1163x401x FT Mode**

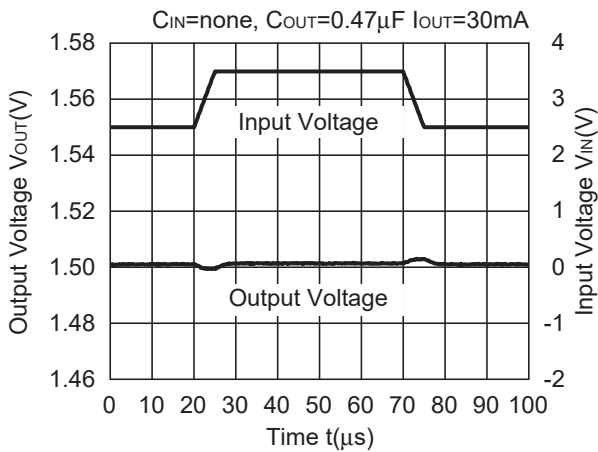


**R1163x401x LP Mode**

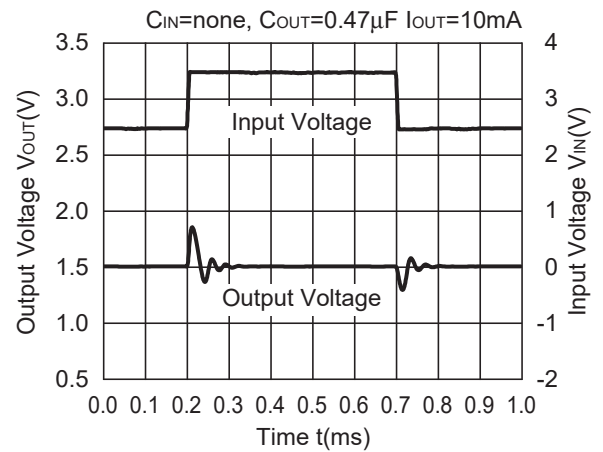


**12) Input Transient Response**

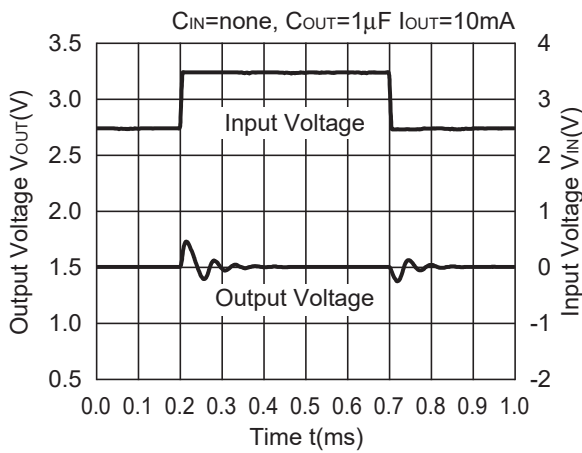
**R1163x151x FT Mode**



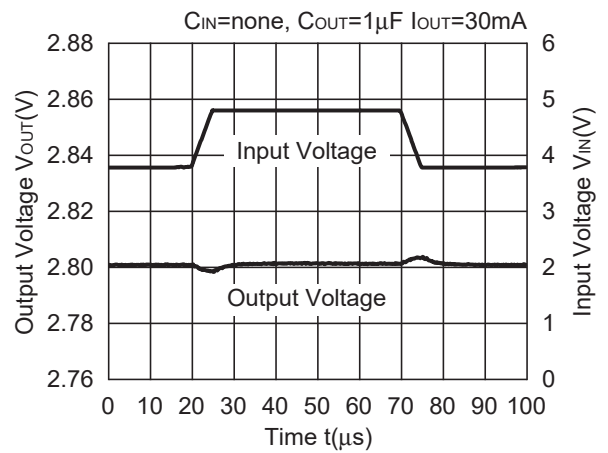
**R1163x151x LP Mode**



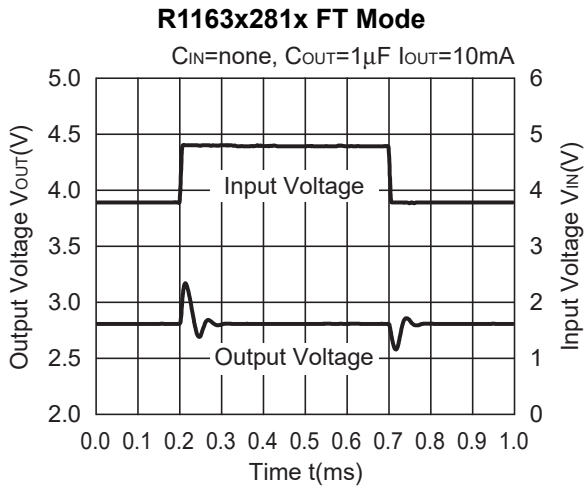
**R1163x151x LP Mode**



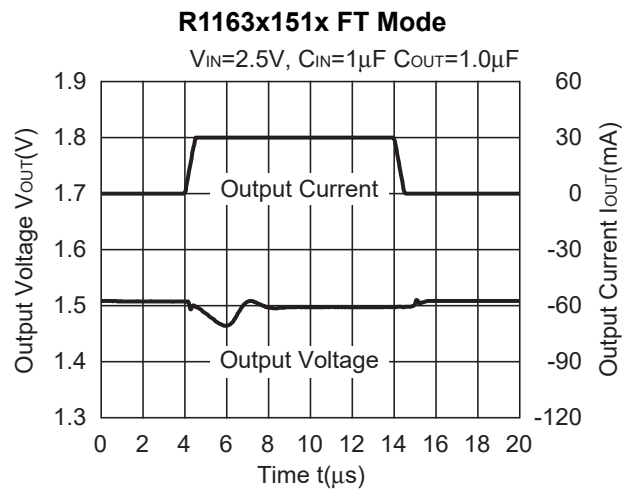
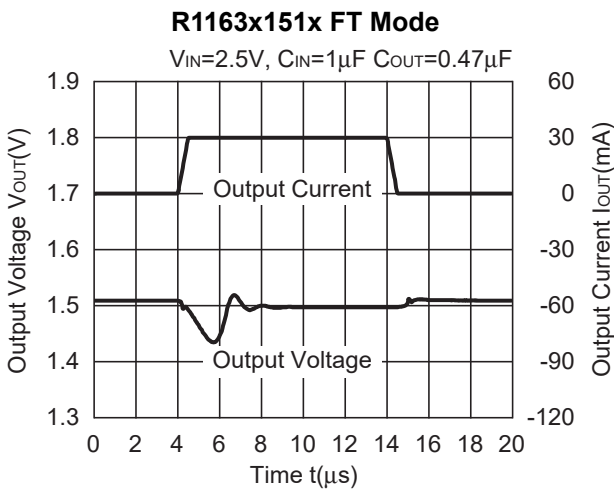
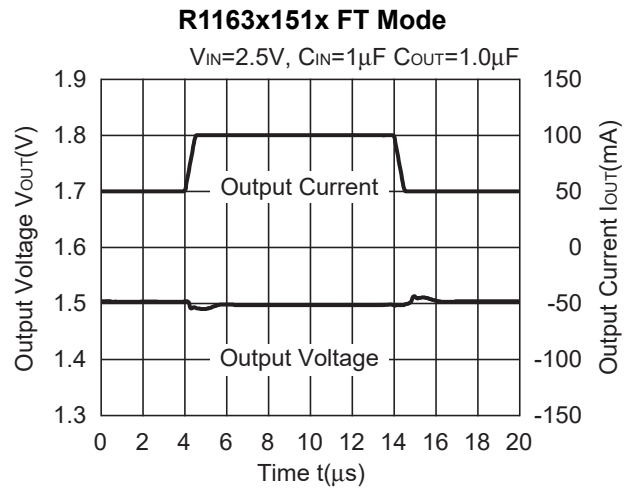
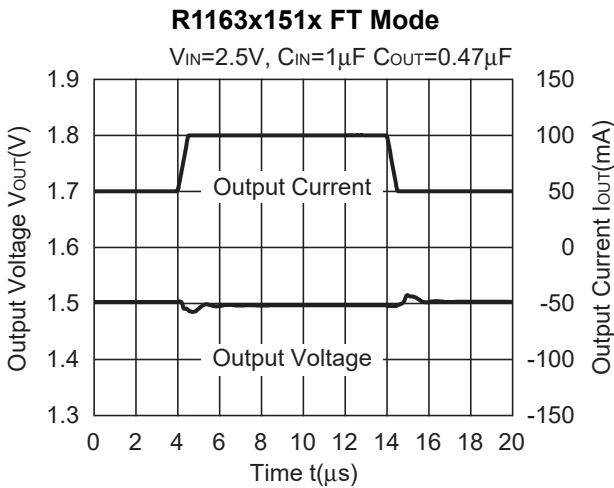
**R1163x281x FT Mode**

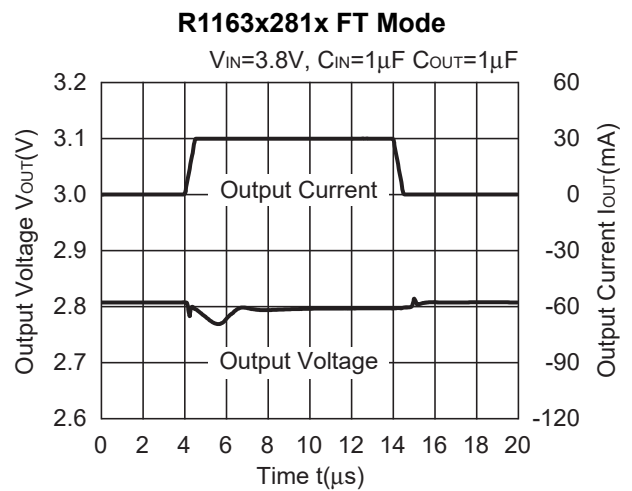
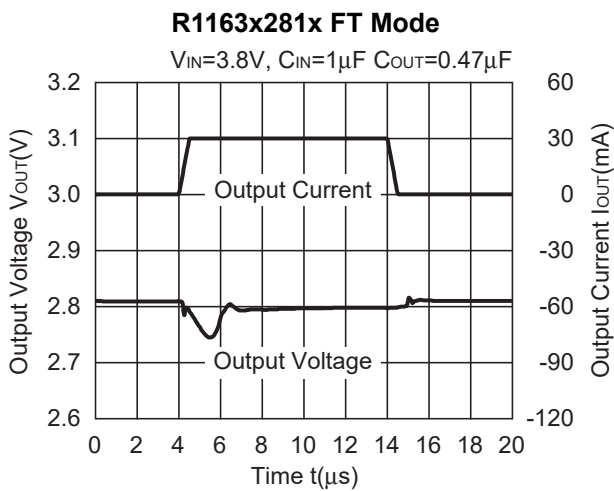
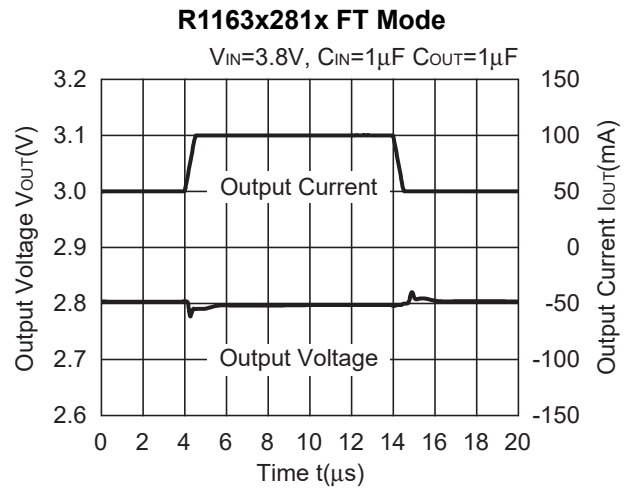
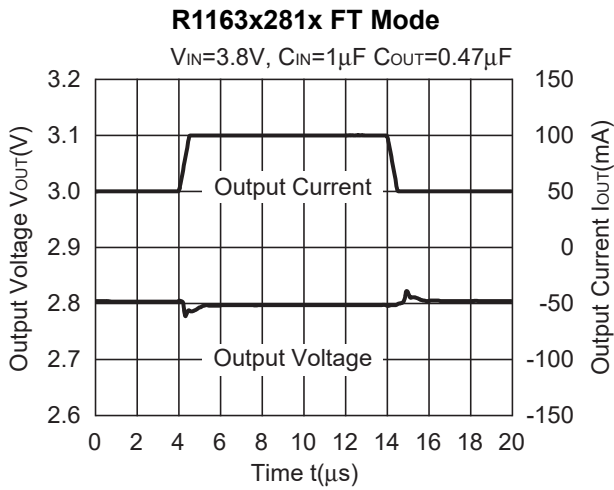
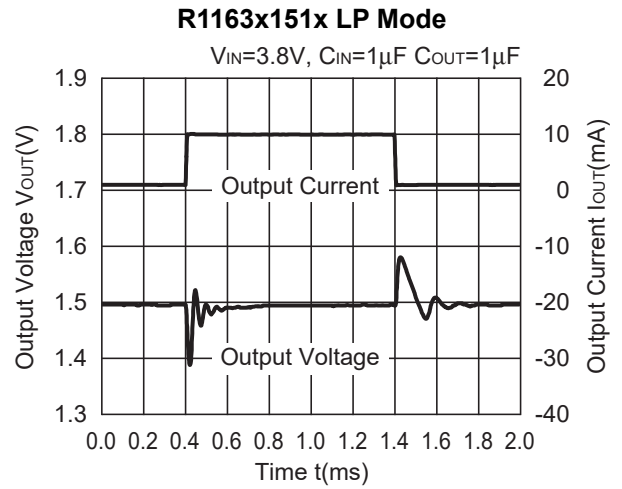
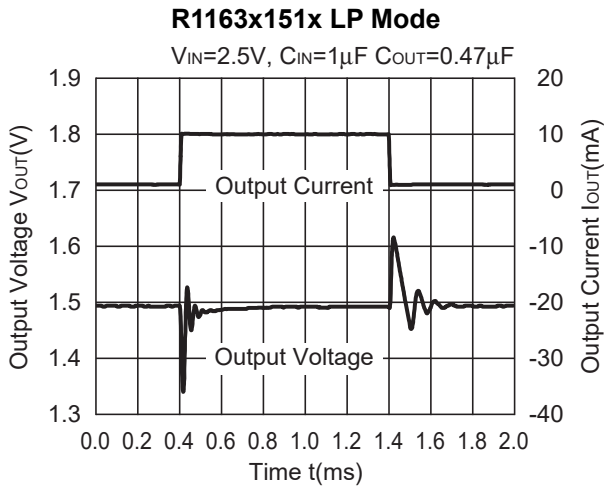


**R1163x**

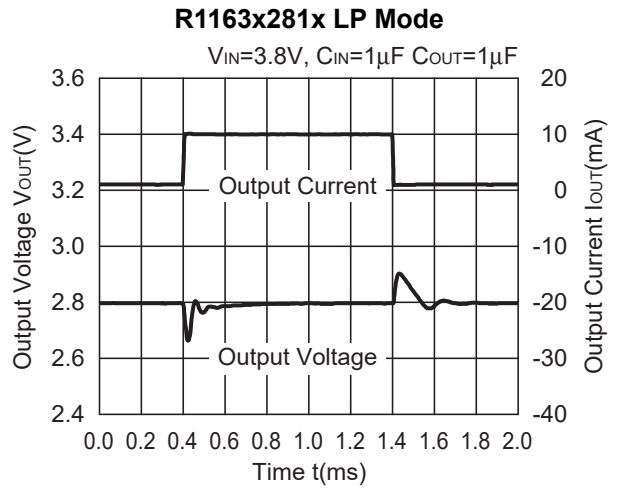
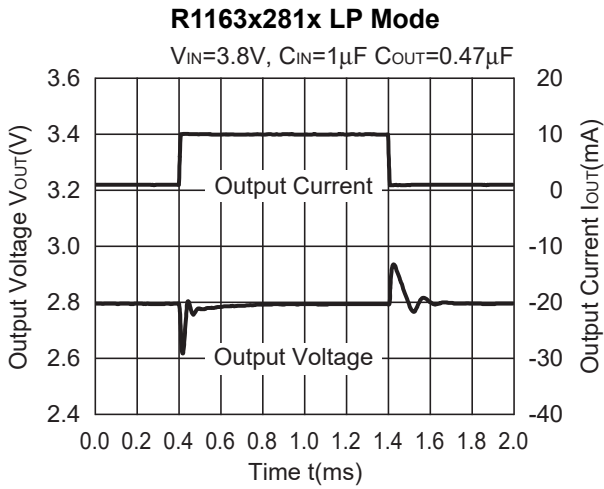


**13) Load Transient Response**

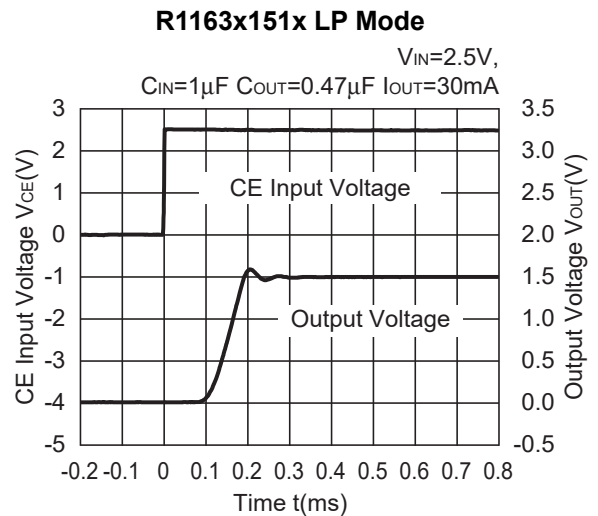
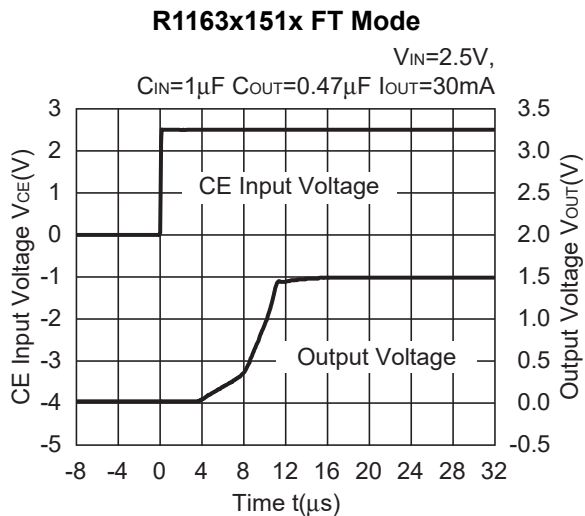
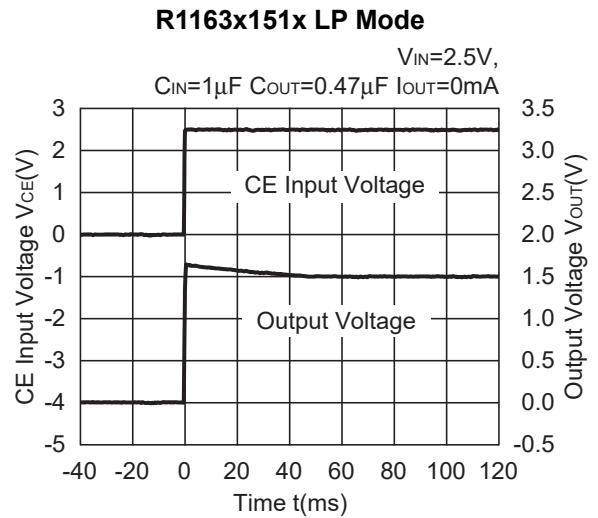
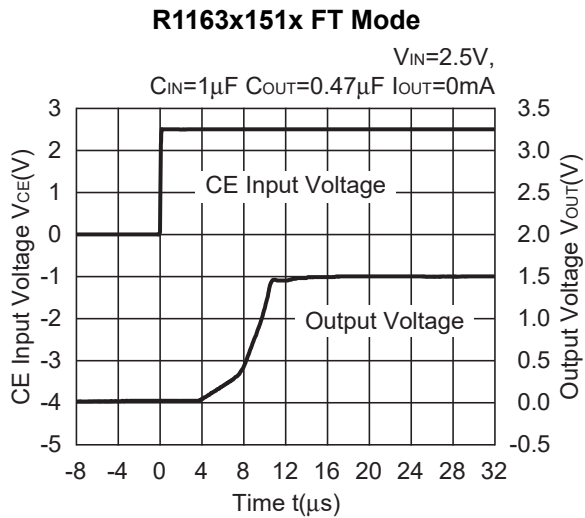




**R1163x**

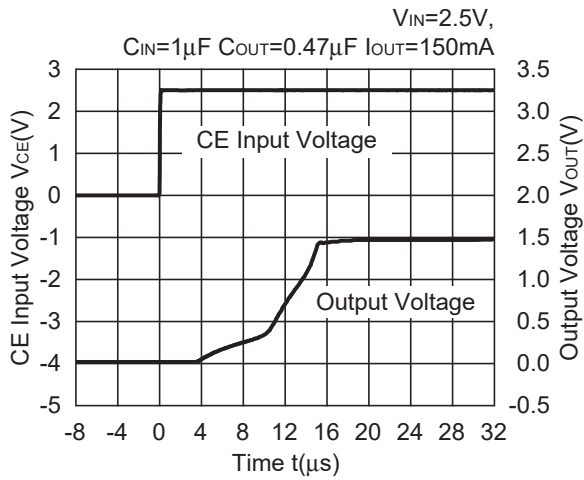


**14) Turn on speed with CE pin**

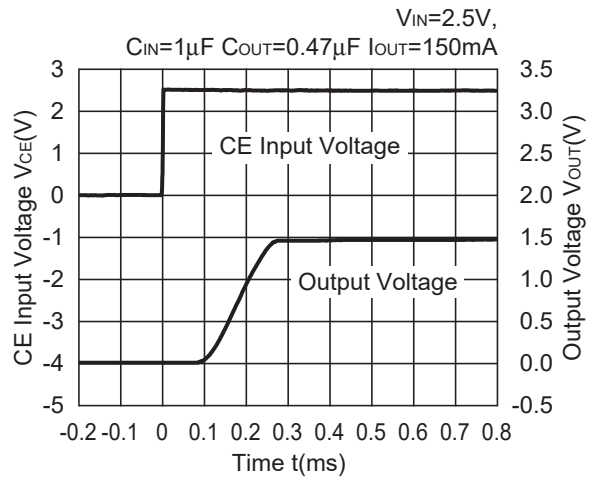




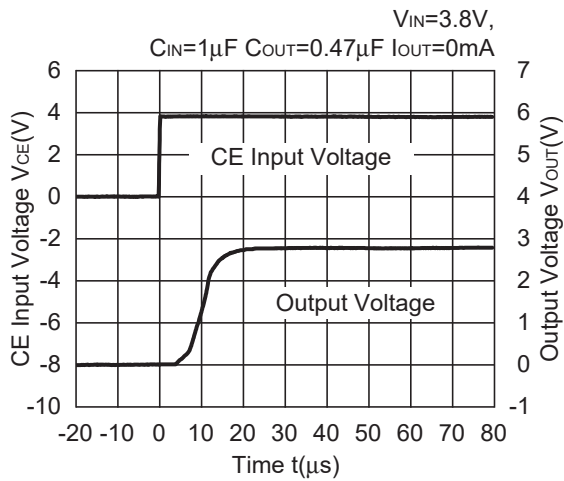
**R1163x151x FT Mode**



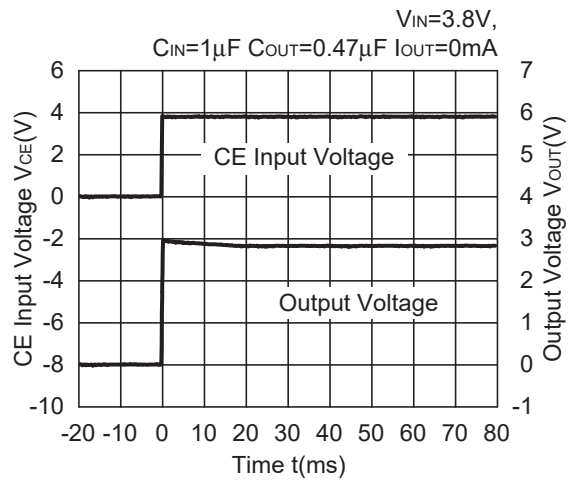
**R1163x151x LP Mode**



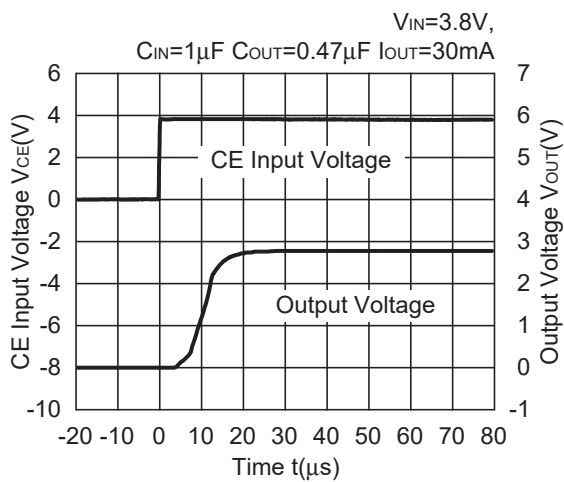
**R1163x281x FT Mode**



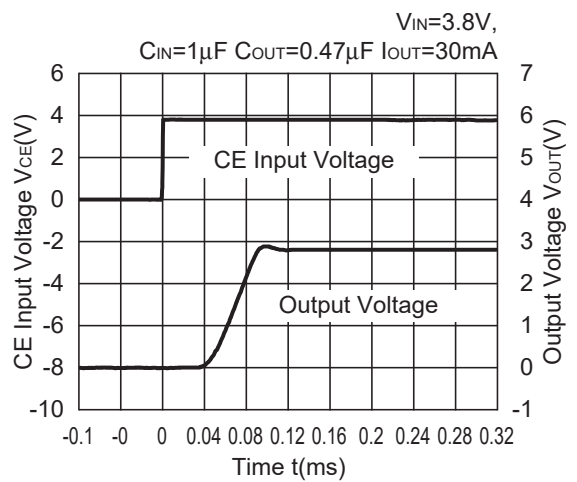
**R1163x281x LP Mode**



**R1163x281x FT Mode**

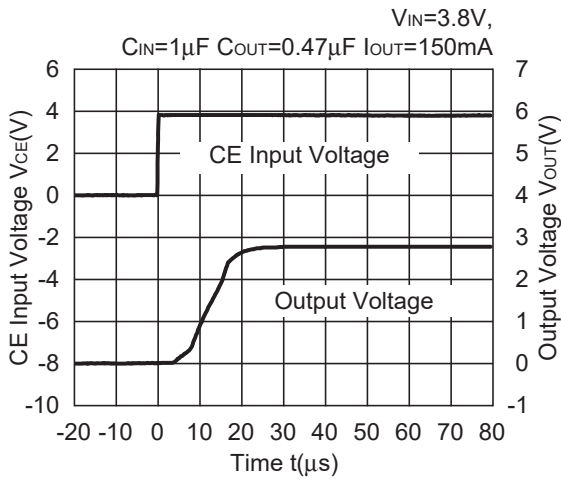


**R1163x281x LP Mode**

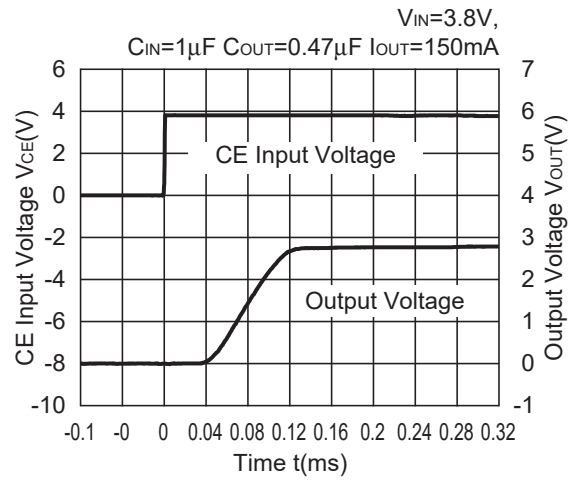


**R1163x**

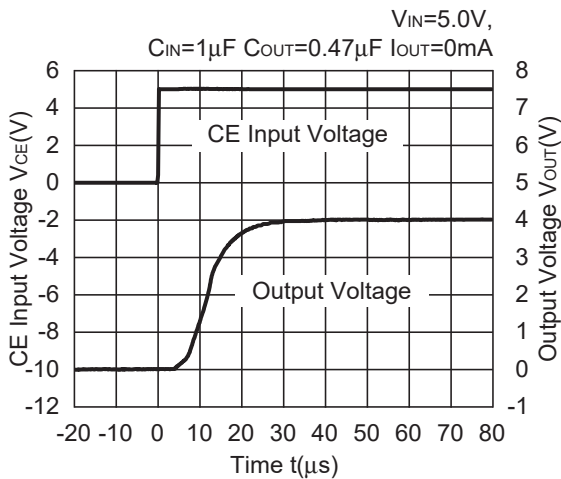
**R1163x281x FT Mode**



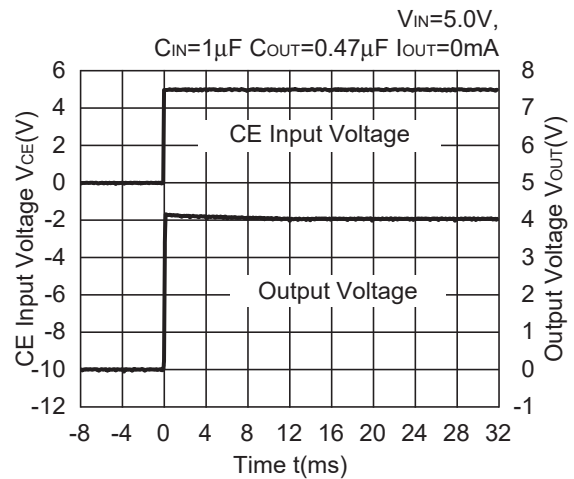
**R1163x281x LP Mode**



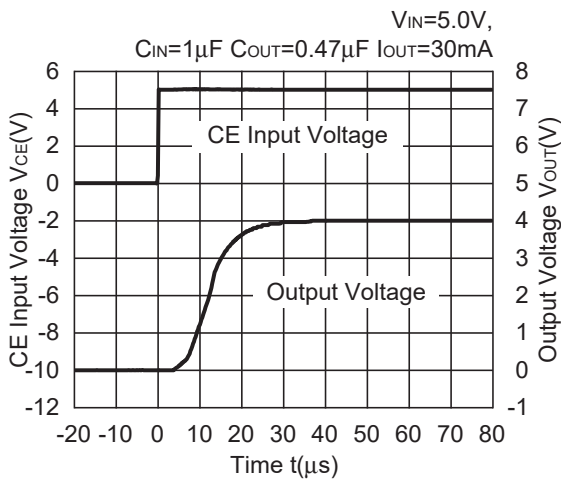
**R1163x401x FT Mode**



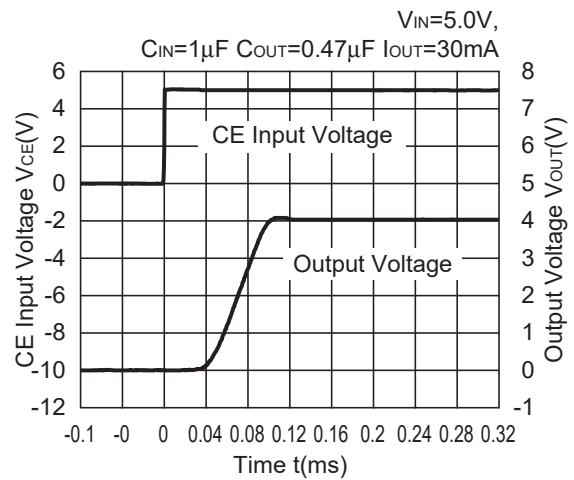
**R1163x401x LP Mode**



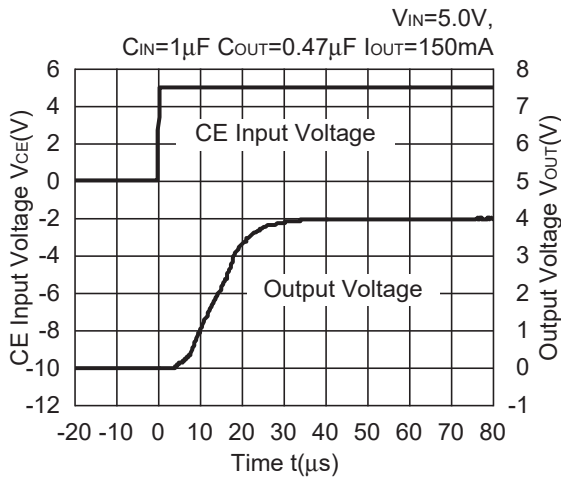
**R1163x401x FT Mode**



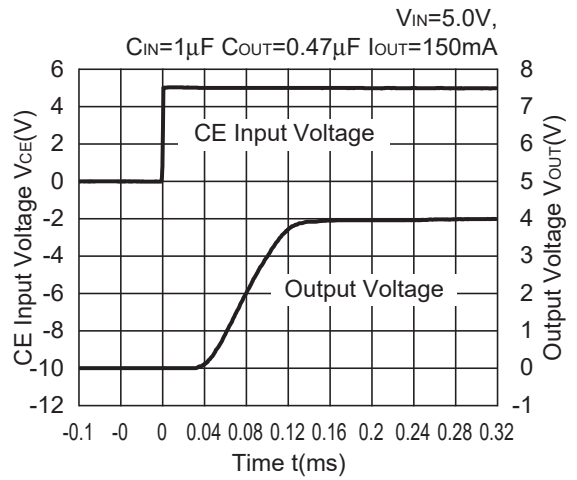
**R1163x401x LP Mode**



**R1163x401x FT Mode**

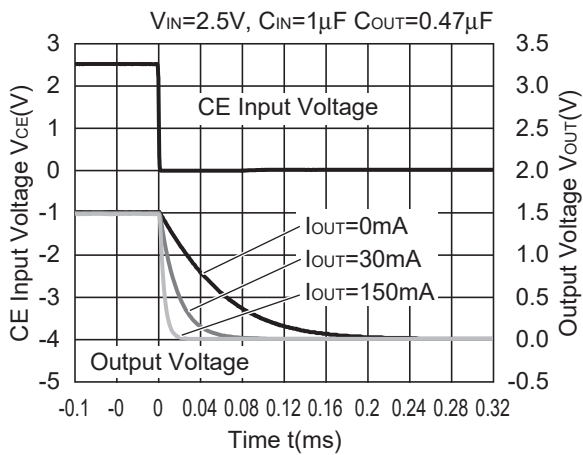


**R1163x401x LP Mode**

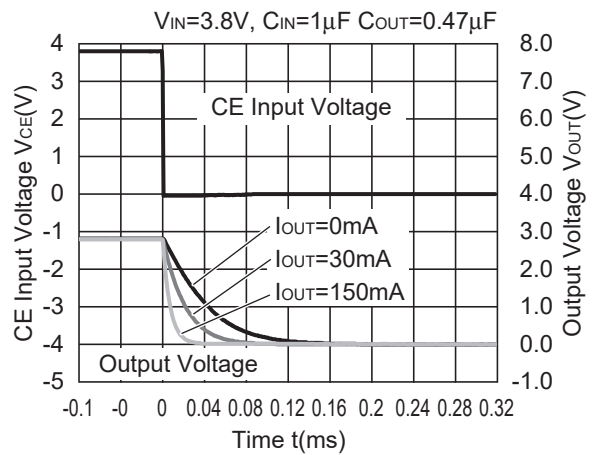


**15) Turn off speed with CE pin**

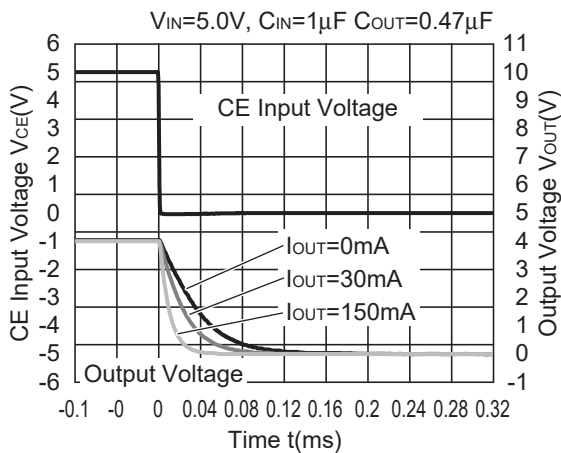
**R1163x151xD**



**R1163x281xD**



**R1163x401xD**

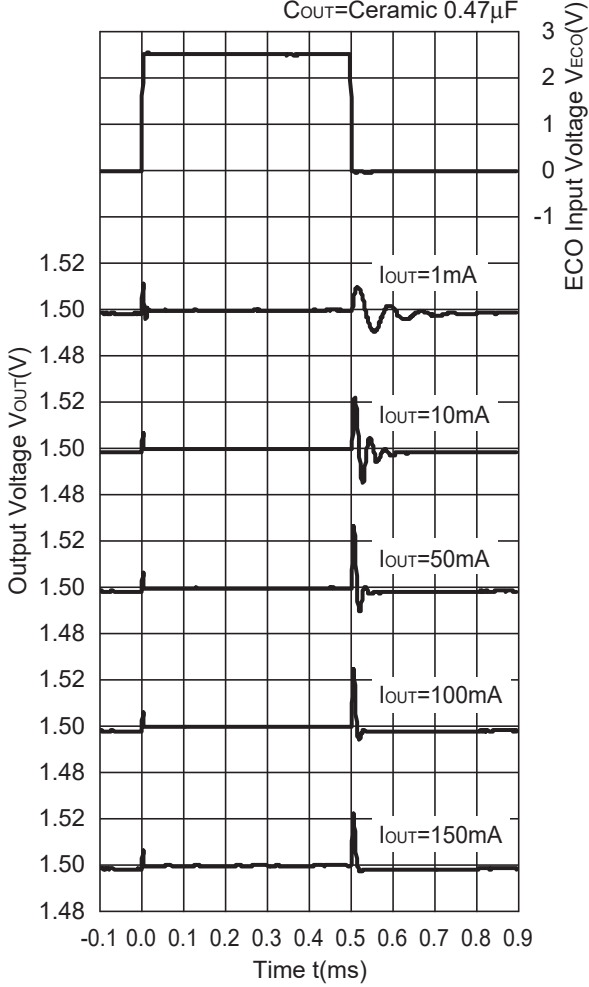


**R1163x**

**16) Output Voltage at Mode alternative point**

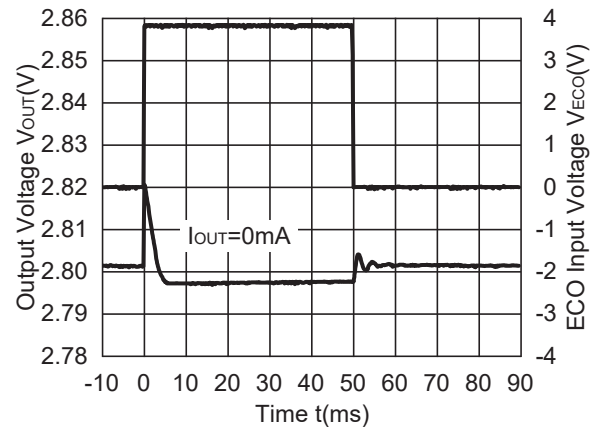
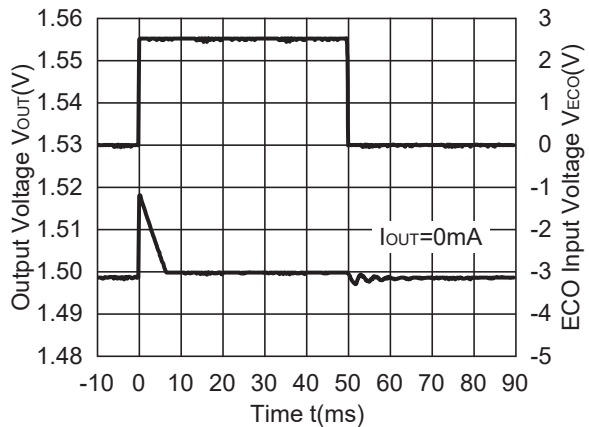
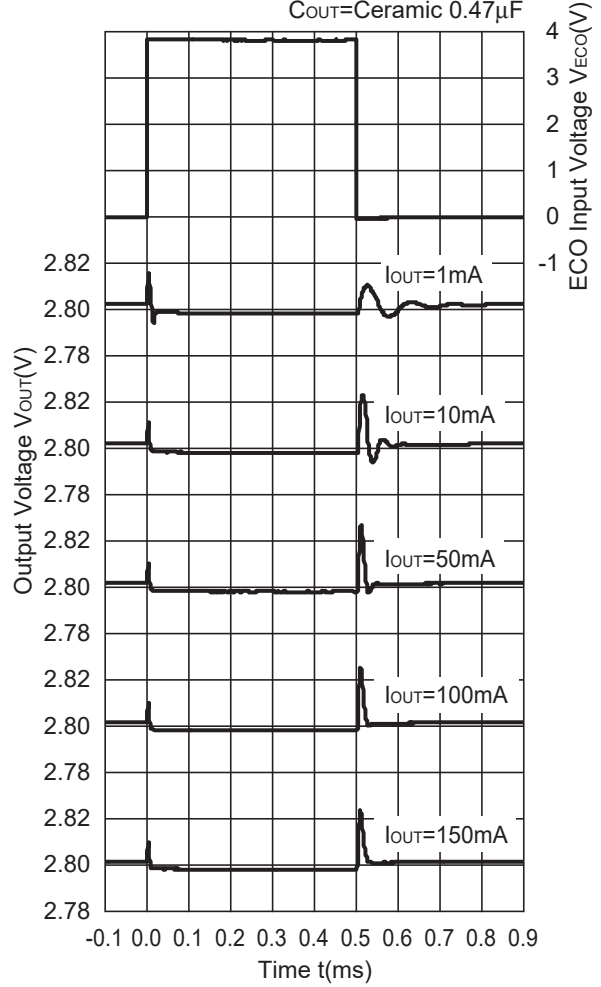
**R1163x151B/D**

$V_{IN}=2.5V$ ,  $C_{IN}=\text{Ceramic } 1.0\mu F$ ,  
 $C_{OUT}=\text{Ceramic } 0.47\mu F$



**R1163x281B/D**

$V_{IN}=3.8V$ ,  $C_{IN}=\text{Ceramic } 1.0\mu F$ ,  
 $C_{OUT}=\text{Ceramic } 0.47\mu F$



## TECHNICAL NOTES

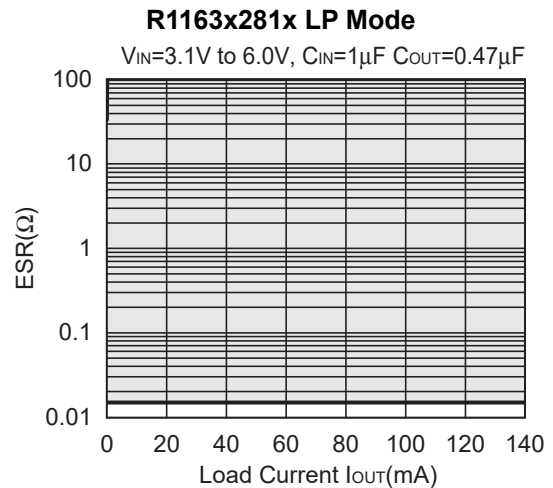
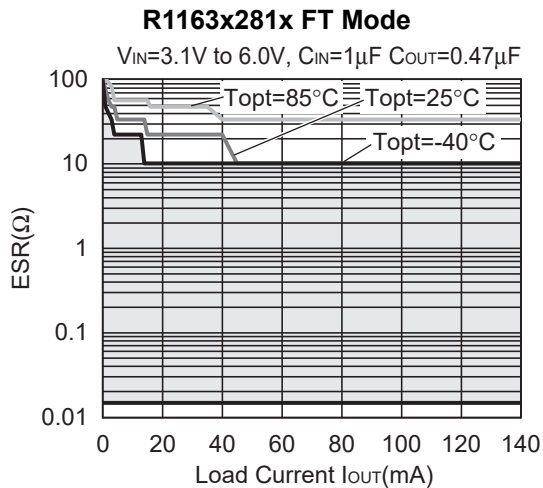
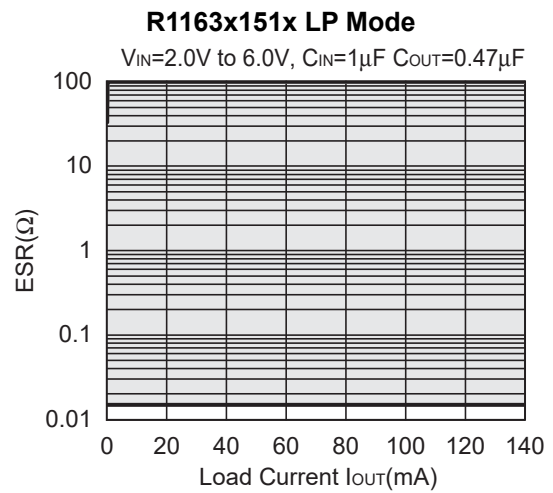
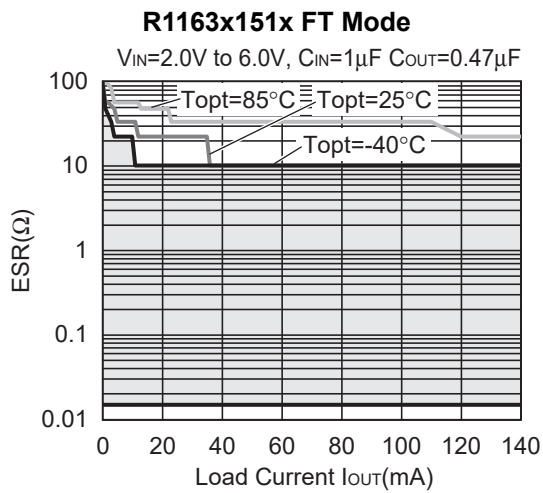
When using these ICs, consider the following points:

In these ICs, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, be sure to use a capacitor  $C_{OUT}$  with good frequency characteristics and ESR (Equivalent Series Resistance) in the range described as follows:

The relations between  $I_{OUT}$  (Output Current) and ESR of Output Capacitor are shown below. The conditions when the white noise level is under  $40\mu\text{V}$  (Avg.) are marked as the hatched area in the graph.

### <Test conditions>

#### (1) Frequency band: 10Hz to 2MHz





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