

Description

The HSP6024A is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

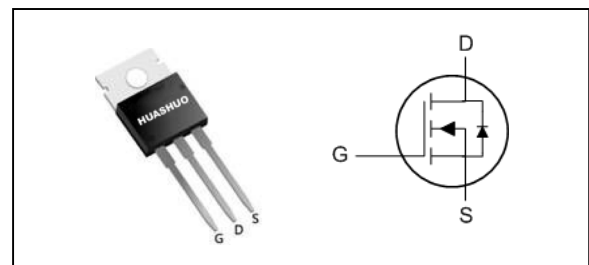
The HSP6024A meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

- Super Low Gate Charge
- 100% EAS Guaranteed
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Product Summary

V_{DS}	60	V
$R_{DS(ON),max}$	4.8	m Ω
I_D	200	A

TO220 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current ¹	200	A
$I_D@T_C=25^\circ C$	Continuous Drain Current ⁶	120	A
$I_D@T_C=100^\circ C$	Continuous Drain Current ^{1,6}	140	A
I_{DM}	Pulsed Drain Current ²	340	A
EAS	Single Pulse Avalanche Energy ³	245	mJ
I_{AS}	Avalanche Current	70	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	260	W
$P_D@T_A=25^\circ C$	Total Power Dissipation ⁴	2.02	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	0.45	$^\circ C/W$



Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	60	---	---	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =30A	---	3.8	4.8	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	2.5	---	4.5	V
I _{DSS}	Drain-Source Leakage Current	V _{DS} =48V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =48V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =30A	---	50	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	1.4	---	Ω
Q _g	Total Gate Charge (10V)	V _{DS} =48V, V _{GS} =10V, I _D =15A	---	83.7	---	nC
Q _{gs}	Gate-Source Charge		---	28.6	---	
Q _{gd}	Gate-Drain Charge		---	29.3	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =30V, V _{GS} =10V, R _G =3.3Ω, I _D =48A	---	38.1	---	ns
T _r	Rise Time		---	73.3	---	
T _{d(off)}	Turn-Off Delay Time		---	51.6	---	
T _f	Fall Time		---	26.1	---	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	5580	---	pF
C _{oss}	Output Capacitance		---	571	---	
C _{rss}	Reverse Transfer Capacitance		---	278	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	80	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V
t _{rr}	Reverse Recovery Time	I _F =30A, di/dt=100A/μs,	---	30	---	nS
Q _{rr}	Reverse Recovery Charge	T _J =25°C	---	55	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V_{DD}=50V,V_{GS}=10V,L=0.1mH,I_{AS}=70A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.
- 6.Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.



Typical Characteristics

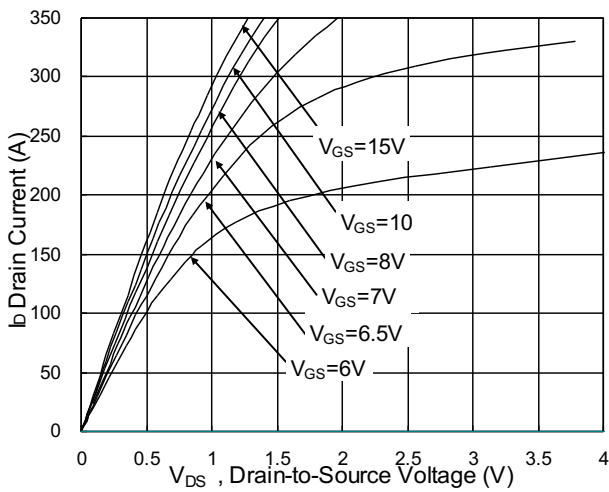


Fig.1 Typical Output Characteristics

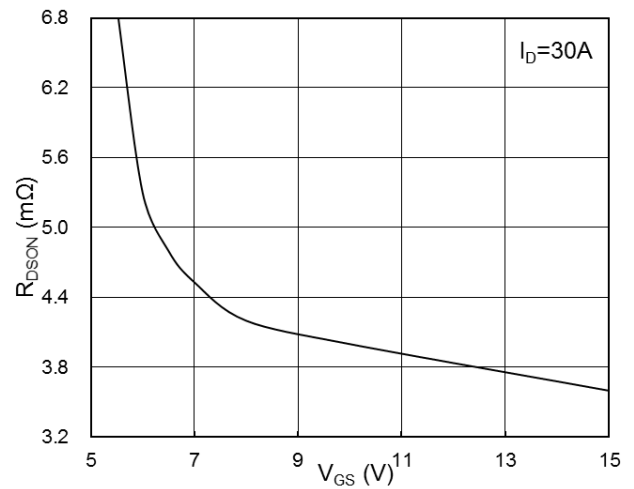


Fig.2 On-Resistance vs. G-S Voltage

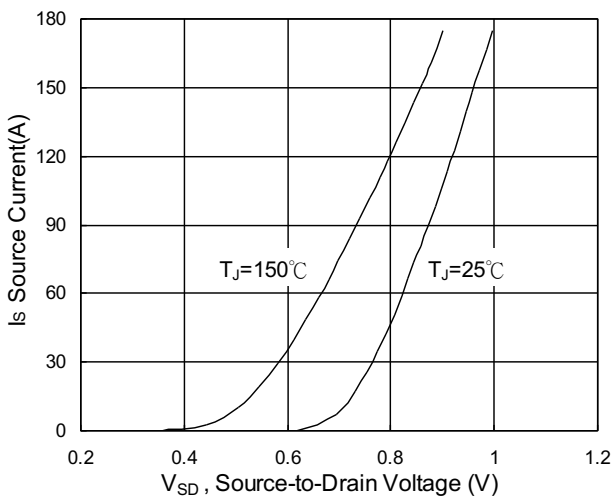


Fig.3 Source Drain Forward Characteristics

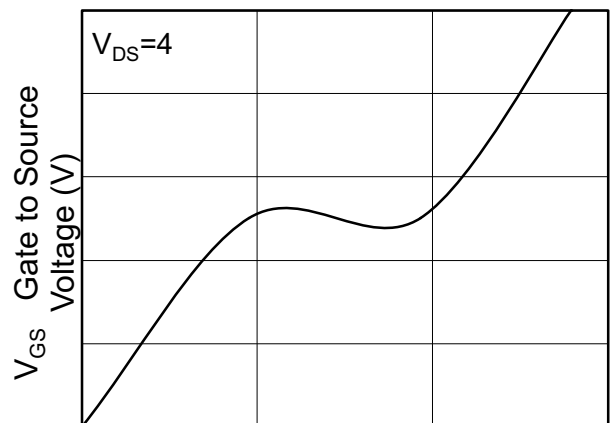


Fig.4 Gate-Charge Characteristics

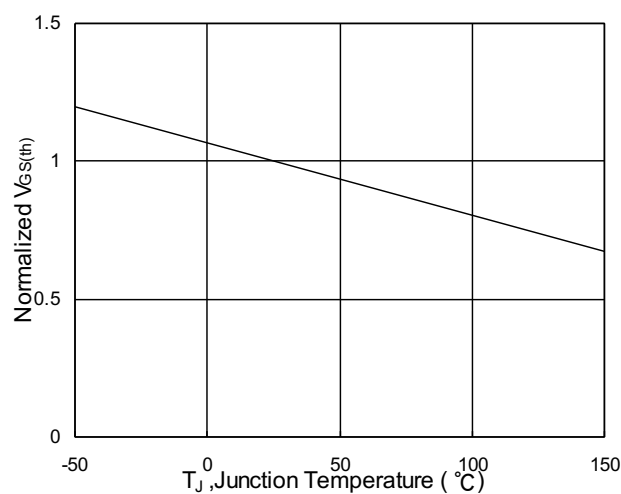


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

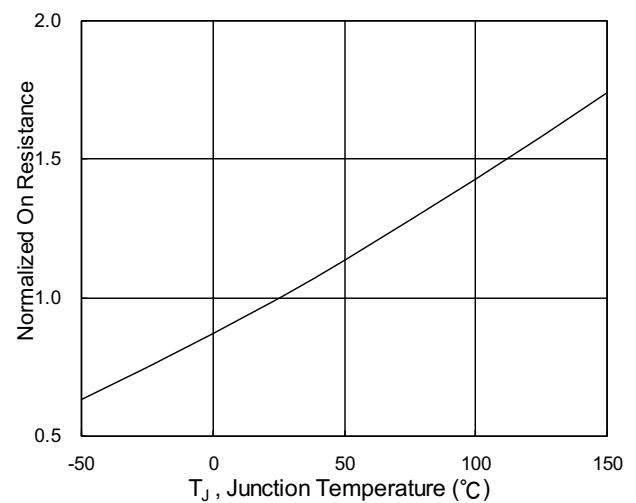


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

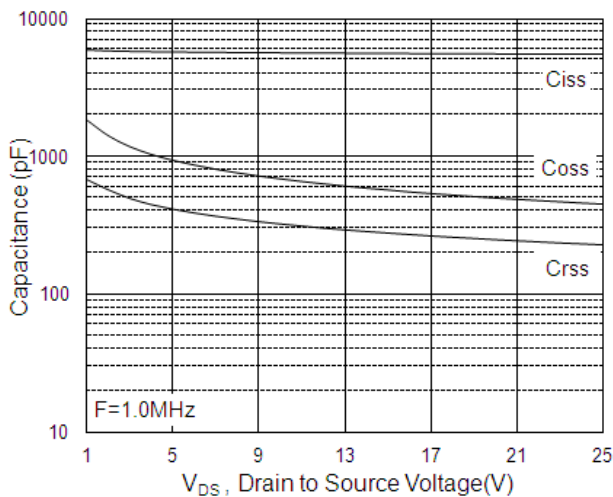


Fig.7 Capacitance

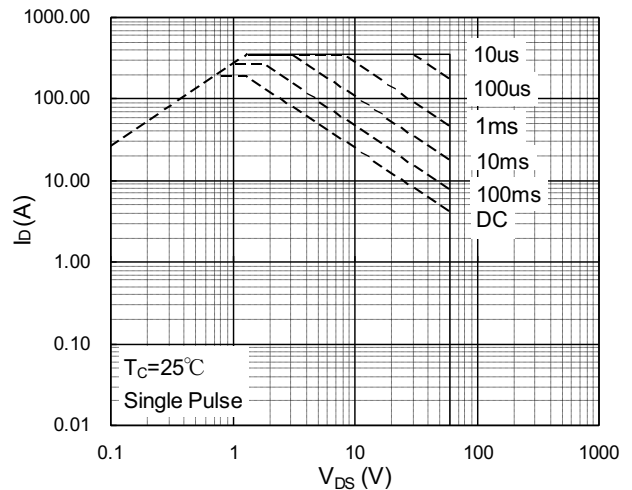


Fig.8 Safe Operating Area

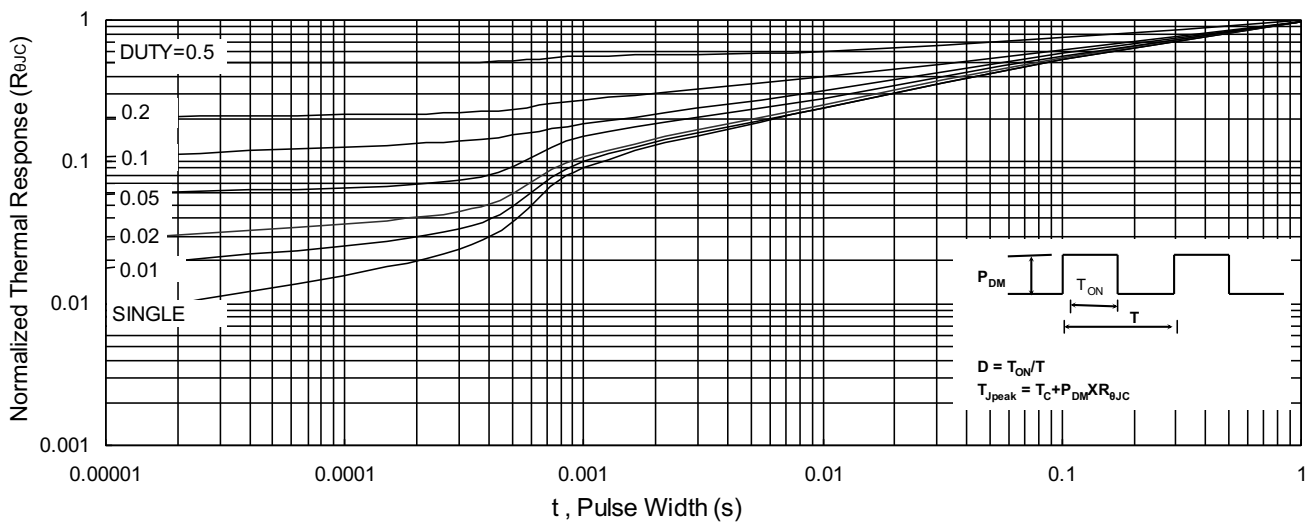


Fig.9 Normalized Maximum Transient Thermal Impedance

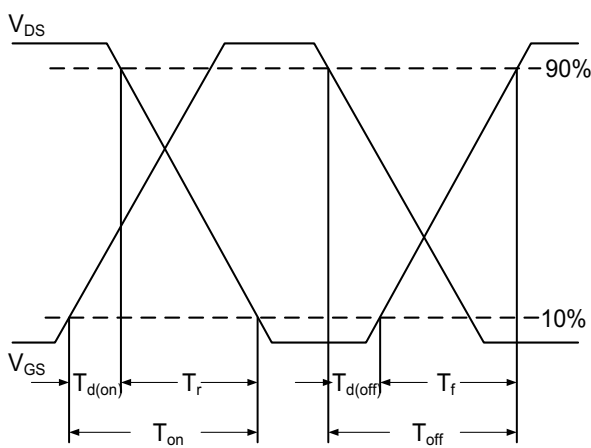


Fig.10 Switching Time Waveform

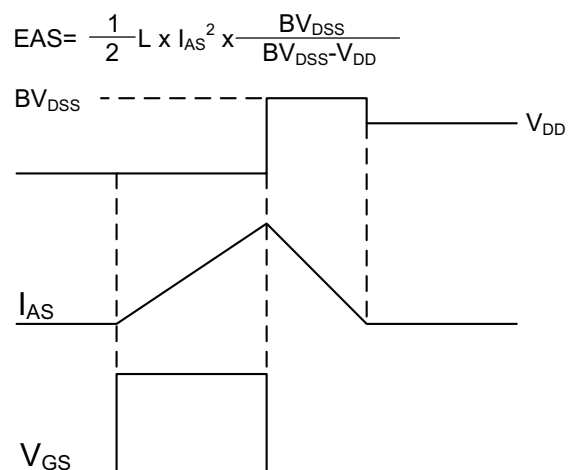


Fig.11 Unclamped Inductive Switching