#### SN54F109, SN74F109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

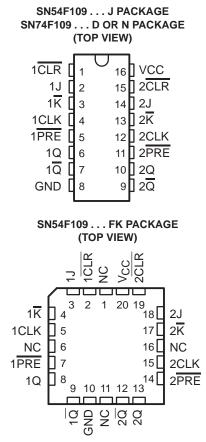
SDFS047A - MARCH 1987 - REVISED OCTOBER 1993

#### Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

### description

These devices contain two independent  $J-\overline{K}$ positive-edge-triggered flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When  $\overline{PRE}$  and  $\overline{CLR}$  are inactive (high), data at the J and  $\overline{K}$  input meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and  $\overline{K}$  inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding  $\overline{K}$  and trying J high. They also can perform as D-type flip-flops if J and  $\overline{K}$  are tied together.

The SN54F109 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74F109 is characterized for operation from 0°C to 70°C.



NC - No internal connection

		FUNC		ADLE			
		INPUTS			OUTPUTS		
PRE	CLR	CLK	J	ĸ	Q	Q	
L	Н	Х	Х	Х	Н	L	
н	L	Х	Х	Х	L	н	
L	L	Х	Х	Х	H‡	H‡	
н	Н	$\uparrow$	L	L	L	Н	
н	Н	$\uparrow$	Н	L	Тор	gle	
н	Н	$\uparrow$	L	Н	Q <sub>0</sub>	Q <sub>0</sub>	
н	Н	$\uparrow$	Н	Н	н	L	
н	Н	L	Х	Х	Q <sub>0</sub>	$\overline{Q}_0$	

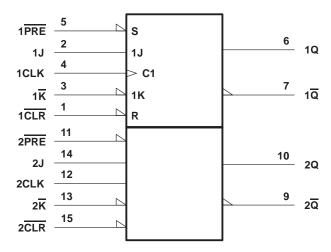
FUNCTION TABLE

<sup>†</sup> The output levels are not guaranteed to meet the minimum levels for V<sub>OH</sub>. Furthermore, this configuration is nonstable; that is, it will not persist when PRE or CLR returns to its inactive (high) level.

## SN54F109, SN74F109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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#### logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–1.2 V to 7 V
Input current range	30 mA to 5 mA
Voltage range applied to any output in the high state	$\dots$ -0.5 V to V <sub>CC</sub>
Current into any output in the low state	40 mA
Operating free-air temperature range: SN54F109	−55°C to 125°C
SN74F109	0°C to 70°C
Storage temperature range	. −65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

#### recommended operating conditions

		S	N54F109	Ð	S	SN74F109				
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT		
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
VIH	High-level input voltage	2			2			V		
VIL	Low-level input voltage			0.8			0.8	V		
IIK	Input clamp current			-18			-18	mA		
IOH	High-level output current			- 1			- 1	mA		
IOL	Low-level output current			20			20	mA		
TA	Operating free-air temperature	-55		125	0		70	°C		



## SN54F109, SN74F109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

D		TEO	S	N54F10	9	S	•	UNIT		
F/	ARAMETER	TES	MIN	TYP†	MAX	MIN	TYP <sup>†</sup>	MAX	UNIT	
VIK		V <sub>CC</sub> = 4.5 V,	lı = – 18 mA			-1.2			-1.2	V
Varia		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = – 1 mA	2.5	3.4		2.5	3.4		V
VOH		V <sub>CC</sub> = 4.75 V,	I <sub>OH</sub> = – 1 mA				2.7			v
VOL		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 20 mA		0.3	0.5		0.3	0.5	V
Ц		V <sub>CC</sub> = 5.5 V,	$V_{I} = 7 V$			0.1			0.1	mA
IIH		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20			20	μA
lu.	J, <del>K</del> , CLK		V <sub>1</sub> = 0.5 V			- 0.6			- 0.6	mA
۱	PRE or CLR	V <sub>CC</sub> = 5.5 V,	v] = 0.5 v			- 1.8			- 1.8	mA
los‡		V <sub>CC</sub> = 5.5 V,	$V_{O} = 0$	-60		-150	-60		-150	mA
ICC		V <sub>CC</sub> = 5.5 V,	See Note 2		11.7	17		11.7	17	mA

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

\* Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. NOTE 2: I<sub>CC</sub> is measured with J, K, CLK, and PRE grounded then with J, K, CLK, and CLR grounded.

#### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			T <sub>A</sub> = 2	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C ′F74		F109	SN74	F109	UNIT
			MIN MAX MIN MAX MI				MIN	MAX	
f <sub>clock</sub> Clock frequency			0	100	0	70	0	90	MHz
÷	Pulse duration	CLK high, PRE or CLR low	4		4		4		-
t <sub>W</sub>		CLK low	5		5		5		ns
		High	3		3		3		
t <sub>su</sub>	Setup time, data before CLK↑	Low	3		3		3		ns
	Setup time, inactive-state before CLK <sup>\$</sup>	PRE or CLR to CLK	2		2		2		
÷.	Hold time, data after CLK <sup>↑</sup>	High	1		1		1		
th		Low	1		1		1		ns

§ Inactive-state setup time is also referred to as recovery time.

#### switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>I</sub> RI	CC = 5 V L = 50 p L = 500 9 A = 25°C	<b>F,</b> Ω,	CL RL	= 50 pF = 500 Ω		V,	UNIT
		, ,	′F109			SN54	F109	SN74F109		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax			100	150		70		90		MHz
<sup>t</sup> PLH	CLK	Q or $\overline{Q}$	3	4.9	7	3	9	3	8	ns
<sup>t</sup> PHL	CLK		3.6	5.8	8	3.6	10.5	3.6	9.2	115
<sup>t</sup> PLH	PRE or CLR	Q or $\overline{Q}$	2.4	4.8	7	2.4	9	2.4	8	ns
<sup>t</sup> PHL	FRE OF CER	2012	2.7	6.6	9	2.7	11.5	2.7	10.5	115

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 3: Load circuits and waveforms are shown in Section 1.





## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9758001Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9758001Q2A SNJ54F 109FK	Samples
5962-9758001QEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9758001QE A SNJ54F109J	Samples
5962-9758001QFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9758001QF A SNJ54F109W	Samples
JM38510/34102B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34102B2A	Samples
JM38510/34102BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34102BEA	Samples
JM38510/34102BFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34102BFA	Samples
M38510/34102B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34102B2A	Samples
M38510/34102BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34102BEA	Samples
M38510/34102BFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34102BFA	Samples
SN74F109D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F109	Samples
SN74F109DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F109	Samples
SN74F109N	ACTIVE	PDIP	Ν	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74F109N	Samples
SNJ54F109FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9758001Q2A SNJ54F 109FK	Samples
SNJ54F109J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9758001QE A SNJ54F109J	Samples



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54F109W	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9758001QF A SNJ54F109W	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(<sup>5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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#### OTHER QUALIFIED VERSIONS OF SN54F109, SN74F109 :



• Catalog : SN74F109

Military : SN54F109

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

## PACKAGE MATERIALS INFORMATION

Texas Instruments

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### TAPE AND REEL INFORMATION





### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal	

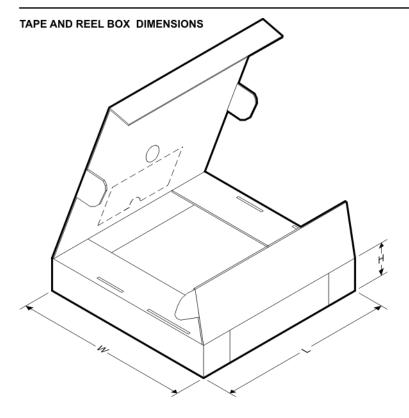
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F109DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1



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## PACKAGE MATERIALS INFORMATION

3-Aug-2021



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F109DR	SOIC	D	16	2500	340.5	336.1	32.0

LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N\*\*) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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# D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) –16x0,55 -14x1,27 -14x1,27 16x1,50 5,40 5.40 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 .55 Example 1. Solder Mask Opening (See Note E) -0,07 All Around

NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16



J (R-GDIP-T\*\*) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



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