4.5 Ω R_{ON}, Triple/Quad SPDT ±5 V, +12 V, +5 V, and +3.3 V Switches

Data Sheet

ADG1633/ADG1634

FEATURES

- 4.5 Ω typical on resistance
- 1 Ω on-resistance flatness
- Up to 206 mA continuous current
- ±3.3 V to ±8 V dual-supply operation
- 3.3 V to 16 V single-supply operation
- No V_L supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation

ADG1633

- 16-lead TSSOP and 16-lead, 3 mm × 3 mm LFCSP

ADG1634

- 20-lead TSSOP and 20-lead, 4 mm × 4 mm LFCSP

APPLICATIONS

- Communication systems
- Medical systems
- Audio signal routing
- Video signal routing
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Relay replacements

GENERAL DESCRIPTION

The ADG1633 and ADG1634 are monolithic industrial CMOS (*i*CMOS®) analog switches comprising three independently selectable single-pole, double-throw (SPDT) switches and four independently selectable SPDT switches, respectively.

All channels exhibit break-before-make switching action that prevents momentary shorting when switching channels. An $\overline{EN}$ input on the ADG1633 (LFCSP and TSSOP packages) and ADG1634 (LFCSP package only) is used to enable or disable the devices. When disabled, all channels are switched off.

The ultralow on resistance and on-resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications, where low distortion is critical. *i*CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

FUNCTIONAL BLOCK DIAGRAMS

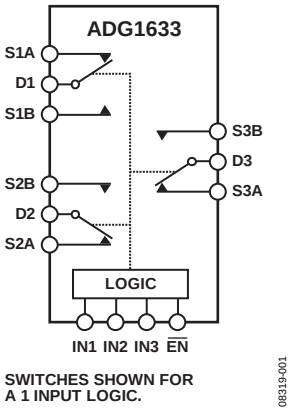

Figure 1. ADG1633 TSSOP and LFCSP

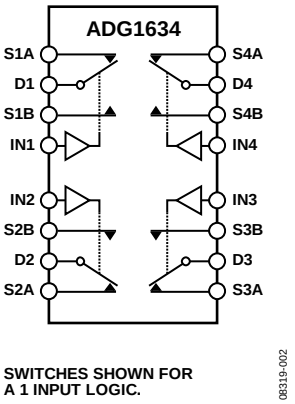

Figure 2. ADG1634 TSSOP

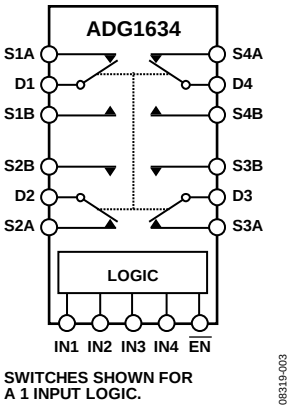

Figure 3. ADG1634 LFCSP

Rev. B

Document Feedback

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9/2014—Rev. 0 to Rev. A

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Updated Outline Dimensions 17
Changes to Ordering Guide 19

7/2009—Revision 0: Initial Version

SPECIFICATIONS

±5 V DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	4.5			Ω typ	V_S = ±4.5 V, I_S = −10 mA; see Figure 26
	5	7	8	Ω max	V_{DD} = ±4.5 V, V_{SS} = ±4.5 V
On-Resistance Match Between Channels (ΔR_{ON})	0.12			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	0.25	0.3	0.35	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	1			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	1.3	1.7	2	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = ±4.5 V, V_D = ±4.5 V; see Figure 27
	±0.1	±1.5	±12	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = ±4.5V, V_D = ±4.5 V; see Figure 27
	±0.15	±2	±20	nA max	
Channel On Leakage, I_D, I_S (On)	±0.02			nA typ	V_S = V_D = ±4.5 V; see Figure 28
	±0.15	±2	±20	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±1			nA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	8			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	161			ns typ	R_L = 300 Ω, C_L = 35 pF
	200	236	264	ns max	V_S = 2.5 V; see Figure 29
t_{ON} ($\overline{EN}$)	61			ns typ	R_L = 300 Ω, C_L = 35 pF
	79	88	98	ns max	V_S = 2.5 V; see Figure 31
t_{OFF} ($\overline{EN}$)	162			ns typ	R_L = 300 Ω, C_L = 35 pF
	199	232	259	ns max	V_S = 2.5 V; see Figure 31
Break-Before-Make Time Delay, t_D	44			ns typ	R_L = 300 Ω, C_L = 35 pF
			30	ns min	V_{S1} = V_{S2} = 2.5 V; see Figure 30
Charge Injection	−12.5			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 33
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 35
Total Harmonic Distortion + Noise (THD + N)	0.3			% typ	R_L = 110 Ω, V_S = 5 V p-p, f = 20 Hz to 20 kHz; see Figure 36
−3 dB Bandwidth	103			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 34
C_S (Off)	19			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	33			pF typ	V_S = 0 V, f = 1 MHz
C_D, C_S (On)	57			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
V_{DD}/V_{SS}			±3.3/±8	V min/max	

[1] Guaranteed by design, but not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	4			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 26
	4.5	6.5	7.5	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels (ΔR_{ON})	0.12			Ω typ	V_S = 10 V, I_S = −10 mA
	0.25	0.3	0.35	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.9			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	1.2	1.6	1.9	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 27
	±0.1	±1.5	±12	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 27
	±0.15	±2	±20	nA max	
Channel On Leakage, I_D, I_S (On)	±0.02			nA typ	V_S = V_D = 1 V or 10 V; see Figure 28
	±0.15	±2	±20	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±1			nA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	8			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	127			ns typ	R_L = 300 Ω, C_L = 35 pF
	151	182	205	ns max	V_S = 8 V; see Figure 29
t_{ON} ($\overline{EN}$)	31			ns typ	R_L = 300 Ω, C_L = 35 pF
	38	43	47	ns max	V_S = 8 V; see Figure 31
t_{OFF} ($\overline{EN}$)	128			ns typ	R_L = 300 Ω, C_L = 35 pF
	152	180	200	ns max	V_S = 8 V; see Figure 31
Break-Before-Make Time Delay, t_D	45			ns typ	R_L = 300 Ω, C_L = 35 pF
			30	ns min	V_{S1} = V_{S2} = 8 V; see Figure 30
Charge Injection	−12.4			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 33
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 35
Total Harmonic Distortion + Noise (THD + N)	0.3			% typ	R_L = 110 Ω, V_S = 5 V p-p, f = 20 Hz to 20 kHz; see Figure 36
−3 dB Bandwidth	109			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 34
C_S (Off)	19			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	32			pF typ	V_S = 6 V, f = 1 MHz
C_D, C_S (On)	56			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 12 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
TSSOP	300			μA typ	Digital inputs = 5 V
			480	μA max	
LFCSP	375			μA typ	Digital inputs = 5 V
			600	μA max	
V_{DD}			3.3/16	V min/max	

[1] Guaranteed by design, but not subject to production test.

5 V SINGLE SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	8.5			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA; see Figure 26
	10	12.5	14	Ω max	V_{DD} = 4.5 V, V_{SS} = 0 V
On-Resistance Match Between Channels (ΔR_{ON})	0.15			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA
	0.3	0.35	0.4	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	1.7			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA
	2.3	2.7	3	Ω max	
LEAKAGE CURRENTS					V_{DD} = 5.5 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V; see Figure 27
	±0.1	±1.5	±12	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V; see Figure 27
	±0.15	±2	±20	nA max	
Channel On Leakage, I_D, I_S (On)	±0.02			nA typ	V_S = V_D = 1 V or 4.5 V; see Figure 28
	±0.15	±2	±20	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±1			nA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	8			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	199			ns typ	R_L = 300 Ω, C_L = 35 pF
	254	303	337	ns max	V_S = 2.5 V; see Figure 29
t_{ON} ($\overline{EN}$)	68			ns typ	R_L = 300 Ω, C_L = 35 pF
	90	102	110	ns max	V_S = 2.5 V; see Figure 31
t_{OFF} ($\overline{EN}$)	201			ns typ	R_L = 300 Ω, C_L = 35 pF
	256	300	333	ns max	V_S = 2.5 V; see Figure 31
Break-Before-Make Time Delay, t_D	57			ns typ	R_L = 300 Ω, C_L = 35 pF
			37	ns min	V_{S1} = V_{S2} = 2.5 V; see Figure 30
Charge Injection	−5			pC typ	V_S = 2.5 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 33
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 35
Total Harmonic Distortion + Noise (THD + N)	0.27			% typ	R_L = 110 Ω, f = 20 Hz to 20 kHz, V_S = 3.5 V p-p; see Figure 36
−3 dB Bandwidth	104			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 34
C_S (Off)	21			pF typ	V_S = 2.5 V, f = 1 MHz
C_D (Off)	37			pF typ	V_S = 2.5 V, f = 1 MHz
C_D, C_S (On)	62			pF typ	V_S = 2.5 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 5.5 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
V_{DD}			3.3/16	V min/max	

[1] Guaranteed by design, but not subject to production test.

3.3 V SINGLE SUPPLY

V_{DD} = 3.3 V, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	13.5	15	16.5	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA; see Figure 26, V_{DD} = 3.3 V, V_{SS} = 0 V
On-Resistance Match Between Channels (ΔR_{ON})	0.25	0.28	0.3	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
On-Resistance Flatness ($R_{FLAT(ON)}$)	5	5.5	6.5	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
LEAKAGE CURRENTS					V_{DD} = 3.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = 0.6 V/3 V, V_D = 3 V/0.6 V; see Figure 27
	±0.1	±1.5	±12	nA max	
Drain Off Leakage, I_D (Off)	±0.01			nA typ	V_S = 0.6 V/3 V, V_D = 3 V/0.6 V; see Figure 27
	±0.15	±2	±20	nA max	
Channel On Leakage, I_D, I_S (On)	±0.01			nA typ	V_S = V_D = 0.6 V or 3 V; see Figure 28
	±0.15	±2	±20	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±1			nA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	8			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	309			ns typ	R_L = 300 Ω, C_L = 35 pF
	429	466	508	ns max	V_S = 1.5 V; see Figure 29
t_{ON} ($\overline{EN}$)	132			ns typ	R_L = 300 Ω, C_L = 35 pF
	184	201	210	ns max	V_S = 1.5 V; see Figure 31
t_{OFF} ($\overline{EN}$)	313			ns typ	R_L = 300 Ω, C_L = 35 pF
	416	470	509	ns max	V_S = 1.5 V; see Figure 31
Break-Before-Make Time Delay, t_D	81			ns typ	R_L = 300 Ω, C_L = 35 pF
			48	ns min	V_{S1} = V_{S2} = 1.5 V; see Figure 30
Charge Injection	−10			pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 33
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 35
Total Harmonic Distortion + Noise (THD + N)	0.6			% typ	R_L = 110 Ω, f = 20 Hz to 20 kHz, V_S = 2 V p-p; see Figure 36
−3 dB Bandwidth	117			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 34
C_S (Off)	22			pF typ	V_S = 1.5 V, f = 1 MHz
C_D (Off)	39			pF typ	V_S = 1.5 V, f = 1 MHz
C_D, C_S (On)	64			pF typ	V_S = 1.5 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 3.6 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
V_{DD}			3.3/16	V min/max	

[1] Guaranteed by design, but not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S OR D

Table 5. ADG1633

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, S OR D				
V_{DD} = +5 V, V_{SS} = −5 V				
TSSOP (θ_{JA} = 112.6°C/W)	126	84	56	mA max
LFCSP (θ_{JA} = 48.7°C/W)	206	126	70	mA max
V_{DD} = 12 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	133	87	56	mA max
LFCSP (θ_{JA} = 48.7°C/W)	213	133	73	mA max
V_{DD} = 5 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	98	70	45	mA max
LFCSP (θ_{JA} = 48.7°C/W)	157	105	63	mA max
V_{DD} = 3.3 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	77	56	38	mA max
LFCSP (θ_{JA} = 48.7°C/W)	129	87	56	mA max

Table 6. ADG1634

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, S OR D				
V_{DD} = +5 V, V_{SS} = −5 V				
TSSOP (θ_{JA} = 95°C/W)	112	77	52	mA max
LFCSP (θ_{JA} = 30.4°C/W)	220	136	73	mA max
V_{DD} = 12 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 95°C/W)	119	80	52	mA max
LFCSP (θ_{JA} = 30.4°C/W)	234	140	73	mA max
V_{DD} = 5 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 95°C/W)	87	63	42	mA max
LFCSP (θ_{JA} = 30.4°C/W)	171	112	66	mA max
V_{DD} = 3.3 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 95°C/W)	70	52	35	mA max
LFCSP (θ_{JA} = 30.4°C/W)	140	94	59	mA max

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to V_{SS}	18 V
V_{DD} to GND	−0.3 V to +18 V
V_{SS} to GND	+0.3 V to −18 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	450 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D[2]	Data + 15%
Operating Temperature Range	
Industrial (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, θ_{JA} Thermal Impedance, 0 Airflow (4-Layer Board)	112.6°C/W
20-Lead TSSOP, θ_{JA} Thermal Impedance, 0 Airflow (4-Layer Board)	95°C/W
16-Lead LFCSP (3 mm × 3 mm), θ_{JA} Thermal Impedance, 0 Airflow (4-Layer Board)	48.7°C/W
16-Lead LFCSP (4 mm × 4 mm), θ_{JA} Thermal Impedance, 0 Airflow (4-Layer Board)	30.4°C/W
Reflow Soldering Peak Temperature, Pb free	260°C

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.
[2] See Table 5 and Table 6.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

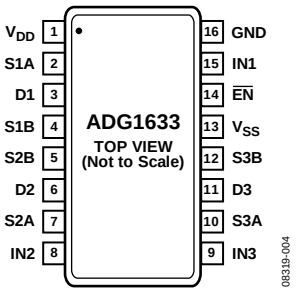


Figure 4. ADG1633 TSSOP Pin Configuration

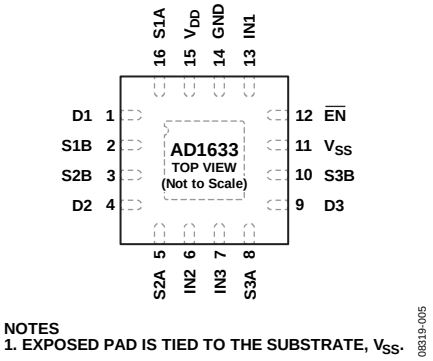


Figure 5. ADG1633 LFCSP Pin Configuration

Table 8. ADG1633 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	15	V_{DD}	Most Positive Power Supply Potential.
2	16	S1A	Source Terminal 1A. Can be an input or an output.
3	1	D1	Drain Terminal 1. Can be an input or an output.
4	2	S1B	Source Terminal 1B. Can be an input or an output.
5	3	S2B	Source Terminal 2B. Can be an input or an output.
6	4	D2	Drain Terminal 2. Can be an input or an output.
7	5	S2A	Source Terminal 2A. Can be an input or an output.
8	6	IN2	Logic Control Input 2.
9	7	IN3	Logic Control Input 3.
10	8	S3A	Source Terminal 3A. Can be an input or an output.
11	9	D3	Drain Terminal 3. Can be an input or an output.
12	10	S3B	Source Terminal 3B. Can be an input or an output.
13	11	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
14	12	$\overline{EN}$	Active Low Digital Input. When this pin is high, the device is disabled and all switches are off. When this pin is low, INx logic inputs determine the on switches.
15	13	IN1	Logic Control Input 1.
16	14	GND	Ground (0 V) Reference.
N/A	17	EP	Exposed Pad. The exposed pad is tied to the substrate, V_{SS}.

Table 9. ADG1633 Truth Table

$\overline{EN}$	INx	SxA	SxB
1	X[1]	Off	Off
0	0	Off	On
0	1	On	Off

[1] X = don't care.

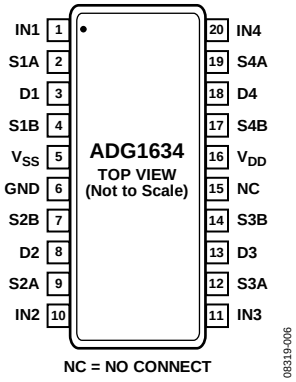


Figure 6. ADG1634 TSSOP Pin Configuration

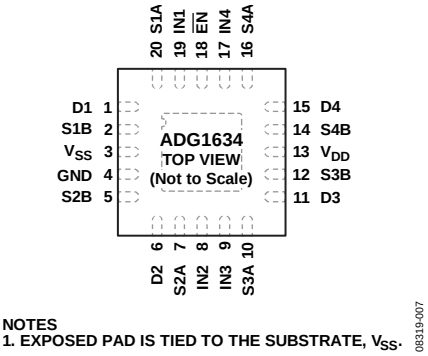


Figure 7. ADG1634 LFCSP Pin Configuration

Table 10. ADG1634 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	IN1	Logic Control Input 1.
2	20	S1A	Source Terminal 1A. Can be an input or an output.
3	1	D1	Drain Terminal 1. Can be an input or an output.
4	2	S1B	Source Terminal 1B. Can be an input or an output.
5	3	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
6	4	GND	Ground (0 V) Reference.
7	5	S2B	Source Terminal 2B. Can be an input or an output.
8	6	D2	Drain Terminal 2. Can be an input or an output.
9	7	S2A	Source Terminal 2A. Can be an input or an output.
10	8	IN2	Logic Control Input 2.
11	9	IN3	Logic Control Input 3.
12	10	S3A	Source Terminal 3A. Can be an input or an output.
13	11	D3	Drain Terminal 3. Can be an input or an output.
14	12	S3B	Source Terminal 3B. Can be an input or an output.
15	N/A	NC	No Connect.
16	13	V_{DD}	Most Positive Power Supply Potential.
17	14	S4B	Source Terminal 4B. Can be an input or an output.
18	15	D4	Drain Terminal 4. Can be an input or an output.
19	16	S4A	Source Terminal 4A. Can be an input or an output.
20	17	IN4	Logic Control Input 4.
N/A	18	$\overline{EN}$	Active Low Digital Input. When this pin is high, the device is disabled and all switches are off. When this pin is low, INx logic inputs determine the on switches.
N/A	21	EP	Exposed Pad. The exposed pad is tied to the substrate, V_{SS}.

Table 11. ADG1634 TSSOP Truth Table

INx	**SxA**	**SxB**
0	Off	On
1	On	Off

Table 12. ADG1634 LFCSP Truth Table

$\overline{EN}$	**INx**	**SxA**	**SxB**
1	X[1]	Off	Off
0	0	Off	On
0	1	On	Off

[1] X = don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

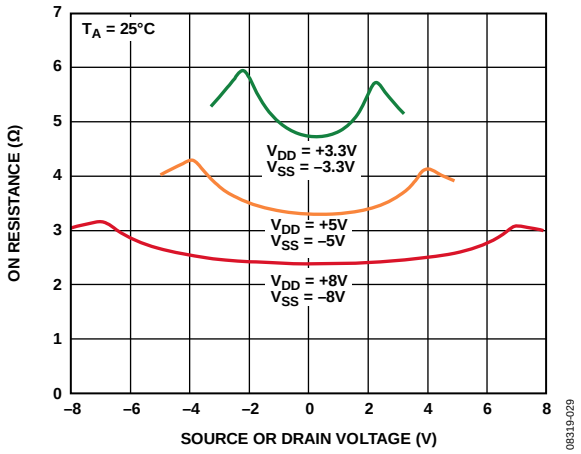


Figure 8. On Resistance vs. V_D (V_S), Dual Supply

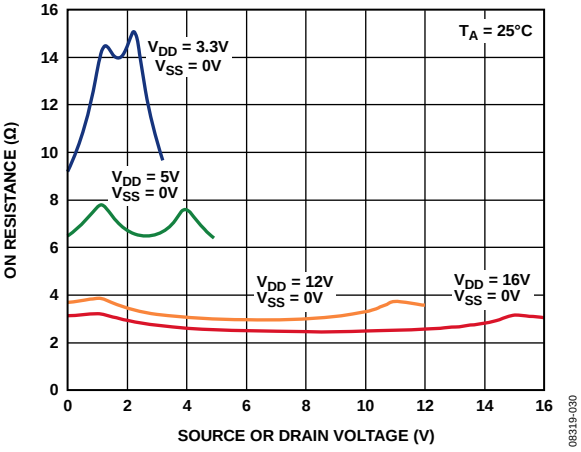


Figure 9. On Resistance vs. V_D (V_S), Single Supply

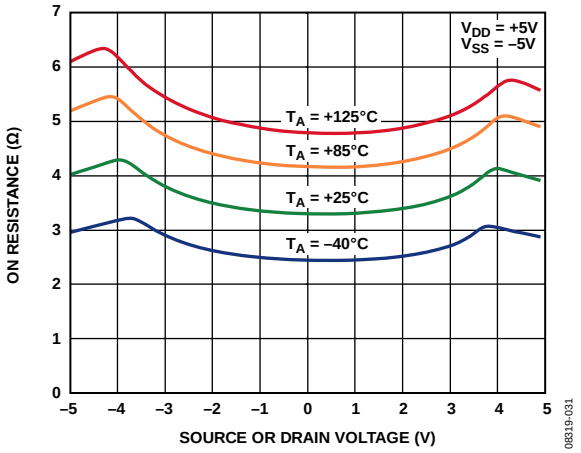


Figure 10. On Resistance vs. V_D (V_S) for Different Temperatures, ±5 V Dual Supply

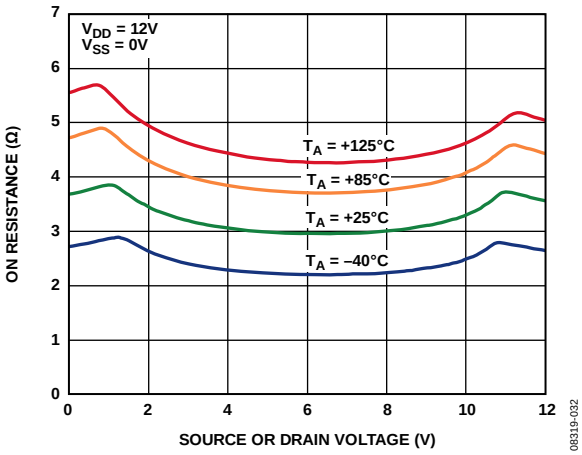


Figure 11. On Resistance vs. V_D (V_S) for Different Temperatures, 12 V Single Supply

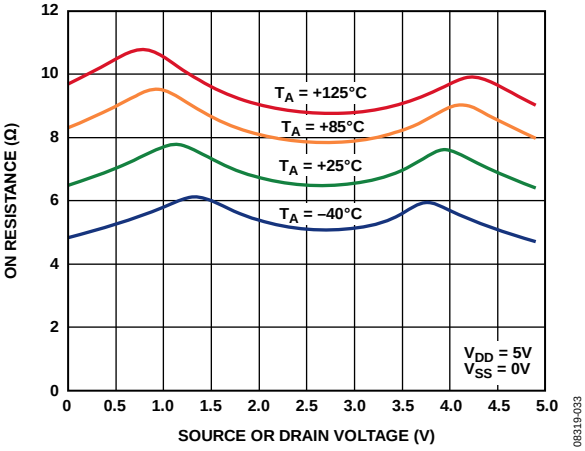


Figure 12. On Resistance vs. V_D (V_S) for Different Temperatures, 5 V Single Supply

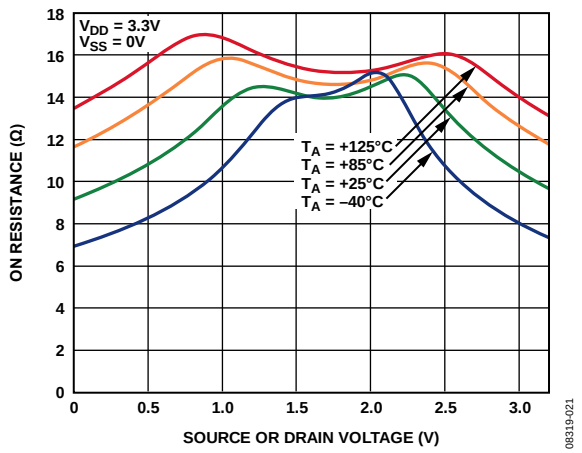


Figure 13. On Resistance vs. V_D (V_S) for Different Temperatures, 3.3 V Single Supply

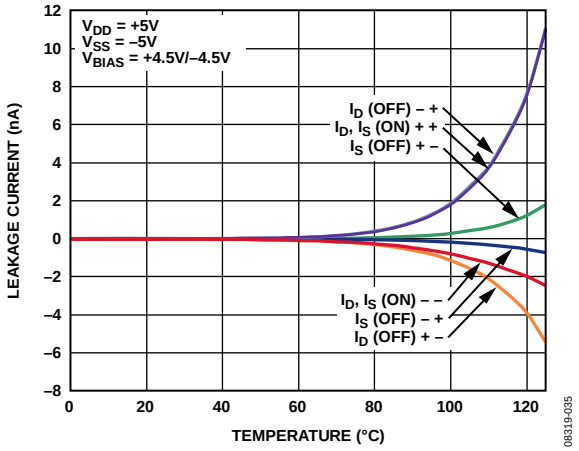


Figure 14. ADG1633 Leakage Currents vs. Temperature, ±5 V Dual Supply

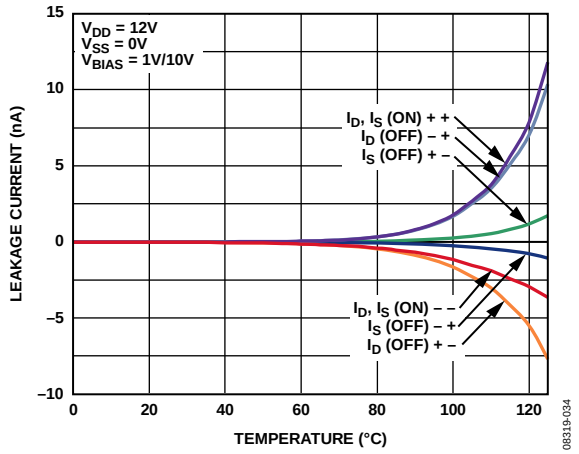


Figure 15. ADG1633 Leakage Currents vs. Temperature, 12 V Single Supply

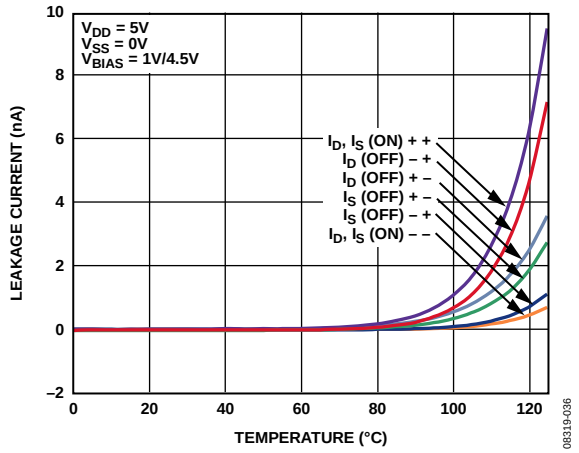


Figure 16. ADG1633 Leakage Currents vs. Temperature, 5 V Single Supply

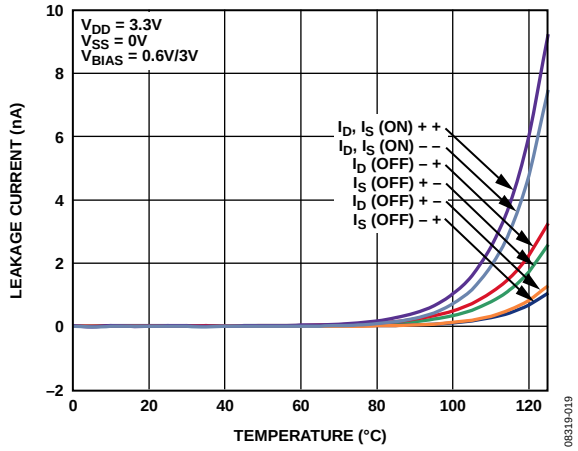


Figure 17. ADG1633 Leakage Currents vs. Temperature, 3.3 V Single Supply

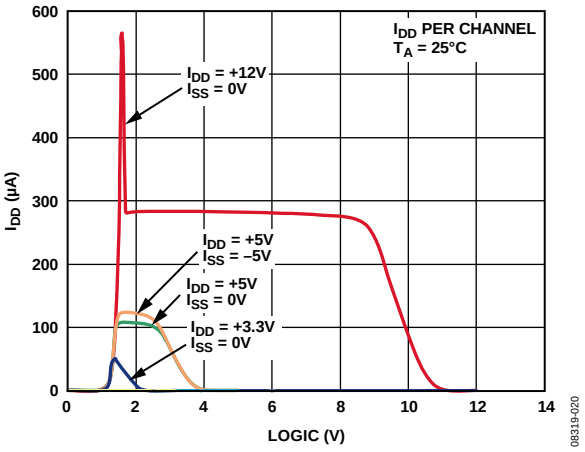


Figure 18. I_{DD} vs. Logic Level

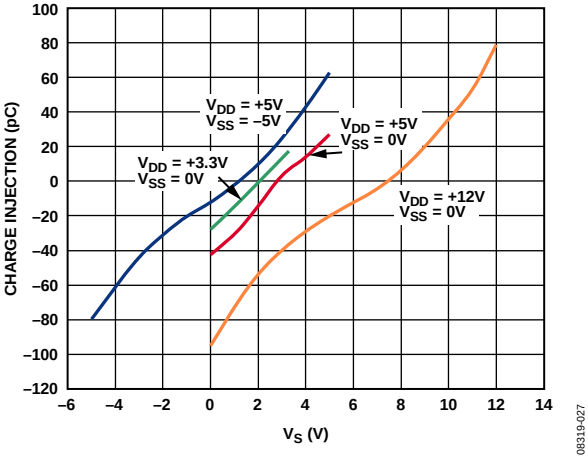


Figure 19. Charge Injection vs. Source Voltage

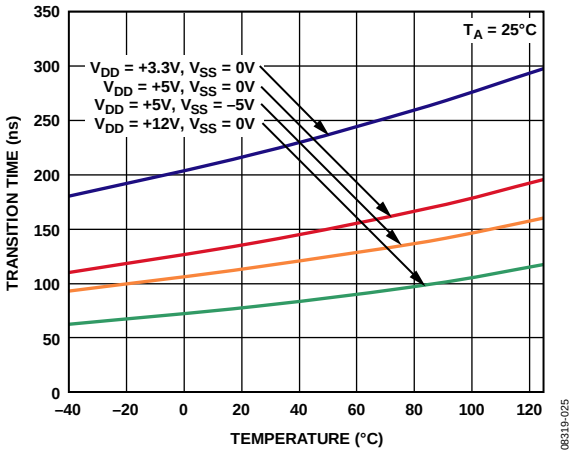


Figure 20. Transition Time vs. Temperature

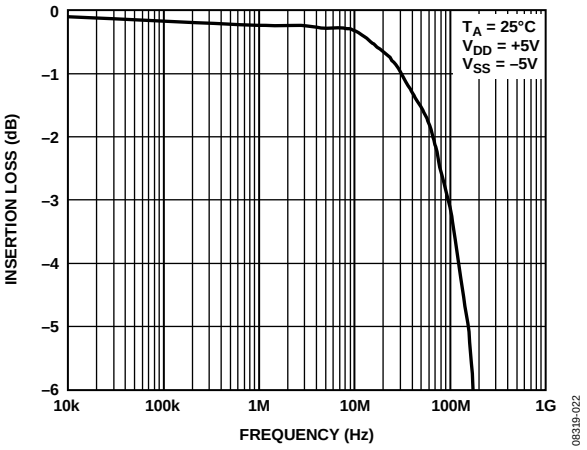


Figure 23. On Response vs. Frequency

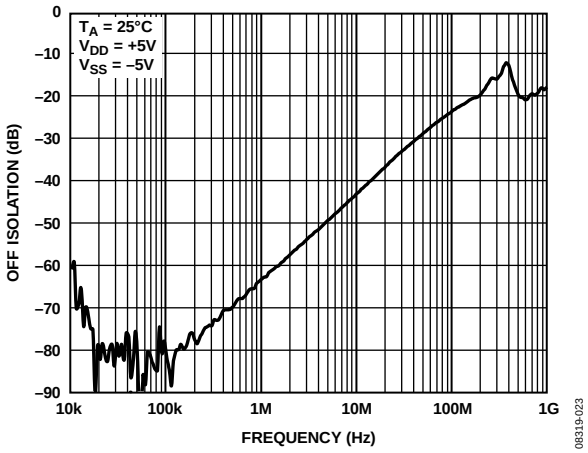


Figure 21. Off Isolation vs. Frequency

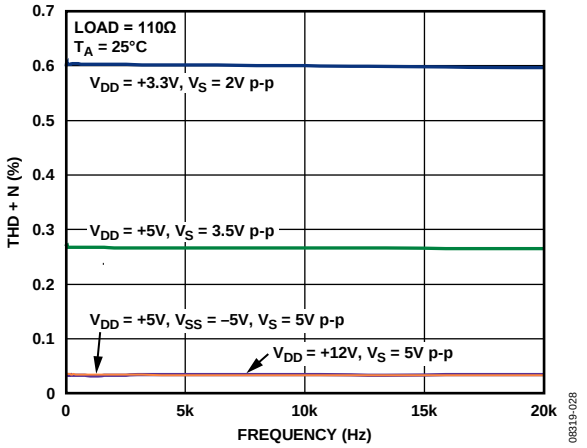


Figure 24. THD + N vs. Frequency

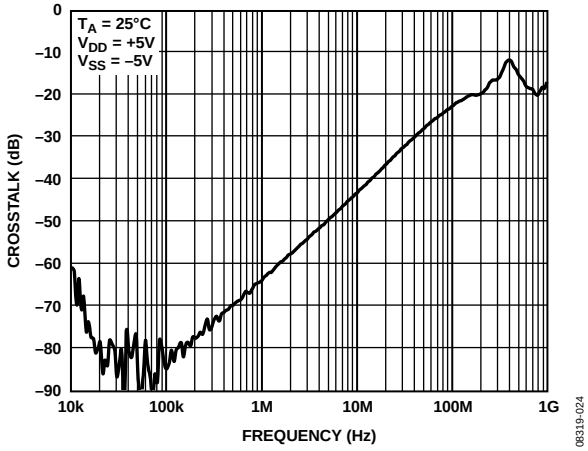


Figure 22. Crosstalk vs. Frequency

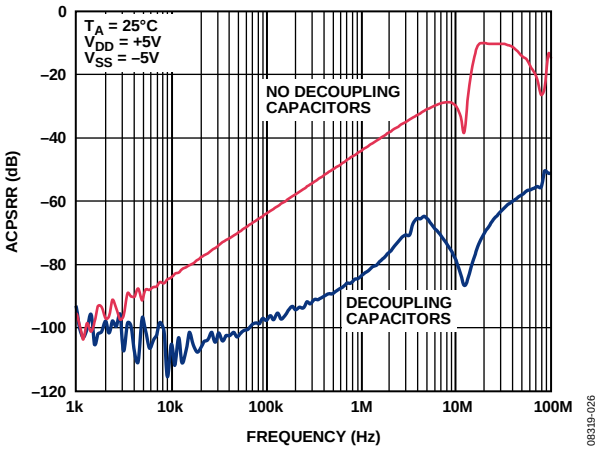


Figure 25. ACPSRR vs. Frequency

TEST CIRCUITS

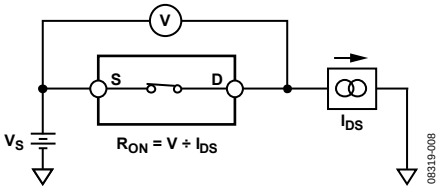


Figure 26. On Resistance

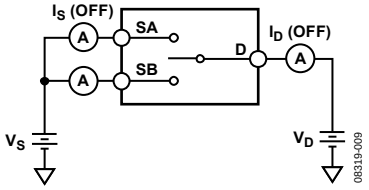


Figure 27. Off Leakage

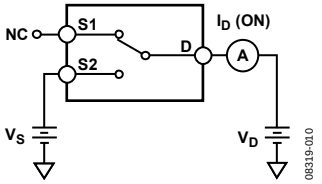


Figure 28. On Leakage

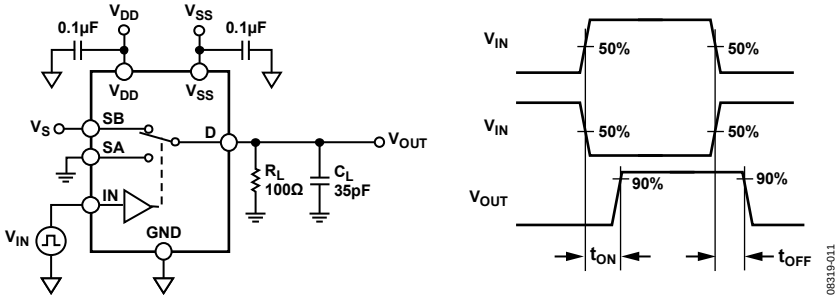


Figure 29. Switching Timing

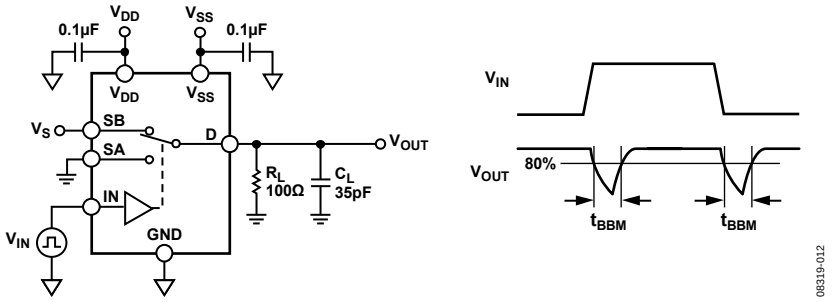


Figure 30. Break-Before-Make Delay, t_D

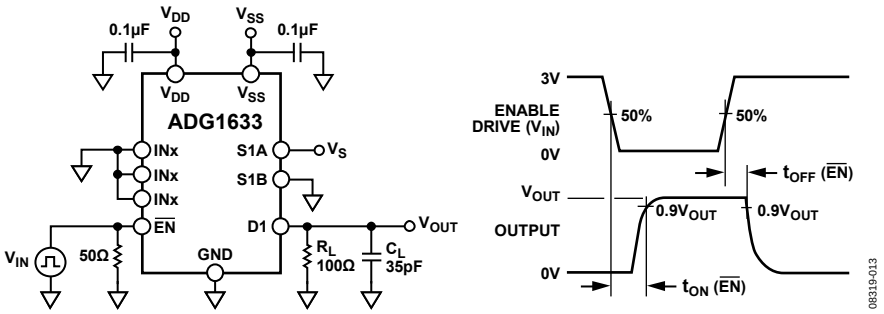


Figure 31. Enable Delay, t_{ON} ($\overline{EN}$), t_{OFF} ($\overline{EN}$)

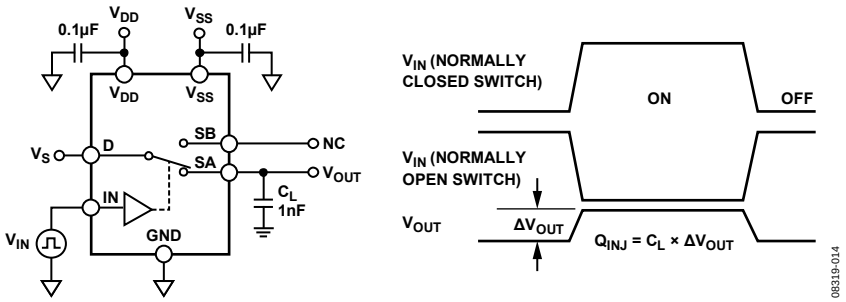


Figure 32. Charge Injection

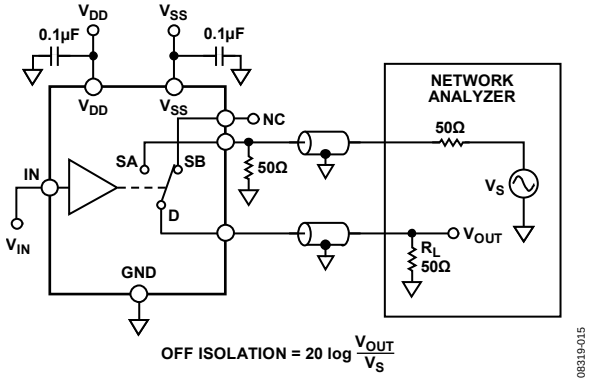


Figure 33. Off Isolation

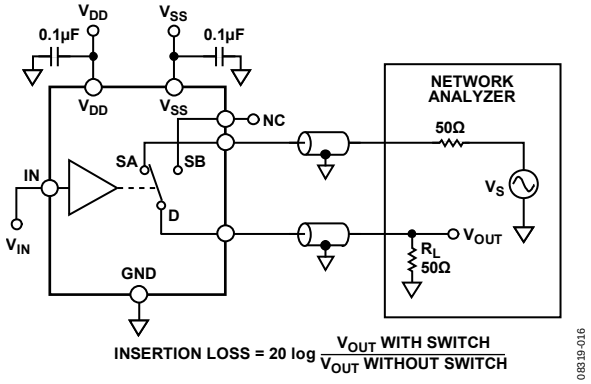


Figure 34. Bandwidth

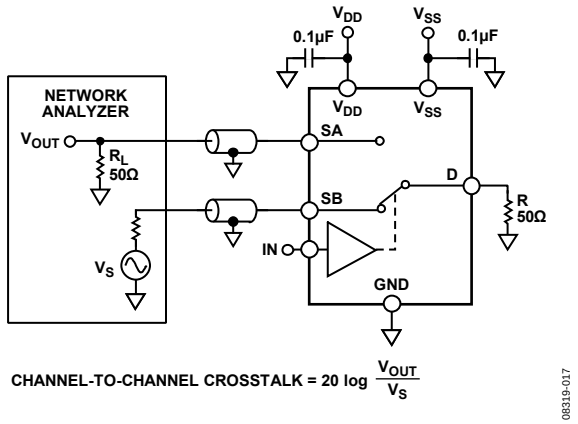


Figure 35. Channel-to-Channel Crosstalk

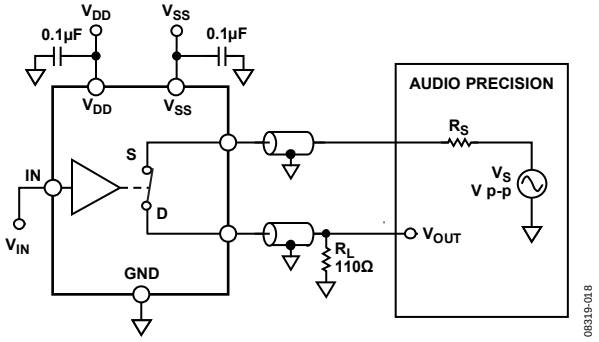


Figure 36. THD + Noise

TERMINOLOGY

R_{ON}
Ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}
The difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$
The difference between the maximum and minimum value of on resistance measured.

I_S (Off)
Source leakage current when the switch is off.

I_D (Off)
Drain leakage current when the switch is off.

I_D, I_S (On)
Channel leakage current when the switch is on.

V_D (V_S)
Analog voltage on Terminal D and Terminal S.

C_S (Off)
Channel input capacitance for off condition.

C_D (Off)
Channel output capacitance for off condition.

C_D, C_S (On)
On switch capacitance.

C_{IN}
Digital input capacitance.

t_{ON} ($\overline{EN}$)

Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} ($\overline{EN}$)
Delay time between the 50% and 90% points of the digital input and switch off condition.

t_{TRANS}
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{BBM}
Off time measured between the 80% point of both switches when switching from one address state to another.

V_{IL}
Maximum input voltage for Logic 0.

V_{IH}
Minimum input voltage for Logic 1.

I_{IL} (I_{IH})
Input current of the digital input.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

Off Isolation
A measure of unwanted signal coupling through an off channel.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

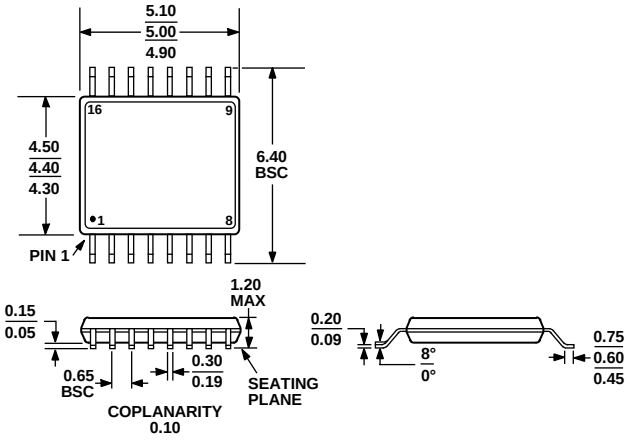
Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Total Harmonic Distortion + Noise (THD + N)
The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

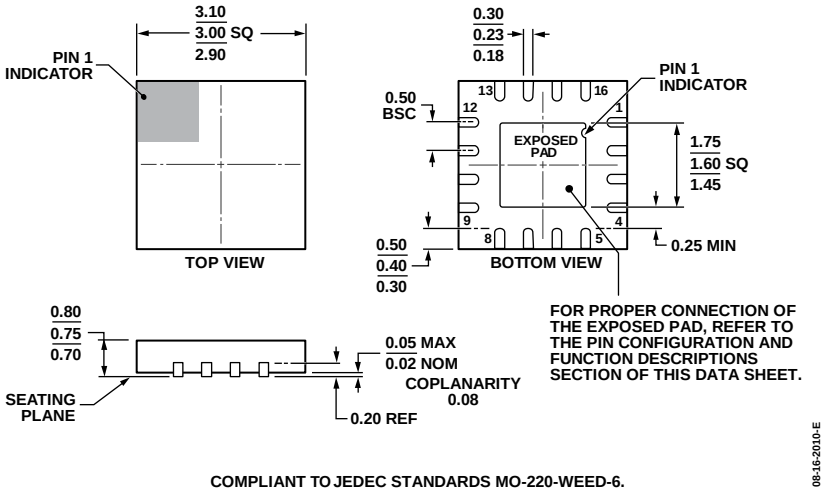
AC Power Supply Rejection Ratio (ACPSRR)
A measure of the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 37. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 38. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm and 0.75 mm Package Height
(CP-16-22)
Dimensions shown in millimeters

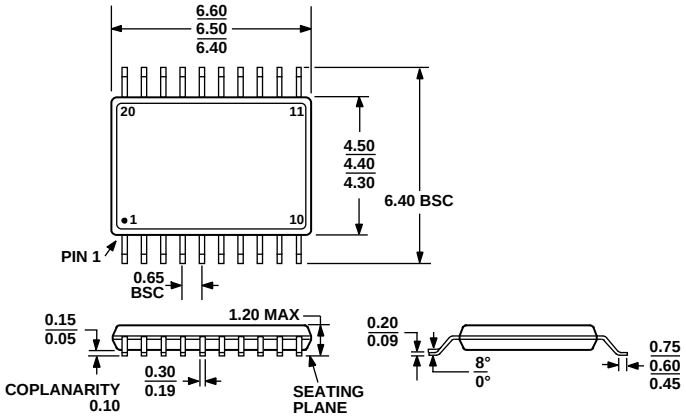


Figure 39. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

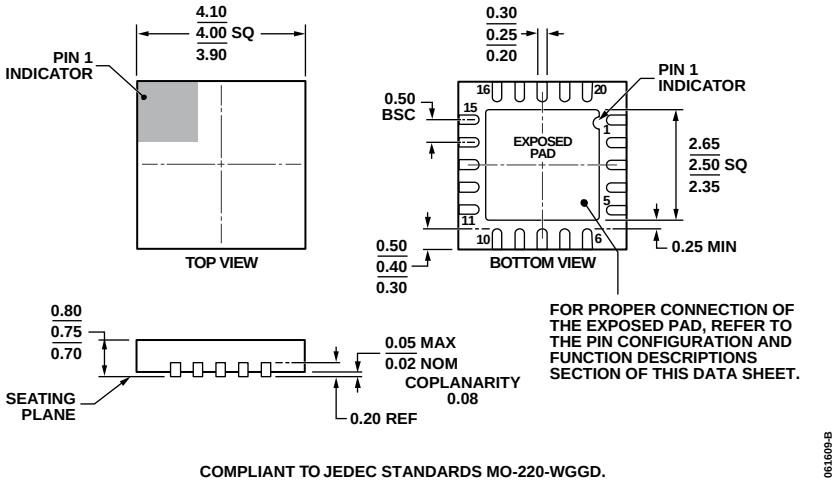


Figure 40. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Description	$\overline{EN}$ Pin	Package Option	Branding
ADG1633BRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	Yes	RU-16	
ADG1633BRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	Yes	RU-16	
ADG1633BCPZ-REEL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	Yes	CP-16-22	SD3
ADG1634BRUZ	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	No	RU-20	
ADG1634BRUZ-REEL7	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	No	RU-20	
ADG1634BCPZ-REEL7	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	Yes	CP-20-10	

[1] Z = RoHS Compliant Part.

D08319-0-8/16(B)

Mouser Electronics

Authorized Distributor

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Analog Devices Inc.:

ADG1633BRUZ ADG1634BRUZ ADG1634BRUZ-REEL7 ADG1633BCPZ-REEL7 ADG1633BRUZ-REEL7