HEWLETT® PACKARD

Low Input Current Logic Gate Optocouplers

Technical Data

HCPL-2200
HCPL-2219

Features

- **2.5 kV/μs Minimum Common Mode Rejection (CMR) at V_{CM} = 400 V (HCPL-2219)**
- **Compatible with LSTTL, TTL, and CMOS Logic**
- **Wide V_{CC} Range (4.5 to 20 V)**
- **2.5 Mbd Guaranteed over Temperature**
- **Low Input Current (1.6 mA)**
- **Three State Output (No Pullup Resistor Required)**
- **Guaranteed Performance from 0°C to 85°C**
- **Hysteresis**
- **Safety Approval**
  UL Recognized -2500 V rms for 1 minute
  CSA Approved
  VDE 0884 Approved with V_{IORM} = 630 V peak (HCPL-2219 Option 060 Only)
- **MIL-STD-1772 Version Available (HCPL-5200/1)**

Applications

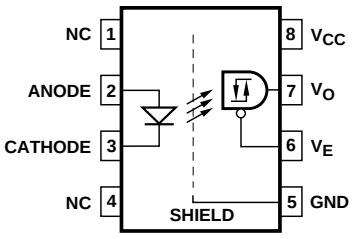
- **Isolation of High Speed Logic Systems**
- **Computer-Peripheral Interfaces**
- **Microprocessor System Interfaces**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **Isolated Buss Driver**
- **High Speed Line Receiver**

Description

The HCPL-2200/2219 are optically coupled logic gates that combine a GaAsP LED and an integrated high gain photo detector. The detector has a three state output stage and has a detector threshold with hysteresis. The three state output eliminates the need for a pullup resistor and allows for direct drive of data busses. The hysteresis provides differential mode noise immunity and eliminates the potential for output signal chatter.

A superior internal shield on the HCPL-2219 guarantees common mode transient immunity of 2.5 kV/μs at a common mode voltage of 400 volts.

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	Z
OFF	H	Z
ON	L	H
OFF	L	L

A 0.1 μF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

The Electrical and Switching Characteristics of the HCPL-2200/2219 are guaranteed over the temperature range of 0°C to 85°C and a V_{CC} range of 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed optocouplers. Logic signals are transmitted with a typical propagation delay of 160 nsec. The HCPL-2200/2219 are useful for isolating high speed logic interfaces, buffering of input and output lines, and implementing isolated line receivers in high noise environments.

Selection Guide

Minimum CMR			8-Pin DIP (300 Mil)		Small-Outline SO-8	Widebody (400 Mil)	Hermetic
dV/dt (V/μs)	V_{CM} (V)	Input On-Current (mA)	Single Channel Package	Dual Channel Package	Single Channel Package	Single Channel Package	Single and Dual Channel Packages
1,000	50	1.6	HCPL-2200[1] HCPL-2201 HCPL-2202		HCPL-0201	HCNW2201	
		1.8		HCPL-2231			
2,500	400	1.6	HCPL-2219[1]				
5,000[2]	300[2]	1.6	HCPL-2211 HCPL-2212		HCPL-0211	HCNW2211	
		1.8		HCPL-2232			
1,000	50	2.0					HCPL-52XX HCPL-62XX

Notes:
1. HCPL-2200/2219 devices include output enable/disable functionality.
2. Minimum CMR of 10 kV/μs with V_{CM} = 1000 V can be achieved with input current, I_F, of 5 mA.

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

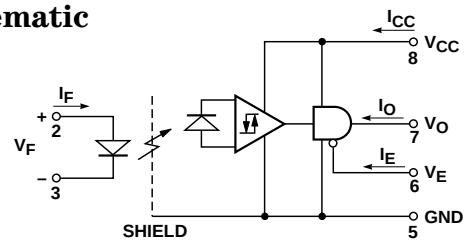
HCPL-2219#XXX

- 060 = VDE 0884 V_{IORM} = 630 Vpeak Option*
- 300 = Gull Wing Surface Mount Option
- 500 = Tape and Reel Packaging Option

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

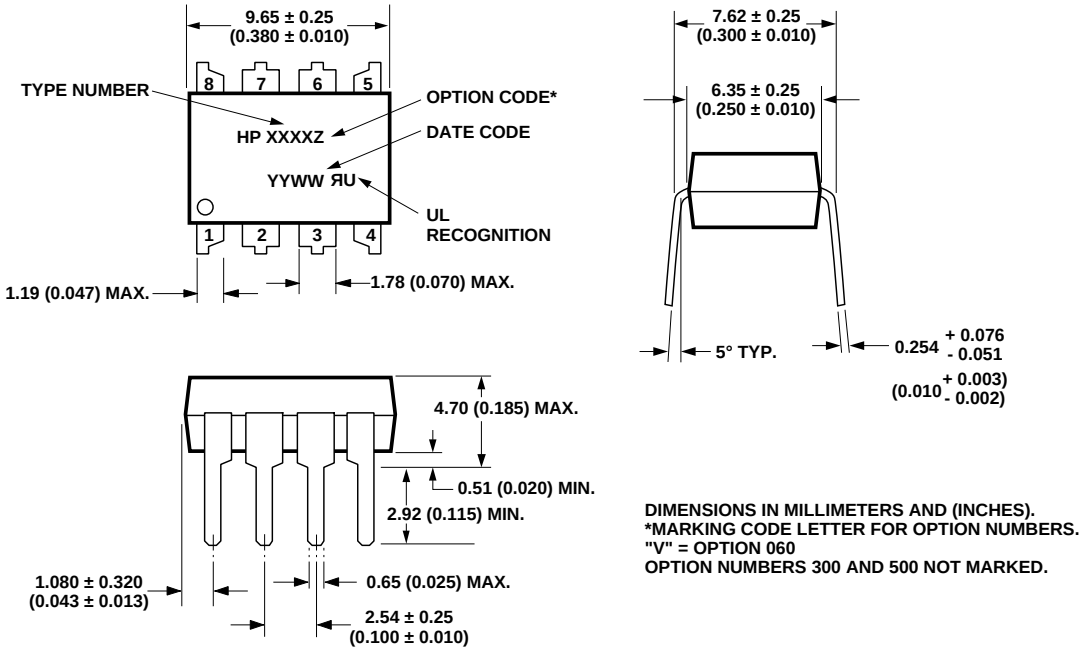
*For HCPL-2219 only.

Schematic



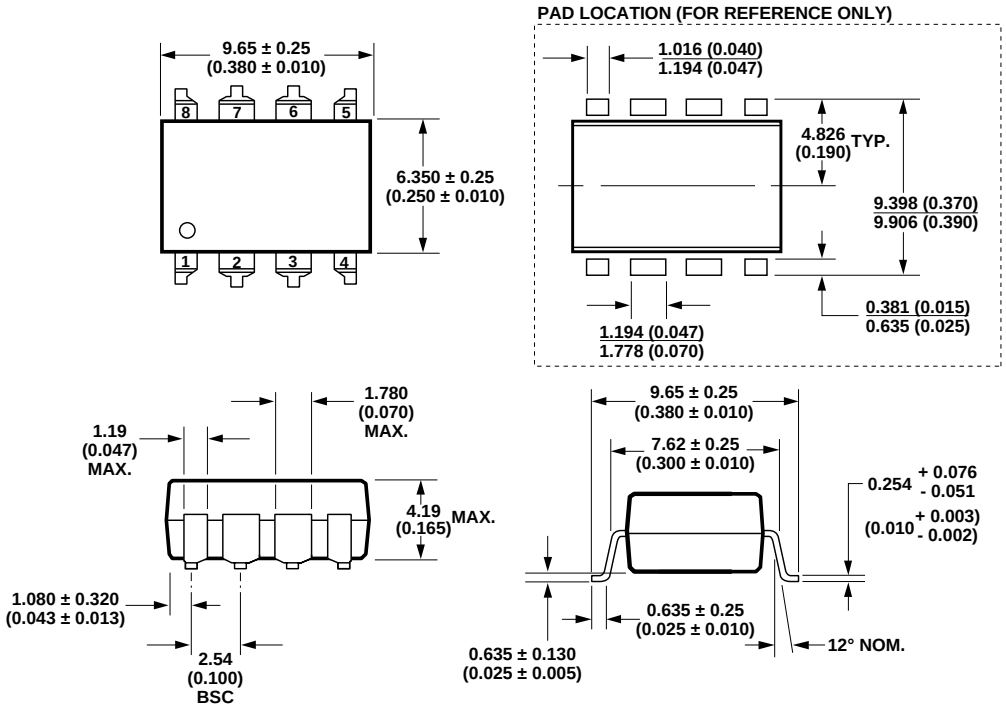
Package Outline Drawings

8-Pin DIP Package



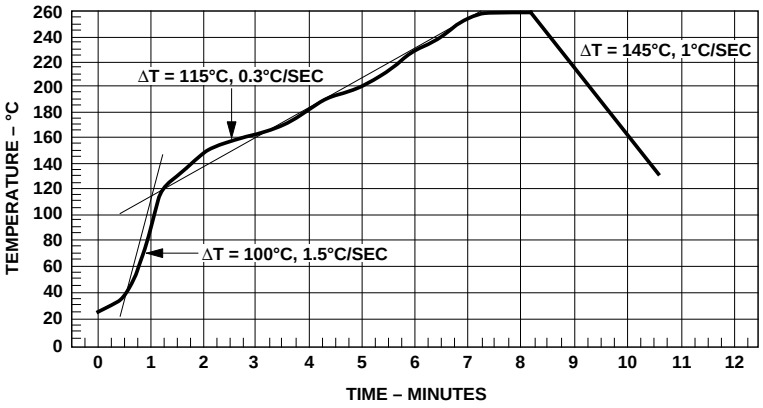
DIMENSIONS IN MILLIMETERS AND (INCHES).
*MARKING CODE LETTER FOR OPTION NUMBERS.
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

8-Pin DIP Package with Gull Wing Surface Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

Maximum Solder Reflow Thermal Profile



Note: Use of nonchlorine activated fluxes is highly recommended.

Regulatory Information

The HCPL-2200/2219 have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92. (HCPL-2219 Option 060 Only)

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Min. External Tracking Path (External Creepage)	L(IO2)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCPL-2219 OPTION 060 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 12, Thermal Derating curve.) Case Temperature Input Current Output Power	 T_S $I_{S,INPUT}$ $P_{S,OUTPUT}$	 175 230 600	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section, (VDE 0884), for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings

(No Derating Required up to 70°C)

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	85	°C	1
Average Forward Input Current	$I_{F(AVG)}$		10	mA	
Peak Transient Input Current (≤ 1 µs Pulse Width, 300 pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	V_R		5	V	
Average Output Current	I_O		25	mA	
Supply Voltage	V_{CC}	0	20	V	
Three State Enable Voltage	V_E	-0.5	20	V	
Output Voltage	V_O	-0.5	20	V	
Total Package Power Dissipation	P_T		210	mW	1
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Package Outline Drawings section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	V
Enable Voltage High	V_{EH}	2.0	20	V
Enable Voltage Low	V_{EL}	0	0.8	V
Forward Input Current	$I_{F(ON)}$	1.6*	5	mA
Forward Input Current	$I_{F(OFF)}$	–	0.1	mA
Operating Temperature	T_A	0	85[1]	°C
Fan Out	N		4	TTL Loads

*The initial switching threshold is 1.6 mA or less. It is recommended that 2.2 mA be used to permit at least a 20% CTR degradation guardband.

Electrical Specifications

For 0°C ≤ T_A[1] ≤ 85°C, 4.5 V ≤ V_{CC} ≤ 20 V, 1.6 mA ≤ $I_{F(ON)}$ ≤ 5 mA, 2.0 V ≤ V_{EH} ≤ 20 V, 0.0 V ≤ V_{EL} ≤ 0.8 V, 0 mA ≤ $I_{F(OFF)}$ ≤ 0.1 mA. All Typicals at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 3 mA unless otherwise specified. See Note 7.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Logic Low Output Voltage	V_{OL}			0.5	V	I_{OL} = 6.4 mA (4 TTL Loads)		1	
Logic High Output Voltage	V_{OH}	2.4	*		V	I_{OH} = -2.6 mA *V_{OH} = V_{CC} - 2.1 V		2	
Output Leakage Current (V_{OUT} > V_{CC})	I_{OHH}			100	µA	V_O = 5.5 V	I_F = 5 mA, V_{CC} = 4.5 V		
				500	µA	V_O = 20 V			
Logic High Enable Voltage	V_{EH}	2.0			V				
Logic Low Enable Voltage	V_{EL}			0.8	V				
Logic High Enable Current	I_{EH}			20	µA	V_{EN} = 2.7 V			
				100	µA	V_{EN} = 5.5 V			
			0.004	250	µA	V_{EN} = 20 V			
Logic Low Enable Current	I_{EL}			-0.32	mA	V_{EN} = 0.4 V			
Logic Low Supply Current	I_{CCL}		4.5	6.0	mA	V_{CC} = 5.5 V	I_F = 0 mA, I_O = Open, V_E = Don't Care		
			5.25	7.5	mA	V_{CC} = 20 V			
Logic High Supply Current	I_{CCH}		2.7	4.5	mA	V_{CC} = 5.5 V	I_F = 5 mA, I_O = Open, V_E = Don't Care		
			3.1	6.0	mA	V_{CC} = 20 V			
High Impedance State Output Current	I_{OZL}			-20	µA	V_O = 0.4 V	V_{EN} = 2 V, I_F = 5 mA		
	I_{OZH}			20	µA	V_O = 2.4 V	V_{EN} = 2 V, I_F = 5 mA		
				100	µA	V_O = 5.5 V			
				500	µA	V_O = 20 V			
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	V_O = V_{CC} = 5.5 V	I_F = 0 mA		2
		40			mA	V_O = V_{CC} = 20 V			
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5 V	I_F = 5 mA, V_O = GND		2
		-25			mA	V_{CC} = 20 V			
Input Current Hysteresis	I_{HYS}		0.12		mA	V_{CC} = 5 V		3	
Input Forward Voltage	V_F		1.5	1.7	V	T_A = 25°C	I_F = 5 mA	4	
				1.75					
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA			
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.7		mV/°C	I_F = 5 mA			
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V, Pins 2 and 3			

Switching Specifications (AC)

For 0°C ≤ T_A[1] ≤ 85°C, 4.5 V ≤ V_{CC} ≤ 20 V, 1.6 mA ≤ $I_{F(ON)}$ ≤ 5 mA, 0.0 mA ≤ $I_{F(OFF)}$ ≤ 0.1 mA.
All Typicals at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 3 mA unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		210		ns	Without Peaking Capacitor	5, 6	4, 5
			160	300		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		170		ns	Without Peaking Capacitor	5. 6	4. 5
			115	300		With Peaking Capacitor		
Output Enable Time to Logic High	t_{PZH}		25		ns		7, 9	
Output Enable Time to Logic Low	t_{PZL}		28		ns		7, 8	
Output Disable Time from Logic High	t_{PHZ}		105		ns		7, 9	
Output Disable Time from Logic Low	t_{PLZ}		60		ns		7, 8	
Output Rise Time (10-90%)	t_r		55		ns		5, 10	
Output Fall Time (90-10%)	t_f		15		ns		5, 10	

Parameter	Sym.	Device	Min.	Units	Test Conditions		Fig.	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	HCPL-2200	1,000	V/µs	$\|V_{CM}\|$ = 50 V	I_F = 1.6 mA, V_{CC} = 5 V, T_A = 25°C	11	6
		HCPL-2219	2,500	V/µs	$\|V_{CM}\|$ = 400 V			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	HCPL-2200	1,000	V/µs	$\|V_{CM}\|$ = 50 V	V_F = 0 V, V_{CC} = 5 V, T_A = 25°C	11	6
		HCPL-2219	2,500	V/µs	$\|V_{CM}\|$ = 400 V			

Package Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	2500			V rms	RH ≤ 50%, t = 1 min., T_A = 25°C		3, 8
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 VDC		3
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 VDC		3

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage," publication number 5963-2203E.

Notes:

1. Derate total package power dissipation, P_T, linearly above 70°C free air temperature at a rate of 4.5 mW/°C.
2. Duration of output short circuit time should not exceed 10 ms.
3. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
5. When the peaking capacitor is omitted, propagation delay times may increase by 100 ns.
6. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V).
7. Use of a 0.1 µF bypass capacitor connected between pins 5 and 8 is recommended.
8. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for one second (leakage detection current limit, $I_{I-O} \leq 5$ µA). This test is performed before the 100% production test for partial discharge (Method b) shown in the VDE 0884 Insulation Characteristics Table, if applicable.

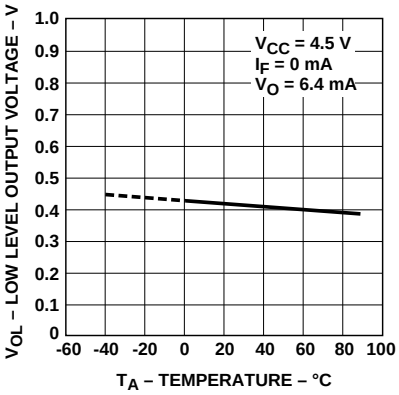


Figure 1. Typical Logic Low Output Voltage vs. Temperature.

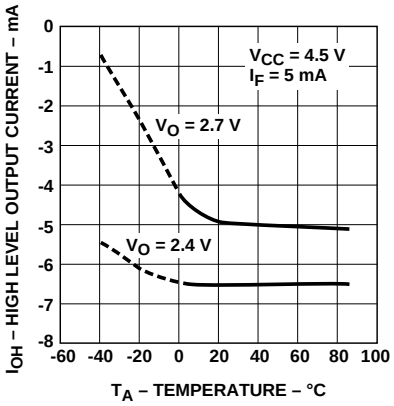


Figure 2. Typical Logic High Output Current vs. Temperature.

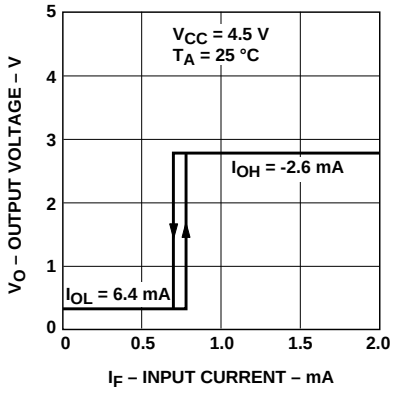


Figure 3. Output Voltage vs. Forward Input Current.

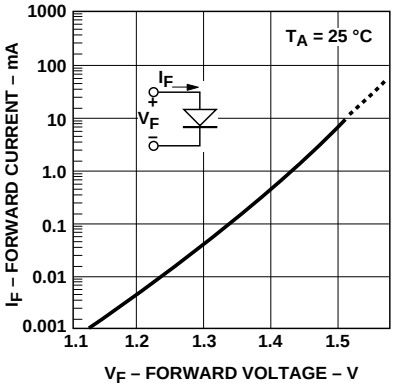


Figure 4. Typical Input Diode Forward Characteristic.

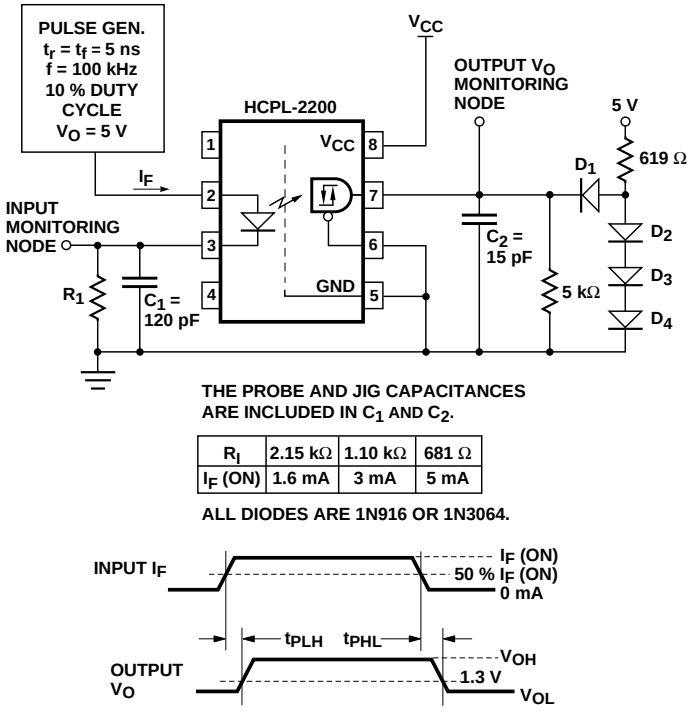


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f.

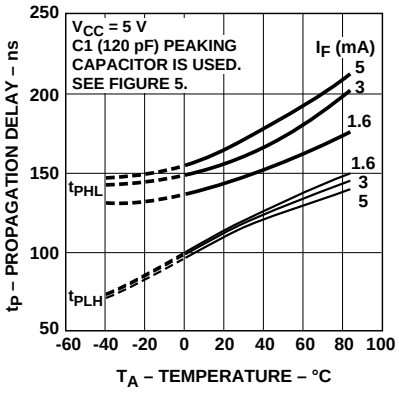


Figure 6. Typical Propagation Delays vs. Temperature.

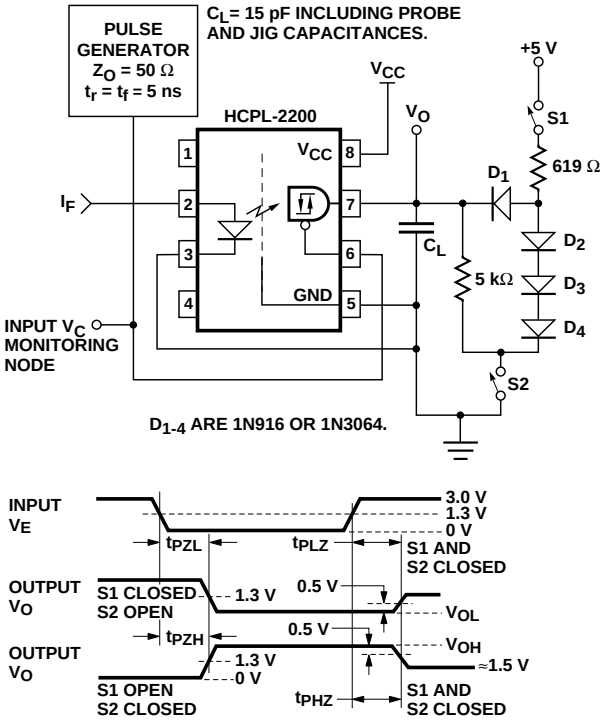


Figure 7. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}.

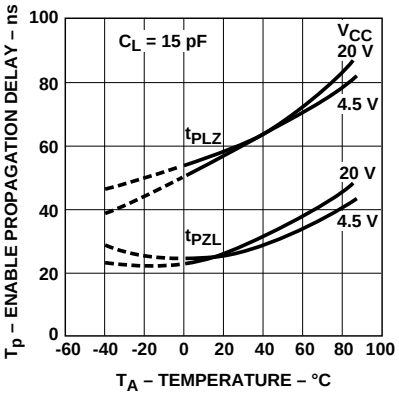


Figure 8. Typical Logic Low Enable Propagation Delay vs. Temperature.

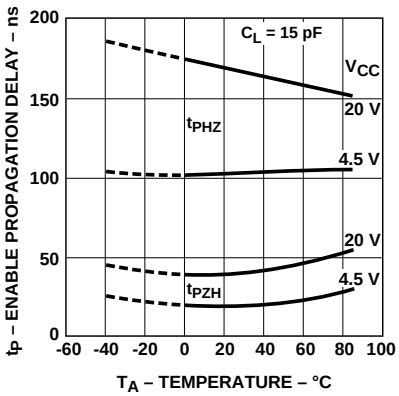


Figure 9. Typical Logic High Enable Propagation Delay vs. Temperature.

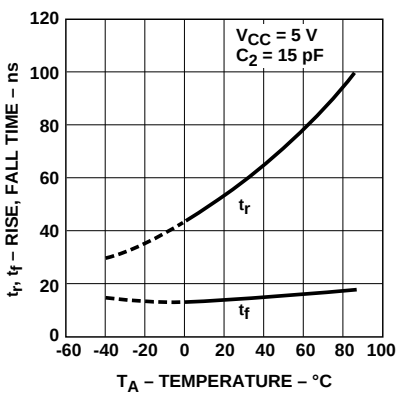


Figure 10. Typical Rise, Fall Time vs. Temperature.

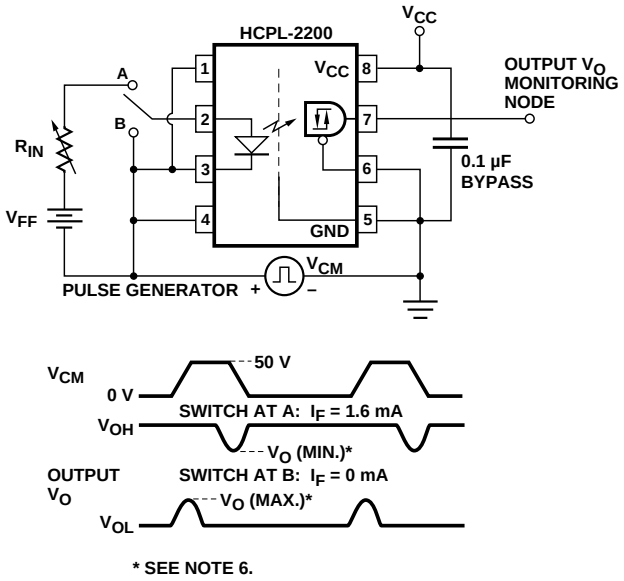


Figure 11. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

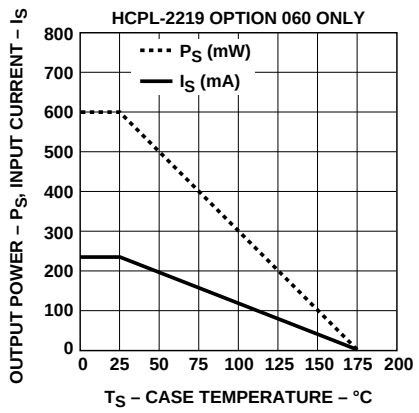


Figure 12. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

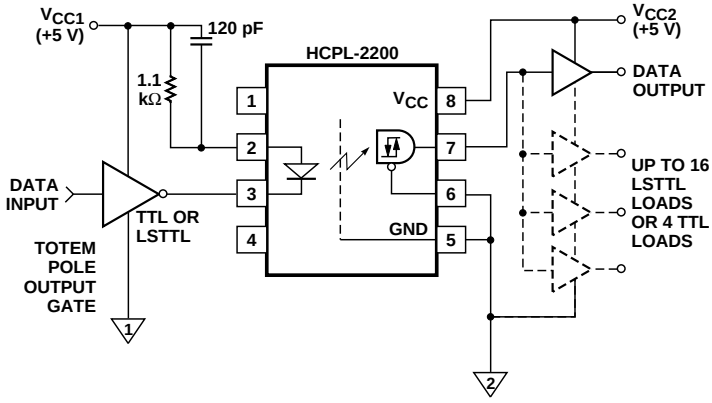


Figure 13. Recommended LSTTL to LSTTL Circuit.

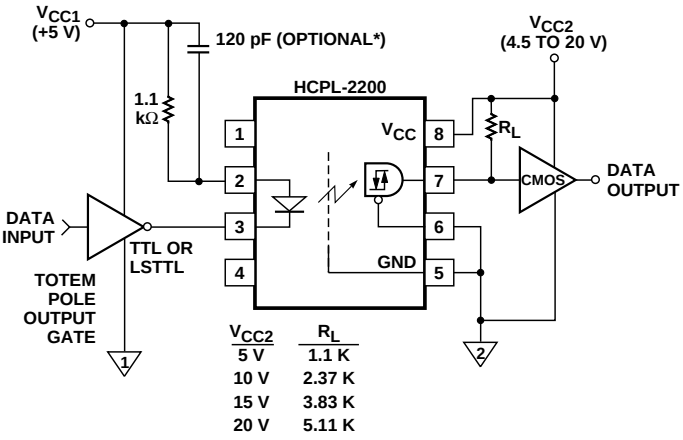


Figure 14. LSTTL to CMOS Interface Circuit.

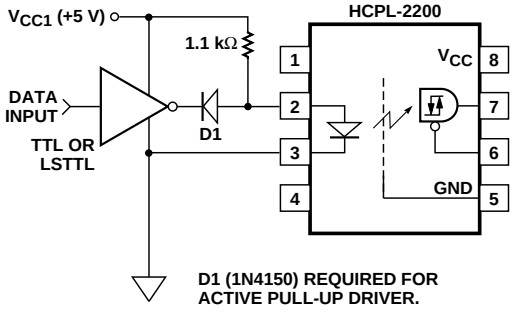


Figure 15. Recommended LED Drive Circuit.

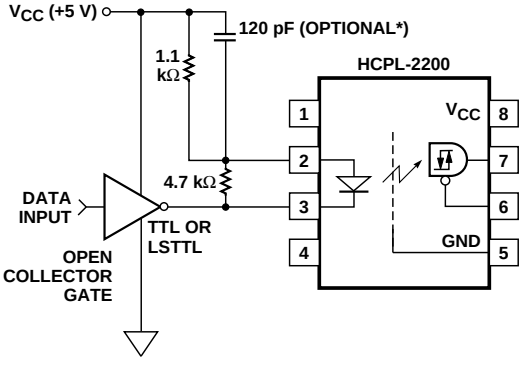


Figure 16. Series LED Drive with Open Collector Gate (4.7 kΩ Resistor Shunts I_{OH} from the LED).

*The 120 pF capacitor may be omitted in applications where 500 ns propagation delay is sufficient.