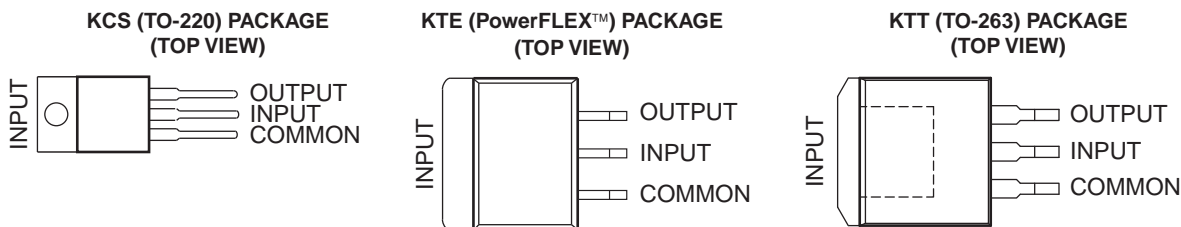


FEATURES

- 3-Terminal Regulators
- Output Current up to 1.5 A
- No External Components
- Internal Thermal-Overload Protection
- High Power-Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation



DESCRIPTION/ORDERING INFORMATION

This series of fixed-negative-voltage integrated-circuit voltage regulators is designed to complement Series μA7900 in a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 1.5 A of output current. The internal current limiting and thermal shutdown features of these regulators essentially make them immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power-pass element in precision regulators.

ORDERING INFORMATION⁽¹⁾

T _J	V _{O(NOM)}	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	–12 V	TO-220, short shoulder – KCS	Tube of 50	UA7912CKCS	UA7912C
		PowerFLEX™ – KTE	Reel of 2000	UA7908CKTER	UA7908C
	–8 V	TO-220, short shoulder – KCS	Tube of 50	UA7908CKCS	UA7908C
		PowerFLEX – KTE	Reel of 2000	UA7905CKTER	UA7905C
	–5 V	TO-220, short shoulder – KCS	Tube of 50	UA7905CKCS	UA7905C
		TO-263 – KTT	Reel of 500	UA7905CKTTR	UA7905C

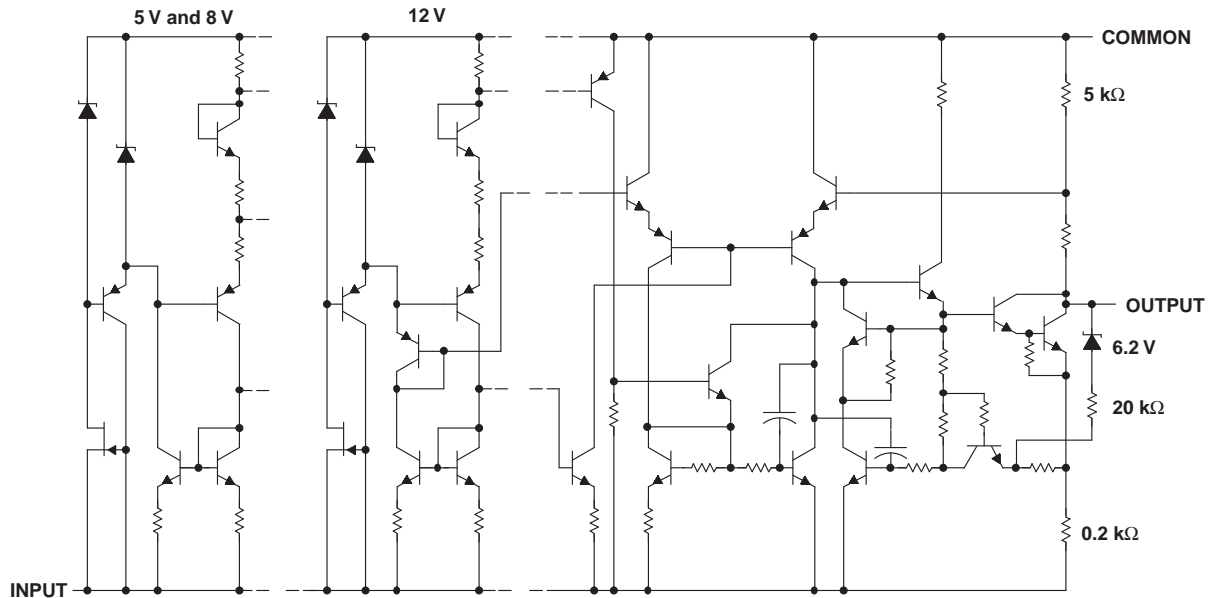
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerFLEX, PowerPAD are trademarks of Texas Instruments.

SCHEMATIC



All component values are nominal.

Absolute Maximum Ratings⁽¹⁾

over virtual junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_i	Input voltage		-35	V
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Package Thermal Data⁽¹⁾

PACKAGE	BOARD	θ_{JA}	θ_{JC}	θ_{JP} ⁽²⁾
PowerFLEX (KTE)	High K, JESD 51-5	23°C/W	3°C/W	2.7°C/W
TO-220 (KCS)	High K, JESD 51-5	19°C/W	17°C/W	3°C/W
TO-263 (KTT)	High K, JESD 51-5	25.3°C/W	18°C/W	1.94°C/W

- (1) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(2) For packages with exposed thermal pads, such as QFN, PowerPAD™, or PowerFLEX, θ_{JP} is defined as the thermal resistance between the die junction and the bottom of the exposed pad.

Recommended Operating Conditions

		MIN	MAX	UNIT	
V_i	Input voltage	μA7905	-7	-25	V
		μA7908	-10.5	-25	
		μA7912	-14.5	-30	
I_O	Output current		1.5	A	
T_J	Operating virtual junction temperature	0	125	°C	

μA7905 Electrical Characteristics

at specified virtual junction temperature, $V_I = -10\text{ V}$, $I_O = 500\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_J^{(1)}$	μA7905C			UNIT
			MIN	TYP	MAX	
Output voltage ⁽²⁾	$I_O = 5\text{ mA to }1\text{ A}$, $V_I = -7\text{ V to }-20\text{ V}$, $P_D \leq 15\text{ W}$	25°C	-4.8	-5	-5.2	V
		0°C to 125°C	-4.75		-5.25	
Input regulation	$V_I = -7\text{ V to }-25\text{ V}$			12.5	50	mV
	$V_I = -8\text{ V to }-12\text{ V}$			4	15	
Ripple rejection	$V_I = -8\text{ V to }-12\text{ V}$, $f = 120\text{ Hz}$	0°C to 125°C	54	60		dB
Output regulation	$I_O = 5\text{ mA to }1.5\text{ A}$			15	100	mV
	$I_O = 250\text{ mA to }750\text{ mA}$			5	50	
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C		-0.4		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		125		μV
Dropout voltage	$I_O = 1\text{ A}$	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	$V_I = -7\text{ V to }-25\text{ V}$			0.15	0.5	mA
	$I_O = 5\text{ mA to }1\text{ A}$			0.08	0.5	
Peak output current		25°C		2.1		A

- (1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.
- (2) This specification applies only for dc power dissipation permitted by absolute maximum ratings.

μA7908 Electrical Characteristics

at specified virtual junction temperature, $V_I = -14\text{ V}$, $I_O = 500\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_J^{(1)}$	μA7908C			UNIT
			MIN	TYP	MAX	
Output voltage ⁽²⁾	$I_O = 5\text{ mA to }1\text{ A}$, $V_I = -10.5\text{ V to }-23\text{ V}$, $P_D \leq 15\text{ W}$	25°C	-7.7	-8	-8.3	V
		0°C to 125°C	-7.6		-8.4	
Input regulation	$V_I = -10.5\text{ V to }-25\text{ V}$			12.5	160	mV
	$V_I = -11\text{ V to }-17\text{ V}$			4	80	
Ripple rejection	$V_I = -11.5\text{ V to }-21.5\text{ V}$, $f = 120\text{ Hz}$	0°C to 125°C	54	60		dB
Output regulation	$I_O = 5\text{ mA to }1.5\text{ A}$			15	160	mV
	$I_O = 250\text{ mA to }750\text{ mA}$			5	80	
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C		-0.6		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		200		μV
Dropout voltage	$I_O = 1\text{ A}$	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	$V_I = -10.5\text{ V to }-25\text{ V}$			0.15	1	mA
	$I_O = 5\text{ mA to }1\text{ A}$			0.08	0.5	
Peak output current		25°C		2.1		A

- (1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.
- (2) This specification applies only for dc power dissipation permitted by absolute maximum ratings.

μA7900 SERIES NEGATIVE-VOLTAGE REGULATORS

SLVS058H–JUNE 1976–REVISED NOVEMBER 2006

μA7912 Electrical Characteristics

at specified virtual junction temperature, $V_I = -19\text{ V}$, $I_O = 500\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_J^{(1)}$	μA7912C			UNIT
			MIN	TYP	MAX	
Output voltage ⁽²⁾	$I_O = 5\text{ mA to }1\text{ A}$, $V_I = -14.5\text{ V to }-27\text{ V}$, $P_D \leq 15\text{ W}$	25°C	-11.5	-12	-12.5	V
		0°C to 125°C	-11.4		-12.6	
Input regulation	$V_I = -14.5\text{ V to }-25\text{ V}$			5	80	mV
	$V_I = -16\text{ V to }-22\text{ V}$			3	30	
Ripple rejection	$V_I = -15\text{ V to }-25\text{ V}$, $f = 120\text{ Hz}$	0°C to 125°C	54	60		dB
Output regulation	$I_O = 5\text{ mA to }1.5\text{ A}$			15	200	mV
	$I_O = 250\text{ mA to }750\text{ mA}$			5	75	
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C		-0.8		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		300		μV
Dropout voltage	$I_O = 1\text{ A}$	25°C		1.1		V
Bias current		25°C		2	3	mA
Bias current change	$V_I = -14.5\text{ V to }-25\text{ V}$			0.04	0.5	mA
	$I_O = 5\text{ mA to }1\text{ A}$			0.06	0.5	
Peak output current		25°C		2.1		A

- (1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.
- (2) This specification applies only for dc power dissipation permitted by absolute maximum ratings.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA7905CKCS	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	UA7905C	Samples
UA7905CKCSE3	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	UA7905C	Samples
UA7905CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	RoHS & Green	SN	Level-3-245C-168 HR	0 to 125	UA7905C	Samples
UA7908CKCS	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	UA7908C	Samples
UA7908CKCSE3	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	UA7908C	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA7905CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

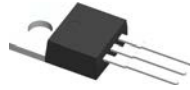
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA7905CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0

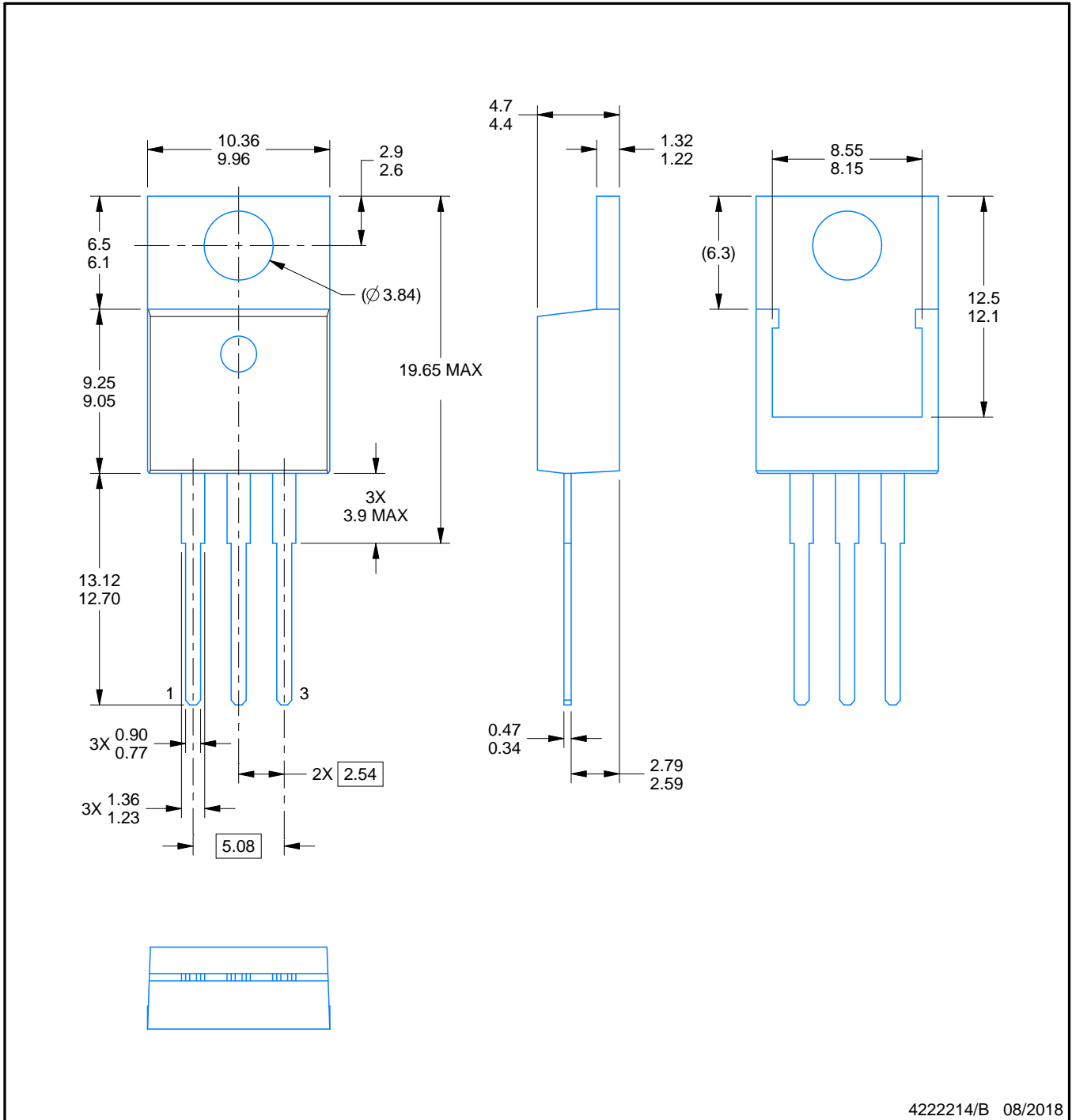
KCS0003B



PACKAGE OUTLINE

TO-220 - 19.65 mm max height

TO-220



4222214/B 08/2018

NOTES:

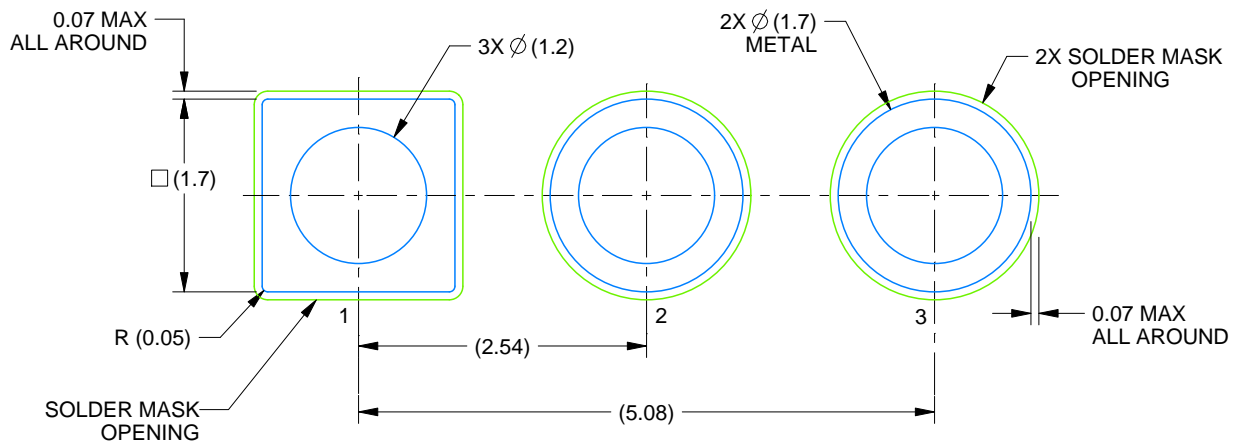
1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.

EXAMPLE BOARD LAYOUT

KCS0003B

TO-220 - 19.65 mm max height

TO-220

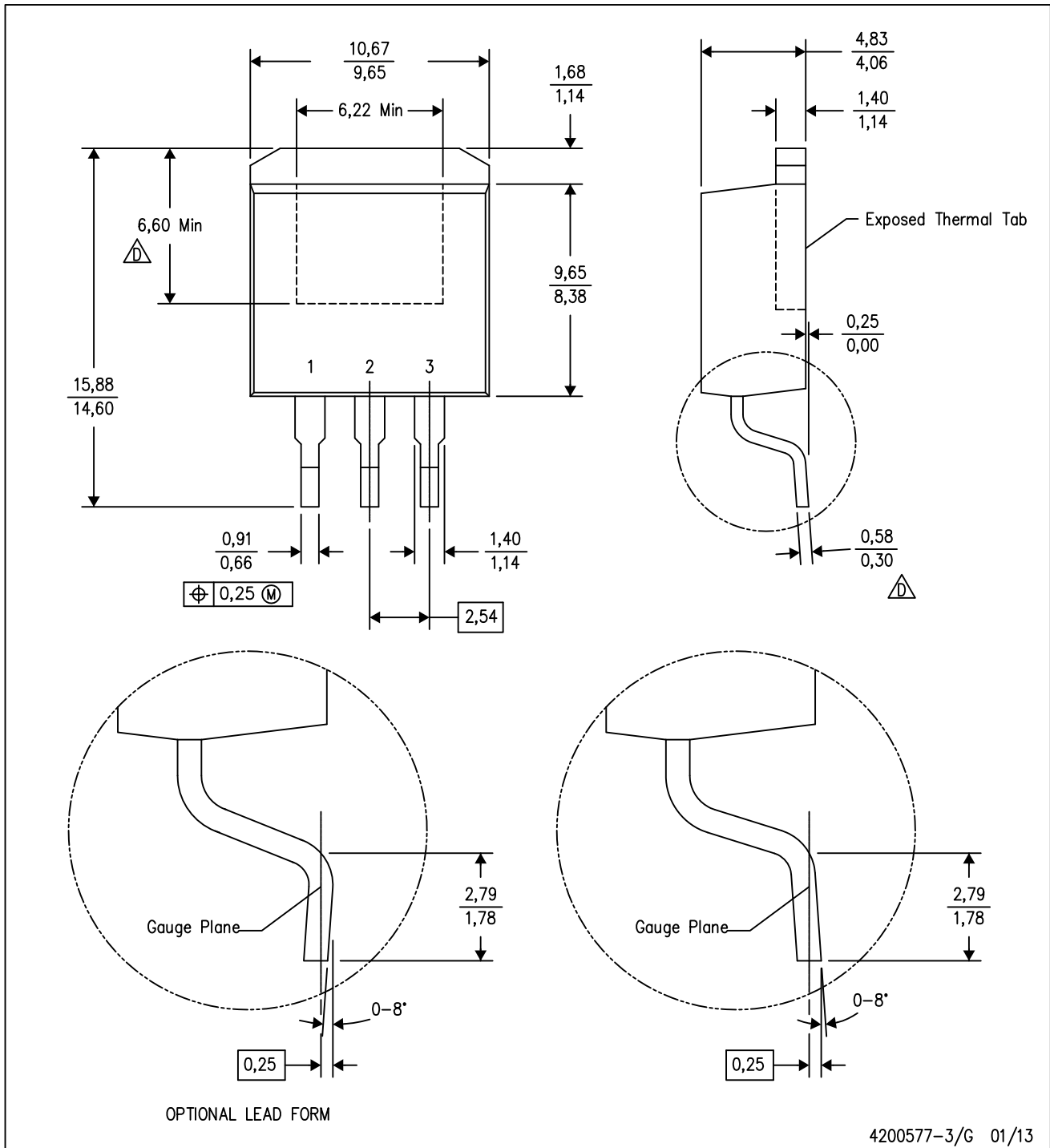


LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

4222214/B 08/2018

KTT (R-PSFM-G3)

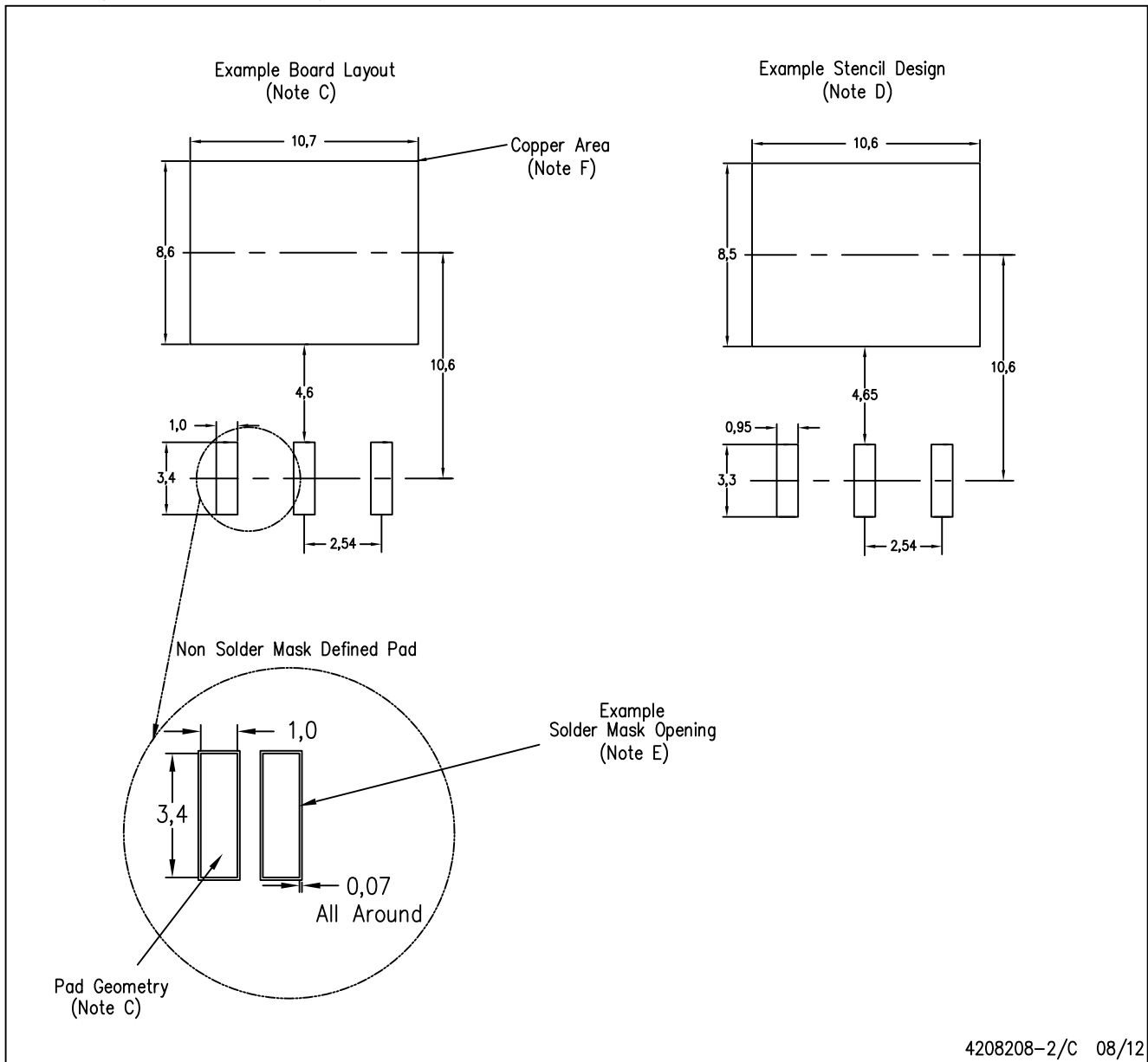
PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- △ Falls within JEDEC TO-263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-SM-782 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
 - F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated