LC²MOS, High Speed, 4-Channel/8-Channel 10-Bit ADCs

Data Sheet

AD7777/AD7778

FEATURES

AD7777: 4-channel
AD7778: 8-channel
Fast 10-bit ADC
5 V supply
Half scale conversion option
Fast interface port
Power-down mode

APPLICATIONS

Instrumentation

GENERAL DESCRIPTION

The AD7777/AD7778 are high speed, multichannel, 10-bit analog-to-digital converters (ADCs) primarily intended for use in R/W head positioning servos found in high density hard disk drives. They have unique input signal conditioning features that make them ideal for use in such single-supply applications.

By setting a bit in a control register within both the 4-channel AD7777 and the 8-channel AD7778, the input channels can be independently sampled or any two channels can be simultaneously sampled. For both the AD7777 and AD7778, the specified input signal range is $V_{BIAS} \pm V_{SWING}$. However, if the RTN pin is biased at, for example, 2 V, the analog input signal range becomes 0 V to 2 V for all input channels (see the Changing the Analog Input Voltage Range section). The bias voltage, V_{BIAS}, is the offset of the midpoint code of the ADC from ground and is supplied either by an onboard reference available to the user (REFOUT) or by an external voltage reference applied to REFIN. The full-scale range (FSR) of the ADC is equal to $2 \times V_{SWING}$ where V_{SWING} is nominally equal to REFIN/2. Additionally, when placed in the half scale conversion mode, the value of REFIN is converted, which allows the channel offsets to be measured.

Control register loading, ADC register reading, channel selection, and the conversion start are under the control of the microprocessor. The twos complement coded ADCs are easily interfaced to a standard 16-bit microprocessor unit bus via their 10-bit data port and standard microprocessor control lines.

The AD7777/AD7778 are fabricated in linear compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic.

The AD7777 is available in a 28-lead, wide-body SOIC package. The AD7778 is available in a 44-lead MQFP.

FUNCTIONAL BLOCK DIAGRAMS

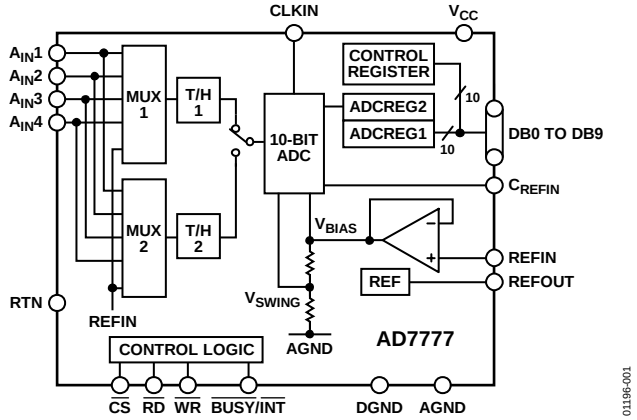

Figure 1. AD7777

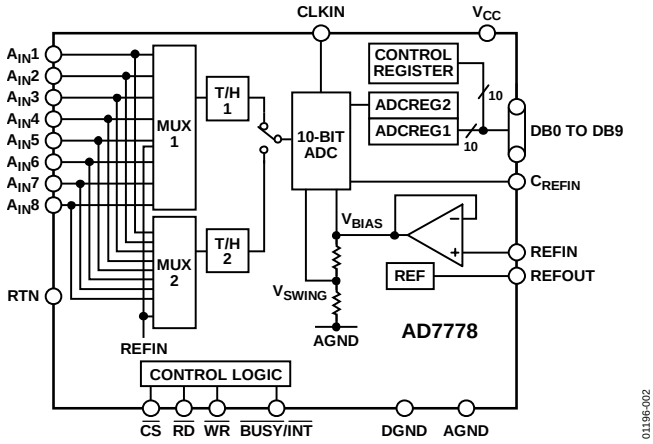

Figure 2. AD7778

Rev. B Document Feedback

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REVISION HISTORY

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SPECIFICATIONS

V_{CC} = 5 V ± 5%; AGND = DGND = 0 V; CLKIN = 8 MHz; RTN = 0 V; C_{REFIN} = 10 nF; all specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 1.

Parameter	Symbol	A Version	Unit	Test Conditions/Comments
DC ACCURACY				
Resolution[1]		10	Bits max	
Relative Accuracy		±1	LSB max	See the Terminology section
Differential Nonlinearity		±1	LSB max	No missing codes; see Terminology
Bias Offset Error		±12	LSB max	See the Terminology section
Bias Offset Error Match		10	LSB max	Between channels, see the Terminology section
Positive or Negative Full-Scale Error		±12	LSB max	See the Terminology section
Positive or Negative Full-Scale Error Match		10	LSB max	Between channels, see the Terminology section
ANALOG INPUTS				
Input Voltage Range				
All Inputs		$V_{BIAS} \pm V_{SWING}$	V min/max	
Input Current		200	µA max	$V_{IN} = V_{BIAS} \pm V_{SWING}$; any channel
REFERENCE INPUT				
REFIN		1.9/2.1	V min/max	For specified performance
REFIN Input Current		200	µA max	
REFERENCE OUTPUT				
REFOUT		1.9/2.1	V min/max	Nominal REFOUT = 2.0 V
DC Output Impedance		5	Ω typ	
Reference Load Change		±2	mV max	For reference load current change of 0 µA to ±500 µA
		±5	mV max	For reference load current change of 0 mA to ±1 mA, do not change the reference load during conversion
Short Circuit Current[2]		20	mA max	See the Terminology section
LOGIC OUTPUTS				
DB0 to DB9, $\overline{BUSY}/\overline{INT}$				
Output Low Voltage	V_{OL}	0.4	V max	Since current (I_{SINK}) = 1.6 mA
Output High Voltage	V_{OH}	4.0	V min	Source current (I_{SOURCE}) = 200 µA
Floating State Leakage Current		±10	µA max	
Floating State Capacitance[2]		10	pF max	
ADC Output Coding		Twos complement		
LOGIC INPUTS				
DB0 to DB9, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, CLKIN				
Input Low Voltage	V_{INL}	0.8	V max	
Input High Voltage	V_{INH}	2.4	V min	
Input Leakage Current		10	µA max	
Input Capacitance[2]		10	pF max	
CONVERSION TIMING				
Acquisition Time		4.5 t_{CLKIN}	ns min	See the Terminology section
		5.5 t_{CLKIN} + 70	ns max	
Single Conversion		14 t_{CLKIN}	ns max	
Double Conversion		28 t_{CLKIN}	ns max	
Period of CLKIN Input Clock	t_{CLKIN}	125/500	ns min/max	
Minimum High Time for CLKIN		50	ns min	
Minimum Low Time for CLKIN		40	ns min	

Parameter	Symbol	A Version	Unit	Test Conditions/Comments
POWER REQUIREMENTS				
V_{CC} Range		4.75/5.25	V min/max	For specified performance
Supply Current	I_{CC}			
Normal Mode		15	mA max	$\overline{CS}$ = $\overline{RD}$ = 5 V, CR8 = 0
Power-Down Mode		1.5	mA max	CR8 = 1, all linear circuitry off
Power-Up Time to Operational Specifications		500	µs max	From power-down mode
DYNAMIC PERFORMANCE				See the Terminology section
Signal-to-Noise-and-Distortion Ratio	SINAD	−56	dB min	V_{IN} = 99.88 kHz full-scale sine wave with sampling frequency ($f_{SAMPLING}$) = 380.95 kHz
Total Harmonic Distortion	THD	−60	dB min	V_{IN} = 99.88 kHz full-scale sine wave with $f_{SAMPLING}$ = 380.95 kHz
Intermodulation Distortion	IMD	−75	dB typ	fa = 103.2 kHz, fb = 96.5 kHz with $f_{SAMPLING}$ = 380.95 kHz, both signals are sine waves at half scale amplitude
Channel to Channel Isolation		−90	dB typ	V_{IN} = 100 kHz full-scale sine wave with $f_{SAMPLING}$ = 380.95 kHz

[1] 1 LSB = (2 × V_{SWING})/1024 = 1.95 mV for V_{SWING} = 1.0 V.
[2] Guaranteed by design, not production tested.

TIMING SPECIFICATIONS

V_{CC} = +5 V ± 5%; AGND = DGND = 0 V; all specifications T_{MIN} to T_{MAX} (−40°C to +85°C), unless otherwise noted.

Table 2.

Parameter[1, 2]	Symbol	Limit at T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
INTERFACE TIMING				
$\overline{CS}$ Falling Edge to $\overline{WR}$ or $\overline{RD}$ Falling Edge	t_1	0	ns min	
$\overline{WR}$ or $\overline{RD}$ Rising Edge to $\overline{CS}$ Rising Edge	t_2	0	ns min	
$\overline{WR}$ Pulse Width	t_3	53	ns min	
$\overline{CS}$ or $\overline{RD}$ Active to Valid Data[3, 4]	t_4	60	ns max	Timed from whichever occurs last
Bus Relinquish Time after $\overline{RD}$[3, 5]	t_5	10	ns min	
		45	ns max	
Data Valid to $\overline{WR}$ Rising Edge	t_6	55	ns min	
Data Valid after $\overline{WR}$ Rising Edge	t_7	10	ns min	
$\overline{WR}$ Rising Edge to $\overline{BUSY}$ Falling Edge	t_8	1.5 t_{CLKIN}	ns min	CR9 = 0
		2.5 t_{CLKIN} + 70	ns max	
$\overline{WR}$ Rising Edge to $\overline{BUSY}$ Rising Edge or $\overline{INT}$ Falling Edge	t_9	19.5 t_{CLKIN} + 70	ns max	Single conversion, CR6 = 0
	t_{10}	33.5 t_{CLKIN} + 70	ns max	Double conversion, CR6 = 1
$\overline{WR}$ or $\overline{RD}$ Falling Edge to $\overline{INT}$ Rising Edge	t_{11}	60	ns max	CR9 = 1

[1] See Figure 3 to Figure 5.
[2] All input signals are specified with rise time (t_R) = fall time (t_F) = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[3] 100% production tested. All other times are guaranteed by design, but not production tested.
[4] t_4 is measured with the load circuit of Figure 6 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[5] t_5 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 6. The measured time is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that t_5 is the true bus relinquish time of the device and, as such, is independent of the external bus loading capacitance.

Timing Diagrams

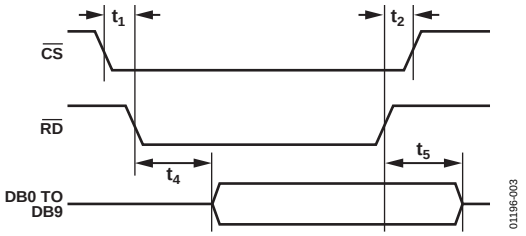


Figure 3. Read Cycle Timing

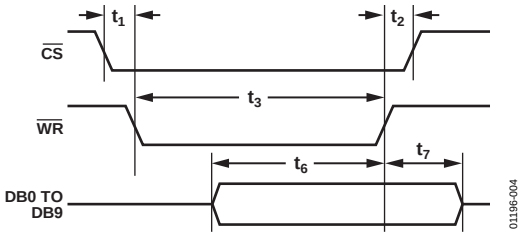


Figure 4. Write Cycle Timing

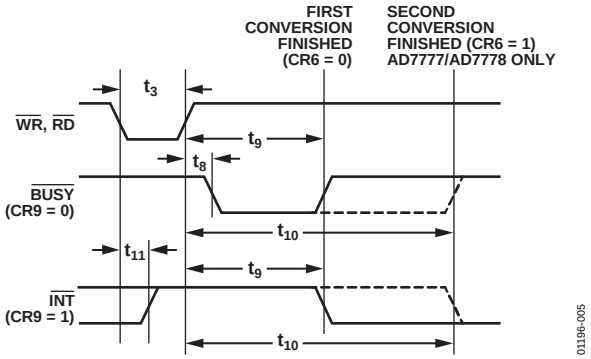


Figure 5. $\overline{BUSY}$/$\overline{INT}$ Timing

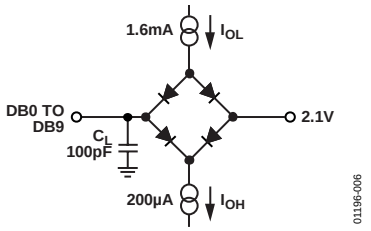


Figure 6. Load Circuit for Bus Timing Characteristics

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC} to AGND or DGND	−0.3 V to +7 V
AGND, RTN to DGND	−0.3 V to V_{CC} + 0.3 V
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, CLKIN, DB0 to DB9, $\overline{BUSY}$/$\overline{INT}$ to DGND	−0.3 V to V_{CC} + 0.3 V
Analog Input Voltage to AGND	−0.3 V to V_{CC} + 0.3 V
REFOUT to AGND	−0.3 V to V_{CC} + 0.3 V
REFIN to AGND	−0.3 V to V_{CC} + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
SOIC Package, Power Dissipation	875 mW
θ_{JA} Thermal Impedance	75°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
MQFP Package, Power Dissipation	500 mW
θ_{JA} Thermal Impedance	95°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

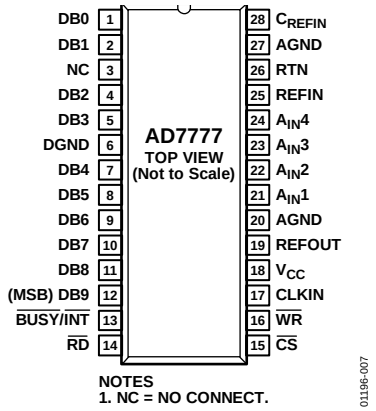


Figure 7. AD7777 Pin Configuration

Table 4. AD7777 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4, 5, 7 to 12	DB0 to DB9	Input/Output Data Bus. This is a bidirectional data port from which ADC output data can be read and to which control register data can be written. DB9 is the MSB.
3	NC	No Connect.
6	DGND	Digital Ground. DGND is the ground reference for the digital circuitry.
13	$\overline{BUSY}/\overline{INT}$	Busy/Interrupt Output. Active low logic output indicating ADC status. This logic output has two modes of operation, depending on whether CR9 of the control register is set low or high, as follows: If CR9 is set low, the $\overline{BUSY}/\overline{INT}$ output behaves as a $\overline{BUSY}$ signal. The $\overline{BUSY}$ signal goes low and stays low for the duration of a single conversion. If simultaneous sampling is selected, $\overline{BUSY}$ stays low for the duration of both conversions. If CR9 is set high, $\overline{BUSY}/\overline{INT}$ output behaves as an interrupt signal. The $\overline{INT}$ signal goes low and remains low after either a single conversion is completed or after a double conversion is completed if simultaneous sampling is selected. With CR9 high, the falling edge of $\overline{WR}$ or $\overline{RD}$ resets the $\overline{INT}$ line high.
14	$\overline{RD}$	Read Input (Active Low). $\overline{RD}$ is used in conjunction with $\overline{CS}$ to enable the data outputs from the ADC registers.
15	$\overline{CS}$	Chip Select Input. The device is selected when this input is low.
16	$\overline{WR}$	Write Input (Active Low). $\overline{WR}$ is used in conjunction with $\overline{CS}$ to write data to the control register. Data is latched to the registers on the rising edge of $\overline{WR}$. Following the rising edge of $\overline{WR}$, the analog input is acquired and a conversion is started.
17	CLKIN	Clock Input.
18	V_{CC}	5 V Power Supply.
19	REFOUT	Voltage Reference Output. This pin provides the internal voltage reference, which is nominally 2.0 V. REFOUT provides the bias voltage (V_{BIAS}) for the input channels.
20, 27	AGND	Analog Ground.
21 to 24	$A_{IN}1$ to $A_{IN}4$	Analog Input 1 to Analog Input 4. The analog input range is $V_{BIAS} \pm V_{SWING}$, where V_{BIAS} and V_{SWING} are defined by the reference voltage applied to REFIN. Input resistance between any of the analog input pins and AGND is 10 kΩ or greater.
25	REFIN	Voltage Reference Input. The AD7777 is specified over a voltage reference range of 1.9 V to 2.1 V with a nominal value of 2.0 V. This REFIN voltage provides the V_{BIAS} and V_{SWING} levels for the input channels. V_{BIAS} is equal to REFIN, and V_{SWING} is nominally equal to REFIN/2. Input resistance between this REFIN pin and AGND is 10 kΩ or greater.
26	RTN	Signal Return Path for Input Channels. Normally, RTN is connected to AGND at the package.
28	C_{REFIN}	Reference Decoupling Capacitor. A 10 nF capacitor must be connected from this pin to AGND to ensure correct operation of the high speed ADC.

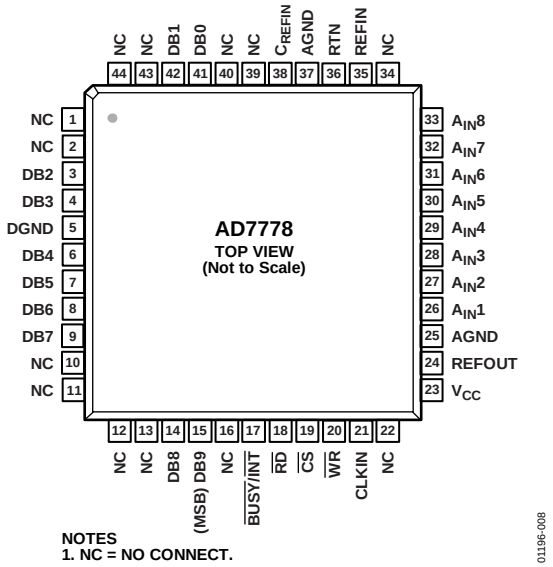


Figure 8. AD7778 Pin Configuration

Table 5. AD7778 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 10, 11 to 13, 16, 22, 34, 39, 40, 43, 44	NC	No Connect.
3, 4, 6 to 9, 14, 15, 41, 42	DB0 to DB9	Input/Output Data Bus. This is a bidirectional data port from which ADC output data can be read and to which control register data can be written. DB9 is the MSB.
5	DGND	Digital Ground. DGND is the ground reference for the digital circuitry.
17	$\overline{\text{BUSY}}/\overline{\text{INT}}$	Busy/Interrupt Output. Active low logic output indicating ADC status. This logic output has two modes of operation depending on whether CR9 of the control register is set low or high, as follows: If CR9 is set low, the $\overline{\text{BUSY}}/\overline{\text{INT}}$ output behaves as a $\overline{\text{BUSY}}$ signal. The $\overline{\text{BUSY}}$ signal goes low and stays low for the duration of a single conversion. If simultaneous sampling is selected, $\overline{\text{BUSY}}$ stays low for the duration of both conversions. If CR9 is set high, $\overline{\text{BUSY}}/\overline{\text{INT}}$ output behaves as an interrupt signal. The $\overline{\text{INT}}$ signal goes low and remains low after either a single conversion is completed or after a double conversion is completed if simultaneous sampling is selected. With CR9 high, the falling edge of $\overline{\text{WR}}$ or $\overline{\text{RD}}$ resets the $\overline{\text{INT}}$ line high.
18	$\overline{\text{RD}}$	Read Input (Active Low). $\overline{\text{RD}}$ is used in conjunction with $\overline{\text{CS}}$ to enable the data outputs from the ADC registers
19	$\overline{\text{CS}}$	Chip Select Input. The device is selected when this input is low.
20	$\overline{\text{WR}}$	Write Input (Active Low). $\overline{\text{WR}}$ is used in conjunction with $\overline{\text{CS}}$ to write data to the control register. Data is latched to the registers on the rising edge of $\overline{\text{WR}}$. Following the rising edge of $\overline{\text{WR}}$, the analog input is acquired and a conversion is started.
21	CLKIN	Clock Input.
23	V_{CC}	5 V Power Supply.
24	REFOUT	Voltage Reference Output. This pin provides the internal voltage reference, which is nominally 2.0 V. REFOUT provides the bias voltage (V_{BIAS}) for the input channels.
25, 37	AGND	Analog Ground.
26 to 33	$A_{IN}1$ to $A_{IN}8$	Analog Input 1 to Analog Input 8. The analog input range is $V_{BIAS} \pm V_{SWING}$, where V_{BIAS} and V_{SWING} are defined by the reference voltage applied to REFIN. Input resistance between any of the analog input pins and AGND is 10 kΩ or greater.
35	REFIN	Voltage Reference Input. The AD7778 is specified over a voltage reference range of 1.9 V to 2.1 V with a nominal value of 2.0 V. This REFIN voltage provides the V_{BIAS} and V_{SWING} levels for the input channels. V_{BIAS} is equal to REFIN, and V_{SWING} is nominally equal to REFIN/2. Input resistance between this REFIN pin and AGND is 10 kΩ or greater.
36	RTN	Signal Return Path for Input Channels. Normally RTN is connected to AGND at the package.
38	C_{REFIN}	Reference Decoupling Capacitor. A 10 nF capacitor must be connected from this pin to AGND to ensure correct operation of the high speed ADC.

TERMINOLOGY

Relative Accuracy
For the AD7777/AD7778, relative accuracy or endpoint nonlinearity is the maximum deviation, in LSBs, of the actual code transition points of the ADC from a straight line drawn between the endpoints of the ADC transfer function.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified maximum differential nonlinearity of ±1 LSB ensures no missed codes.

Bias Offset Error
For an ideal 10-bit ADC, the output code for an input voltage equal to V_{BIAS} is midscale. The bias offset error is the difference between the actual midpoint voltage for midscale code and V_{BIAS}, expressed in LSBs.

Bias Offset Error Match
Bias offset error match is a measure of how closely the bias offset errors of all channels track each other. The bias offset error match of any channel must be no further away than 10 LSBs from the bias offset error of any other channel, regardless of whether the channels are independently sampled or simultaneously sampled.

Positive and Negative Full-Scale Error
The input channels of the ADC can be considered to have bipolar (positive and negative) input ranges, but are referred to V_{BIAS} (or REFIN) instead of AGND. Positive full-scale error for the ADC is the difference between the actual input voltage required to produce the positive full-scale code transition and the ideal input voltage (V_{BIAS} + V_{SWING} −1.5 LSB), expressed in LSBs. Negative full-scale error is similarly specified for the minus full-scale code transition, relative to the ideal input voltage for this transition (V_{BIAS} − V_{SWING} + 0.5 LSB). Note that the full-scale errors for the ADC input channels are measured after their respective bias offset errors have been adjusted out.

Positive and Negative Full-Scale Error Match
Positive and negative full-scale error match is a measure of how closely the full-scale errors of all channels track each other. The full-scale error match of any channel must be no further than 10 LSBs from the respective full-scale error of any other channel, regardless of whether the channels are independently sampled or simultaneously sampled.

Short-Circuit Current
Short-circuit current is defined as the maximum current that flows either into or out of the REFOUT pin if this pin is shorted to any potential between 0 V and V_{CC}. This condition can be allowed for up to 10 sec provided that the power dissipation of the package is not exceeded.

Signal-to-Noise-and-Distortion (SINAD) Ratio
SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics, but excluding dc. The value for SINAD is given in decibels.

Total Harmonic Distortion, THD
Total harmonic distortion is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels. For the AD7777/ AD7778, total harmonic distortion (THD) is defined as

$$20 \log \frac{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2\right)}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the individual harmonics.

Intermodulation Distortion, IMD
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products, of order (m + n), at sum and difference frequencies of mfa + nfb, where m and n = 0, 1, 2, 3. Intermodulation terms are those for which m or n is not equal to zero. For example, the second-order terms include (fa + fb) and (fa – fb) and the third-order terms include (2 fa + fb), (2 fa – fb), (fa + 2 fb), and (fa – 2 fb).

Channel to Channel Isolation
Channel to channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 100 kHz sine wave signal to any one of the input channels and monitoring the remaining channels. The figure given is the worst case across channels.

THEORY OF OPERATION

ADC TRANSFER FUNCTION

For the AD7777/AD7778, an input signal of the form $V_{BIAS} \pm V_{SWING}$ is expected. This V_{BIAS} signal level operates as a pseudoground to which all input signals must be referred. The V_{BIAS} level is determined by the voltage applied to the REFIN pin. The REFIN pin can be driven by an external voltage source or, alternatively, by the on-board 2 V reference, available at REFOUT. The magnitude of the input signal swing is equal to $V_{BIAS}/2$ (or REFIN/2) and is set internally. With a REFIN of 2 V, the analog input signal level varies from 1 V to 3 V, that is, 2 ± 1 V. Figure 9 shows the transfer function of the ADC and its relationship to V_{BIAS} and V_{SWING}. The half scale twos complement code of the ADC (0x000 or 00 0000 0000 binary), occurs at an input voltage equal to V_{BIAS}. The input FSR of the ADC is equal to 2 V_{SWING}, so that the positive full-scale transition (0x1FE to 0x1FF) occurs at a voltage equal to $V_{BIAS} + V_{SWING} - 1.5$ LSBs, and the negative full-scale code transition (0x200 to 0x201) occurs at a voltage = $V_{BIAS} - V_{SWING} + 0.5$ LSBs.

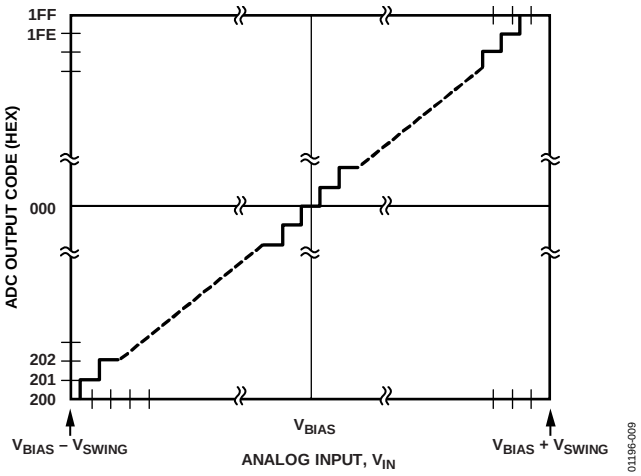


Figure 9. ADC Transfer Function

CONTROL REGISTER

The control register is 10 bits wide and can only be written to. On power-on, all bit locations in the control register are automatically loaded with 0s. For the quad channel AD7777, CR2 and CR5 are don't care bits. Individual bit functions are described in the following sections.

CR0 TO CR2

CR0 to CR2 determine which channel is selected and converted for single-channel operation. For simultaneous sampling operation, CR0 to CR2 hold the address of one of the two channels to be sampled.

Table 6. AD7777 CR0 to CR2 Bit Descriptions

CR2	CR1	CR0	Description
X[1]	0	0	Select $A_{IN}1$
X[1]	0	1	Select $A_{IN}2$
X[1]	1	0	Select $A_{IN}3$
X[1]	1	1	Select $A_{IN}4$

[1] X means don't care.

Table 7. AD7778 CR0 to CR2 Bit Descriptions

CR2	CR1	CR0	Description
0	0	0	Select $A_{IN}1$
0	0	1	Select $A_{IN}2$
0	1	0	Select $A_{IN}3$
0	1	1	Select $A_{IN}4$
1	0	0	Select $A_{IN}5$
1	0	1	Select $A_{IN}6$
1	1	0	Select $A_{IN}7$
1	1	1	Select $A_{IN}8$

CR3 TO CR5

CR3 to CR5 are only applicable for simultaneous sampling with the AD7777 or AD7778 when CR3 to CR5 hold the address of the second channel to be sampled.

Table 8. AD7777 CR3 to CR5 Bit Descriptions

CR5	CR4	CR3	Description
X[1]	0	0	Select $A_{IN}1$
X[1]	0	1	Select $A_{IN}2$
X[1]	1	0	Select $A_{IN}3$
X[1]	1	1	Select $A_{IN}4$

[1] X means don't care.

Table 9. AD7778 CR3 to CR5 Bit Descriptions

CR5	CR4	CR3	Description
0	0	0	Select $A_{IN}1$
0	0	1	Select $A_{IN}2$
0	1	0	Select $A_{IN}3$
0	1	1	Select $A_{IN}4$
1	0	0	Select $A_{IN}5$
1	0	1	Select $A_{IN}6$
1	1	0	Select $A_{IN}7$
1	1	1	Select $A_{IN}8$

CR6

CR6 determines whether operation is on a single channel or simultaneous sampled on two channels.

Table 10.

CR6	Description
0	Single-channel operation. The channel select address is contained in CR0 to CR2.
1	Two channels simultaneously sampled and sequentially converted. The channel select addresses is contained in CR0 to CR2 and CR3 to CR5.

CR7

CR7 determines whether the device is in the normal operating mode or in the half scale test mode.

Table 11. CR7 Bit Descriptions

CR7	Description
0	Normal operating mode
1	Half scale test mode

In the half scale test mode, REFIN is internally connected as an analog input. In this mode, CR0 to CR2 and CR3 to CR5 are all don't care bits because it is REFIN that is converted. For the AD7777 and AD7778, the contents of CR6 still determine whether a single or a double conversion is carried out on the REFIN level.

CR8

CR8 determines whether the device is in the normal operating mode or in the power-down mode.

Table 12. CR8 Bit Descriptions

CR8	Description
0	Normal operating mode
1	Power-down mode

In the power-down mode, all linear circuitry is turned off and the REFOUT output is weakly (5 kΩ) pulled to AGND. The input impedance of the analog inputs and of the REFIN input remains the same in either normal mode or power-down mode (see the Power-Down section).

CR9

CR9 determines whether the $\overline{\text{BUSY}}/\overline{\text{INT}}$ output flag goes low and remains low during conversions or goes low and remains low after the conversions are complete.

Table 13. CR9 Bit Descriptions

CR9	$\overline{\text{BUSY}}/\overline{\text{INT}}$ Functionality
0	Output goes low and remains low during conversions.
1	Output goes low and remains low after conversions are complete.

ADC CONVERSION START TIMING

Figure 10 shows the operating waveforms for the start of a conversion cycle. On the rising edge of $\overline{WR}$, the conversion cycle starts with the acquisition and tracking of the selected ADC channel, $A_{IN}1$ to $A_{IN}8$. The analog input voltage is held 40 ns (typically) after the first rising edge of CLKIN following four complete CLKIN cycles. If t_D (time between $\overline{WR}$ rising and the first falling edge of CLKIN, as shown in Figure 10) is greater than 12 ns, the falling edge of CLKIN is seen as the first falling clock edge. If t_D is less than 12 ns, the first falling clock edge to be recognized does not occur until one cycle later.

Following the hold on the analog inputs, two complete CLKIN cycles are elapse for settling purposes before the conversion of the MSB is completed. The conversion of the MSB occurs approximately 40 ns after the rising edge of CLKIN, as shown in Figure 10. It takes up to two more CLKIN cycles for the second MSB conversion. The succeeding bit decisions are made approximately 40 ns after each rising edge of CLKIN until the conversion is complete.

At the end of conversion, if a single conversion is requested (CR6 = 0), the $\overline{BUSY}/\overline{INT}$ line changes state (as programmed by CR9) and the successive approximation register (SAR) contents are transferred to ADC Register 1, ADCREG1. The SAR is then reset in readiness for a new conversion. If simultaneous sampling is requested (CR6 = 1), no change occurs in the status of the $\overline{BUSY}/\overline{INT}$ output, and the ADC automatically starts the second conversion. At the end of this conversion, the $\overline{BUSY}/\overline{INT}$ line changes state (as programmed by CR9) and the SAR contents are transferred to ADC Register 2, ADCREG2.

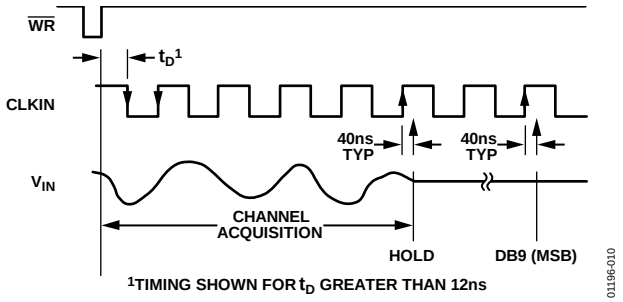


Figure 10. ADC Conversion Start Timing

TRACK-AND-HOLD

The track-and-hold amplifiers on the analog inputs of the AD7777/AD7778 allow the ADC to accurately convert an input sine wave of 2 V p-p amplitude up to a frequency of 189 kHz, the Nyquist frequency of the ADC when operated at its maximum throughput rate of 378 kHz. This maximum rate of conversion includes conversion time and the time between conversions. Because the input bandwidth of the track-and-hold is much greater than 189 kHz, the input signal must be band limited to avoid folding unwanted signals into the band of interest.

POWER-DOWN

The AD7777/AD7778 can be placed in a power-down mode simply by writing a logic high to CR8 of the control register. The following changes are effected immediately upon writing a 1 to CR8:

- Any conversion in progress is terminated.
- If a conversion is in progress, the leading edge of $\overline{WR}$ immediately drives the $\overline{BUSY}/\overline{INT}$ output high.
- All the linear circuitry is turned off.
- The REFOUT output stops being driven and is weakly (5 kΩ) pulled to analog ground.

The control inputs ($\overline{CS}$, $\overline{WR}$, and $\overline{RD}$) retain their functions as inputs while the AD7777/AD7778 are in power-down mode. If no conversions are in progress when the AD7777/AD7778 are placed into power-down mode, the contents of the ADC registers, ADCREG1 and ADCREG2, are retained during power-down and can be read as normal. On returning to normal operating mode, a new conversion (or conversions, dependent on CR6) is automatically started. Upon completion, the invalid conversion results are loaded into the ADC registers, losing the previous valid results.

To achieve the lowest possible power consumption in the power-down mode, attention must be paid to the state of the digital and analog inputs and outputs, as follows:

- Because each analog input channel is connected to AGND via a resistive divider (the input resistance of which does not change between normal and power-down modes), driving the analog input signals to 0 V or as close as possible to 0 V minimizes the power dissipated in the input signal conditioning circuitry.
- Similarly, the REFIN input is connected to AGND via a resistive divider, the input resistance of which does not change between normal and power-down modes. If an external reference is being used, driving this reference input to 0 V or as close as possible to 0 V minimizes the power dissipated in the input signal conditioning circuitry.
- Because the REFOUT pin is typically pulled to AGND via a 5 kΩ resistor, any voltage greater than 0 V to which this output may be pulled by external circuitry dissipates unnecessary power.
- Hold all digital inputs ($\overline{CS}$, $\overline{WR}$, and $\overline{RD}$) at V_{CC} or as close as possible. Hold CLKIN as close as possible to either 0 V or V_{CC}.
- Because the $\overline{BUSY}/\overline{INT}$ output is actively driven to a logic high, any loading on this pin to 0 V dissipates power.

The AD7777/AD7778 comes out of the power-down mode when a Logic 0 is written to CR8 of the control register. Note that the contents of the other bits in the control register are retained when the device is placed in power-down and are valid when power is restored. However, coming out of power-down

provides an opportunity to reload the complete contents of the control register without any extra instructions.

MICROPROCESSOR INTERFACING CIRCUITS

The AD7777/AD7778 family of ADCs is intended to interface to digital signal processors (DSPs) such as the TMS320 family and microcontrollers such as the 80C196 family.

Figure 11 shows the AD7777/AD7778 interfaced to the TMS320C10 at 20.5 MHz and the TMS320C14 at 25 MHz. Figure 12 shows the interface with the TMS320C25 at 40 MHz. Note that one wait state is required with this interface.

Figure 13 shows the interface with the 80C196KB at 12 MHz and the 80C196KC at 16 MHz. One wait state is required with the 16 MHz microcontroller. The 80C196 is configured to operate with a 16-bit multiplexed address/data bus.

Table 14 provides a truth table for the AD7777/AD7778 and summarizes their microprocessor interfacing features. Note that a read instruction to any of the devices while a conversion is in progress immediately stops that conversion and returns unreliable data over the data bus.

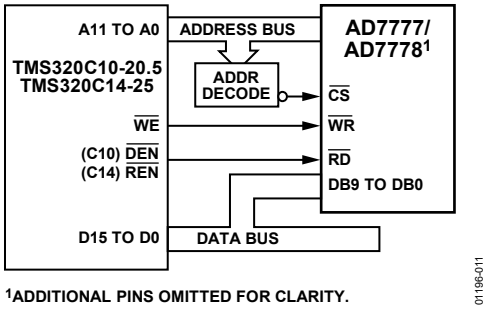


Figure 11. AD7777/AD7778 to TMS320C10 and TMS320C14 Interface

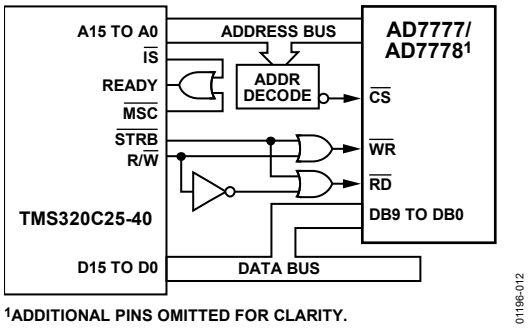


Figure 12. AD7777/AD7778 to TMS320C25 Interface

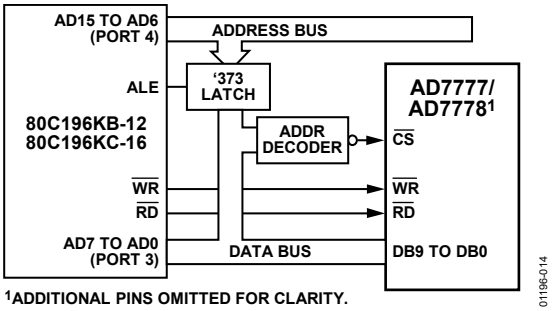


Figure 13. AD7777/AD7778 to 80C196KB/802C196KC Interface

Table 14. AD7777/AD7778 Truth Table for Microprocessor Interfacing

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	DB0 to DB9	Function/Comments
1	X[1]	X[1]	High Z	Data port high impedance
0	1	High to low	CR Data	Load control register data to the control register and start a conversion.
0	Low to high	1	ADC data	ADC data placed on data bus. Depending upon CR6 of the control register, one or two read instructions are required. If CR6 is low, that is, with single-channel conversion selected, a read instruction returns the contents of ADCREG1. Succeeding read instructions continue to return the contents of ADCREG1. If CR6 is high, that is, simultaneous sampling (double conversion) selected, the first read instruction returns the contents of ADCREG1, whereas the second read instruction returns the contents of ADCREG2. A third read instruction returns ADCREG1 again, the fourth ADCREG2, and so on.

[1] X means don't care.

APPLICATIONS INFORMATION

DIGITAL SIGNAL PROCESSING APPLICATIONS

In digital signal processing application areas like voice recognition, echo cancellation, and adaptive filtering, the dynamic characteristics (SINAD, THD, and IMD) of the ADC are critical. The AD7777/AD7778 are specified dynamically as well as with standard dc specifications. Because the track-and-hold amplifier has a wide bandwidth, place an antialiasing filter on the analog inputs to avoid aliasing high frequency noise back into the bands of interest.

The dynamic performance of the ADC is evaluated by applying a sine wave signal of very low distortion to a single analog input which is sampled at 380.95 kHz. A fast Fourier transform (FFT) plot or histogram plot is then generated from which the SINAD, harmonic distortion, and dynamic differential nonlinearity data can be obtained. Similarly, for intermodulation distortion, an input signal consisting of two pure sine waves at different frequencies is applied to the AD7777/AD7778.

Figure 14 shows a 2048-point FFT plot for a single channel of the AD7777/AD7778 with an input signal of 99.88 kHz. The SNR is 58.7 dB. Figure 14 shows that most of the harmonics are buried in the noise floor. The harmonics are taken into account when calculating the SINAD.

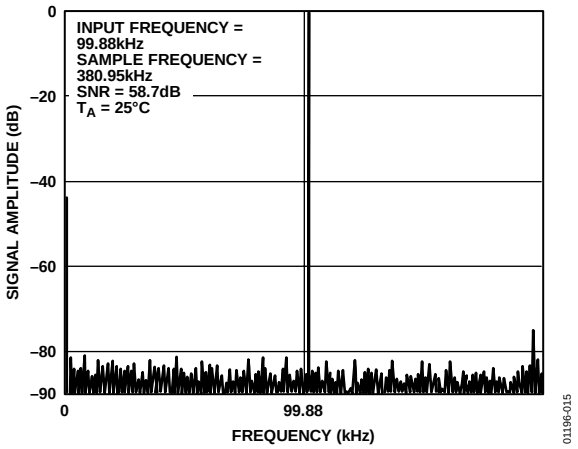


Figure 14. ADC FFT Plot

The relationship between SINAD and resolution (n) is expressed by the following equation:

$$SINAD = (6.02n + 1.76)\ \text{dB} \quad (1)$$

This equation is for an ideal device with no differential or integral linearity errors. These errors cause a degradation in SINAD. By working backward from Equation 1, it is possible to measure the ADC performance expressed in effective number of bits (n).

$$n(effective) = \frac{SINAD - 1.76}{6.02}$$

where *SINAD* is given in decibels.

The effective number of bits vs. input frequency for a single channel of the AD7777/AD7778 is shown in Figure 15. The effective number of bits is typically 9.5.

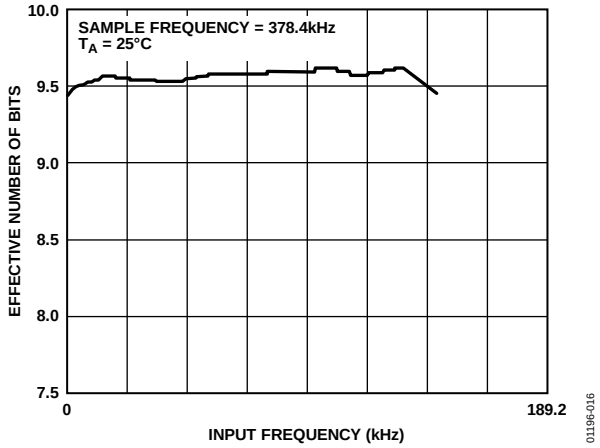


Figure 15. Effective Number of Bits vs. Input Frequency

Changing the Analog Input Voltage Range

By biasing the RTN pin above AGND, it is possible to change the analog input voltage range from its $V_{BIAS} \pm V_{SWING}$ format to a more traditional 0 V to reference voltage range. The new input range can be described as offset voltage (V_{OFFSET}) to (V_{OFFSET} + REFIN), where $0\ V \le V_{OFFSET} \le 1\ V$.

To produce this range, the RTN pin must be biased to (REFIN – $2 \times V_{OFFSET}$). For instance, if RTN is tied to REFOUT, the analog input range becomes 0 V to 2 V. The fixed 2 V analog input voltage span of the ADC can range from 1 V to 3 V (RTN = 0 V) to 0 V to 2 V (RTN = 2 V), that is, with proper biasing, an input signal range from 0.3 V to 2.3 V can be covered. Both the relative accuracy and differential nonlinearity performance remain essentially unchanged in this mode, whereas the SNR and THD performance are typically 2 dB to 3 dB worse than typical.

LAYOUT HINTS

Ensure that the digital and analog grounds are separated as much as possible in the layout for the printed circuit board. Take care not to run any digital tracks along an analog signal track. Guard (screen) the analog inputs with RTN.

Establish a single-point analog ground separate from the logic system ground and as close as possible to the AD7777/AD7778. Connect both the RTN and AGND pins on the AD7777/AD7778 and all other signal grounds to this single-point analog ground. In turn, connect this star ground to the digital ground at one point only, preferably at the low impedance power supply itself.

Low impedance analog and digital power supply common returns are important for correct operation of the devices. Therefore, make the foil width for these tracks as wide as possible.

To ensure a low impedance 5 V power supply at the actual V_{CC} pin, it is necessary to use bypass capacitors from the pin itself to DGND. A 4.7 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor is sufficient.

ADC CORRUPTION

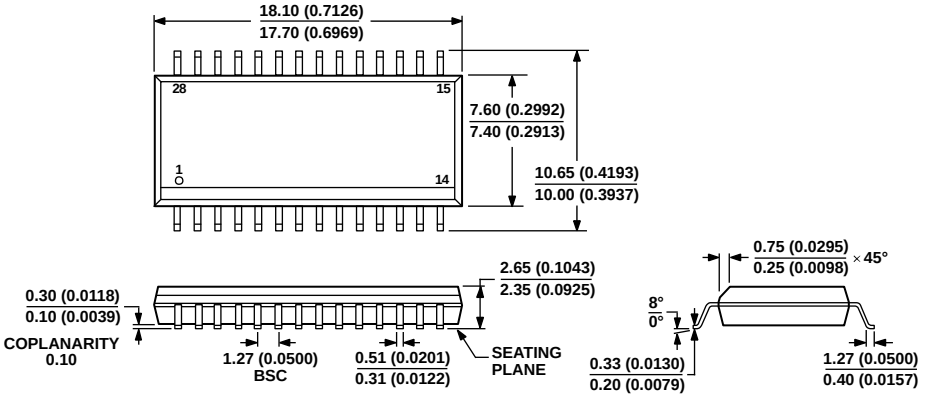
Executing a read instruction to the AD7777/AD7778 while a conversion is in progress immediately halts the conversion and returns invalid data over the data bus. Monitor the $\overline{BUSY}/\overline{INT}$ output pin closely and prevent all read instructions to the AD7777/AD7778 when this output shows that a conversion is in progress.

Executing a write instruction to the AD7777/AD7778 while a conversion is in progress immediately halts the conversion when the falling edge of $\overline{WR}$ is driving the $\overline{BUSY}/\overline{INT}$ output high. The analog input is sampled as normal, and a new conversion sequence (dependent upon CR6) starts.

ADC CONVERSION TIME

Although each conversion takes only 14 CLKIN cycles, it can take between 4.5 and 5.5 CLKIN cycles to acquire the analog inputs after the $\overline{WR}$ input goes high and before any conversions start.

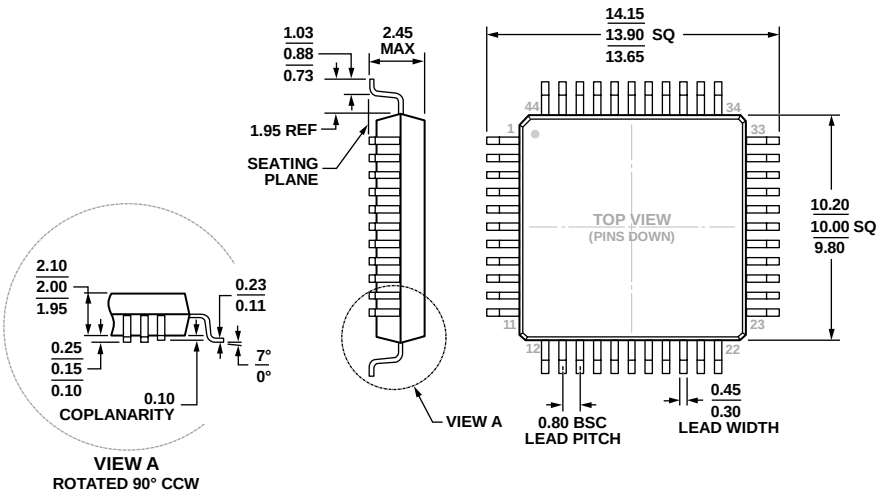
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AE
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

06-07-2006-A

Figure 16. 28-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-28)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-112-AA-2

06-10-20014-B

Figure 17. 44-Lead Metric Quad Flat Package [MQFP]
(S-44-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	No. of Channels	Package Description	Package Option
AD7777ARZ	−40°C to +85°C	4	28-Lead Standard Small Outline Package [SOIC_W]	RW-28
AD7777ARZ-REEL	−40°C to +85°C	4	28-Lead Standard Small Outline Package [SOIC_W]	RW-28
AD7778ASZ	−40°C to +85°C	8	44-Lead Metric Quad Flat Package [MQFP]	S-44-2

[1] Z = RoHS Compliant Part.

D01196-4/20(B)

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