

# PSMN3R4-30BLE

N-channel 30 V 3.4 m $\Omega$  logic level MOSFET in D2PAK **Product data sheet** 

#### 1. **Product profile**

### 1.1 General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

#### 1.2 Features and benefits

- Enhanced forward biased safe operating area for superior linear mode operation
- Very low Rdson for low conduction losses

### 1.3 Applications

- Electronic fuse
- Hot swap
- Load switch
- Soft start

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	-	30	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V; <u>Fig. 1</u>	[1]	-	-	120	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	-	178	W
Static charact	eristics						
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ Fig. 12		-	2.95	3.4	mΩ
		$V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 12		-	4.25	5	mΩ
Dynamic char	acteristics						
$Q_{GD}$	gate-drain charge	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; V <sub>DS</sub> = 15 V; Fig. 14; Fig. 15		-	12.2	-	nC
Q <sub>G(tot)</sub>	total gate charge	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; V <sub>DS</sub> = 15 V; Fig. 14; Fig. 15		-	81	-	nC



Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Avalanche ruggedness							
E <sub>DS(AL)S</sub>	non-repetitive drain- source avalanche energy	$V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_D$ = 120 A; $V_{sup} \le$ 30 V; unclamped; $R_{GS}$ = 50 Ω; Fig. 3		-	-	246	mJ

[1] Capped at 120A due to package

### 2. Pinning information

**Table 2.** Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D I
2	D	drain[1]		
3	S	source		G TITA
mb	D	mounting base; connected to drain	1 3 D2PAK (SOT404)	mbb076 S

[1] It is not possible to make connection to pin 2.

### 3. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PSMN3R4-30BLE	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404		

## 4. Marking

#### Table 4. Marking codes

Type number	Marking code
PSMN3R4-30BLE	PSMN3R4-30BLE

### 5. Limiting values

### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	30	V
$V_{DGR}$	drain-gate voltage	$T_j \le 175 ^{\circ}\text{C}; T_j \ge 25 ^{\circ}\text{C}; R_{GS} = 20 \text{k}\Omega$	-	30	V

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Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>GS</sub>	gate-source voltage			-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <u>Fig. 1</u>		-	119	Α
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>	[1]	-	120	Α
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 °C$ ; Fig. 4		-	672	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	178	W
T <sub>stg</sub>	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
T <sub>sld(M)</sub>	peak soldering temperature			-	260	°C
Source-dra	in diode		1			
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[1]	-	120	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$		-	672	Α
Avalanche	ruggedness		1			
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_D$ = 120 A; $V_{sup} \le$ 30 V; unclamped; $R_{GS}$ = 50 Ω; Fig. 3		-	246	mJ

#### [1] Capped at 120A due to package

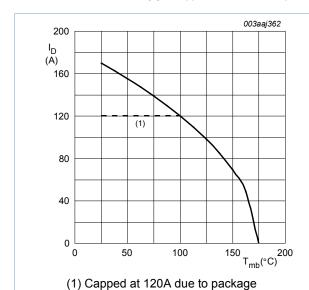


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \ge 10V$$

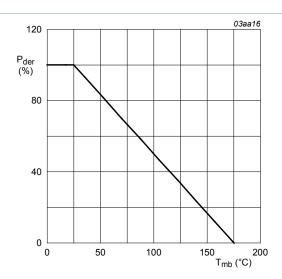


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

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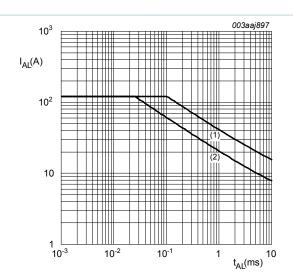
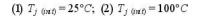


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time



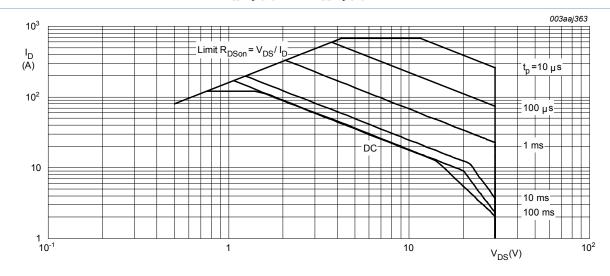


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$$T_{mb} = 25^{\circ}C$$
;  $I_{DM}$  is a single pulse

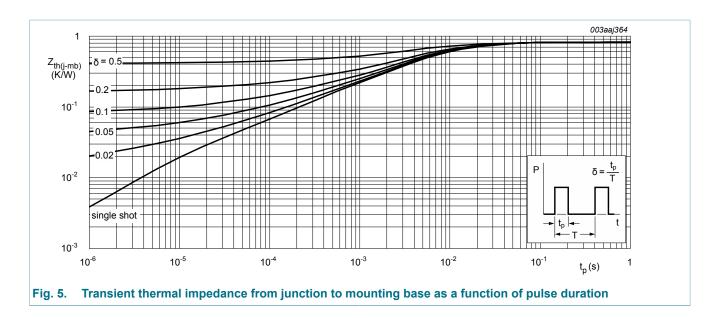
### 6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	Fig. 5	-	0.73	0.84	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	minimum footprint; FR4 board	-	50	-	K/W

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### 7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics		<u> </u>			
V <sub>(BR)DSS</sub>	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	27	-	-	V
	breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 10	0.5	-	-	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; Fig. 11; Fig. 10	1.3	1.7	2.15	V
	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 10	-	-	2.45	V	
I <sub>DSS</sub> drain leakage current	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	0.2	5	μA
	V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 100 °C	-	-	100	μA	
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	10	100	nA
		V <sub>GS</sub> = -16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	10	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS}$ = 10 V; $I_{D}$ = 25 A; $T_{j}$ = 25 °C; Fig. 12	-	2.95	3.4	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 100 °C; Fig. 13; Fig. 12	-	-	5.1	mΩ
		$V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 12	-	4.25	5	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; Fig. 13; Fig. 12	-	-	6.5	mΩ

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_G$	internal gate resistance (AC)	f = 1 MHz	0.5	1	2	Ω
Dynamic ch	aracteristics		'			
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 10 V; Fig. 14; Fig. 15	-	81	-	nC
		I <sub>D</sub> = 25 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 4.5 V; Fig. 14; Fig. 15	-	37	-	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V	-	79	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 4.5 V;	-	13.9	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate- source charge	Fig. 14; Fig. 15	-	7.5	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate- source charge		-	6.4	-	nC
Q <sub>GD</sub>	gate-drain charge		-	12.2	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 15 V; <u>Fig. 14</u> ; <u>Fig. 15</u>	-	3.2	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 0 V; f = 1 MHz;	-	4682	-	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 16</u>	-	909	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	438	-	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS}$ = 15 V; $R_L$ = 0.6 $\Omega$ ; $V_{GS}$ = 4.5 V;	-	35.7	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 4.7 \Omega; T_j = 25 °C$	-	101	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	49	-	ns
t <sub>f</sub>	fall time		-	51.2	-	ns
Source-drai	in diode		1		1	
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <u>Fig. 17</u>	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = 100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	37	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 15 V	-	38	-	nC

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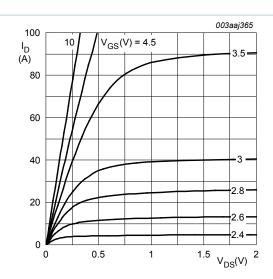


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values



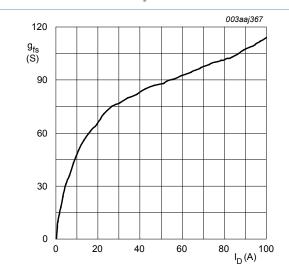


Fig. 8. Forward transconductance as a function of drain current; typical values

$$T_j = 25$$
°C;  $V_{DS} = 10V$ 

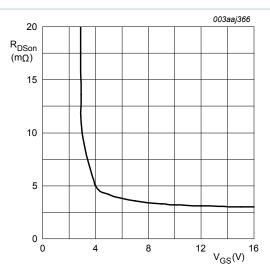


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^{\circ}C; I_D = 25A$$

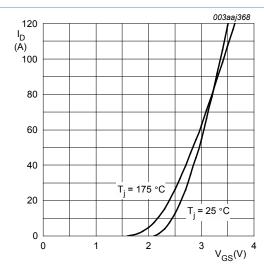


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$$V_{DS} = 10V$$

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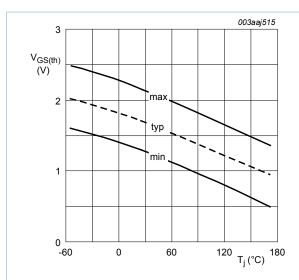


Fig. 10. Gate-source threshold voltage as a function of junction temperature



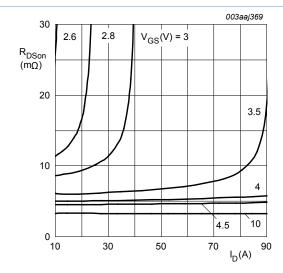


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^{\circ}C$$

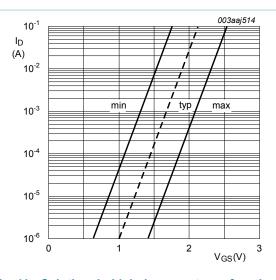


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^{\circ}C; \ V_{DS} = 5V$$

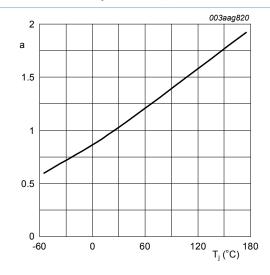


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$\mathbf{a} = \frac{R_{DSon}}{R_{DSonOSSC}}$$

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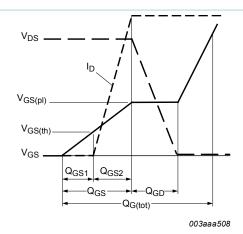


Fig. 14. Gate charge waveform definitions

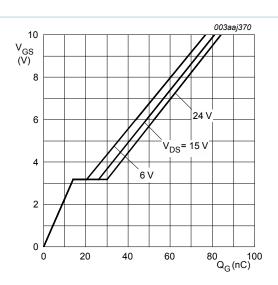


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}C; I_D = 25A$$

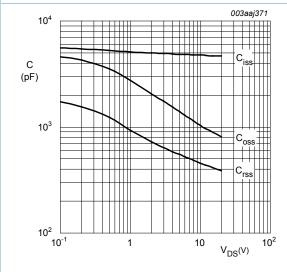
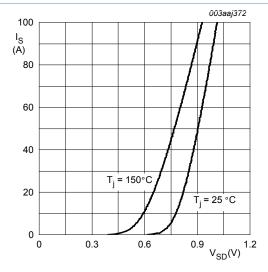


Fig. 16. Input, output and reverse transfer capacitances | Fig. 17. Source current as a function of source-drain as a function of drain-source voltage; typical values

$$V_{GS} = \mathbf{0}V; \ f = \mathbf{1}MHz$$



voltage; typical values

$$V_{GS} = 0V$$

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### 8. Package outline

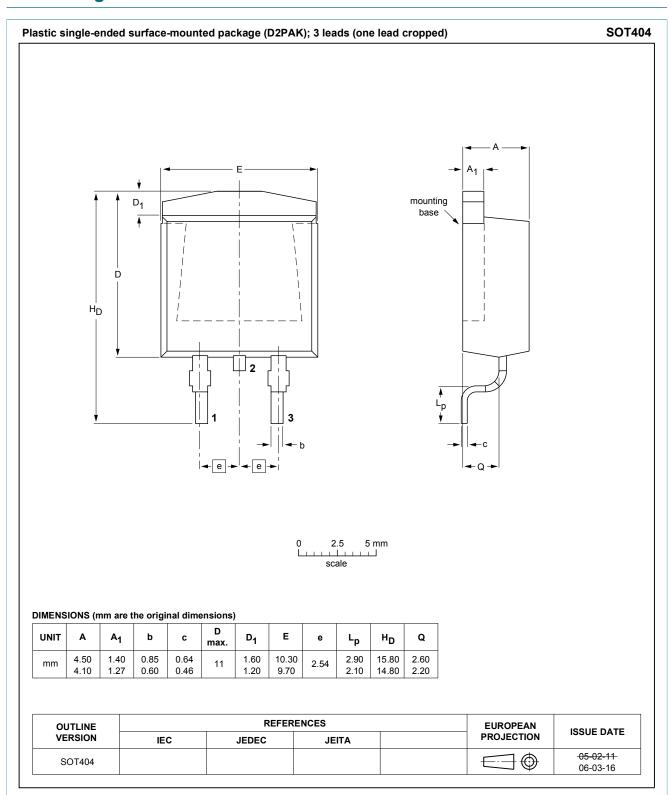


Fig. 18. Package outline D2PAK (SOT404)

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