High Power CCFL Controller for Wide Dimming Range and Maximum Lamp Lifetime

FEATURES

- **Ultrawide Multimode Dimming™ Range**
- **Multiple Lamp Capability**
- **Programmable PWM Dimming Range and Frequency**
- **Precision Maximum and Minimum Lamp Currents Maximize Lamp Lifetime**
- **No Lamp Flicker Under All Supply and Load Conditions**
- **Open Lamp Detection and Protection**
- 350kHz Switching Frequency
- 1.5A MOSFET Gate Driver
- 100mV Current Sense Threshold
- 5V Reference Voltage Output
- The 16-Lead SSOP Package

APPLICATIONS

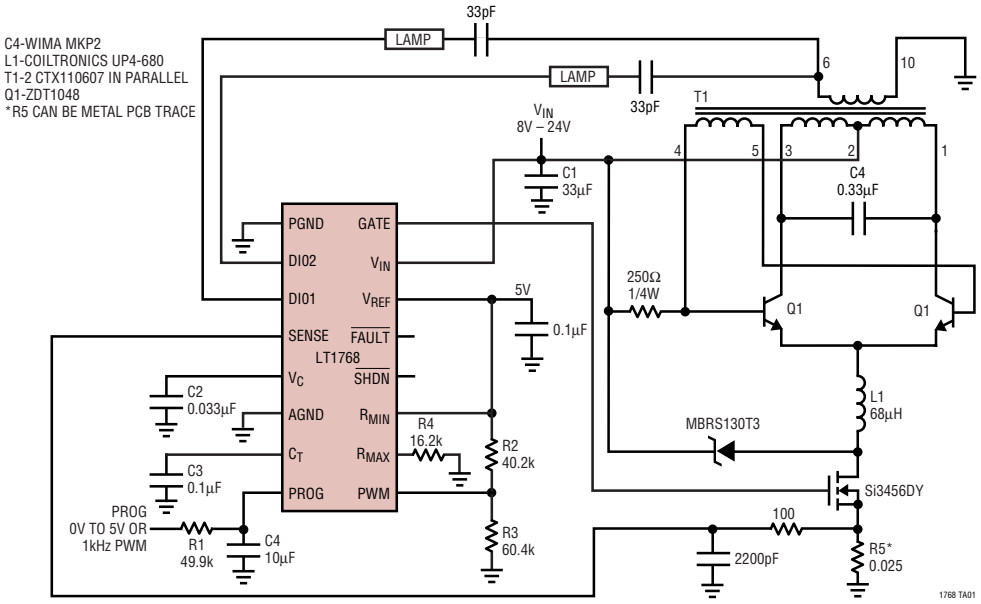
- Desktop Flat Panel Displays
- Multiple Lamp Displays
- Notebook LCD Displays
- Point of Sale Terminal Displays

DESCRIPTION

The LT®1768 is designed to control single or multiple cold cathode fluorescent lamp (CCFL) displays. A unique Multimode Dimming scheme* combines both linear and PWM control functions to maximize lamp life, efficiency, and dimming range. Accurate maximum and minimum lamp currents can be easily set. The LT1768 can detect and protect against lamp failures and overvoltage start-up conditions. It is designed to provide maximum flexibility with a minimum number of external components.

The LT1768 is a current mode PWM controller with a 1.5A MOSFET driver for high power applications. It contains a 350kHz oscillator, 5V reference, and a current sense comparator with a 100mV threshold. It operates from an 8V to 24V input voltage. The LT1768 also has undervoltage lockout, thermal limit, and a shutdown pin that reduces supply current to 65µA. It is available in a small 16-lead SSOP package.

TYPICAL APPLICATION



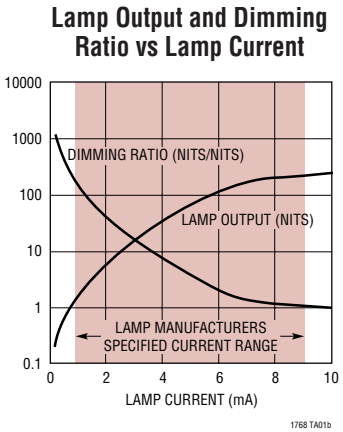


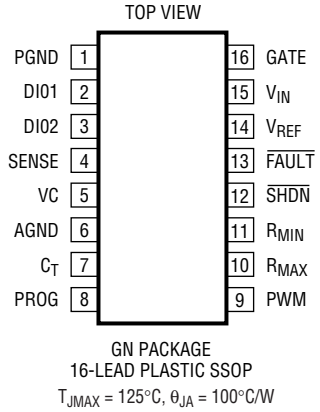
Figure 1. 14W CCFL Supply Produces a 100:1 Dimming Ratio While Maintaining Minimum and Maximum Lamp Current Specifications

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltage (V_{IN} Pin) 28V
$\overline{SHDN}$ Pin Voltage 28V
$\overline{FAULT}$ Pin Voltage 28V
PROG Pin Voltage 5.5V
PWM Pin Voltage 4.5V
C_T Pin Voltage 4.5V
SENSE Pin Voltage 1V
DIO1, DIO2 Input Current ..... ±50mA
R_{MAX} Pin Source Current 750µA
R_{MIN} Pin Source Current 750µA
V_{REF} Pin Source Current 10mA
Operating Junction Temperature Range
LT1768C ..... 0°C to 125°C
LT1768I ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1768CGN LT1768IGN
GN PART MARKING
1768 1768I

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{VIN} = 12V, $I_{DIO1/2}$ = 250µA, V_{PROG} = 0V, V_{PWM} = 2.5V, I_{RMAX} = –100µA, I_{RMIN} = –100µA, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Supply Current	9V< V_{VIN} < 24V	●		7	8	mA
$I_{\overline{SHDN}}$	Supply Current in Shutdown	$V_{\overline{SHDN}}$ = 0V	●		65	100	µA
	$\overline{SHDN}$ Pin Pull-Up Current	$V_{\overline{SHDN}}$ = 0V	●	4	7	12	µA
	$\overline{SHDN}$ Threshold Voltage	$V_{\overline{SHDN}}$ Off to On	●	0.6	1.26	1.8	V
	$\overline{SHDN}$ Threshold Hysteresis		●	100	200	300	mV
	V_{IN} Undervoltage Lockout	V_{IN} Off to On	●	7.2	7.9	8.2	V
	V_{IN} Undervoltage Lockout	V_{IN} On to Off	●	7.1	7.4	7.6	V
V_{REF}	REF Voltage	I_{REF} = –1mA	●	4.9	5	5.1	V
	REF Line Regulation	ΔV_{VIN} 8V to 24V I_{REF} = –1mA	●		7	20	mV
	REF Load Regulation	ΔI_{REF} –1mA to –10mA	●		10	20	mV
V_{RMAX}	R_{MAX} Pin Voltage		●	1.225	1.25	1.275	V
V_{RMIN}	R_{MIN} Pin Voltage		●	1.22	1.26	1.30	V
FSW	Switching Frequency	V_{PROG} = 0.75V, V_{SENSE} = 0V	●	300	350	410	kHz
	Maximum Duty Cycle	V_{PROG} = 0.75V, V_{SENSE} = 0V			93		%
	Minimum ON Time	V_{PROG} = 0.75V, V_{SENSE} = 150mV			125		ns
I_{PROG}	PROG Pin Input Bias Current	V_{PROG} = 5V	●		100	500	nA
V_{PROG}	PROG Pin Voltage for Zero Lamp Current PROG Pin Voltage for Minimum Lamp Current PROG Pin Voltage for Maximum Lamp Current	(Note 2) (Note 3) (Note 4)	● ● ●	0.45 0.9 3.8	0.5 1 4	0.55 1.1 4.2	V V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{VIN} = 12V, $I_{DIO1/2}$ = 250µA, V_{PROG} = 0V, V_{PWM} = 2.5V, I_{RMAX} = –100µA, I_{RMIN} = –100µA, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{PWM}	PWM Input Bias Current		●		0.6	4	µA
	PWM Duty Cycle	V_{PROG} = 1.75		45	50	55	%
	PWM Frequency	C_T = 0.22µF (Note 7)		90	110	130	Hz
$V_{DIO1/2}$	DIO1/2 Positive Voltage DIO1/2 Negative Voltage	I_{DIO} = 14mA I_{DIO} = –14mA			1.7 –1.1	1.9 –1.3	V V
$V_{VCCLAMP}$	VC High Clamp Voltage VC Switching Threshold	V_{PROG} = 4.5V (Note 8) V_{PROG} = 4.5V (Note 8)		3.6 0.5	3.7 0.7	3.9 0.95	V V
I_{SENSE}	SENSE Input Bias Current	V_{SENSE} = 0V			–25	–30	µA
V_{SENSE}	SENSE Threshold for Current Limit	V_{VC} = $V_{VCCLAMP}$, Duty Cycle <50%, V_{PROG} = 1V V_{VC} = $V_{VCCLAMP}$, Duty Cycle 80%, V_{PROG} = 1V		85	100 90	115	mV mV
	$I_{DIO1/2}$ to I_{RMAX} Ratio	V_{PROG} = 4.5V (Note 5)	●	94	98	104	A/A
		V_{PROG} = 4.5V, I_{DIO1} or I_{DIO2} = 0, V_{VC} = 2.5V, (Note 5)		45	49	55	A/A
	$I_{DIO1/2}$ to I_{RMIN} Ratio	V_{PROG} < 0.75V (Note 6)	●	9	10	11	A/A
		V_{PROG} < 0.75V, I_{DIO1} or I_{DIO2} = 0, V_{VC} = 2.5V, (Note 6)		9	10	11	A/A
I_{GATE}	GATE Drive Peak Source Current GATE Drive Peak Sink Current				1.5 1.5		A A
	GATE Drive Saturation Voltage	V_{VIN} = 12V, I_{GATE} = –100mA, V_{PROG} = 4.5V	●	9.8	10.2		V
	GATE Drive Clamp Voltage	V_{VIN} = 24V, I_{GATE} = –10mA, V_{PROG} = 4.5V	●		12.5	14	V
	GATE Drive Low Saturation Voltage	I_{GATE} = 100mA	●		0.4	0.6	V
	Open LAMP Threshold	(Note 9)		100	125	150	µA
	$\overline{FAULT}$ Pin Saturation Voltage	$I_{\overline{FAULT}}$ = 1mA, I_{DIO1}, I_{DIO2} = 0µA, V_{PROG} = 4.5V			0.2	0.3	V
	$\overline{FAULT}$ Pin Leakage Current	$V_{\overline{FAULT}}$ = 5V			20	100	nA
	Thermal ShutdownTemperature				160		°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: This is the threshold voltage where the lamp current switches from zero current to minimum lamp current. For V_{PROG} less than the threshold voltage, lamp current will be at zero. For V_{PROG} greater than the threshold voltage, lamp current will be equal to the minimum lamp current. Minimum lamp current is set by the value of the resistor from the R_{MIN} pin to ground. See Applications Information for more details.

Note 3: This is the threshold voltage where the device starts to pulse width modulate the lamp current. For V_{PROG} less than the threshold voltage, lamp current will be equal to the minimum lamp current. For V_{PROG} greater than the threshold voltage, lamp current will be pulse width modulated between the minimum lamp current and some higher value. Minimum lamp current is set by the value of the resistor from the R_{MIN} pin to ground. The higher value lamp current is a function of the R_{MAX} resistor to ground value, and the voltages on the PWM and PROG pins. See Applications Information for more details.

Note 4: This is the threshold voltage where the lamp current reaches its maximum value. For V_{PROG} greater than the threshold voltage, there will be no increase in lamp current. For V_{PROG} less than the threshold voltage, lamp current will be at some lower value. Maximum lamp current is set by the value of the resistor from the R_{MAX} pin to ground. The lower value lamp current is a function of the R_{MIN} and R_{MAX} resistors, and the voltages on the PWM and PROG pins. See Applications Information for more details.

Note 5: $I_{DIO1/2}$ to I_{RMAX} ratio is determined by setting I_{RMAX} to –100µA, V_{PROG} to 4.5V, V_{VC} to 2.5V, and then ramping a DC current out of the DIO1/2 pins from zero until the DC current in the VC voltage source current equals zero. The $I_{DIO1/2}$ to I_{RMAX} ratio is then defined as (I_{DIO1} + I_{DIO2})/I_{RMAX}. See Applications Information for more details.

Note 6: $I_{DIO1/2}$ to I_{RMIN} ratio is determined by setting I_{RMIN} to –100µA, V_{PROG} to 0.75V, V_{VC} to 2.5V, and then ramping a DC current out of the DIO1/2 pins from zero until the DC current in the VC voltage source current equals zero. The $I_{DIO1/2}$ to I_{RMIN} ratio is then defined as (I_{DIO1} + I_{DIO2})/I_{RMIN}. See Applications Information for more details.

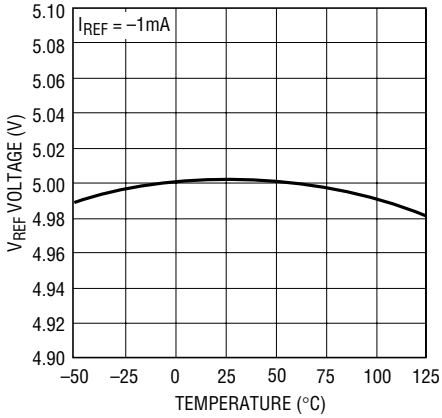
Note 7: The PWM frequency is set by the equation PWMFREQ = 22Hz/C_T(µF).

Note 8: For VC voltages less than the switching threshold, GATE switching is disabled.

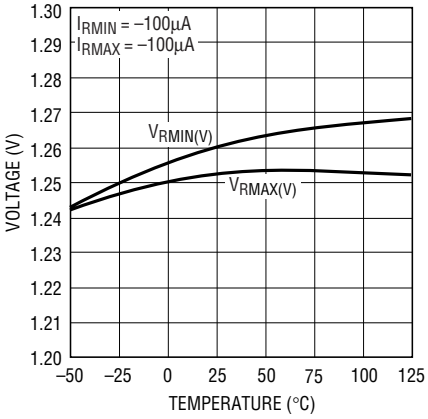
Note 9: An open lamp will be detected if either I_{DIO1} or I_{DIO2} is less than the threshold current for at least 1 full PWM cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

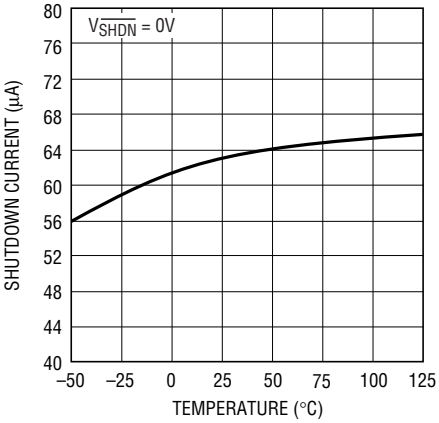
V_{REF} vs Temperature



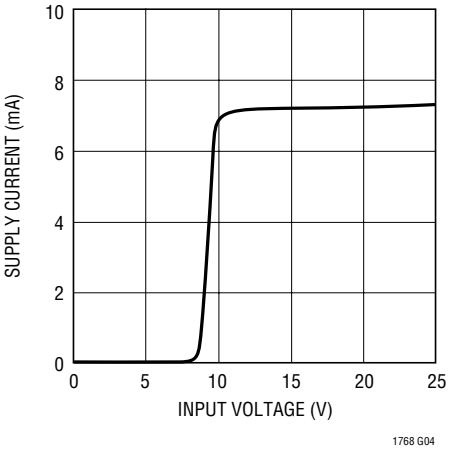
V_{RMIN}, V_{RMAX} vs Temperature



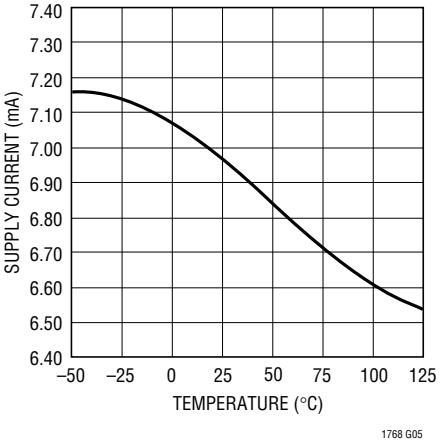
Supply Current in Shutdown vs Temperature



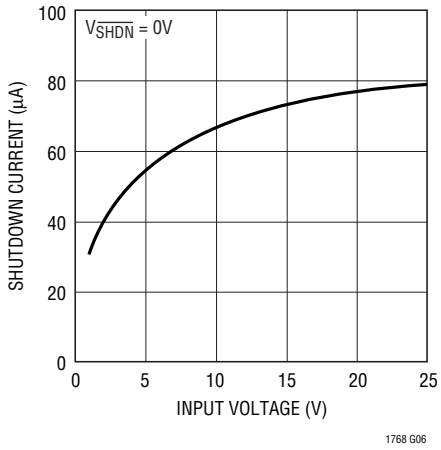
Supply Current vs Input Voltage



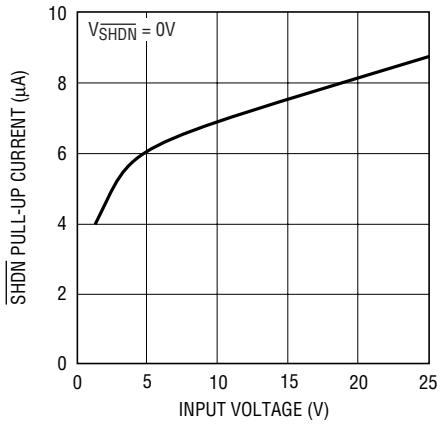
Supply Current vs Temperature



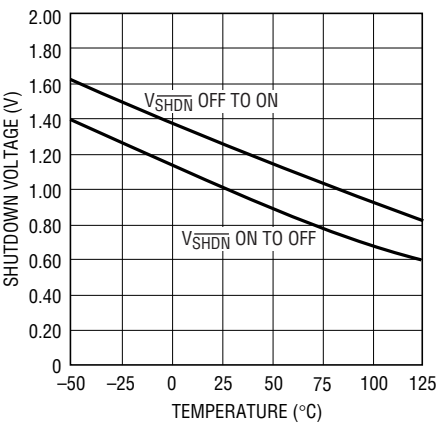
Supply Current in Shutdown vs Input Voltage



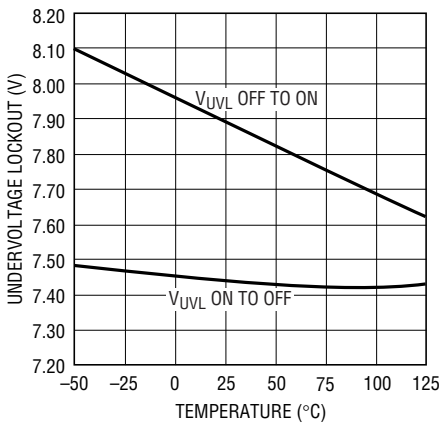
$\overline{SHDN}$ Pull-Up Current vs Input Voltage



Shutdown Threshold Voltage vs Temperature

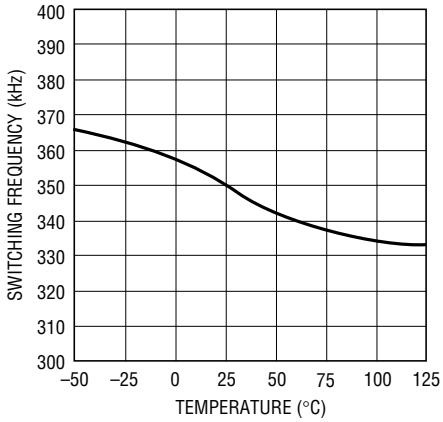


Undervoltage Lockout Threshold vs Temperature

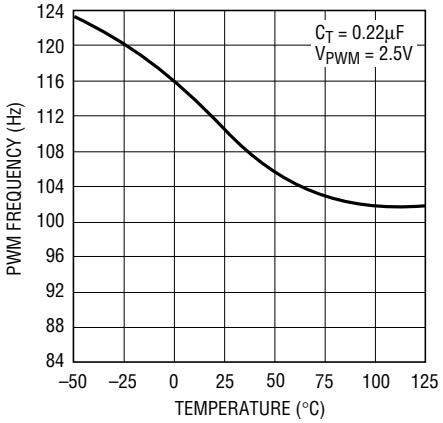


TYPICAL PERFORMANCE CHARACTERISTICS

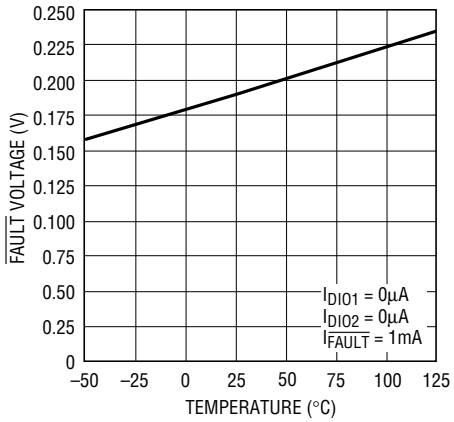
Switching Frequency vs Temperature



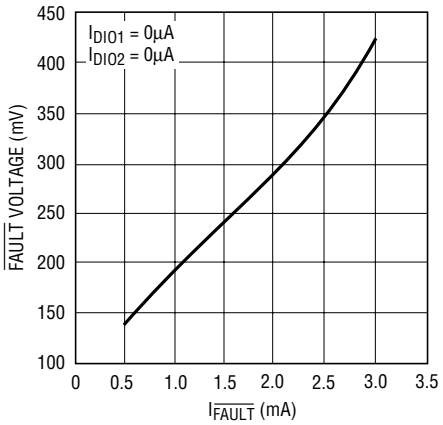
PWM Frequency vs Temperature



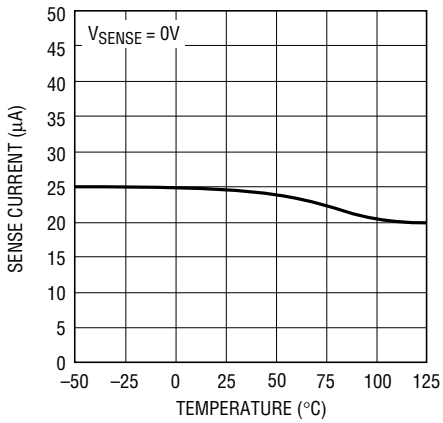
$\overline{FAULT}$ Pin Saturation Voltage vs Temperature



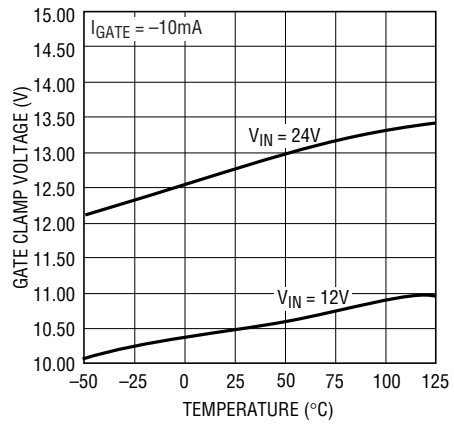
$\overline{FAULT}$ Pin Saturation Voltage vs Current



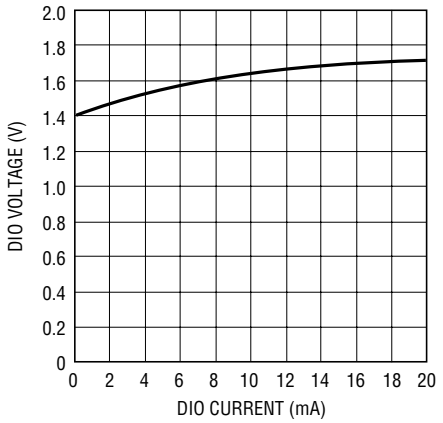
Sense Pin Bias Current vs Temperature



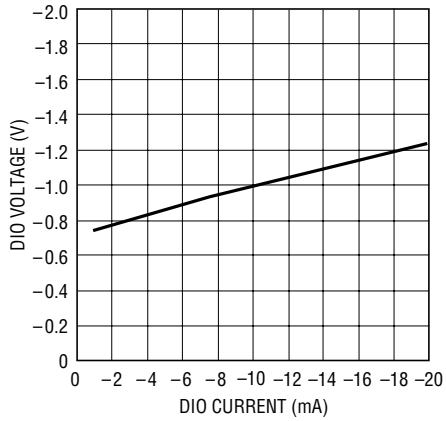
Maximum Gate Voltage vs Temperature



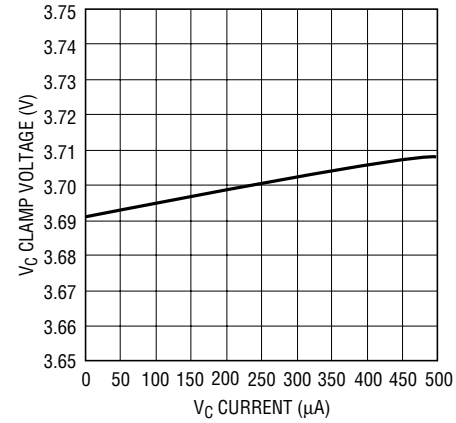
DIO Pin Voltage vs Current



DIO Pin Voltage vs Current

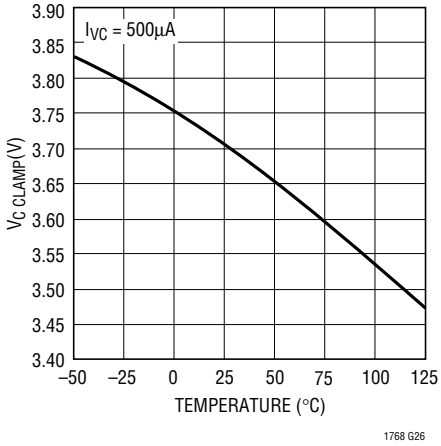


VC Clamp Voltage vs Current

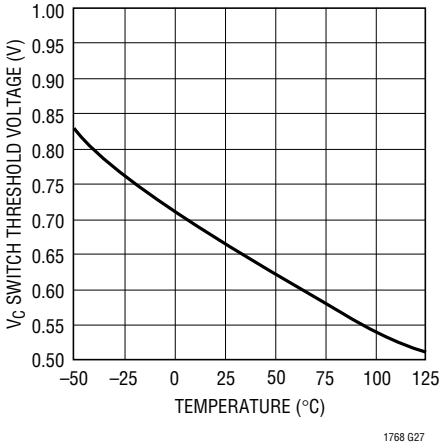


TYPICAL PERFORMANCE CHARACTERISTICS

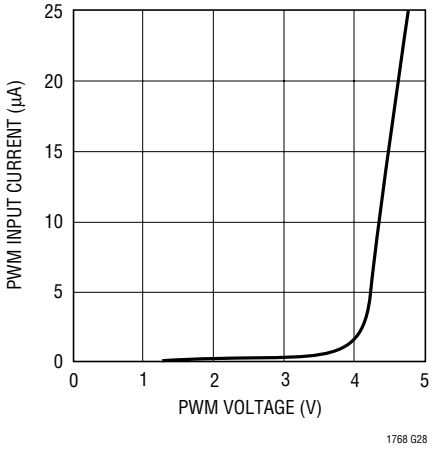
VC Clamp Voltage vs Temperature



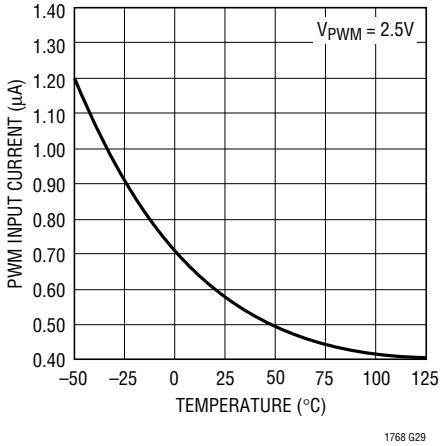
VC Switching Threshold vs Temperature



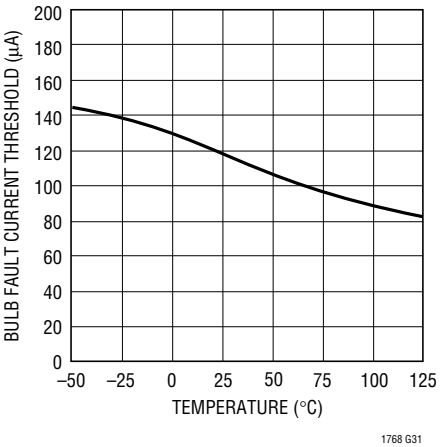
PWM Pin Input Current vs Voltage



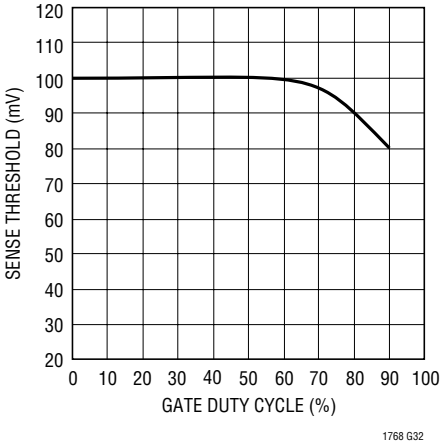
PWM Pin Input Current vs Temperature



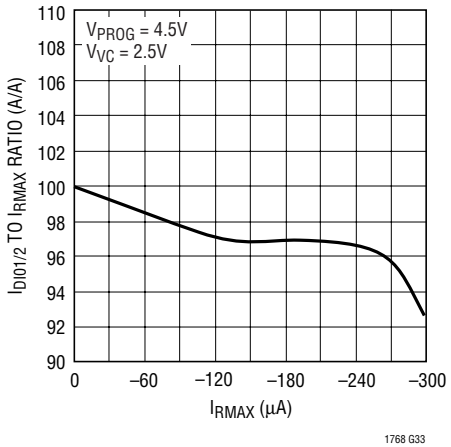
Lamp Fault Current Threshold vs Temperature



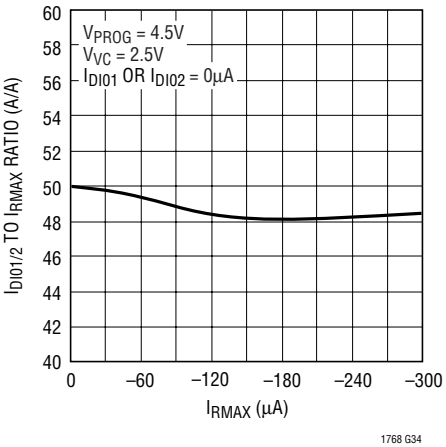
Maximum Sense Threshold vs Gate Drive Duty Cycle



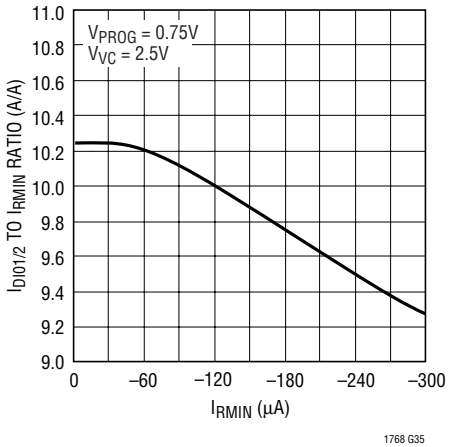
$I_{DIO1/2}$ to I_{RMAX} Ratio vs R_{MAX} Current



$I_{DIO1/2}$ to I_{RMAX} Ratio vs R_{MAX} Current with a Lamp Fault



$I_{DIO1/2}$ to I_{RMIN} Ratio vs R_{MIN} Current



PIN FUNCTIONS

PGND (Pin 1): The PGND pin is the high current ground path. High switching current transients and lamp current flow through the PGND pin.

DIO1/DIO2 (Pins 3/2): Each DIO pin is the common connection between the cathode and anode of two internal diodes. The remaining terminals of the diodes are connected to PGND. In a typical application, the DIO1/2 pins are connected to the low voltage side of the lamps. Bidirectional lamp current flows into the DIO1/2 pins and their diodes conduct alternately on the half cycles. The diode that conducts on the negative cycle has a percentage of its current diverted into the VC pin. This current nulls against the programming current specified by the PROG and PWM pins. A single capacitor on the VC pin provides both stable loop compensation and an averaging function to the half wave-rectified lamp current. The diode that conducts on the positive cycle is used to detect open lamp conditions. If the current in either of the DIO pins on the positive cycle is less than 125μA for a minimum of 1 PWM cycle, then the FAULT pin will be activated and the maximum source current into the VC pin will be reduced by approximately 50%. If the current in both of the DIO pins on the positive cycle is less than 125μA, and the VC pin hits its clamp value (indicating either an open lamp or lamp lowside short to ground fault condition) for a minimum of 1 PWM cycle, the gate drive will be latched off. The latch can be cleared by setting the PROG voltage to zero or placing the LT1768 in shutdown mode.

SENSE (Pin 4): The SENSE pin is the input to the current sense comparator. The threshold of the comparator is a function of the voltage on the VC pin and the switch duty cycle. The maximum threshold is set at 100mV for duty cycle less than 50% which corresponds to approximately 3.7V on the VC pin. The SENSE pin has a bias current of 25μA, which flows out of the pin.

VC (Pin 5): The VC pin is the summing junction for the programming current and the half wave rectified lamp current and is also an input to the current sense comparator . A fraction of the voltage on the VC pin is compared to the voltage on the SENSE pin (switch current) for switch turnoff. During normal operation the VC pin sits between 0.7V (zero switch current) and 3.7V (maximum switch current). A single capacitor between VC and AGND provides lamp current averaging and single pole loop compensation.

AGND (Pin 6): The AGND pin is the low current analog ground. It is the negative sense terminal for the internal reference and current sense amplifier. Connect critical external components that terminate to ground directly to this pin for best performance.

C_T (Pin 7): The value of capacitance on the C_T pin determines the PWM modulation frequency. The transfer function of capacitance to frequency equals $22Hz/C_T(\mu F)$. The frequency present on the C_T pin also determines the maximum time allowed for lamp fault conditions. If the current in either DIO1 or DIO2 is less than 125μA for a minimum of 1 PWM period, the FAULT pin is activated and the maximum allowable lamp current is reduced by approximately 50%. If the current in both DIO1 and DIO2 is absent for a minimum of 1 PWM period, and the VC pin is clamped at 3.7V, the FAULT pin is activated and the gate drive of the part is internally latched off. The latch can be cleared by setting the PROG voltage to zero or placing the LT1768 in shutdown mode.

PROG (Pin 8): The PROG pin controls the lamp current by converting a DC input voltage range of 0V to 5V to source current into the VC pin. The transfer function from programming voltage to VC current is illustrated in the following table.

PROG (V)	VC SOURCE CURRENT (μA)
$V_{PROG} < 0.5$	0
$0.5 < V_{PROG} < 1.0$	I_{RMIN}
$1.0 < V_{PROG} < V_{PWM}$	PWM Mode*
$V_{CT} > V_{PROG}$	I_{RMIN}
$V_{CT} < V_{PROG}$	$5 \bullet I_{RMAX} \bullet (V_{PWM} – 1V)/ 3V$
$V_{PROG} > 4.0$	$5 \bullet I_{RMAX}$

*PWM Duty Cycle = $[1 – (V_{PWM} – V_{PROG})/(V_{PWM} – 1V)] \bullet 100\%$

PWM (Pin 9): The PWM pin controls the percentage of the PROG range between 1V and 4V that is to be pulse width modulated. The percentage is defined by $[(V_{PWM}-1)/ 3] \bullet 100\%$. The minimum and maximum percentages are 25% (1.75V) and 100% (4V) respectively. Taking the PWM pin above the 4V maximum will cause significant PWM input current to flow. (See PWM Input Current vs Voltage curve in Typical Performance Characteristics).

PIN FUNCTIONS

R_{MAX} (Pin 10): The R_{MAX} pin outputs a regulated voltage of 1.25V that is to be loaded with an external resistor. The current through the external resistor sets the maximum lamp current. Maximum lamp current in a dual lamp application will be approximately equal to 100 times I_{RMAX} when the voltage on the PROG pin is greater than 4V. The value of R_{RMAX} must be greater than 5K and less than $[R_{RMIN} \bullet 2.5 \bullet (V_{PWM-1}/3)]$ for proper PWM operation.

R_{MIN} (Pin 11): The R_{MIN} pin outputs a regulated voltage of 1.26V that is to be loaded with an external resistor. The current through the external resistor sets the minimum lamp current. Minimum lamp current in a dual lamp application will be approximately 10 times the value of I_{RMIN} when the voltage on the PROG pin is between 0.5V and 1V. To set the minimum current to zero (I_{RMIN} = 0μA) for maximum dimming range, connect the R_{MIN} pin to the V_{REG} pin. The value of R_{RMIN} ($R_{RMIN} = \infty$ when R_{MIN} is connected to V_{REG}) must be greater than the value of $R_{RMAX}/[0.4 \bullet (V_{PWM-1})/3]$ for proper PWM operation.

$\overline{SHDN}$ (Pin 12): The $\overline{SHDN}$ pin controls the operation of the LT1768. Pulling the $\overline{SHDN}$ pin above 1.26V or leaving the pin open will result in normal operation of the LT1768. Pulling the $\overline{SHDN}$ pin below 1V causes a complete shutdown of the LT1768 which results in a typical quiescent current of 65μA. The $\overline{SHDN}$ pin has an internal 7μA pull-up source to V_{IN} and 200mV of voltage hysteresis.

$\overline{FAULT}$ (Pin 13): The $\overline{FAULT}$ pin is an open collector output with a sink capability of 1mA that is activated when lamp current falls below 125μA in either DIO1 or DIO2 for at least 1 full PWM cycle.

V_{REF} (Pin 14): The V_{REF} pin is a regulated 5V output that is derived from the V_{IN} pin. The regulated voltage provides up to 10mA of current to power external circuitry. During undervoltage lockout, shutdown mode or thermal shutdown, drive to the V_{REF} pin will be disabled.

V_{IN} (Pin 15): The V_{IN} pin is the voltage supply pin for the LT1768. For normal operation, the V_{IN} pin must be above an undervoltage lockout of 7.9V and below a maximum of 24V.

GATE (Pin 16): The GATE pin is the output of a NPN high current output stage used to drive the gate of an external MOSFET. It has a dynamic source and sink capability of 1.5A. During normal operation, the GATE pin is driven high at the beginning of each oscillator period and then low when the appropriate current in the switch is reached. The GATE pin has a minimum on time of 125ns and a maximum duty cycle of 93% at a frequency of 350kHz. For input voltages less than 13V the gate will be driven to within 2V of V_{IN}. For input voltages greater than 13V the gate pin high level will be clamped at a typical voltage of 12.5V.

BLOCK DIAGRAM

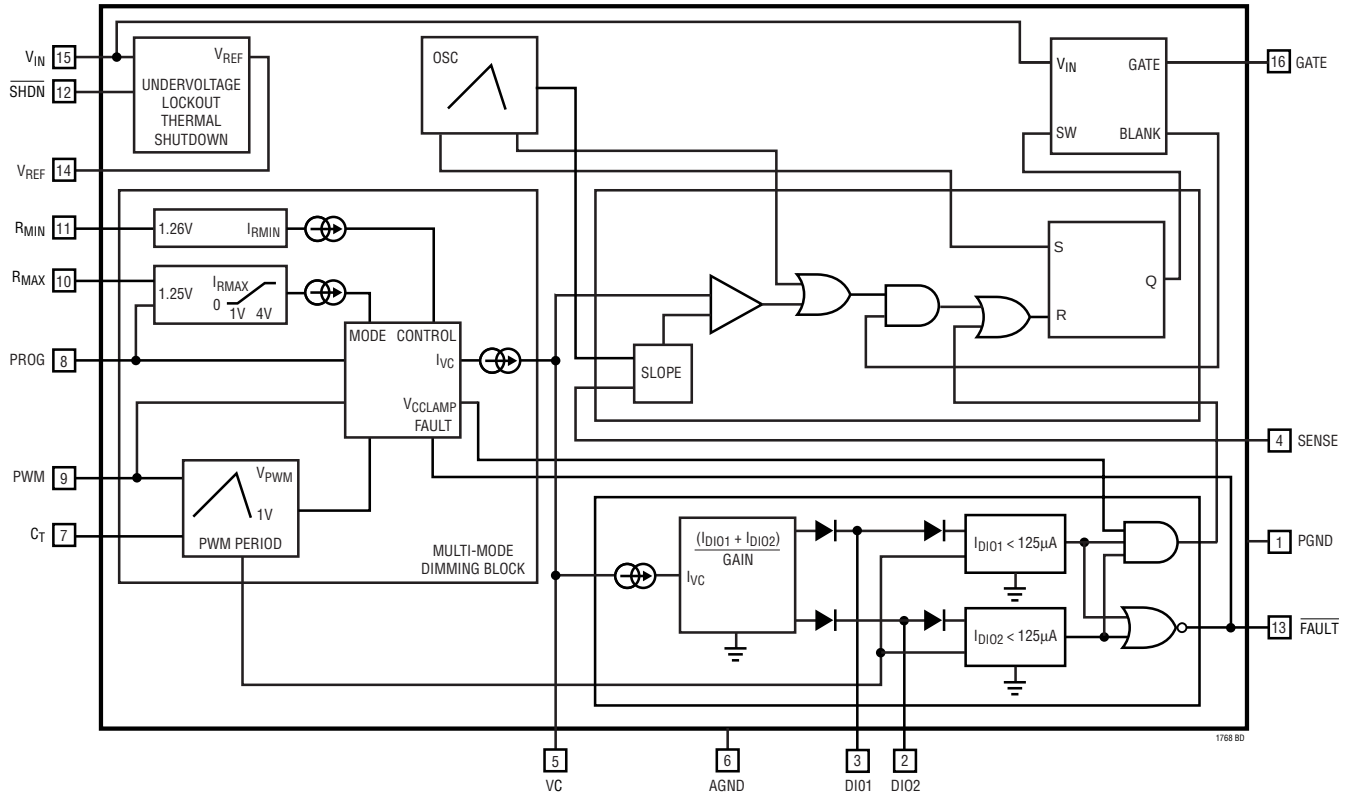


Figure 2. LT1768 Block Diagram

APPLICATIONS INFORMATION

INTRODUCTION

The current trend in desktop monitor design is to migrate the LCD (liquid crystal display) technology used in laptops and instruments to the popular desktop display sizes. As LCD size increases uniform backlighting requires multiple high power lamps. In addition, the lamps must have a dimming range and lifetime expectancy comparable to previous generations of desktop displays. Cold cathode fluorescent lamps (CCFLs) provide the highest available efficiency for backlighting LCD displays. The CCFL requires a high voltage supply for operation. Typically, over 1000 volts is required to initiate CCFL operation, with sustaining voltages from 200V to 800V. A CCFL can operate from DC, but migration effects damage the CCFL and shorten its lifetime. To achieve maximum life CCFL drive should be sinusoidal, contain zero DC component, and not exceed the CCFL manufacturers minimum and maximum operating current ratings. Low crest factor sinusoidal CCFL drive also maximizes current to light conversion, reduces display flicker, and minimizes EMI and RF emissions. The LT1768 high power CCFL controller, with its Multimode Dimming, provides the necessary lamp drive to enable a wide dimming range while maintaining lamp lifetime in multiple lamp CCFL applications.

BASIC OPERATION

Referring to the circuit in Figure 1, CCFL current is controlled by a DC voltage on the PROG pin of the LT1768. The DC voltage on the PROG pin feeds the LT1768's Multimode Dimming block and is converted to source current into the VC pin. As the VC pin voltage rises, the LT1768's GATE pin is pulse width modulated at 350kHz. The GATE pulse width is determined on a cycle by cycle basis by the voltage on the SENSE pin (L1's current multiplied by SENSE resistor R5) exceeding a predetermined voltage set by the VC pin.

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The current mode pulse width modulation produces an average current in inductor L1 proportional to the VC voltage. Inductor L1 then acts as a switched mode current source for a current driven Royer class converter with efficiencies as high as 90%. T1, C4 and Q1 comprise the Royer class converter which provides the CCFLs with a zero DC, 60kHz sinusoidal waveform whose amplitude is based on the average current in L1. Sinusoidal current from both CCFLs is then returned to the LT1768 through the DIO1/2 pins. A fraction of the CCFL current from the negative half of its sine wave pulls against the internal current source at the VC pin closing the loop. A single capacitor on the VC pin provides loop compensation and CCFL current averaging, which results in constant CCFL current. Varying the value of the internal current source via the Multimode Dimming block varies the CCFL current and resultant CCFL light intensity.

Multimode Dimming

Previous backlighting solutions have used a traditional error amplifier in the control loop to regulate lamp current. The approach converted AC current into a DC voltage for the input of the error amplifier. This approach used several time constants in order to provide stable loop compensation. This compensation scheme meant that the loop had to be fairly slow and that the output overshoot with start-up or load conditions had to be carefully evaluated in terms of transformer stress and breakdown voltage requirements. In addition, intensity control schemes were limited to linear or PWM control. Linear intensity control schemes provide the highest efficiency backlight circuits but either limit dimming range, or violate lamp minimum or maximum CCFL current specifications to achieve wide dimming ratios. PWM control schemes offer wide dimming range but produce waveforms that may degrade CCFL life, and waste power at higher CCFL currents. The LT1768's Multimode Dimming eliminates the error amplifier concept entirely and combines the best of both control schemes to extend CCFL life while providing the widest possible dimming range.

The error amplifier is eliminated by summing the current out of the Multimode Dimming block with a fraction of feedback lamp current to form the control loop. This topology reduces the number of time constants in the control loop by combining the error signal conversion scheme and frequency compensation into a single capacitor (VC pin). The control loop thus exhibits the response of a single pole system, allows for faster loop transient response and minimizes overshoot under start-up or overload conditions.

Referring to Figure 2, the source current into the VC pin from the Multimode Dimming block (and resultant CCFL current) has five distinct modes of operation. Which mode is in use is determined by the voltages on the PROG and PWM pins, and the currents that flow out of the R_{MAX} and R_{MIN} pins.

Off Mode (V_{PROG} < 0.5V), sets the VC source current to zero, actively pulls VC to ground, and inhibits the GATE pin from switching which results in zero lamp current.

Minimum current mode (0.5V < V_{PROG} < 1V) sets the VC source current equal to the current out of the 1.26V referenced R_{MIN} pin. The minimum VC source current determines the dimming range of the display. Setting R_{RMIN} to produce the manufacturer's minimum specified CCFL current guarantees the maximum CCFL lifetime for all PROG voltages, but limits the dimming range. Setting R_{RMIN} to produce currents less than the manufacturer's minimum specified CCFL current increases dimming range, but places restrictions on the PROG voltage for normal operation in order to maximize lifetime. To achieve the maximum dimming ratio possible, I_{RMIN} should be set to zero by connecting the R_{MIN} pin to the V_{REF} pin.

For example, the circuit in Figure 1 produces a dimming ratio of 100:1 at 1mA of lamp current, but sets the minimum CCFL current to zero (R_{MIN} is connected to V_{REF}). In this case, the PROG voltage must be kept above 1.12V to limit the CCFL current to 1mA (1mA is only a typical minimum lamp current used for illustration, consult lamp specifications for actual minimum allowable value) during normal operation in order to meet CCFL specifications to maximize lifetime. It should be noted that taking the PROG voltage in Figure 1 down to 1V (0mA CCFL current) enables dimming ratios greater than 500:1, but violates minimum CCFL current specifications in most lamps and is not recommended. Alternatively, disconnecting R_{MIN} from V_{REF} and adding a 10kΩ resistor from R_{MIN} to AGND in Figure 1 sets the minimum CCFL current

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per lamp to 1mA for all PROG voltages but limits the dimming ratio to 6:1.

Trace B in Figures 3a and 3b shows Figure 1's CCFL current waveform operating at 1mA in PWM mode.

Maximum current mode (V_{PROG} > 4V) sets the VC source current to five times the current out of the 1.25V referenced R_{MAX} pin. Setting R_{RMAX} to produce CCFL current equal to the manufacturer's maximum rating in this mode insures no degradation in the specified lamp lifetime. For example, setting R4 in the circuit in Figure 1 to 16.2k sets the maximum CCFL current to 9mA (9mA is only a typical maximum lamp current used for illustration, consult lamp specifications for the actual value). Trace A in Figure 3a and 3b shows Figure 1's CCFL current waveform operating at 9mA in maximum current mode.

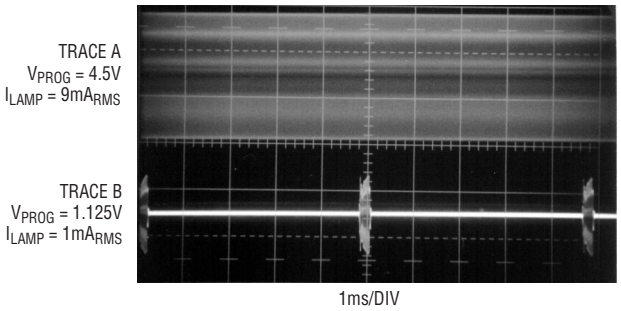

Figure 3a. CCFL Current for Circuit in Figure 1

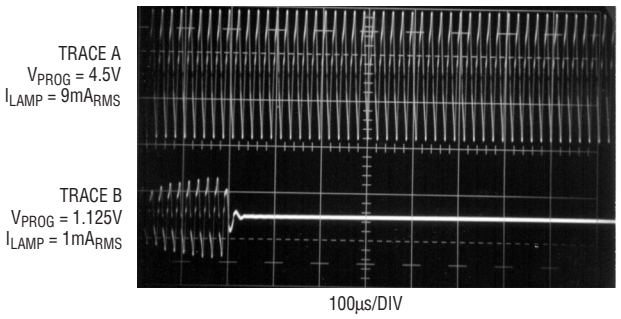

Figure 3b. CCFL Current for Circuit in Figure 1

In linear mode (V_{PWM} < V_{PROG} < 4V), VC source current is controlled linearly with the voltage on the PROG pin. The equation for the VC source current in linear mode is I_{VC} = (V_{PROG} – 1V)/3V (I_{RMAX} • 5). For the best current to light conversion and highest efficiency, V_{PWM} should be set to make the LT1768 normally operate in the linear mode. For example, in the circuit in Figure 1, linear mode runs from V_{PROG} = 3V to V_{PROG} = 4V with lamp current equal to (3mA)(V_{PROG}–1V)/1V.

In PWM Mode (1V < V_{PROG} < V_{PWM}), the VC source current is modulated between the value set by minimum current mode and the value for I_{VC} in linear mode with V_{PROG} = V_{PWM}. The PWM frequency is equal to 22Hz/C_T(µF) with its duty cycle set by the voltages on the PROG and PWM pins and follows the equation:

$$DC = [1 – (V_{PWM} – V_{PROG})/(V_{PWM} – 1V)] • 100\%$$

The LT1768's PWM mode enables wide dimming ratios while reducing the high crest factor found in PWM only dimming solutions. In the example of Figure 1, PWM mode runs from V_{PROG} = 1V to V_{PROG} = 3V with CCFL current modulated between 0mA and 6mA. The PWM modulation frequency is set to 220Hz by capacitor C3.

When combined, these five modes of operation allow creation of a DC controlled CCFL current profile that can be tailored to each particular display. With linear mode CCFL current control over the most widely used current range, and PWM mode at the low end, the LT1768 enables wide dimming ratios while maximizing CCFL lifetimes.

Lamp Feedback Current

In a typical application, the DIO1/2 pins are connected to the low voltage side of the lamps. Each DIO pin is the common connection between the cathode and anode of two internal diodes (see Block Diagram). The remaining terminals of the diodes are connected to PGND. Bidirectional lamp current flows into the DIO1/2 pins and their diodes conduct alternately on the half cycles. The diode that conducts on the negative cycle has a percentage of its current diverted into the VC pin. This current nulls against the VC source current specified by the Multimode Dimming section. A single capacitor on the VC pin provides both stable loop compensation and an averaging function to the halfwave-rectified lamp current. Therefore, current into the VC pin from the lamp current programming section relates to *average* lamp current.

The overall gain from the resistor current to average lamp current is equal to the gain from the Multimode Dimming block divided by the gain from the DIO pin to the VC pin,

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and is dependant on the operating mode. For dual lamp displays, the transfer function for minimum current mode (I_{DIO}/I_{RMIN}) is equal to 10A/A, and for maximum current mode (I_{DIO}/I_{RMAX}) is equal to 100A/A.

The transfer functions discussed above are between R_{MAX} and R_{MIN} current and average lamp current *not* RMS lamp current. Due to the differences between the average and RMS functions, the actual overall transfer function between actual lamp current and R_{MIN}/R_{MAX} current must be empirically determined, and is dependant on the particular lamp/display housing combination used. For example, in the circuit of Figure 1 setting R_{RMIN} to 10kΩ and R_{RMAX} to 16.8Ω, sets the minimum and maximum RMS lamp currents for the example display to 1mA and 9mA per lamp respectively. Figure 4 shows the lamp current vs programming voltage for the circuit in Figure 1.

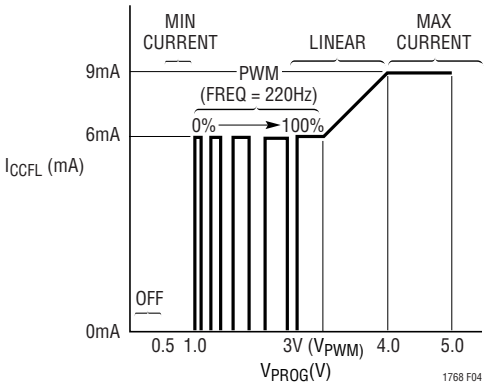

Figure 4. Lamp Current vs PROG Voltage for the Circuit in Figure 1

Choosing R_{RMAX} and R_{RMIN} and V_{PWM}

The value for R_{RMAX} should be determined by setting V_{PROG} to 4.5V then adjusting R_{RMAX} to produce the maximum allowable current specified by the lamp manufacturer.

The voltage for the PWM pin should then be set so that the LT1768 normally operates in linear mode. A typical value for V_{PWM} is approximately 2.5V, which limits the PWM region to 50% of the V_{PROG} input voltage range.

The value for R_{RMIN} should be chosen to either produce the minimum manufacturer specified lamp current or enable a wide dimming range. If a minimum specified current is desired, the V_{PROG} should be set to 0.75V and R_{RMIN} adjusted to produce the specified current. If a wide dimming range is desired, V_{PROG} should be set to 0.75V and R_{RMIN} adjusted to produce the required dimming ratio. Care must be taken when adjusting R_{RMIN} to produce extreme dimming ratios. The minimum lamp current set by R_{RMIN} must be able to fully illuminate the lamp or thermometering (uneven illumination) will occur. If the desired dimming ratio can't be achieved by adjusting R_{RMIN}, the minimum lamp current can be set to zero by connecting the R_{MIN} pin to the V_{REF} pin. If the minimum current is set to less than the open lamp threshold current (approximately 125μA), the $\overline{\text{FAULT}}$ pin will be activated for PROG voltages between 0.5V and 1V.

The values chosen for R_{RMAX} and R_{RMIN} are extremely critical in determining the lifetime of the display. It is imperative that proper measurement techniques, such as those cited in the references, be used when determining R_{RMAX} and R_{RMIN} values.

Lamp Fault Modes and Single Lamp Operation

The DIO pin diodes that conduct on the positive cycle are used to detect open lamp fault conditions. If the current in either of the DIO pins on the positive half cycle is less than 125μA due to either an open lamp or lamp lowside short to ground, for a minimum of 1 PWM cycle, then the $\overline{\text{FAULT}}$ pin will be activated and the lamp programming current into the VC pin in high level PWM mode, linear mode, and maximum current mode, will be reduced by approximately 50%. Halving the VC source current will cut the total lamp current to approximately one half of its programmed value. This function insures that the maximum lamp current level set by R_{RMAX} will not be exceeded even under fault conditions. If the current in both of the DIO pins on the positive cycle is less than 125μA, and the VC pin hits its clamp value (indicating an open lamp or lamp lowside short to ground fault condition) for a minimum of 1 PWM cycle, the gate drive will be latched off. The latch can be cleared by setting the PROG voltage to zero or placing the LT1768 in shutdown mode.

Since open lamp fault conditions produce high voltage AC waveforms, it is imperative that proper layout spacings between the high voltage and DIO lines be observed. Coupling capacitance as low as 0.5pF between the high

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voltage and DIO lines can cause enough current flow to fool the open lamp detection. In situations where coupling can't be avoided, resistors can be added from the DIO pins to ground to increase the open lamp threshold. When resistors from the DIO pins to ground are added, the values for R_{RMAX} and R_{RMIN} may need to be increased from their nominal values to compensate for the additional current.

For single lamp operation, the lowside of the lamp should be connected to both DIO pins, and the values of R_{RMAX} and R_{RMIN} increased to two times the values that would be used in a dual lamp configuration. In single lamp mode all fault detection will operate as in the dual lamp configuration, but the open lamp threshold will double. If the increase in the open lamp threshold is not acceptable, a positive offset current can be added to reduce the open lamp threshold by placing a resistor between the REF and DIO pins (a 33k resistor will reduce the open lamp threshold by approximately 100μA $((V_{REF}^{-} V_{DIO}^{+})/33k)$. When an offset current is added, the values for R_{RMAX} and R_{RMIN} may need to be increased from their nominal values to compensate for the offset current.

VC Compensation

As previously mentioned a single capacitor on the VC pin combines the error signal conversion, lamp current averaging and frequency compensation. Careful consideration should be given to the value of capacitance used. A large value (1μF) will give excellent stability at high lamp currents but will result in degraded line regulation in PWM mode. On the other hand , a small value (10nF) will give excellent PWM response but might result in overshoot and poor load regulation. The value chosen will depend on the maximum load current and dimming range. After these parameters are decided upon, the value of the VC capacitor should be increased until the line regulation becomes unacceptable. A typical value for the VC capacitor is 0.033μF. For further information on compensation please refer to the references or consult the factory.

Current Sense Comparator

The LT1768 is a current mode PWM controller. Under normal operating conditions the GATE is driven high at the start of every oscillator cycle. The GATE is driven back low when the current reaches a threshold level proportional to the voltage on the VC pin. The GATE then remains low until the start of the next oscillator cycle. The peak current is thus proportional to the VC voltage and controlled on a cycle by cycle basis. The peak switch current is normally sensed by placing a sense resistor in the source lead of the output MOSFET. This resistor converts the switch current to a voltage that can be compared to a fraction of the VC voltage $[(V_{VC} – V_{DIODE})/30]$. For normal conditions and a GATE duty cycle below 50%, the switch current limit will correspond to $I_{PK} = 0.1/R_{SENSE}$. For GATE duty cycles above 50% the switch current limit will be reduced to approximately 90mV at 80% duty cycle to avoid subharmonic oscillations associated with current mode controllers.

When the lamp current is programmed to PWM mode, the VC pin will slew between voltages that represent the minimum and maximum PWM lamp currents. The slew time affects the line regulation at low duty cycle, and should be kept low by making the sense resistor as small as possible. The lowest value of sense resistor is determined by switching transients and other noise due to layout configurations. A good rule of thumb is to set the sense resistor so that the voltage on the VC pin equals 2.5V when the PWM current is in maximum mode ($V_{PROG} = V_{PWM}$). Typical values of the sense resistor run in the 25mΩ to 50mΩ range for large displays, and can be implemented with a copper trace on the PCB.

Since the maximum threshold at the SENSE pin is only 100mV, switching transients and other noise can prematurely trip the comparator. The LT1768 has a blanking period of 100ns which prohibits premature switch turn off, but further filtering the sense resistor voltage is recommended. A simple RC filter is adequate for most applications. (Figure 5.)

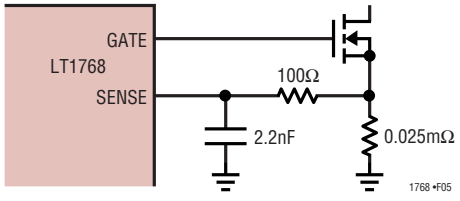

Figure 5. Sense Pin Filter

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GATE

The LT1768 has a single high current totem pole output stage. This output stage is capable of driving up to ±1.5A of output current. Cross-conduction current spikes in the totem pole output have been eliminated. The GATE pin is intended to drive an N-channel MOSFET switch. Rise and fall times are typically 50ns with a 3000pF load. A clamp is built into the device to prevent the GATE pin from rising above 13V in order to protect the gate of the MOSFET switch.

The GATE pin connects directly to the emitter of the upper NPN drive transistor and the collector of the lower NPN drive transistor in the totem pole. The collector of the lower transistor, which is N-type silicon, forms a P-N junction with the substrate of the device. This junction is reversed biased during normal operation.

In some applications the parasitic LC of the external MOSFET gate can ring and pull the GATE pin below ground. If the GATE pin is pulled negative by more than a diode drop the parasitic diode formed by the collector of the GATE NPN and the substrate will turn on. This can cause erratic operation of the device. In these cases a Schottky clamp diode is recommended from the GATE pin to ground. (Figure 6.)

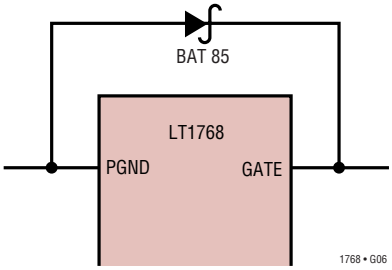

Figure 6. Schottky Gate Clamp

Reference

The internal reference of the LT1768 is a trimmed bandgap reference. The reference is used to power the majority of the LT1768 internal circuitry. The reference is inactive if the LT1768 is in undervoltage lockout, shutdown mode, or thermal shutdown. The undervoltage lockout is active when V_{IN} is below 7.9V and the LT1768 is in shutdown mode when the voltage on the $\overline{SHDN}$ pin is pulled below 1V. The $\overline{SHDN}$ pin has 200mV of hysteresis and a 7μA pull-up current source. The LT1768 thermal shutdown temperature is set at 160°C. A buffered version of the internal 5V is present at the V_{REF} pin and is capable of supplying up to 10mA of current. Note that using any substantial amount of current from the V_{REF} pin will increase power dissipation in the device, which will reduce the useful operating ambient temperature range.

Supply and Input Voltage Sequencing

For most applications, where the $\overline{SHDN}$ pin is left floating, and the voltages on the PWM and PROG pins are derived from the V_{REF} pin, the LT1768 will power-up and power-down correctly when the voltage to the V_{IN} pin is applied and removed. In applications where the voltage inputs for the V_{IN} pin, $\overline{SHDN}$ pin, PWM pin, and the PROG pin originate from different sources (power supply, microprocessors etc.), care must be taken during power up/down sequences. For proper operation during the power-up sequence, the voltage on the following pins must be taken from zero to their appropriate values in the following order; V_{IN} pin, $\overline{SHDN}$ pin, PWM pin and PROG pin. For proper operation during the power-down sequence, the order must be reversed. For example, in the circuit of Figure 1 where the $\overline{SHDN}$ pin is left floating, and the PWM pin voltage is derived from a resistor divider to the V_{REF} pin, the proper power-up sequence would be to take the V_{IN} pin from zero to its value then apply either a voltage or PWM signal to the PROG pin. The power-down sequence for the circuit in Figure 1 would be to take the PROG pin voltage to zero, then take the V_{IN} pin voltage to zero.If the PROG voltage in the circuit of Figure 1 is present before the V_{IN} supply voltage, proper power supply sequecing can be achieved by implementing the circuit shown in Figure 7.

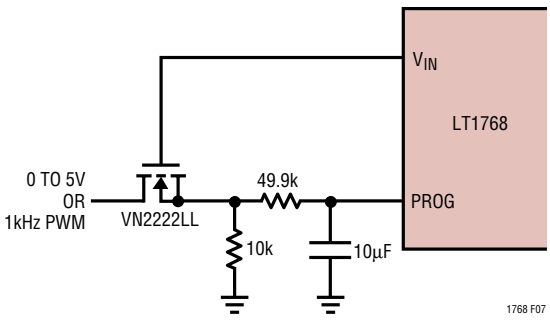

Figure 7. Circuit Insures Proper Supply Sequencing When Dimming Voltage Exists Before Main Power Supply

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Supply Bypass and Layout Considerations

Proper supply bypassing and layout techniques must be used to insure proper regulation, avoid display flicker, and insure long term reliability.

Figure 8 shows the application's critical high current paths in thick lines. Ideally, all components in the high current path should be placed as close as possible and connected with short thick traces. The most critical consideration is that T1's center tap, the Schottky diode D1, LT1768's V_{IN} pin, and a low ESR capacitor (C1) be connected directly together with minimum trace between them. If space constraints prohibit the transformer T1 placement next to C1, local bypassing (C2) for the center tap of transformer T1 should be used.

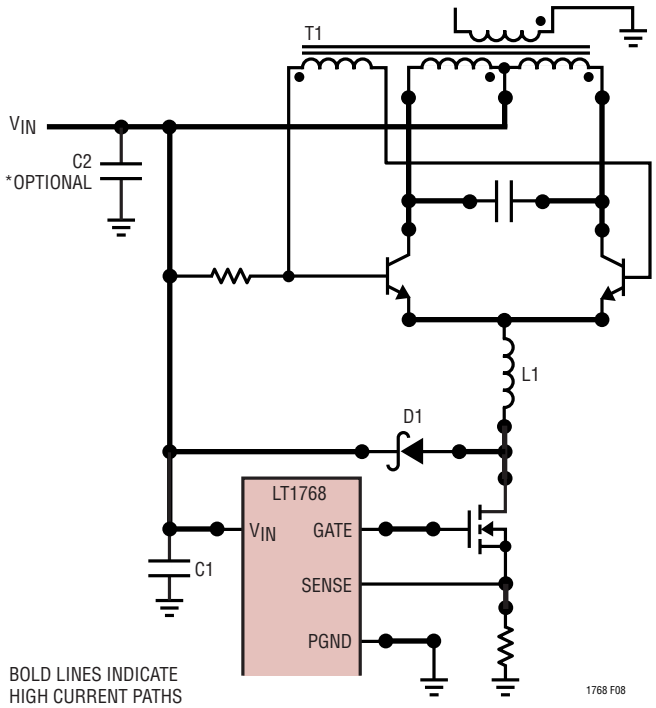


Figure 8

Special attention is also required for the layout of the high voltage section to avoid any unpleasant surprises. Please refer to the references for an extensive discussion on high voltage layout techniques.

Applications Support

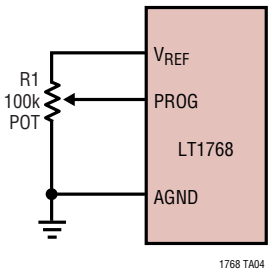
Linear Technology invests an enormous amount of time, resources, and technical expertise in understanding, designing and evaluating backlight solutions for systems designers. The design of an efficient and compact backlight system is a study of compromise in a transduced electronic system. Every aspect of the design is interrelated and any design change requires complete re-evaluation for all other critical design parameters. Linear Technology has engineered one of the most complete test and evaluation setups for backlight designs and understands the issues and trade-offs in achieving a compact, efficient and economical customer solution. Linear Technology welcomes the opportunity to discuss, design, evaluate, and optimize any backlight system with a customer. For further information on backlight designs, consult the references below.

References

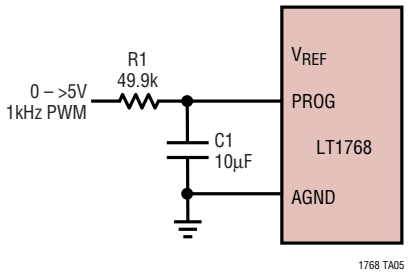
1. Williams, Jim. November 1995. A Fourth Generation of LCD Backlight Technology. Linear Technology Corporation, Application Note 65.

TYPICAL APPLICATIONS

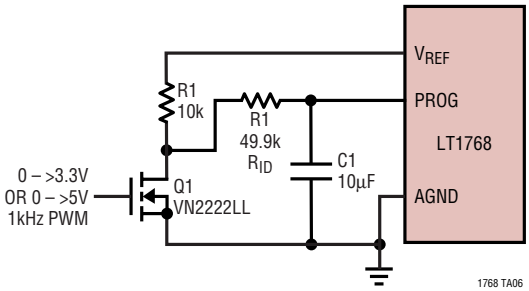
DC Intensity Control



PWM Intensity Control

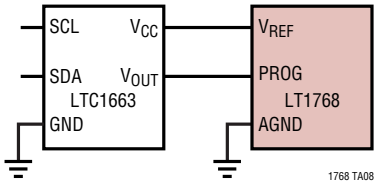


PWM Intensity Control From 3.3V or 5V Logic

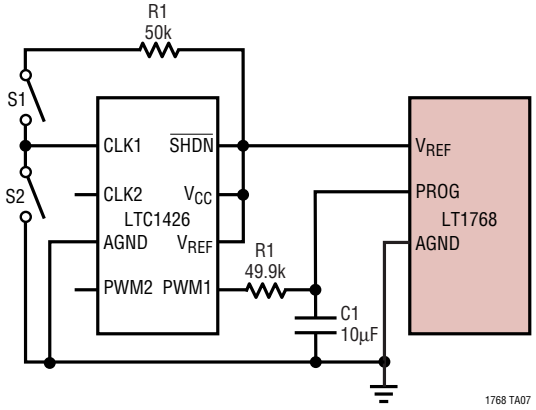


TYPICAL APPLICATIONS

2-Wire Serial interface Intensity Control

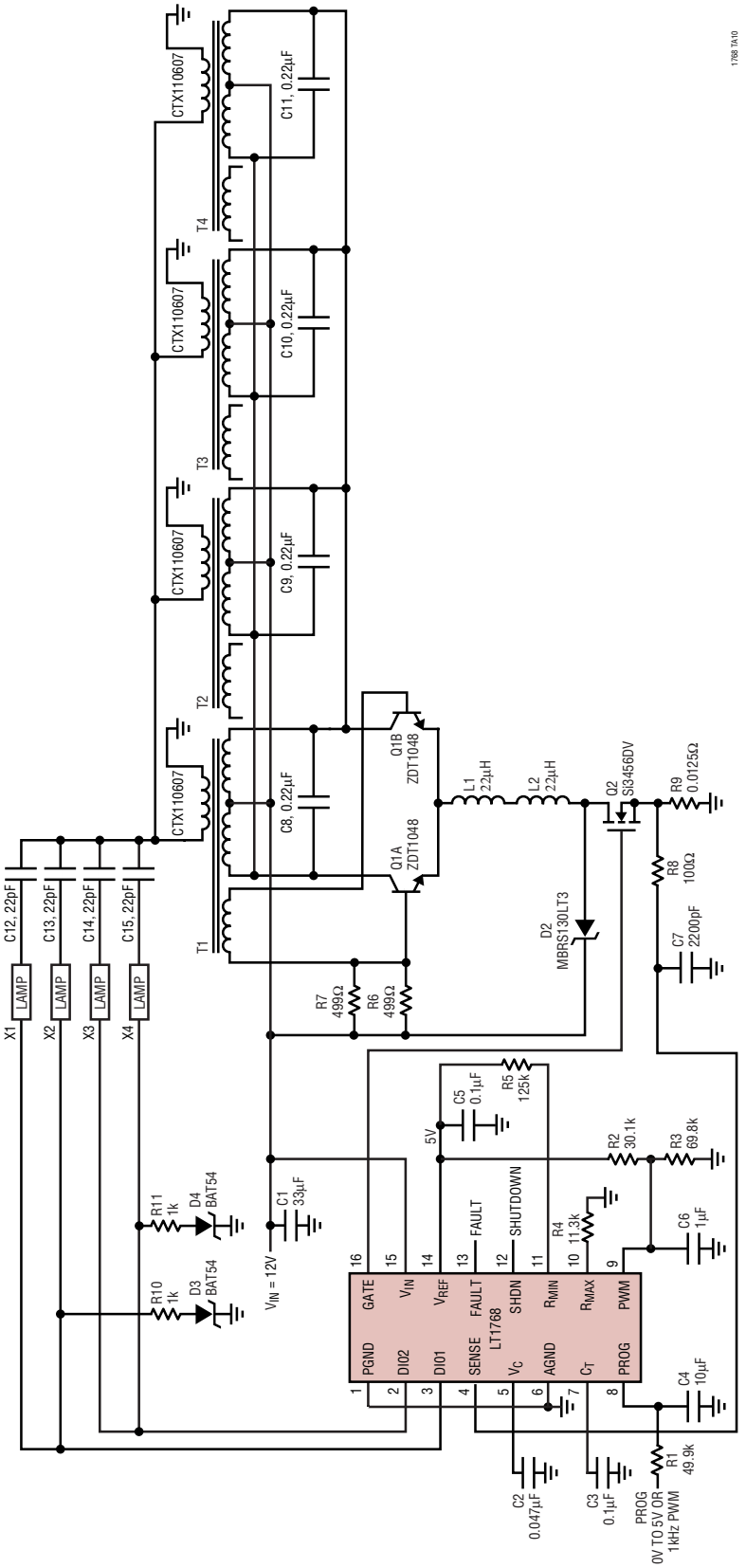


Pushbutton Intensity Control



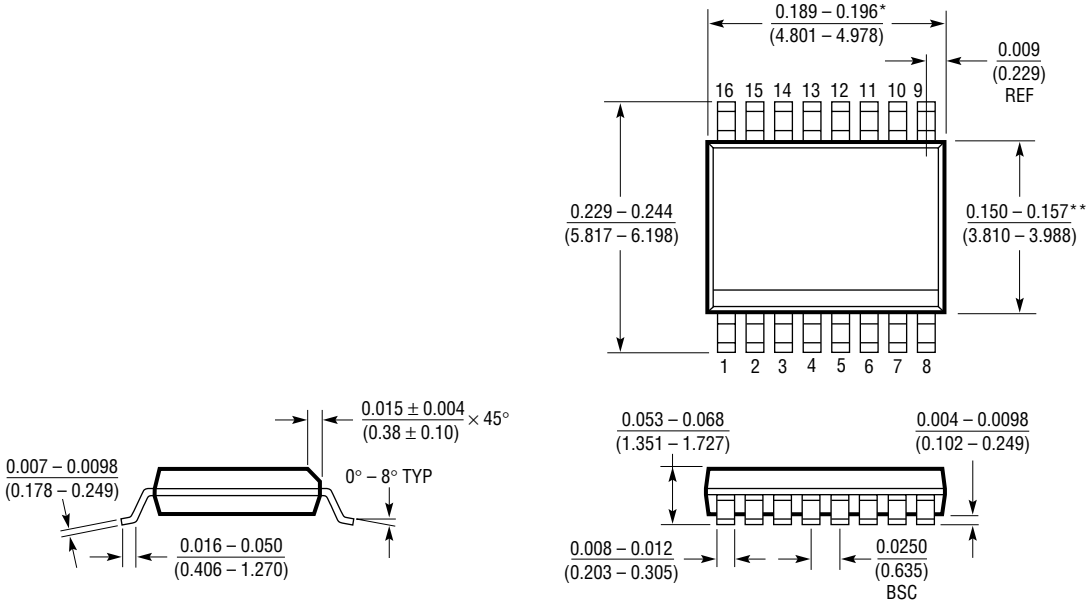
TYPICAL APPLICATIONS

24 Watt Four Lamp CCFL Supply



PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



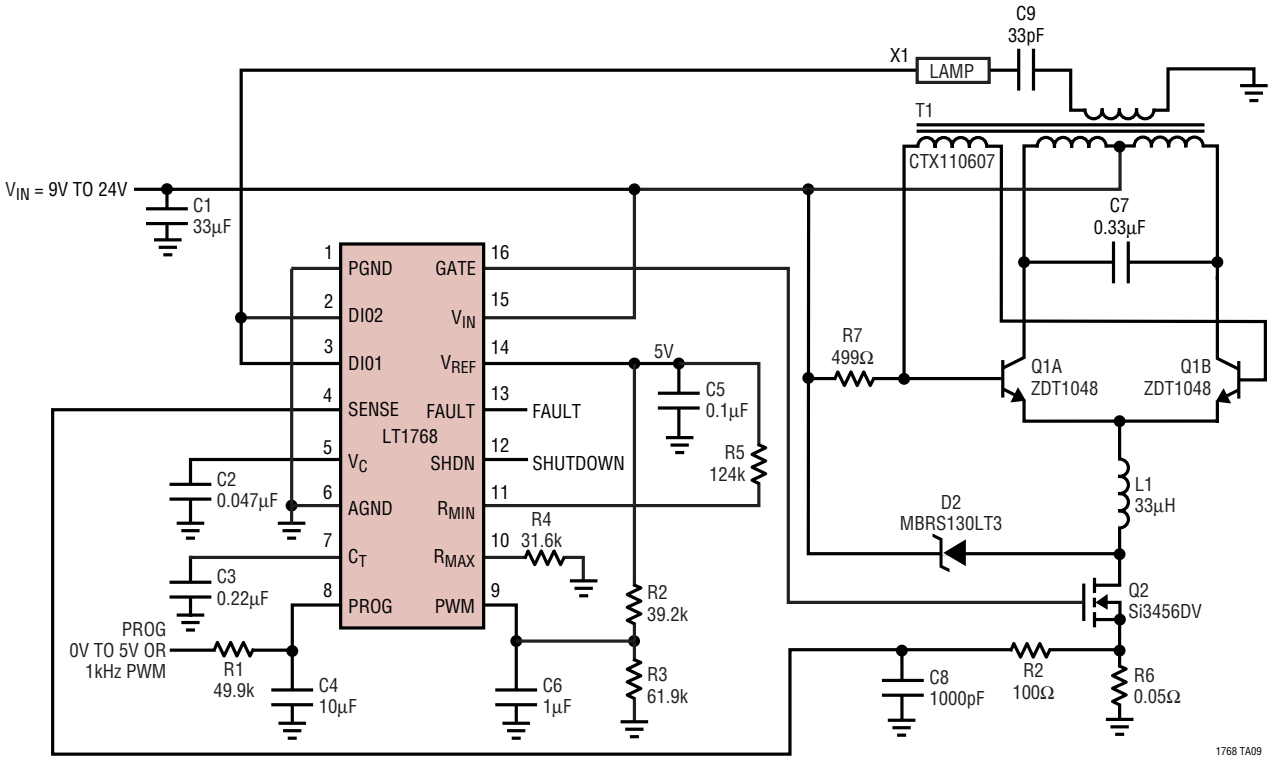
* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 1098

TYPICAL APPLICATION

4 Watt Single Lamp CCFL Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1170	Current Mode Switching Regulator	5.0A, 100kHz
LT1182/LT1183	CCFL/LCD Contrast Switching Regulators	$3V \le V_{IN} \le 30V$, CCFL Switch: 1.25A, LCD Switch: 625mA, Open Lamp Protection, Positive or Negative Contrast
LT1184	CCFL Current Mode Switching Regulator	1.25A, 200kHz
LT1186	CCFL Current Mode Switching Regulator	1.25A, 100kHz, SMBus Interface
LT1372	500kHz, 1.5A Switching Regulator	Small 4.7µH Inductor, Only 0.5 Square Inch of PCB
LT1373	250kHz, 1.5A Switching Regulator	1mA I_Q at 250kHz, Regulates Positive or Negative Outputs
LT1786F	SMBus Controlled CCFL Switching Regulator	Precision 100µA Full Scale Current DAC

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